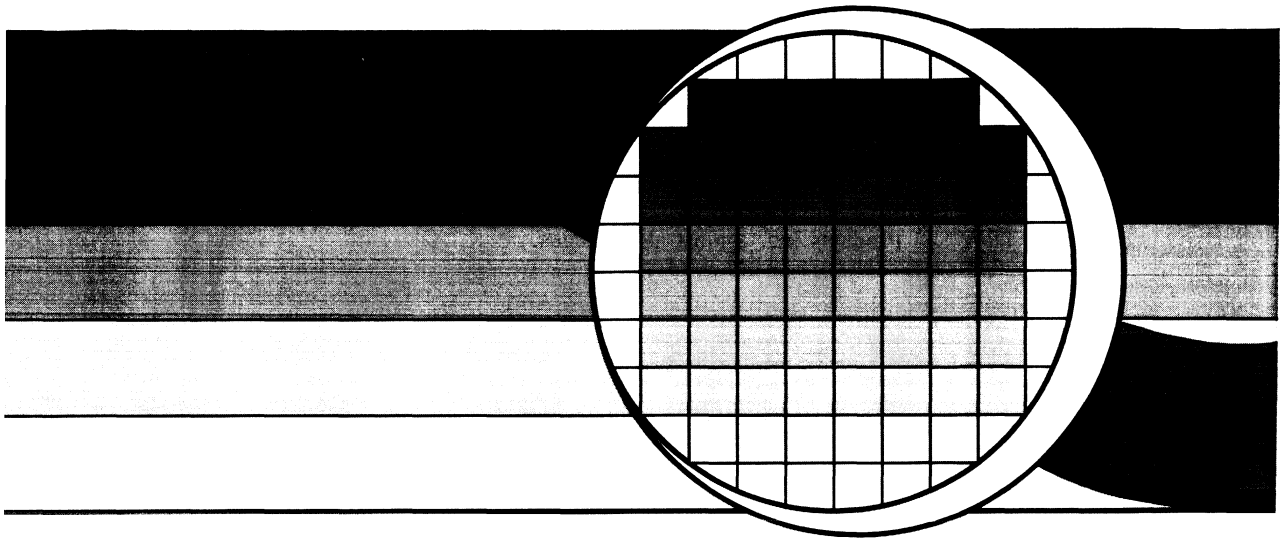
TRW

D A T A B O O K



Data Converters – DSP Products

TRW LSI Products Inc.

- A/D Converters
- D/A Converters
- Linear Products
- Signal Synthesis
- Imaging Products
- Transform Products
- Correlators
- Vector Arithmetic/Filters
- Fixed-Point Arithmetic
- Floating-Point Arithmetic
- Memory/Storage

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La Jolla, CA 92038

Advance Information describes products that are not available at the time of printing. Specifications may change in any manner without notice. Contact TRW for current information.

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TRW LSI Products Inc. components are not designed for use in life support applications, wherein a failure or malfunction of the component can reasonably be expected to result in personal injury. The user of TRW LSI Products Inc. components in life support applications assumes all risk of such use and indemnifies TRW LSI Products Inc. against all damages.

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Standardized Military Drawings

To stem the proliferation of contractor-generated Source Control Drawings (SCDs), the US Government has established a program to create a single government-controlled SCD for each part in the military inventory. This document is called a Standardized Military Drawing (SMD) and is available for use by any contractor. By greatly reducing the number of part numbers thus generated, it is much more practical to maintain an inventory of these products, reducing acquisition time, cost, and overhead.

TRW is a strong supporter of this program. We have a number of products currently in the system and the list is growing rapidly. Identified below are the products in the inventory at the time of publication of this databook, along with the "nearest generic equivalent" TRW part number. Since the Defense Electronics Supply Center (DESC) in Dayton, Ohio controls the detailed spec, we manufacture and test the product strictly in accordance with that spec. If it varies in any way from the standard specification, the SMD is the controlling document. It is important to verify from DESC that you are working from the latest revision of the SMD.

These products are not only available from the government supply channels and from the TRW factory, but many are handled through the normal commercial distribution channels, providing ready access to full-spec military products. They are all fully compliant with the latest release of MIL-STD-883.

If you have a need for a product not listed below, contact the factory. We may be working on it; if not, we will be delighted to work with you to add it to the program.

Standardized Military Drawings

SMD	Suffix	TRW Part Number	Description
5962-87600	01XA	TDC1048B6V	8-Bit 20Msps A/D
	01XC	TDC1048J6V	
	013A	TDC1048C3V	
5962-87786	01VA	TDC1046B8V	6-Bit 20Msps A/D
	01VC	TDC1046J8V	
5962-88532	01XC	TDC1049J0V	9-Bit 30Msps A/D
	01YC	TDC1049J3V	
	01ZA	TDC1049C1V	
5962-88739	01QA	TMC208KB5V	8 x 8 Bit Multiplier
	02QA	TMC208KB5V1	
	03QA	TMC28KUB5V	
	04QA	TMC28KUB5V1	
5962-89711	01JA	TMC2023B7V	64-BitCorrelator
	02JA	TMC2023B7V1	
	013A	TMC2023C3V	
	023A	TMC2023C3V1	
	01LA	TMC2023B2V	
	02LA	TMC2023B2V1	
5962-89446	01LX	TMC2011B2V	Multi-Tap Register
	013X	TMC2011C3V	
	02LX	TMC2111B2V	
	023X	TMC2111C3V	
5962-89715	01XX	TMC2301G8V	Image Resampler
	02XX	TMC2301G8V1	
	01YX	TMC2301L1V	
	02YX	TMC2301L1V1	
5962-89828	01EX	TDC1044B9V	4-Bit 25Msps A/D
5962-90596		TDC1012	12-Bit 20Msps D/A
		TMC2208J4V	8 x 8 Bit MAC
		TMC2310G5V	FFT
		TMC2310G5V1	
		TMC2310L4V	
		TMC2310L4V1	

A/D Converters

TRW offers a line of high performance A/D converters that addresses applications from 50kHz to 100MHz.

For video bandwidths (on the order of 10MHz), we have converters with resolutions of 4 to 10 bits and conversion rates from 18Msps to 100Msps. We pioneered the monolithic video A/D converter in 1977, and in 1989 received an Emmy Award for our contributions to the field of video conversion. The current offerings are the fourth generation products of TRW's commitment to quality video conversion.

The high-resolution high-speed area is addressed by the THC1200 family of 12-bit converters, including the smallest available 10Msps 12-bit A/D (the THC1202) and the unique dual-range THC1200, which provides nearly 16 bits of dynamic range at 8Msps.

For slower high-resolution applications, several new low-power CMOS A/Ds include built-in Track/Hold circuits: the TMC1061 converts at over 500ksps with 10-bit resolution, while the TMC1251/12451 produce 12-bits-plus-sign at 83ksps. The TMC12441 and TMC12451 are tested and specified especially for DSP applications.

The TDC1035 is an an innovative new product that digitizes the peak value of a pulse (as narrow as 12ns) that occurs any time during a user-defined "window". It is ideal for high-energy physics instrumentation, electronic warfare, and instrumentation.

Product	Resolution (Bits)	Conv Rate [1,2] (Msps)	RMS/RMS SNR [1] (dB)	Package		Grade [2]	Notes	Page
TDC1044	4	25	–	B9, N9	16 Pin DIP	C, V, SMD		A103
TDC1046	6	25	33	B8	18 Pin DIP	C, V, SMD		A113
TDC1029	6	100	33	B7	24 Pin CERDIP	C	50MHz Input Bandwidth, ECL Interface.	A67
TDC1047	7	20	39	B7	24 Pin CERDIP	C, V		A121
TDC1147	7	15	36	B7	24 Pin CERDIP	C, V	No Pipeline Delay. Well Suited to Subranging Converter Applications.	A241
TDC1001	8	2.5	–	B8	18 Pin CERDIP	C, A [3]	Successive Approximation Converter.	A3
TDC1025	8	50	44	C1	68 Contact CC	C, A	ECL Interface.	A51
				L1	68 Lead CC	C, A		
TDC1035	8	–	–	B7	24 Pin CERDIP	C, V	Peak Digitizer. Digitizes Peak Value of Pulses as Narrow as 12ns.	A77
TDC1038	8	20	45	B6, N6	28 Pin DIP	C, V	Low Power Version of TDC1048.	A85
				R3	28 Lead PLCC	C		
				E1	Evaluation Board	C		
TDC1048	8	20	45	B6, N6	28 Pin DIP	C, V, SMD	Industry Standard Video A/D.	A131
				C3	28 Contact CC	C, V, SMD		
				R3	28 Lead PLCC	C		
				E1	Evaluation Board	C		
TDC1058	8	20	45	B6, N6	28 Pin DIP	C	New Industry-Standard Video A/D.	A163
				R3	28 Lead PLCC	C	Single +5V Power Supply.	
				E1	Evaluation Board	C	TDC1048 Performance Equivalent.	
THC1068	8	25	44	S7	24 Pin DIP	C, V	Complete A/D System, with Input Amplifier,	A191
				E1	Evaluation Board	C	Reference, and Output Register.	

Notes: 1. Guaranteed. See product specifications for test conditions.

2. A = High Reliability, $T_C = -55°C$ to $125°C$.
   B = Industrial, $T_C = -25°C$ to $85°C$.
   C = Commercial, $T_A = 0°C$ to $70°C$.
   F = Extended Temperature Range, $T_C = -55°C$ to $125°C$.
   V = MIL-STD-883 Compliant, $T_C = -55°C$ to $125°C$
   SMD = Available per Standardized Military Drawing, $T_C = -55°C$ to $125°C$.

3. A = High Reliability, $T_C = -20°C$ to $95°C$.

Product	Resolution (Bits)	Conv Rate [1,2] (Msps)	RMS/RMS SNR [1] (dB)	Package		Grade [2]	Notes	Page
TMC1175	8	30	45	N2	24 Pin DIP	C, V	Low Power CMOS Video A/D with Integral Track/Hold.	A251
				R3	28 Lead PLCC	C		
				E1	Evaluation Board	C		
TDC1049	9	30	48	J0	64 Pin DIP	C, V, SMD	ECL Interface.	A147
				C1	68 Contact CC	C, V, SMD		
				G8	68 Pin PGA	C, V		
				E1	Evaluation Board	C		
THC1069	9	37	47	S5	32 Pin DIP	B, V	Complete A/D System, with Input Amplifier, Reference, and Output Register.	A207
				E1	Evaluation Board	C		
TMC1061	10	0.56	–	B3, N3	20 Pin DIP	B, F	Monolithic CMOS Sampling A/D Converter with Integral Track/Hold.	A179
				M3	20 Pin SOIC	B		
				E1	Evaluation Board	C		
TDC1020	10	20	55	J1	64 pin DIP	C, V	Monolithic Video A/D, TTL Interface, ±2V Input Range.	A31
				G0	68 Pin PGA	C, V		
				E1	Evaluation Board	C		
TAC1020	10	20	55	P3	Module	C	Low Power Replacement for MOD-1020.	A19
THC1070	10	25	54	S5	32 Pin DIP	B, V	Complete A/D System with Input Amplifier and Reference. TTL Interface.	A223
				E1	Evaluation Board	C		
TAC1025	10	25	55	P3	Module	C	Low Power Replacement for ZAD 1025.	A19
THC1200	12	8	62	S3	46 Pin DIP	B, V	Complete A/D System with T/H and Reference. High-Speed Selectable Dual Input Range (±0.167V and ±2.5V).	A253
				E1	Evaluation Board	C		
THC1201	12	10	62	S3	46 Pin DIP	B, V	Complete A/D System with T/H and Reference. ±1.0V Input Range.	A271
				E1	Evaluation Board	C		
THC1202	12	10	62	S3	40 Pin DIP	B, V	Low Cost Complete A/D System with T/H and Reference. Smallest Available at 10Msps.	A287
				E1	Evaluation Board	C		
TMC1241	12+Sign	0.051	–	B6	28 Pin CERDIP	B, F	Monolithic CMOS A/D with Integral Track/Hold.	A305
				E1	Evaluation Board	C		
TMC12441	12+Sign	0.051	76.5	B6	28 Pin CERDIP	B, F	Specified and Tested for DSP Applications.	A337
				E1	Evaluation Board	C		
TMC1251	12+Sign	0.083	–	B7	24 Pin CERDIP	B, F	Monolithic CMOS A/D with Integral Track/Hold. 8-Bit Microprocessor Interface.	A319
				E1	Evaluation Board	C		
TMC12451	12+Sign	0.083	73.5	B7	24 Pin CERDIP	B, F	Specified and Tested for DSP Applications.	A355
				E1	Evaluation Board	C		

Notes: 1. Guaranteed. See product specifications for test conditions.

2. A=High Reliability, $T_C = -55°C$ to 125°C.
B=Industrial, $T_C = -25°C$ to 85°C.
C=Commercial, $T_A = 0°C$ to 70°C.
F=Extended Temperature Range, $T_C = -55°C$ to 125°C.
V=MIL-STD-883 Compliant, $T_C = -55°C$ to 125°C
SMD=Available per Standardized Military Drawing, $T_C = -55°C$ to 125°C.

TDC1001 (400ns)

Successive Approximation A/D Converter

8-Bit, 2.5Msps

The TRW TDC1001 analog-to-digital converter is a high-speed, 8-bit successive approximation device. This bipolar, monolithic converter offers significant advantages in size, cost, and performance, as well as high reliability and low-power consumption.

All digital interfaces are TTL compatible. A single +5VDC supply is required by the digital circuitry while −5VDC is required by the analog portion of the device. The analog and digital ground planes are internally isolated.

The TDC1001 consists of a comparator, reference buffer, 8-bit D/A converter, successive approximation register, output register, and control circuitry.

Features

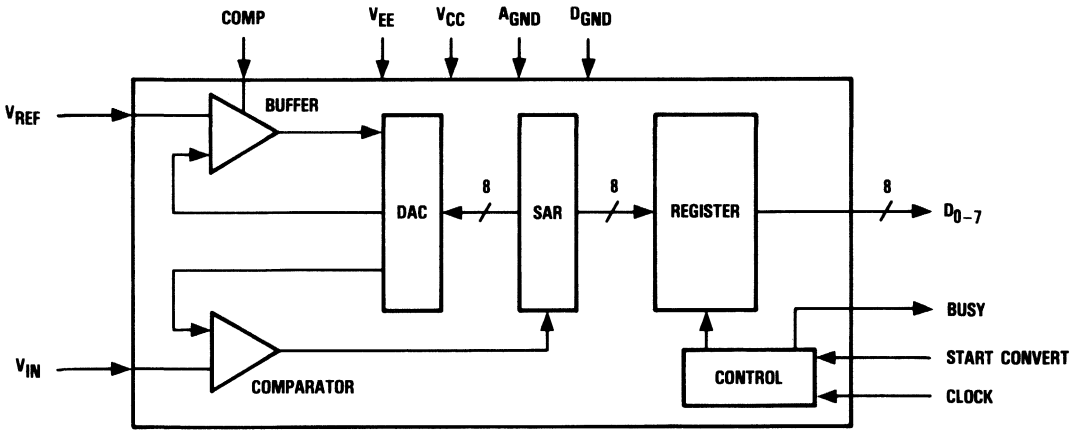
- 8-Bit Resolution
- Binary Output Coding
- TTL Compatible
- ±1/2 LSB Linearity
- Parallel Output Register
- 600mW Power Dissipation
- Available In An 18 Pin CERDIP Package

Applications

- Microprocessor Systems
- Numerical Control Interface
- Data Acquisition Systems

A

Functional Block Diagram



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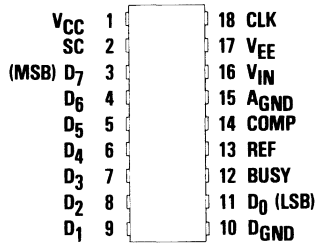
Pin Assignments



18 Pin CERDIP – B8 Package

Functional Description

General Information

The TDC1001 consists of six functional sections: comparator for the analog input, reference buffer, 8-bit D/A converter (DAC), successive approximation register (SAR), output register, and control circuitry. The SAR and comparator will sequentially compare the analog input to the DAC output. The conversion process requires nine clock cycles.

Power

The TDC1001 operates from separate analog and digital power supplies. Analog power (V_{EE}) is −5.0VDC and digital power (V_{CC}) is +5.0VDC. All power and ground pins must be connected.

Separate decoupling for each supply is recommended. The return for I_{EE}, the current drawn from the V_{EE} supply, is A_{GND}. The return for I_{CC}, the current drawn from the V_{CC} supply, is D_{GND}.

Reference

The TDC1001 accepts a nominal input reference voltage of −0.5VDC. The voltage should be supplied by a precision voltage reference, as the accuracy of this voltage will have a significant effect on the overall accuracy of the system. The reference voltage input pin should be bypassed to A_{GND} as close as possible to the device terminal.

Analog Input

The analog input range of the device is set by the reference voltage. This is nominally −0.5VDC with an absolute tolerance of ±0.1VDC. Since the device is a successive approximation type A/D converter, a sample-and-hold circuit may be required in some applications.

Conversion Timing Description

The timing sequence of the TDC1001 is typical of successive approximation converters. Nine clock cycles are required for each conversion. Start Convert must transition from LOW to HIGH a minimum of t_S prior to the leading edge of the first convert pulse, and must remain HIGH a minimum of t_H after the edge.

This first cycle clears the BUSY flag and prepares the device for a new conversion. The following eight clock cycles convert each data bit (MSB first, LSB last). During these eight clock cycles, the analog input must be held stable (to within 1/2 LSB). At t_D nanoseconds after the rising edge of the eighth clock pulse, the seven most significant bits are valid (and the BUSY signal goes LOW). At t_D nanoseconds after the ninth clock pulse the LSB is valid, and the conversion is completed.

Data Outputs

The outputs of the TDC1001 are TTL compatible and capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time (t_D) after the rising edge of Start Convert (SC).

Compensation Pin

The COMPensation pin (COMP), is provided for external compensation of the internal reference amplifier.

The compensation capacitor must be connected between this pin and V_{EE}. A tantalum capacitor greater than 10μF is recommended for proper operation.

Output Coding

An analog input voltage of 0.0V will produce a digital output code of all zeros; an analog input voltage of −0.50V will produce a digital output code of all ones.

Package Interconnections

Signal Type	Signal Name	Function	Value	B8 Package Pins
Power	V_{EE}	Analog Supply Voltage	−5.0VDC	17
	V_{CC}	Digital Supply Voltage	+5.0VDC	1
	A_{GND}	Analog Ground	0.0VDC	15
	D_{GND}	Digital Ground	0.0VDC	10
Reference	V_{REF}	Reference Voltage Input	−0.5VDC	13
Analog Input	V_{IN}	Analog Input	0 to −0.5V	16
Conversion Timing Description	SC	Start Convert Input	TTL	2
	BUSY	Busy Flag Output	TTL	12
	CLK	Convert Clock Input	TTL	18
Outputs	D_7	MSB Output	TTL	3
	D_6		TTL	4
	D_5		TTL	5
	D_4		TTL	6
	D_3		TTL	7
	D_2		TTL	8
	D_1		TTL	9
	D_0	LSB Output	TTL	11
Compensation	COMP	Compensation Pin	>10μF	14

A

Figure 1. Timing Diagram

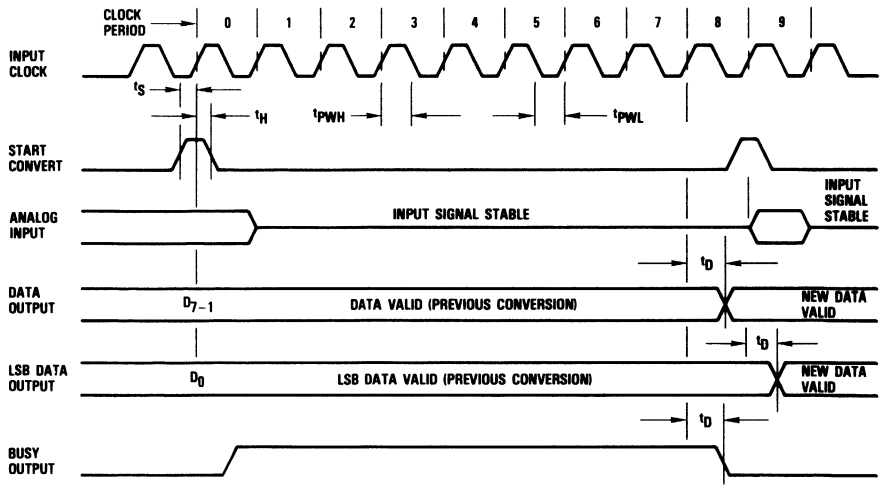


Figure 2. Simplified Analog Input Equivalent Circuit

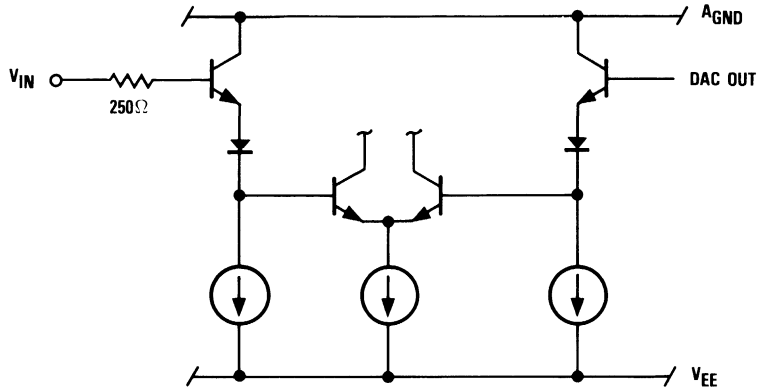


Figure 3. Digital Input Equivalent Circuit

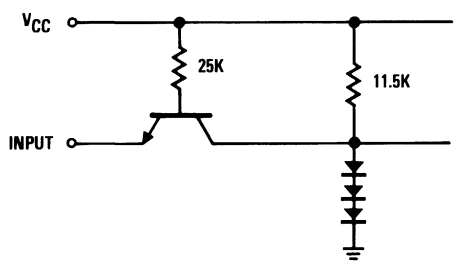
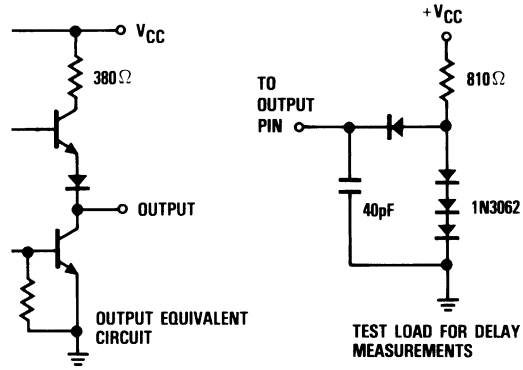


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage

V_{CC} (measured to D_{GND}) ..... 0 to +6.0V
V_{EE} (measured to A_{GND}) ..... 0 to −6.0V
A_{GND} (measured to D_{GND}) ..... −0.5 to + 0.5V

Input Voltages

CLK, SC (measured to D_{GND}) ..... −0.5 to +5.5V
V_{IN}, V_{REF} (measured to A_{GND}) ..... +0.5V to V_{EE}V

Output

Applied voltage (measured to D_{GND}) ..... −0.5 to +5.5V [2]
Applied current, externally forced ..... −1.0 to +6.0mA [3,4]
Short circuit duration (single output in high state to D_{GND}) ..... 1 sec

Temperature

Operating, case ..... −60 to +140°C
junction ..... +175°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Extended Min	Extended Nom	Extended Max	Units
V_{CC}	Positive Supply Voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage	−4.75	−5.0	−5.25	−4.75	−5.0	−5.25	V
A_{GND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0.0	+0.1	−0.1	0.0	+0.1	V
t_{PWL}	Clock Pulse Width, LOW	20			20			ns
t_{PWH}	Clock Pulse Width, HIGH	20			20			ns
t_S	Start Convert, Set-Up Time	7			7			ns
t_H	Start Convert, Hold Time	16			16			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{REF}	Reference Voltage	−0.4	−0.5	−0.6	−0.4	−0.5	−0.6	V
V_{IN}	Analog Input Voltage	0.0		−0.6	0.0		−0.6	V
T_A	Ambient Temperature, Still Air	0		+70				°C
T_C	Case Temperature				−20		+95	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = MAX, Static[1]		40		40	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, T_C = −20°C to +85°C		−80		−80	mA
I_{BIAS}	Analog Input Bias Current			10		10	μA
I_{REF}	Reference Current	V_{REF} = NOM		2.5		2.5	μA
R_{REF}	Total Reference Resistance		200		200		kOhms
R_{IN}	Analog Input Equivalent Resistance	V_{REF} = NOM	50		50		kOhms
C_{IN}	Analog Input Capacitance			10		10	pF
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V		−1.0		−1.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		75		75	μA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OS}	Output Short Circuit Current			−25		−25	mA

Note:
1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Clock Rate	V_{CC}, V_{EE} = MIN	22.5		22.5		MHz
t_C	Conversion Time	V_{CC}, V_{EE} = MIN		400		400	ns
t_D	Digital Output Delay	V_{CC}, V_{EE} = MIN		60		60	ns

Note:
1. Only the falling edge of BUSY is tested.

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error Integral, Independent	V_{CC}, V_{EE} = NOM		0.2		0.2	%
E_{LD}	Linearity Error Differential			0.2		0.2	%
T_{CG}	Gain Temperature Coefficient	V_{CC}, V_{EE} = NOM		+10		+10	ppm/°C
E_O	Offset Voltage			±7		±7	mV
T_{CO}	Offset Temperature Coefficient	V_{CC}, V_{EE} = NOM		−10		−10	μV/°C
E_G	Gain Error			1.5		2.0	%
T_{CIB}	I_{BIAS} Temperature Coefficient	V_{CC}, V_{EE} = NOM		−1.0		−1.0	%/°C

Application

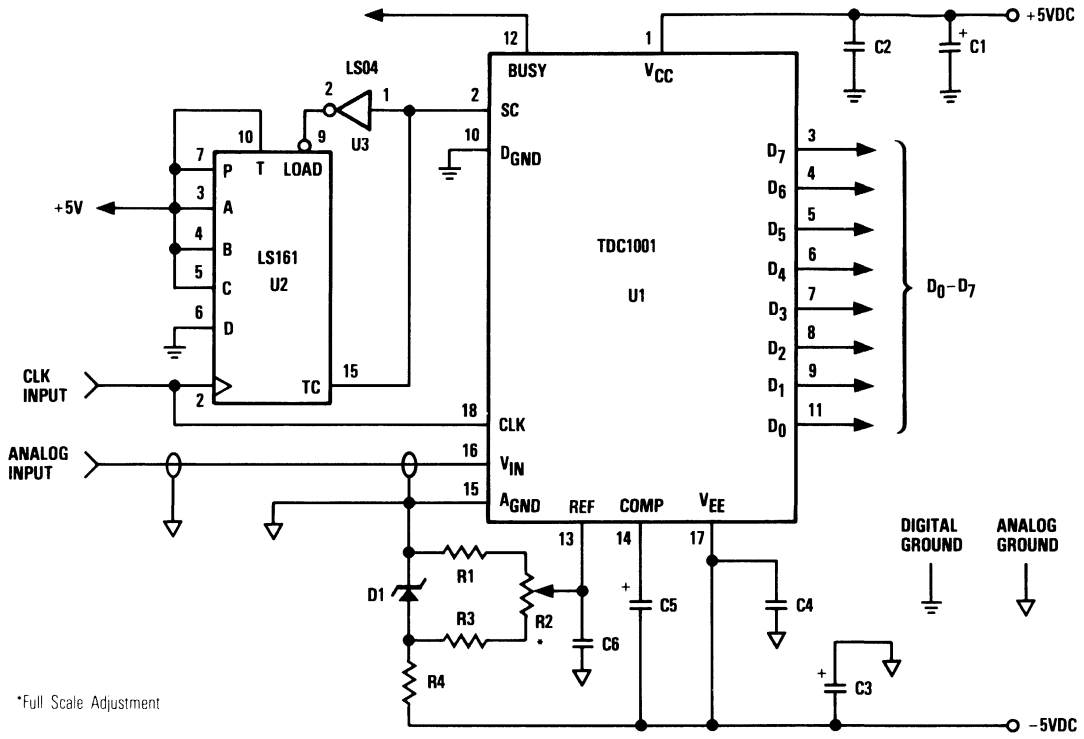
The TDC1001 is a high-speed, TTL compatible, SAR type A/D converter. The combination of very small analog signals and high-speed digital circuitry requires careful design of supporting analog/digital circuitry. Proper physical component layout, trace routing, and provision for sizeable analog and digital grounds are as important as the electrical design.

Two key design areas for fast, accurate A/D conversion are timing and grounding. The timing requirements for this device are detailed in Figure 1. Proper grounding is highly dependent on the board's mechanical layout and design constraints. In general, the noise associated with improper digital and analog ground isolation is synchronous with the clock and appears on the analog input.

Proper Design Practices Include:

- Sensitive signals such as clock, start convert, analog input, and reference should be properly routed and terminated to minimize ground noise pick-up and crosstalk. (Wirewrap is not recommended for these signals).
- Analog and digital ground planes should be substantial and common at one point only. Analog and digital power supplies should be referenced to their respective ground planes.
- Reference voltage should be stable and free of noise. Accuracy of the conversion is highly dependent on the integrity of this signal.
- The analog input should be driven from a low-impedance source (<25 Ohms). This will minimize the possibility of picking up extraneous noise.
- Ceramic high frequency bypass capacitors (0.001 to 0.01μF) should be used at the input pins of V_{CC}, V_{EE}, and REF. All pins should be bypassed to A_{GND} except V_{CC}.
- A tantalum capacitor of greater than 10μF should be connected from COMP (pin 14) to V_{EE}.

Figure 5. Typical Interface Circuit



Parts List

Resistors

R1	909 Ohms	1%	1/8W
R2	100 Ohms		Multi-Turn Cermet Pot
R3	1.33 kOhms	1%	1/8W
R4	2.49 kOhms	1%	1/8W

Capacitors

C1, C3, C5	10.0 μF	25V
C2, C4	0.001 μF	50V
C6	0.005 μF	50V

Integrated Circuits

U1	TDC1001J8	TRW 8-bit A/D Converter
U2	74LS161	TTL 4-bit Counter
U3	74LS04	TTL Hex Inverter
D1	LM113-1.22	1.22V Bandgap Voltage Reference

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1001B8C	STD – T_A = 0°C to 70°C	Commercial	18 Pin CERDIP	1001B8C
TDC1001B8A	EXT – T_C = – 55°C to 125°C	High Reliability	18 Pin CERDIP	1001B8A

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A

TDC1002 (1μsec)
Discontinued – Use TDC1001 for New Designs

Successive Approximation A/D Converter
8-Bit, 2.5MSPS

The TRW TDC1002 analog-to-digital converter is a high-speed, 8-bit successive approximation device. This bipolar, monolithic converter offers significant advantages in size, cost, and performance, as well as high reliability and low-power consumption.

All digital interfaces are TTL compatible. A single +5VDC supply is required by the digital circuitry while -5VDC is required by the analog portion of the device. The analog and digital ground planes are internally isolated.

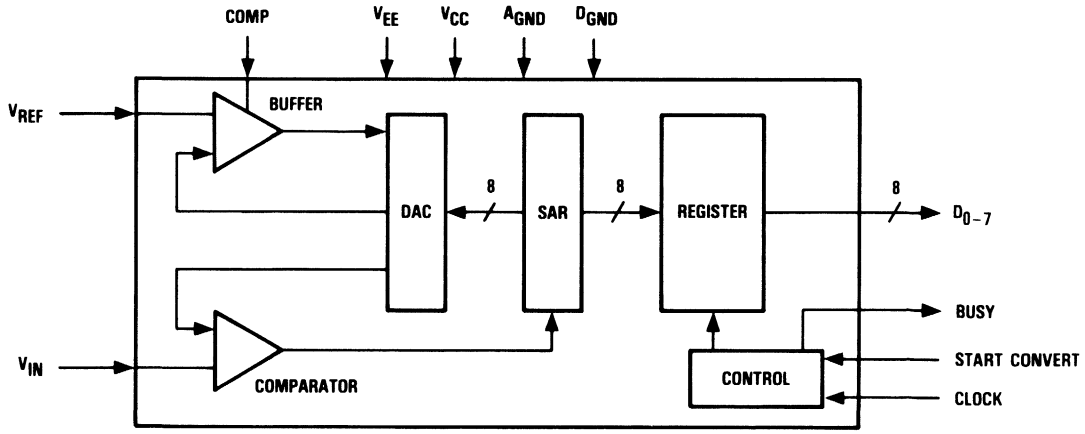
The TDC1002 consists of a comparator, reference buffer, 8-bit D/A converter, successive approximation register, output register, and control circuitry.

Features
- 8-Bit Resolution
- Binary Output Coding
- TTL Compatible
- ±1/2 LSB Linearity
- Parallel Output Register
- 600mW Power Dissipation
- Available In 18 Lead DIP

Applications
- Microprocessor Systems
- Numerical Control Interface
- Data Acquisition Systems

A

Functional Block Diagram



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TDC1007

Use TDC1048, TDC1038, TDC1058, TMC1175 for New Designs

Monolithic Video A/D Converter

8-Bit, 20Msps

The TDC1007 is an 8-bit fully parallel (flash) analog-to-digital converter, capable of digitizing an input signal at rates up to 20Msps (MegaSamples Per Second). It will operate accurately without the use of an external sample-and-hold amplifier, with analog input signals having frequency components up to 7MHz.

A single CONVert (CONV) signal controls the conversion operation of the device which consists of 255 sampling comparators, encoding logic, and a latched output buffer register. The device will recover from a full-scale input step in 20ns. Control inputs are provided to format the output in binary, two's complement, or inverse data coding formats.

The TDC1007 is patented under U.S. Patent No. 3283170 with other patents pending.

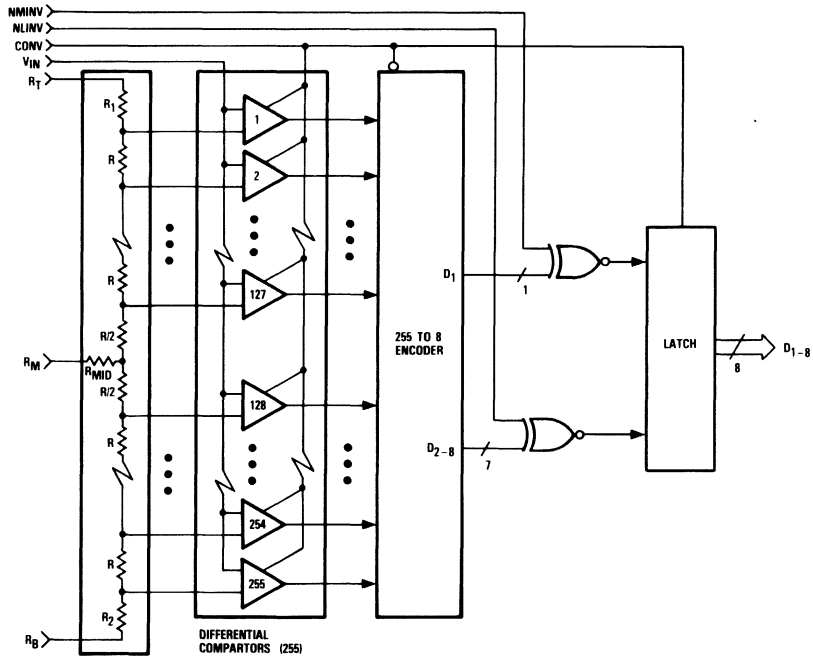
Features

- 8-Bit Resolution
- Conversion Rates Up To 20Msps
- Sample-And-Hold Amplifier Not Required
- Bipolar Monolithic Construction
- TTL Compatible Inputs And Outputs
- Binary Or Two's Complement Mode
- Differential Phase = 1.0 Degree
- Differential Gain = 1.7%

Applications

- Video Systems 3x Or 4x Subcarrier, NTSC Or PAL
- Radar Systems
- High-Speed Multiplexed Data Acquisition
- Digital Signal Processing

Functional Block Diagram



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40G00276 Rev. F – 11/90
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TDC1014

Use TDC1046 for New Designs

Monolithic Video A/D Converter

6-Bit, 25MSPS

The TRW TDC1014 is a 25 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 12MHz into 6-bit digital words. A sample-and-hold circuit is not necessary. All digital inputs and outputs are TTL compatible.

The TDC1014 consists of 63 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

Note: TRW recommends the use of the TDC1046 for new designs.

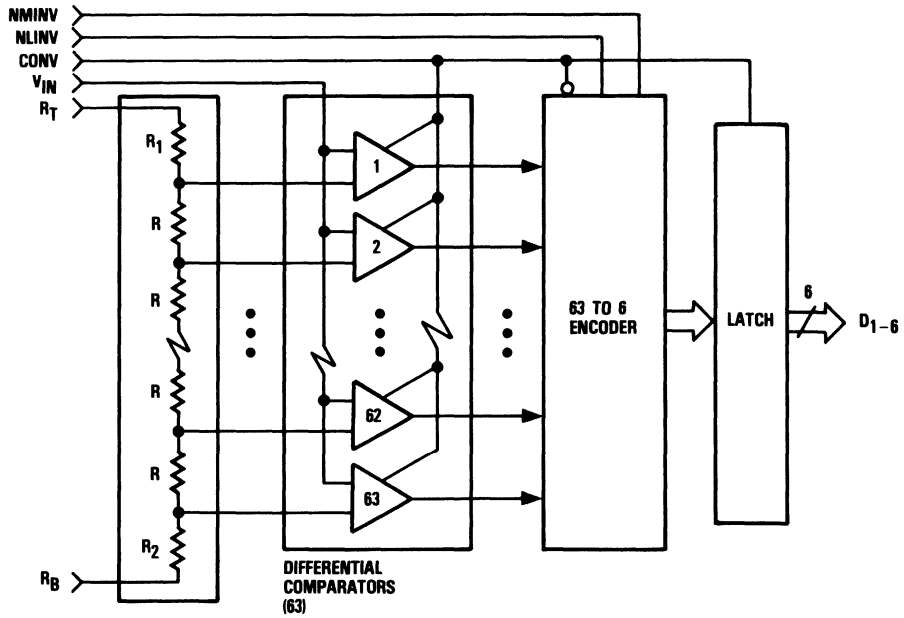
Features

- 6-Bit Resolution
- 1/4 LSB Linearity
- Sample-And-Hold Circuit Not Required
- TTL Compatible
- 25MSPS Conversion Rate
- Selectable Output Format
- Available In 24 Lead CERDIP

Applications

- Low-Cost Video Digitizing
- Medical Imaging
- Data Acquisition
- TV Special Effects
- Video Simulators
- Radar Data Conversion

Functional Block Diagram



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TAC1020 and TAC1025

Complete 10-Bit, 20 and 25 Msps
Analog-To-Digital Converter Boards

The TAC1020 and TAC1025 are A/D converter boards complete with voltage reference, input amplifier, track/hold, timing generator, and output registers. They are direct replacements for the Analog Devices MOD-1020 and offer significant performance improvements while reducing power consumption by more than 50%. Based on TRW's TDC1020 10-bit flash A/D converter, the TAC1020 achieves a 20 Msps (Mega samples per second) conversion rate and the TAC1025 converts at 25 Msps.

The TAC1020 has the exact timing and output characteristics of the MOD-1020. The TAC1025 employs simple pipeline timing which results in a higher conversion rate. All outputs of the TAC1020 are differential ECL compatible and the output format is unsigned magnitude.

Features

- Direct Replacement For MOD-1020
- 10-Bit Resolution
- 20 Msps Conversion Rate For TAC1020
- 25 Msps Conversion Rate For TAC1025
- Only Two Power Supplies Required: +5 And –5.2 Volts
- Power Consumption Reduced By More Than 50%
- Adjustable Input Range And Offset
- 500 Or 1kΩ Input Impedance
- Complete With Voltage Reference And Track/Hold Stage
- Bandwidth Greater Than 60MHz
- Differential ECL Input And Outputs

Applications

- Medical Imaging Systems
- High Quality Video
- Data Acquisition Systems
- Test Equipment
- Digital Communications
- Spectrum Analysis

A

Pin Assignments

Pin	Function	Pin	Function
1	GND	19	$\overline{\text{Bit 8}}$
2	ENCODE	20	Bit 7
3	$\overline{\text{ENCODE}}$	21	$\overline{\text{Bit 7}}$
4	GND	22	$\overline{\text{Bit 6}}$
5	V_{EE}	23	Bit 6
6	N/C (See note 1.)	24	$\overline{\text{Bit 5}}$
7	N/C (See note 1.)	25	Bit 5
8	GND	26	$\overline{\text{Bit 4}}$
9	A_{IN1}	27	Bit 4
10	A_{IN2}	28	Bit 3
11	V_{CC}	29	$\overline{\text{Bit 3}}$
12	GND	30	Bit 2
13	GND	31	$\overline{\text{Bit 2}}$
14	Bit 10 (LSB)	32	$\overline{\text{Bit 1}}$ ($\overline{\text{MSB}}$)
15	$\overline{\text{Bit 10}}$ ($\overline{\text{LSB}}$)	33	Bit 1 (MSB)
16	Bit 9	34	$\overline{\text{DR}}$
17	$\overline{\text{Bit 9}}$	35	GND
18	Bit 8	36	DR

Note: 1. ±15V supplies are not required with the TAC1020 and TAC1025. For compatibility with the MOD-1020, pins 6 and 7 may be connected to +15 and -15 Volts without damage.

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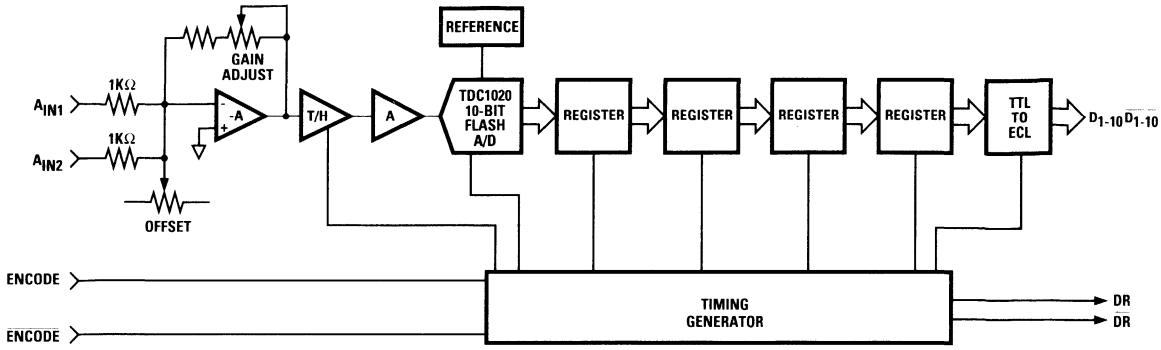
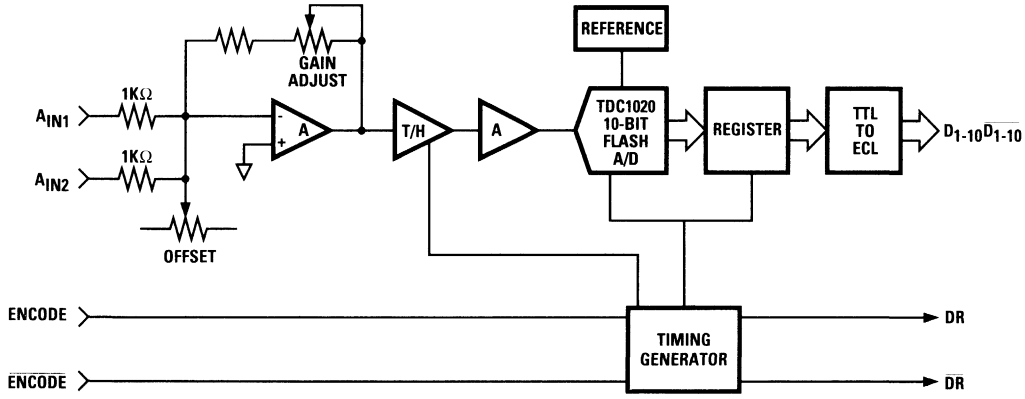
Functional Block Diagram, TAC1020



Functional Block Diagram, TAC1025



Functional Description

General Information

The TAC1020 and TAC1025 are complete Analog-to-Digital converter boards that are based upon TRW's TDC1020 monolithic flash converter integrated circuit. A wideband input amplifier, track/hold, voltage reference, timing and output circuits are included on the boards to make the TAC1020 and TAC1025 complete and very easy to use. The TAC1020 is rated at 20 Msps and has been designed to match the timing and output characteristics of the MOD-1020 board. The TAC1025 achieves 25 Msps by using a simplified pipeline data output design.

Analog Inputs

The analog input to the TAC1020 and TAC1025 has an equivalent circuit as shown in the *Functional Block Diagram*. Input impedances and voltage ranges are selected by using combinations of the two analog inputs, A_{IN1} and A_{IN2}. A 1kΩ input impedance with a 2 Volt peak-to-peak input range is available from either A_{IN1} or A_{IN2}. A 500Ω input impedance with a 1 Volt peak-to-peak input range is achieved by connecting both input pins together. These inputs may also be used to sum two analog signals.

The GAIN potentiometer affords a ±25% adjustment to the input range. The analog input range is factory-adjusted for ±0.5 Volts with input signals applied to A_{IN1} and A_{IN2} simultaneously. The OFFSET adjustment is factory-adjusted for 0.0 Volts. The OFFSET control has sufficient adjustment range to allow the board to be used with a unipolar input ranges of either polarity.

The on-board reference voltages for the TAC1020 and TAC1025 are calibrated at the factory to optimize linearity. Fixed and variable resistors are used to set voltage levels. Changing these resistors is discouraged because AC and DC performance will degrade.

Encode Command

The ENCODE input to the TAC1020 and TAC1025 is differential 10K ECL-compatible with a 100Ω input impedance between ENCODE and $\overline{\text{ENCODE}}$ (pins 2 and 3). The on-board track/hold goes into HOLD after the rising edge of ENCODE. In the TAC1020, the on-board timing generator then takes over the rest of the conversion cycle and data emerges from the outputs according to the *Timing Diagram* of the TAC1020.

The TAC1025 is also controlled by the rising edge of ENCODE, but data progresses through the TAC1025 and emerges at its outputs synchronously with respect to ENCODE. The *Timing Diagram* of the TAC1025 shows the simple pipeline data flow. There are minimum pulse width requirements (t_{PWH}, t_{PWL}) for the ENCODE signal for both TAC1020 and TAC1025.

Outputs and Timing

The outputs of the TAC1020 and TAC1025 are differential 10K ECL-compatible, capable of driving 75 to 100Ω loads connected from each data output to its complement. Data skew between bits is held to within 5 nanoseconds. The output data from the TAC1020 is valid at the falling edge of DR (pin 36). Data from the TAC1025 is synchronous with respect to the rising edge of ENCODE.

Power and Thermal Considerations

The TAC1020 and TAC1025 operates from only two supply voltages, +5 and –5.2 Volts. The two N/C terminals (pins 6 and 7) have no electrical connection to circuitry on the board. These pins are used for +15 and –15 Volt power supplies on the MOD-1020 board, but have no function on the TAC1020 and TAC1025. They may be connected to ±15 Volt power supplies but no current will be drawn from the board.

All power and ground pins must be connected. The TAC1020 and TAC1025 are rated for use at up to 70°C in still air. They may be used at temperatures up to 85°C with 500 LFPM of moving air.

Board Interconnections

Signal Type	Signal Name	Function	Value	Pin
Power	V_{CC}	+5 Volt Supply	+5.0V	11
	V_{EE}	–5.2 Volt Supply	–5.2V	5
Ground	GND	Ground	0.0V	1,4,8,12,13,35
Inputs	A_{IN1}	Analog Input	see text	9
	A_{IN2}	Analog Input	see text	10
	ENCODE	Convert Clock	ECL	2
	$\overline{\text{ENCODE}}$	$\overline{\text{Convert Clock}}$	ECL	3
Outputs	DR	Data Ready	ECL	36
	$\overline{\text{DR}}$	$\overline{\text{Data Ready}}$	ECL	34
	Bit 1	MSB	ECL	33
	$\overline{\text{Bit 1}}$	$\overline{\text{MSB}}$	ECL	32
	Bit 2		ECL	30
	$\overline{\text{Bit 2}}$		ECL	31
	Bit 3		ECL	28
	$\overline{\text{Bit 3}}$		ECL	29
	Bit 4		ECL	27
	$\overline{\text{Bit 4}}$		ECL	26
	Bit 5		ECL	25
	$\overline{\text{Bit 5}}$		ECL	24
	Bit 6		ECL	23
	$\overline{\text{Bit 6}}$		ECL	22
	Bit 7		ECL	20
	$\overline{\text{Bit 7}}$		ECL	21
	Bit 8		ECL	18
	$\overline{\text{Bit 8}}$		ECL	19
	Bit 9		ECL	16
	$\overline{\text{Bit 9}}$		ECL	17
	Bit 10	LSB	ECL	14
	$\overline{\text{Bit 10}}$	$\overline{\text{LSB}}$	ECL	15
	NC	Not Connected	open	6,7

Figure 1. Timing Diagram, TAC1020

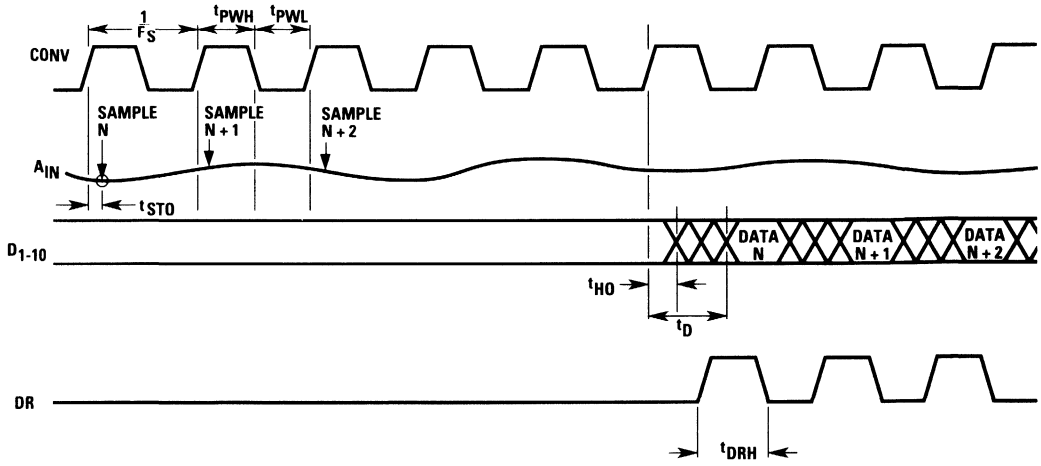
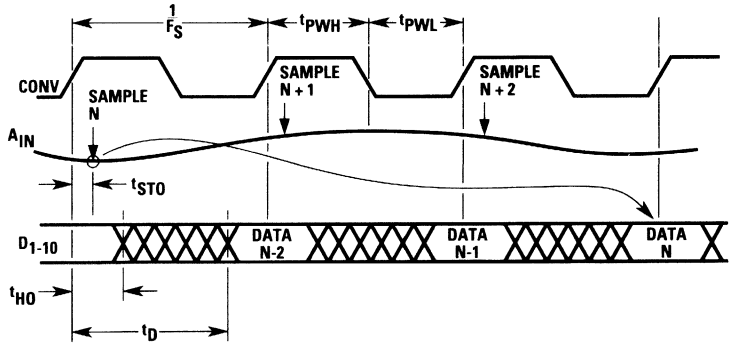


Figure 2. Timing Diagram, TAC1025



Output Coding Table

V_{IN}	$D_1 \bullet\bullet\bullet D_{10}$ MSB LSB
>1.000 V	1111111111
1.000 V	1111111111
0.998 V	1111111110
• •	
• •	
0.002 V	1000000000
0.000 V	0111111111
–0.002 V	0111111110
• •	
• •	
–0.998 V	0000000001
–1.000 V	0000000000

Notes: 1. 2 Volt peak-to-peak input range, A_{IN1} or A_{IN2}.
2. Voltages are at code centers.

Figure 3. ENCODE Input Equivalent Circuit

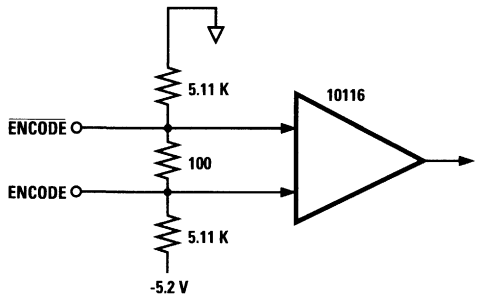
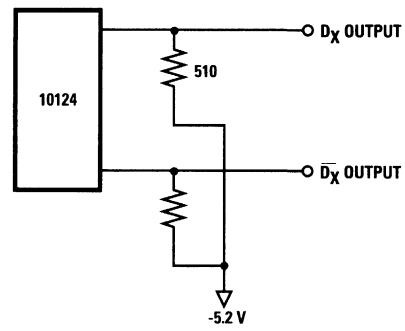


Figure 4. Digital Output Equivalent Circuit



Absolute maximum ratings (beyond which the board may be damaged)[1]

Supply Voltages

V_{CC}	−0.5 to +7.0V
V_{EE}	+0.5 to -7.0V

Input Voltages

V_{IN1} V_{IN2}	V_{CC} to V_{EE}
ENCODE, $\overline{\text{ENCODE}}$	V_{CC} to V_{EE}

Digital Outputs

Applied Voltage[2]	+0.5V to V_{EE}
Applied Current[3]	50mA
Short-circuit duration (single output to GND)	1 sec

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

Operating conditions[1]

Parameter		Conditions	Min	Nom	Max	Unit
V_{CC}	Positive Supply Voltage		4.75	5.0	5.25	V
V_{EE}	Negative Supply Voltage		−5.0	−5.2	−5.5	V
V_{IN}	Analog Input Voltage Range	$A_{IN1} = A_{IN2}$		±0.5		V
		A_{IN1} or A_{IN2}		±1.0		V
t_{PWL}	ENCODE Pulse Width,LOW		15			ns
t_{PWH}	ENCODE Pulse Width, HIGH		10			ns
	ENCODE Signal Duty Cycle				70	%
t_{RT}	ENCODE Pulse Rise Time				5	ns
t_{FT}	ENCODE Pulse Fall Time				5	ns
V_{IL}	Input Voltage, Logic LOW			−1.7		V
V_{IH}	Input Voltage, Logic HIGH			−0.9		V
R_L	Output Load Resistance	Line-to-Line	75			Ω
T_A	Ambient Temperature		0		70	°C

Electrical characteristics[1]

Parameter		Conditions	Min	Typ	Max	Unit
R_{IN}	Analog Input Resistance[2]	$A_{IN1} = A_{IN2}$	495	500	505	Ω
		A_{IN1} or A_{IN2}	990	1000	1010	Ω
C_{IN}	Input Capacitance	A_{IN1}, A_{IN2}		15		pF
V_{OH}	Output Voltage, Logic HIGH	75Ω Line-to-Line		–0.9		V
V_{OL}	Output Voltage, Logic LOW	75Ω Line-to-Line		–1.7		V
TAC1020						
I_{CC}	Positive Supply Current[2]			800	1100	mA
I_{EE}	Negative Supply Current[2]			750	1000	mA
P_D	Power Dissipation	V_{CC}, V_{EE} = Max			7.9	11.3W
TAC1025						
I_{CC}	Positive Supply Current[2]			700	800	mA
I_{EE}	Negative Supply Current[2]			825	900	mA
P_D	Power Dissipation	V_{CC}, V_{EE} = Max			7.8	9.2W

Notes:
1. Unless otherwise specified, parameters are guaranteed for T_A = 0°C to +70°C, V_{CC} = +5.0 Volts, V_{EE} = –5.2 Volts.
2. T_A = 25°C only.
3. Factory potentiometer adjustment.

Switching characteristics[1]

Parameter		Conditions	Min	Typ	Max	Unit
t_{DO}	Data Output Delay Time[2]	C_{LOAD} = 50pF			5	ns
t_R	Digital Output Rise Time			5		ns
t_F	Digital Output Fall Time			5		ns
TAC1020						
f_S	Maximum Conversion Rate	V_{CC}=V_{EE}=Min	20			Msps
t_{STO}	Sampling Time Offset		3	5	7	ns
t_{DRH}	Data Ready Pulse Width	20 Msps	22	25	28	ns
TAC1025						
f_S	Maximum Conversion Rate	V_{CC}=V_{EE}=Min	25			Msps
t_{STO}	Sampling Time Offset		2	2.5	3	ns
t_{DRH}	Data Ready Pulse Width	25 Msps	17	20	26	ns

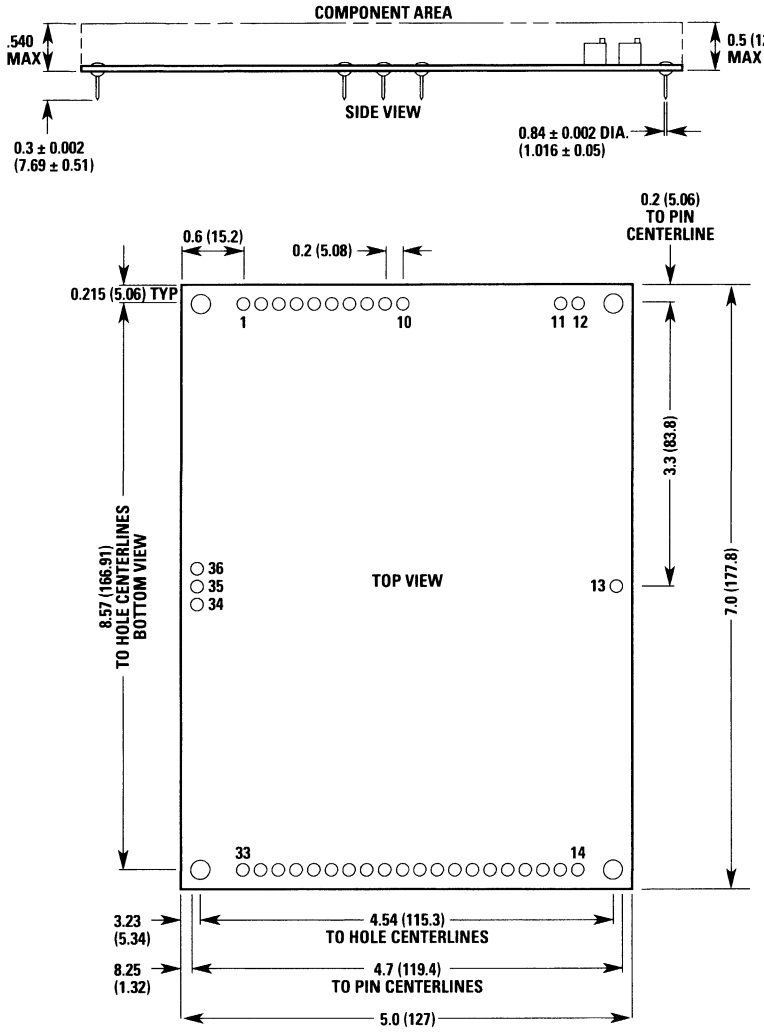
Notes:
1. Unless otherwise specified, parameters are guaranteed for T_A = 0°C to +70°C, V_{CC} = +5.0 Volts, V_{EE} = –5.2 Volts.
2. T_A = 25°C only.
3. Factory potentiometer adjustment.

System performance characteristics[1]

Parameter		Conditions	Min	Nom	Max	Units
LSB	LSB Weight	1V Input Range		1		mV
		2V Input Range		2		mV
E_{LD}	Differential Linearity[2]			±0.6	±1.0	LSB
E_{TC}	Linearity Tempco			5		ppm/°C
E_G	Gain Error[3]			±2		%FS
A_{TC}	Gain Tempco			150		ppm/°C
V_{OS}	Offset Voltage[3]			±15		mV
TC_{OF}	Offset Tempco			100		ppm/°C
E_{AP}	Aperture Error			2	5	ps
t_{TR}	Transient Response	to .1%, FS step	20		ns	
t_{OVR}	Overload Recovery	to .1% 2xFS step	20		ns	
BW	–3dB Input BW	Full-Scale Input	60		MHz	
		–40dBc Input		70		MHz
TAC1020						
SFDR	Spurious Free Dynamic Range, f_S = 20 Msps[2]	f_{IN} = 500kHz	64	68.9		dB
		f_{IN} = 5.0MHz	58	61.3		dB
SINAD	Signal-to-Noise and Distortion Ratio, f_S = 20 Msps[2]	f_{IN} = 500kHz	55	58.1		dB
		f_{IN} = 5.0MHz	50	55.7		dB
TAC1025						
SFDR	Spurious Free Dynamic Range, f_S = 20 Msps[2]	f_{IN} = 500kHz	64	68.9		dB
		f_{IN} = 5.0MHz	53	60.7		dB
		f_{IN} = 10MHz	49	53.2		dB
SINAD	Signal-to-Noise and Distortion Ratio, f_S = 20 Msps[2]	f_{IN} = 500kHz	55	58.2		dB
		f_{IN} = 5.0MHz	51	55.4		dB
		f_{IN} = 10MHz	46	49.1		dB

Notes:
1. Unless otherwise specified, parameters are guaranteed for T_A = 0°C to +70°C, V_{CC} = +5.0 Volts, V_{EE} = –5.2 Volts.
2. T_A = 25°C only.
3. Factory potentiometer adjustment.

Figure 5. Mechanical Configuration



Ordering Information

Product Number	Description	Order Number
TAC1020P3C	20 Msps A/D Converter Board	TAC1020P3C
TAC1025P3C	25 Msps A/D Converter Board	TAC1025P3C

A

Life Support Policy

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TDC1020

High-Speed Monolithic A/D Converter

10-Bit, 20Msps

The TRW TDC1020 is a 20Msps (MegaSample Per Second) full-parallel (flash) analog-to-digital converter, capable of converting a video signal into a stream of 10-bit digital words.

All outputs of the device are TTL compatible, and will provide the conversion in unsigned magnitude, or two's complement format, and either inverted or noninverted. An output signal indicating overflow condition is also provided for added flexibility. All digital inputs to the device are TTL compatible.

Features

- 10-Bit Resolution
- 20Msps Conversion Rate
- Overflow Flag
- Sample-And-Hold Circuit Not Required
- TTL Digital Interface
- Selectable Output Format

Applications

- Medical Imaging Systems
- Video Data Conversion
- Radar Data Conversion
- High-Speed Data Acquisition
- Process Control

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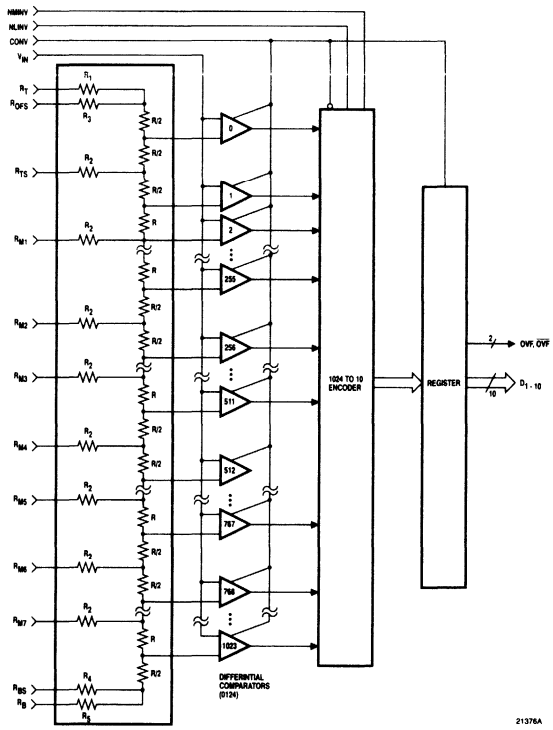
Functional Block Diagram



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Functional Description

General Information

The TDC1020 is a flash analog-to-digital (A/D) converter in which each of the 1024 comparators has one input biased at one of the transition points of the transfer function and all of the other comparator inputs are connected to the analog input signal. The output of the comparator array is sometimes referred to as a "thermometer" code as all of comparators biased at voltages more positive than the input voltage will be off and the rest will be on. The thermometer code from the comparator array is encoded into an 11-bit code (10 data bits plus an overflow bit). The format of the code that is encoded is determined by the format controls NMINV and NLINV so that the data presented to the output latches is in binary, two's complement or inverted data format.

Power and Thermal Management

The TDC1020 operates from two supply voltages, +5.0V and −5.2V. The bulk of the current drawn by the positive supply is returned through the negative supply, however, the positive supply should be referenced to digital ground (D_{GND}) and the negative supply to analog ground (A_{GND}). All power and ground pins must be connected. The maximum power is drawn at the lower limit of the operating temperature range. When the device is being operated at elevated temperatures, the power dissipation drops, however, thermal management will then be a consideration. The TDC1020 is rated for operation in a 70°C ambient temperature in still air.

The power dissipation decreases with increasing temperature. TRW specifies the absolute maximum I_{EE} and I_{CC} specifications in the ***Electrical Characteristics Table***. The worst case conditions are $V_{CC}=5.25V$, $V_{EE}=-5.5V$ and the case temperature equal to 0°C. The case temperature of 0°C is, however, a transient condition since the device immediately warms up and decreases its power dissipation, upon power up. For typical steady state power dissipation as a function of ambient temperature, please see ***Figure 7***.

It is possible to relax the temperature requirements of the device by providing adequate heat sinking.

Reference

The bias voltages for the comparator array are provided by use of a serial chain of 1024 equal-valued resistors across which the reference voltage is applied. Seven equally separated mid-point adjustment taps are provided to allow the user to optimize the integral linearity of the device. In addition, there are sense leads on the top and bottom of the resistor chain which allow the user to minimize the offset and gain errors of the device. It is recommended that the user drive R_{M2}, R_{M4} and R_{M6} in order to obtain optimal device performance. One method for driving the references is shown in the ***Typical Interface Circuit***. The reference top and reference bottom sources must be able to source or sink the reference current and since noise on these leads will lead to inaccurate conversions, they should be bypassed with a capacitor to A_{GND}. There are in addition 4 more reference taps, the use of which is not required to obtain 0.1% integral linearity. It is recommended that these pins be left open (no connection).

Format Control

There are two inputs provided on the TDC1020 which control the output format of the device. When NMINV is connected to a logic LOW, the MSB is inverted. When NLINV is connected to a logic LOW D_2 through D_{10} will be inverted. By using various combinations of these commands the user can select any of the following output data formats: binary, inverted binary, two's complement, inverted two's complement. The ***Output Coding Table*** shows the output formats generated for each of the control states.

Convert

The analog input to the TDC1020 is sampled at a time t_{STO} after the rising edge of the CONV signal. The output data from the 1024 comparators is encoded into the proper format and the final result is transferred to the output latches on the next rising edge. This timing is shown in the ***Timing Diagram (Figure 1)***. Note that there are minimum LOW and HIGH requirements of the CONV signal (t_{PWH}, t_{PWL}) which must be met for proper device operation. In addition, the performance is generally improved if the CONV signal is LOW for as long as possible. A circuit which provides an optimized waveshape CONV signal to the TDC1020 is shown on the ***Typical Interface Circuit***.

Analog Input

The analog input to the TDC1020 has an equivalent circuit shown in *Figure 2*. It should be noted that the major component of the input impedance is capacitance, and the input range is 4Vp-p. A low-impedance driving circuit is recommended for the TDC1020 to obtain good dynamic performance. All analog inputs to the TDC1020 must be connected to insure proper operation of the A/D converter.

Outputs

The data and overflow outputs of the TDC1020 are TTL compatible, capable of driving four low power Schottky TTL (54/74 LS) unit loads. The outputs hold the previous data a minimum time t_{HO} after the rising edge of the CONV signal. New data becomes valid after a maximum delay time, t_D.

No Connects

There are several pins labelled No Connect (NC) which have no electrical connection to the chip. These pins should be connected to A_{GND} for best noise performance.

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TDC1020 Package Interconnections

Signal Type	Signal Name	Function	Value	J1 Package Pins	G0 Package Pins
Power	V_{CC}	Positive Supply Voltage	5.0V	13, 14, 19, 20, 40, 58	K4, K5, L7, K8, C11, B1
	V_{EE}	Negative Supply Voltage	−5.2V	12, 15, 16, 17, 18, 21	L3, L5, K6, L6, K7, L8
	D_{GND}	Digital Ground	0.0V	10, 11, 22, 23	L2, K3, L10, K10
	A_{GND}	Analog Ground	0.0V	43, 55	A10, A3
Reference	R_T	Reference Resistor, Top	2.0V	59	C2
	R_{OFS}	Overflow Sense	2.0V	57	B2
	R_{TS}	Reference Resistor, Top Sense	2.0V	60	C1
	R_{M1}	Reference Resistor, 1/8 Tap	1.5V [1]	54	B3
	R_{M2}	Reference Resistor, 2/8 Tap	1.0V [1]	53	A4
	R_{M3}	Reference Resistor, 3/8 Tap	0.5V [1]	51	A5
	R_{M4}	Reference Resistor, 4/8 Tap	0.0V [1]	49	B6
	R_{M5}	Reference Resistor, 5/8 Tap	−0.5V [1]	47	A8
	R_{M6}	Reference Resistor, 6/8 Tap	−1.0V [1]	45	A9
	R_{M7}	Reference Resistor, 7/8 Tap	−1.5V [1]	44	B9
	R_B	Reference Resistor, Bottom	−2.0V	39	C10
	R_{BS}	Reference Resistor, Bottom Sense	−2.0V	41	B11
Format Control	NMINV	Not MSB Invert	TTL	63	E2
	NLINV	Not LSB Invert	TTL	28	J11
Convert	CONV	Convert	TTL	36	D11
Analog Input	V_{IN}	Analog Signal Input	+2 to −2V	46, 48, 50, 52	B8, B7, B5, B4
Outputs	OVF	Overflow	TTL	1	E1
	$\overline{OVF}$	Overflow Complement	TTL	2	F2
	D_1 MSB	Most Significant Bit	TTL	3	F1
	D_2		TTL	4	G2
	D_3		TTL	5	G1
	D_4		TTL	29	H10
	D_5		TTL	30	H11
	D_6		TTL	31	G11

Note: 1. Measured values.

TDC1020 Package Interconnections (cont.)

Signal Type	Signal Name	Function	Value	J1 Package Pins	G0 Package Pins
Outputs	D_7		TTL	32	F10
	D_8		TTL	33	F11
	D_9		TTL	34	E11
	D_{10} LSB	Least Significant Bit	TTL	35	D10
No Connects	NC	No Connection	Open	6, 7, 8, 9, 24, 25, 26, 27, 37, 38, 42, 56, 61, 62, 64	H2, H1, J2, J1, K1, K2, L4, K9, L9, K11, J10, G10, E10, B10, A7, A6, A2, D2, D1

Output Coding Table

	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
Input	NMINV = 1 NLINV = 1	NMINV = 0 NLINV = 0	NMINV = 0 NLINV = 1	NMINV = 1 NLINV = 0
	MSB – LSB (OVF)			
>2.000V	0000000000(1)	1111111111(1)	1000000000(1)	0111111111(1)
2.000V	0000000000(0)	1111111111(0)	1000000000(0)	0111111111(0)
1.996V	0000000001(0)	1111111110(0)	1000000001(0)	0111111110(0)
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
0.004V	0111111111(0)	1000000000(0)	1111111111(0)	0000000000(0)
0.000V	1000000000(0)	0111111111(0)	0000000000(0)	1111111111(0)
–0.004V	1000000001(0)	0111111110(0)	0000000001(0)	1111111110(0)
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
–1.996V	1111111110(0)	0000000001(0)	0111111110(0)	1000000001(0)
–2.000V	1111111111(0)	0000000000(0)	0111111111(0)	1000000000(0)

Note: Input voltages are at code centers.

Figure 1. Timing Diagram

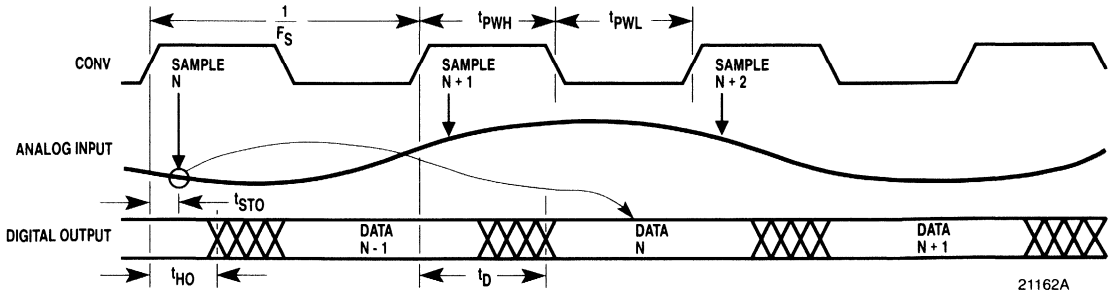
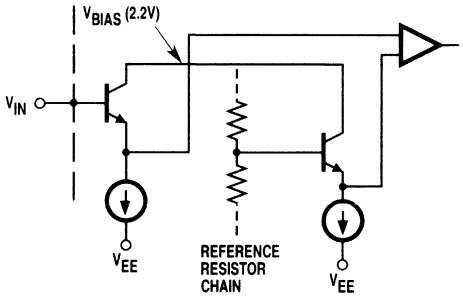
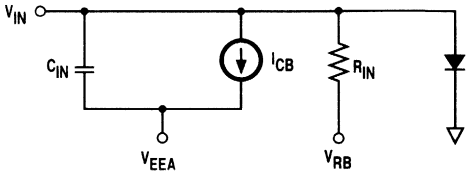


Figure 2. Simplified Analog Input Equivalent Circuits





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

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Figure 3. Equivalent Input Circuits Convert, NMINV, and NLINV

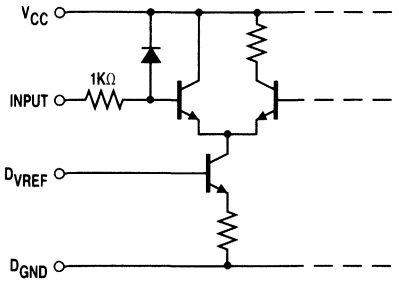

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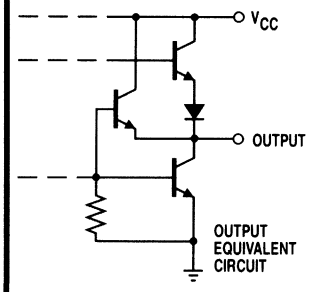
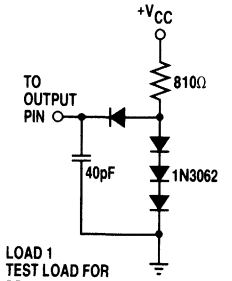
Figure 4. Output Circuits





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Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND}) ..... −0.5 to +6.0V
V_{EE} (measured to A_{GND}) ..... +5.0 to −6.0V
A_{GND} (measured to D_{GND}) ..... −1.0 to +1.0V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND}) ..... −0.5 to +5.5V
V_{IN} (measured to A_{GND}) ..... V_{CC} to V_{EE}V
Any reference (measured to A_{GND}) ..... V_{CC} to V_{EE}V
V_{RT} (measured to V_{RB}) ..... −1.0 to +4.4V

Output

Applied voltage measured to D_{GND} [2] ..... −0.5 to +5.5V
Applied current, externally forced [3,4] ..... −1.0 to +6.0mA
Short-circuit duration (single output in HIGH state to ground) ..... 1 Second
Sense lead current ..... −1.0 to 1.0mA

Temperature

Operating, ambient ..... −55 to +90°C
junction ..... +175°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Commercial			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{EE}	Negative Power Supply Voltage	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	22			22			ns
t_{PWH}	CONV Pulse Width, HIGH	18			20			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{RM2}	Reference Tap, 1/4-Scale	0.8	1.0	1.2	0.8	1.0	1.2	V
V_{RM4}	Reference Tap, 1/2-Scale	−0.2	0.0	0.2	−0.2	0.0	0.2	V
V_{RM6}	Reference Tap, 3/4-Scale	−0.8	−1.0	−1.2	−0.8	−1.0	−1.2	V
V_{RT}	Most Positive Reference Voltage	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{RB}	Most Negative Reference Voltage	−1.8	−2.0	−2.2	−1.8	−2.0	−2.2	V
$V_{RT}-V_{RB}$	Reference Voltage Differential	3.6	4.0	4.4	3.6	4.0	4.4	V

Operating conditions (cont.)

Parameter		Temperature Range						Units
		Commercial			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{IN}	Input Voltage Range	V_{RB}	±2.0	V_{RT}	V_{RB}	±2.0	V_{RT}	V
T_A	Ambient Temperature, C-Grade	0		70				°C
T_C	Case Temperature, V-Grade				−55		125	°C

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Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Commercial		Extended		
			Min	Max	Min	Max	
I_{CC}	Total Positive Supply Current	$V_{CC}=V_{EE}=$ Max		850		850	mA
I_{EE}	Total Negative Supply Current	$V_{EE}=$ Max		−500		−500	mA
I_{REF}	Reference Current	V_{RT}, $V_{RB}=$ Nom		50		50	mA
R_{REF}	Reference Chain Resistance	V_{RT}, $V_{RB}=$ Nom	80		80		Ohms
R_{IN}	Analog Input Resistance	V_{RT}, $V_{RB}=$ Nom, $V_{IN}=V_{RB}$	3000		2000		Ohms
C_{IN}	Analog Input Capacitance	V_{RT}, $V_{RB}=$ Nom, $V_{IN}=V_{RB}$		300		300	pF
I_{CB}	Input Constant Bias	$V_{EE}=$ Max		2		3	mA
I_{IL}	Input Current, Logic LOW	$V_{CC}=$ Max, $V_I=0.5V$		50		50	μA
I_{IH}	Input Current, Logic HIGH	$V_{CC}=$ Max, $V_I=2.4V$		100		100	μA
I_I	Input Current, Maximum	$V_{CC}=$ Max, $V_I=5.25V$		100		100	μA
V_{OL}	Output Voltage, Logic LOW	$V_{CC}=$ Min, $I_{OL}=$ Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	$V_{CC}=$ Min, $I_{OL}=$ Max	2.4		2.4		V
I_{OS}	Short-Circuit Output Current	$V_{CC}=$ Max, output HIGH, one pin to ground, one second duration max.		−35		−35	mA
C_I	Digital Input Capacitance	$T_A=25°C$, f=1MHz		15		15	pF

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Commercial		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	$V_{EE}=$ Min, $V_{CC}=$ Min	20		20		Msps
t_{STO}	Sampling Time Offset	$V_{EE}=$ Max, $V_{CC}=$ Max	3	17	3	17	ns
t_D	Output Delay	$V_{EE}=$ Max, $V_{CC}=$ Max		37		43	ns
t_{HO}	Output Hold Time	$V_{EE}=$ Max, $V_{CC}=$ Max	5		5		ns

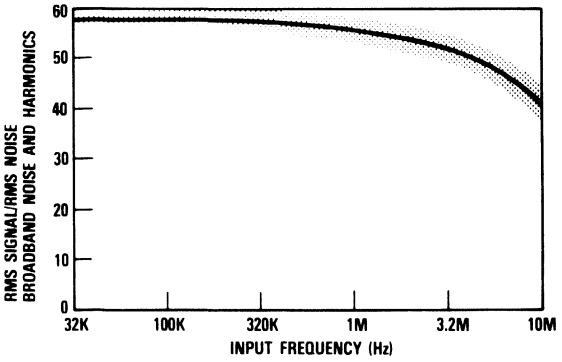
System performance characteristics within specified operating conditions

Parameter		Test Conditions	Typ	Temperature Range				Units
				Commercial		Extended		
				Min	Max	Min	Max	
E_{LI}	Linearity Error, Integral	Reference Taps Open	±0.1		±0.2		±0.2	%
E_{LI}	Linearity Error, Integral	Reference Taps Adjusted	±0.05		±0.1		±0.1	%
E_{LD}	Linearity Error, Differential	Reference Taps Open	±0.05		±0.1		±0.1	%
CS	Code Size			5	225	5	225	% Nominal
E_{OT}	Offset Error, Top				25		30	mV
E_{OB}	Offset Error, Bottom				−30		−35	mV
T_{CO}	Offset Error Tempco				±10		±20	μA/°C
t_{TR}	Transient Response	Full-Scale Input Step, Settling to ±32 LSBs	20		30		30	ns
BW	Full-Power Bandwidth	Full-Scale Input	10	5				MHz
SNR	Signal-to-Noise Ratio	Note 1						
		F_{IN} = 1.0MHz	60	58		58		dB
		F_{IN} = 2.0MHz	59	56		56		dB
		F_{IN} = 5.0MHz	56	52		52		dB
		F_{IN} = 8.0MHz	54	47				dB
		F_{IN} = 10.0MHz	52	43				dB
SINAD	Signal-to-Noise And Distortion	Note 1						
		F_{IN} = 1.0MHz	59	55		52		dB
		F_{IN} = 2.0MHz	58	52		52		dB
		F_{IN} = 5.0MHz	54	48		45		dB
		F_{IN} = 8.0MHz	48	41				dB
		F_{IN} = 10.0MHz	43	39				dB
THD	Total Harmonic Distortion	Note 1						
		F_{IN} = 1.0MHz	−66	−58		−53		dBc
		F_{IN} = 2.0MHz	−64	−56		−53		dBc
		F_{IN} = 5.0MHz	−58	−52		−46		dBc
		F_{IN} = 8.0MHz	−50	−43				dBc
		F_{IN} = 10.0MHz	−44	−41				dBc
SFDR	Spurious-Free Dynamic Range	Note 1						
		F_{IN} = 1.0MHz	70	53		53		dB
		F_{IN} = 2.0MHz	68	54		54		dB
		F_{IN} = 5.0MHz	63	48		48		dB
		F_{IN} = 8.0MHz	55	40				dB
		F_{IN} = 10.0MHz	48	35				dB
E_{AP}	Aperture Error			50				ps
DP	Differential Phase	F_S = 4 x NTSC Subcarrier, Reference Taps Adjusted	0.3		0.5			Degree
DG	Differential Gain	F_S = 4 x NTSC Subcarrier, Reference Taps Adjusted	0.8		1.0			%

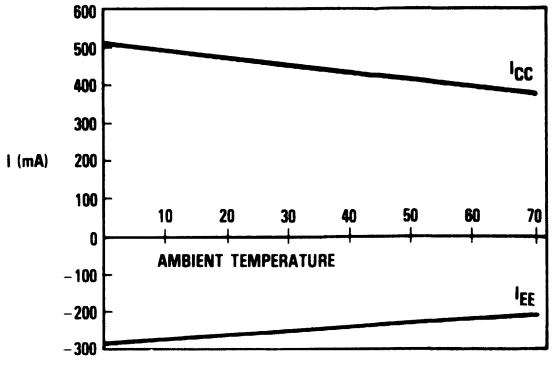
Note: 1. F_S = 20Msps, Reference Taps Adjusted, $V_{CC} = V_{EE}$ = Nom, T_A = 25°C.

Typical Performance Curves

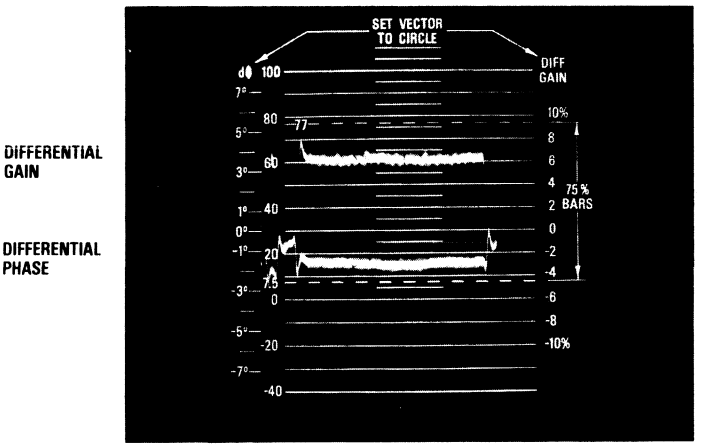
A. Typical SNR vs. Input Frequency



B. Typical Supply Current vs. Temperature



C. Differential Gain (Top) and Phase (Bottom) 15Msps NTSC Modulated Ramp Input



Calibration

Calibration of the TDC1020 consists of adjusting the reference taps so that the converters integral linearity, gain and offset errors are minimized. To minimize the offset errors the sense leads must be used properly. The sense leads are not designed to carry very much current (<1mA) and should therefore be used in a feedback loop to a high-impedance input such as that shown in the *Typical Interface Circuit*. When a circuit similar to that in the *Typical Interface Circuit* is used for generating the reference voltages, calibration can be achieved with the following procedure:

1. Apply an input to the input amplifier which is 1/2 LSB less than full-scale (A/D input = 1.998V) and adjust the gain so that the output of the A/D is toggling between full-scale and one LSB below full-scale (1111111111 and 1111111110 for binary conversions).
2. Apply an input to the input amplifier which is 1/2 LSB greater than zero-scale (A/D input = −1.998V) and adjust V_{RB} via the V_{RB} pot so that the output of the A/D is toggling between 0 and 1 (0000000000 and 0000000001 for binary conversions).

The A/D converter will now be calibrated to provide accurate conversions throughout its input range. To optimize the integral linearity of the device set up the "Subtractive Ramp Test" described on *page 6* of the *TRW Applications Note TP-30, "Understanding Flash A/D Converter Terminology,"* then adjust the mid-point taps to minimize the bow in the error curve.

Typical Interface

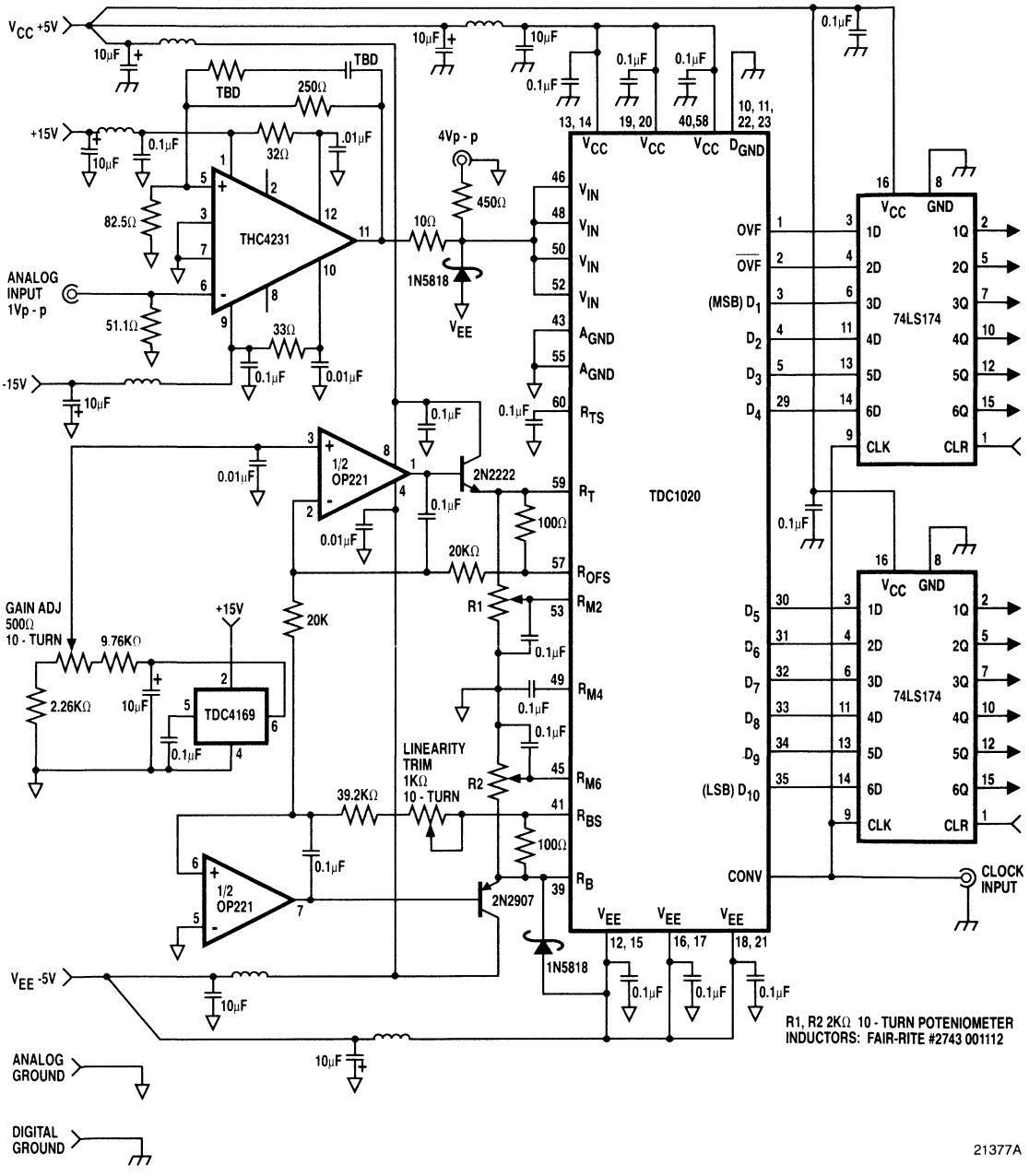
A Typical Interface Circuit is shown of the TDC1020. The analog input amplifier, a THC4231, is used to directly drive the A/D converter. This amplifier is set up to have a gain of four and will provide the recommended +2 to −2V input signal to the TDC1020 when it has a 1Vp-p input signal. All four analog input pins are connected in parallel to decrease the parasitic inductance. An LM313 is used to provide a stable reference voltage which is buffered by a dual op-amp, generating V_{RT} and V_{RB}. Both op-amps have their outputs buffered by an emitter follower to decrease the output impedance seen by the reference resistor chain. To minimize noise coupling into the reference resistor chain, bypass capacitors have been added, bypassing the reference taps to ground.

Since capacitive coupling from the digital signals to the analog input will adversely affect the converter performance, careful attention to board layout is recommended.

As is true with most bipolar integrated circuits, the substrate of the TDC1020 (V_{EE}) must be the most negative potential applied. This rule applies for all conditions of temperature, signal level and power supply sequencing. In many systems, the voltage reference generators and input driving amplifier are powered from voltages greater than the +5 and −5.2V of the TDC1020. Whenever this situation occurs, it is always possible for the V_{EE} inputs of the TDC1020 to be positive with respect to the V_{IN} or V_{RB} inputs when power supplies are cycled ON and OFF.

To protect the TDC1020 from latch-up due to substrate bias, TRW recommends the use of a 1N5818 Schottky diode connected between V_{EE} and V_{IN} and another between V_{EE} and V_{RB} with the anode of each diode connected to V_{EE}. The diodes prevent V_{IN} and V_{RT} from going more than 0.4V more negative than V_{EE}. This protection circuit is shown in *Figure 5*.

Figure 5. Typical Interface Circuit



Evaluation Board

The TDC1020E1C is a Eurocard-style printed circuit board designed to optimize the performance of, and to aid in the evaluation of the TDC1020 A/D converter. The board dimensions are 100mm x 160mm with a standard 64 pin double-row DIN male connector installed. A complementary 64 pin double-row DIN female connector is included with the board. The circuitry on the board includes reference voltage generators, wideband video input amplifier, and a TDC1012 12-bit D/A converter which may be used in evaluating certain parameters of the TDC1020.

The board employs only two conducting sides. Most of the circuit interconnections are on the bottom of the board while the top is mostly solid ground plane. SMA connectors are installed on the board to facilitate analog I/O and clocks. The board is calibrated and tested at the factory and is supplied complete with TDC1020 and TDC1012 installed.

Power and Ground

Four power supply voltages are required for the operation of the TDC1020E1C: $V_{CC} = +5V$, $V_{EE} = -5.2V$, $V+ = +15V$ and $V- = -15V$. All power inputs are decoupled to a single solid ground plane. All GND pins of the board are connected to the ground plane and it is recommended that all GND pins be used.

Voltage Reference Generator

The TDC1020E1C has two voltage reference generator circuits for driving the RT and RB terminals of the TDC1020. A variable +2.0V is applied to RT from U3A and Q2. A variable −2.0V is supplied to RB from U3B and Q1. The GAIN potentiometer, R11, provides ±10% adjustment range to both RT and RB voltages.

Video Input Amplifier

The input amplifier of the TDC1020E1C, U4, is a THC4231 current-feedback amplifier and has been designed to accept a ±0.5V input range and translate that signal to the +2 to −2V range of the TDC1020. The output of this amplifier can be monitored at the P6 SMA connector which is connected to the V_{IN} terminals of the TDC1020 through a 470Ω resistor. The OFFSET potentiometer, R10, gives a ±0.5V offset adjustment range to the board.

A/D Converter Inputs

The clock to the TDC1020, CONV, is normally brought onto the board through the SMA connector labeled "CONV P5." By installing jumper J12, this signal is routed through the edge connector pin B3. A terminating resistor, R25 may be installed on the board for terminating a CONV signal cable. The NMINV and NLINV inputs to the TDC1020 are pulled HIGH with resistors and may be pulled LOW by installing jumpers J15 and J17.

The analog signal input to the TDC1020E1C is brought onto the board by way of the SMA connector labeled "P3" through J9 and J10. A terminating resistor, R7, is included on the board for terminating a 50Ω analog input signal cable. Jumpers J10 and J11 permit the analog input signal to enter the board from edge-connector pin B28.

A/D Converter Data Outputs and D/A Converter Data Inputs

The ten data outputs of the TDC1020 are brought to edge-connector pins B5 through B14. These pins are located directly across the edge-connector from the corresponding data inputs of the TDC1012 D/A converter to simplify connection of A/D outputs to D/A inputs.

D/A Converter Inputs

The clock to the TDC1012 is normally brought onto the board through an SMA connector labeled "P9". This signal may also be brought onto the board from edge-connector pin B29 by installing jumper J21. A location for a terminating resistor, R57 is provided for clock cable termination.

D/A converter outputs are brought to SMA connectors labeled "OUT+ P7" and "OUT− P8." Load resistors of 51.1Ω are provided on the board to facilitate 50Ω cable connection to the board.

Potentiometer R58 is used to adjust the reference voltage to the TDC1012. This voltage is adjusted to −1.0V as part of the factory test and calibration procedure.

Removing jumper, J20, will put the TDC1012 into feedthru (unclocked) mode. This eliminates the requirement for a D/A clock signal, but will degrade the fidelity of the TDC1012 reconstruction.

THC4940 Track/Hold Option

The TDC1020E1C has been designed to accomodate the THC4940 Track/Hold amplifier in the analog signal path prior to the THC4231 wideband input amplifier. To install the THC4940 on the board jumper connections outlined on the ***Jumper Options Table*** should be followed. The TDC1020E1C can be configured to accept the analog input from either the edge-connector or the P3 SMA.

The Track/Hold timing signal is configured for TTL compatibility with the use of J2 and J8 which bias pin 2 of the THC4940 to TTL threshold. J5 applies the $\overline{\text{Hold}}$/Track timing signal to pin 1 of the THC4940. The $\overline{\text{Hold}}$/Track timing signal can be routed from SMA P2 or the edge-connector.

A

TDC1020E1C Eurocard Edge Connector Pinout

GND	A32	B32	V– (–15V)
GND	A31	B31	V+ (+15V)
GND	A30	B30	OVF
GND	A29	B29	D/A CLK INPUT
GND	A28	B28	ANALOG INPUT
GND	A27	B27	NC
GND	A26	B26	NC
GND	A25	B25	NC
GND	A24	B24	D/A CLK
GND	A23	B23	NC
GND	A22	B22	NC
GND	A21	B21	NC
GND	A20	B20	NC
GND	A19	B19	NC
GND	A18	B18	V_{CC} (+5V)
GND	A17	B17	NC
GND	A16	B16	NC
GND	A15	B15	NC
D/A D_1 MSB	A14	B14	A/D D_1 MSB
D/A D_2	A13	B13	A/D D_2
D/A D_3	A12	B12	A/D D_3
D/A D_4	A11	B11	A/D D_4
D/A D_5	A10	B10	A/D D_5
D/A D_6	A9	B9	A/D D_6
D/A D_7	A8	B8	A/D D_7
D/A D_8	A7	B7	A/D D_8
D/A D_9	A6	B6	A/D D_9
D/A D_{10}	A5	B5	A/D D_{10} LSB
D/A D_{11}	A4	B4	$\overline{OE}$
D/A D_{12} LSB	A3	B3	A/D CONV
GND	A2	B2	T/H DIGITAL INPUT
GND	A1	B1	V_{EE} (–5.2V)

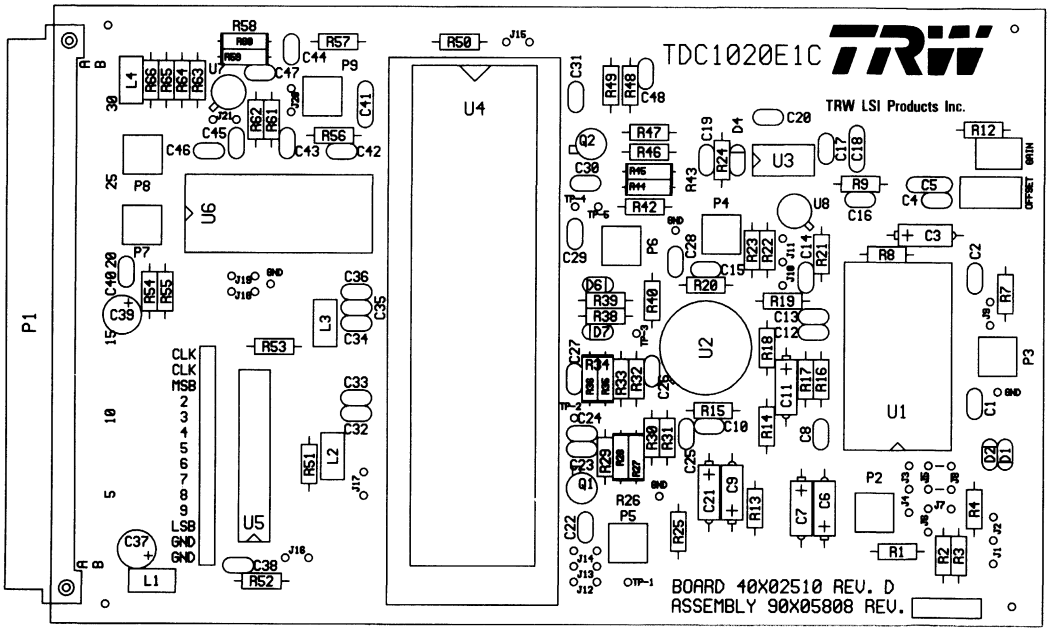
Mating Connectors for TDC1020E1C

AMP	532507-2	Wire-wrap
AMP	532507-1	Solder tail
Robinson-Nugent	RNE-64BS-W-TG30	Wire-wrap
Robinson-Nugent	RNE-64BS-S-TG30	Solder tail
Souriau	8609-264-6115-7550E1	Wire-wrap
Souriau	8609-264-6114-7550E1	Solder tail
Souriau	8609-264-6813-7550E1	Solder tail, right-angle bend

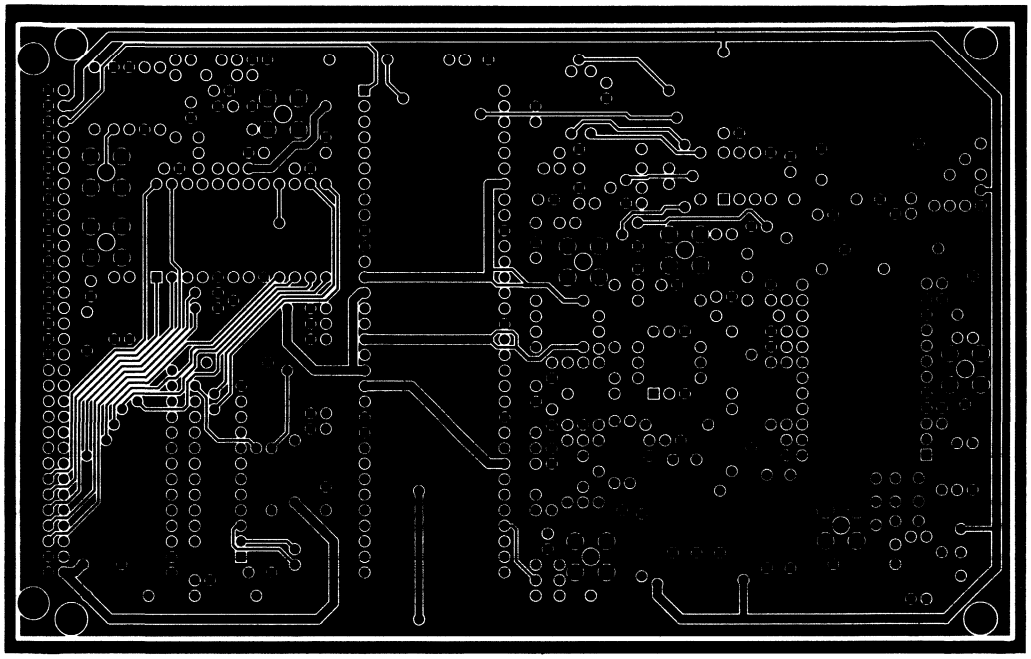
Jumper Options Table

Function	SMA-Connector	Edge-Connector	Termination
Analog Input Signal	for P3, use J9, J10	for B28, use J10, J11	R7
A/D Converter CONV	for P5, use J13	for B3, use J12, J13	R25
D/A Converter CLK	P9	for B29, use J21	R57
		for B3, use J12, J13, J14	R25
T/H Analog Input	for P3, remove J9, J10, J11	for B28, use J9, J11	R7
T/H Timing Input	for P2, use J4	for B2, use J3	J6, R1

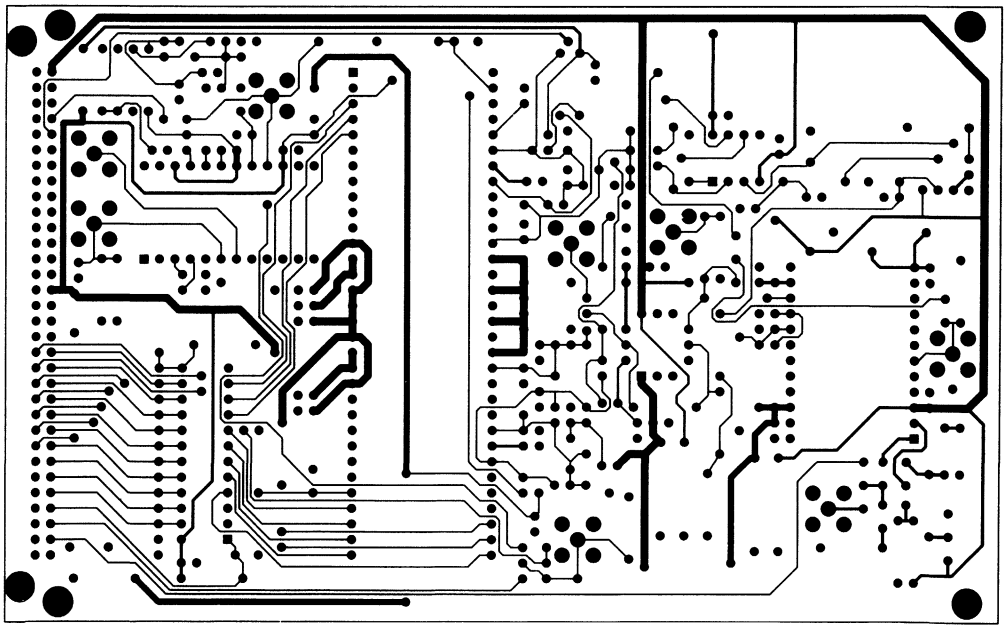
TDC1020E1C Silkscreen Layout



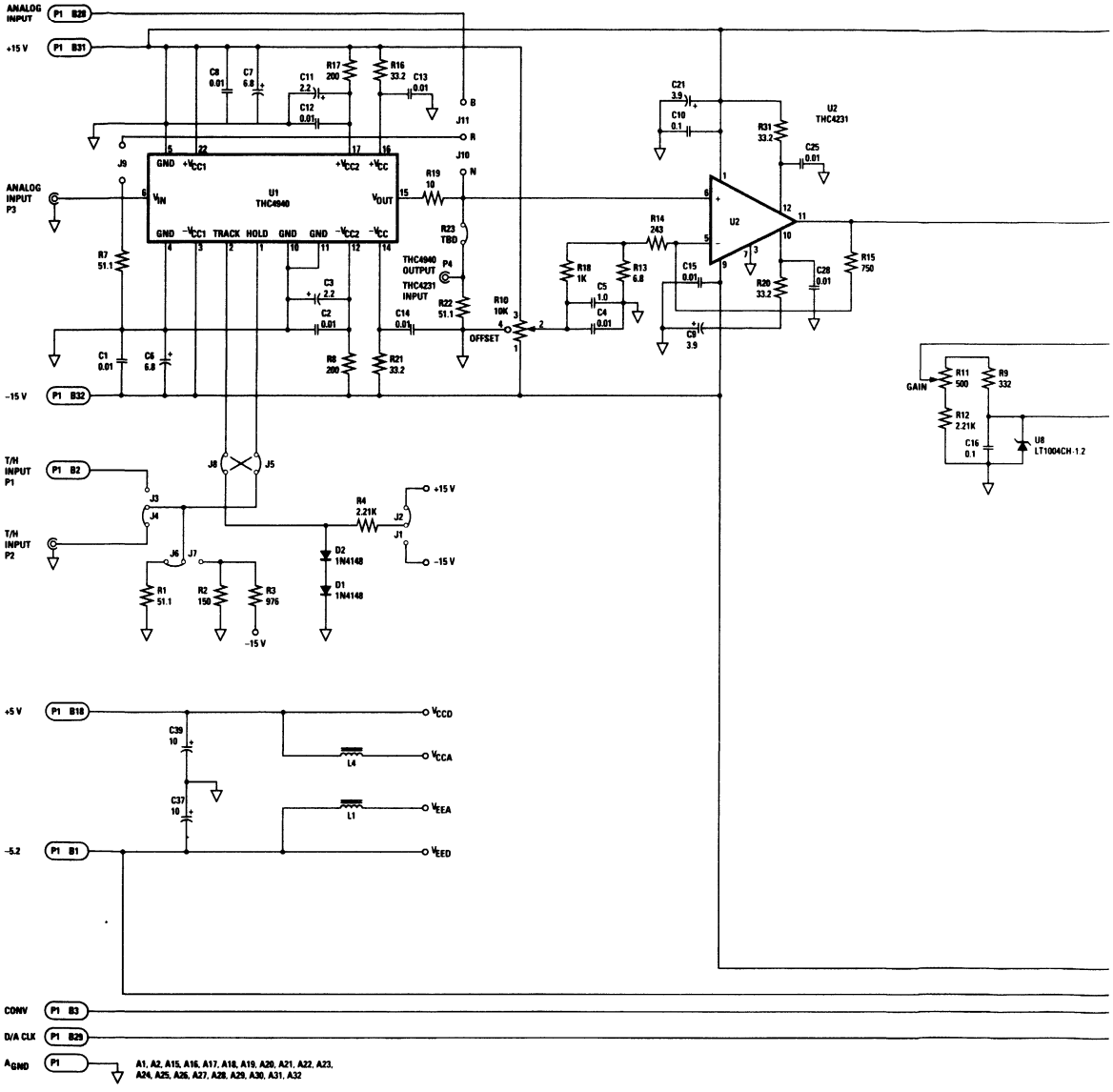
TDC1020E1C Component Side Layout

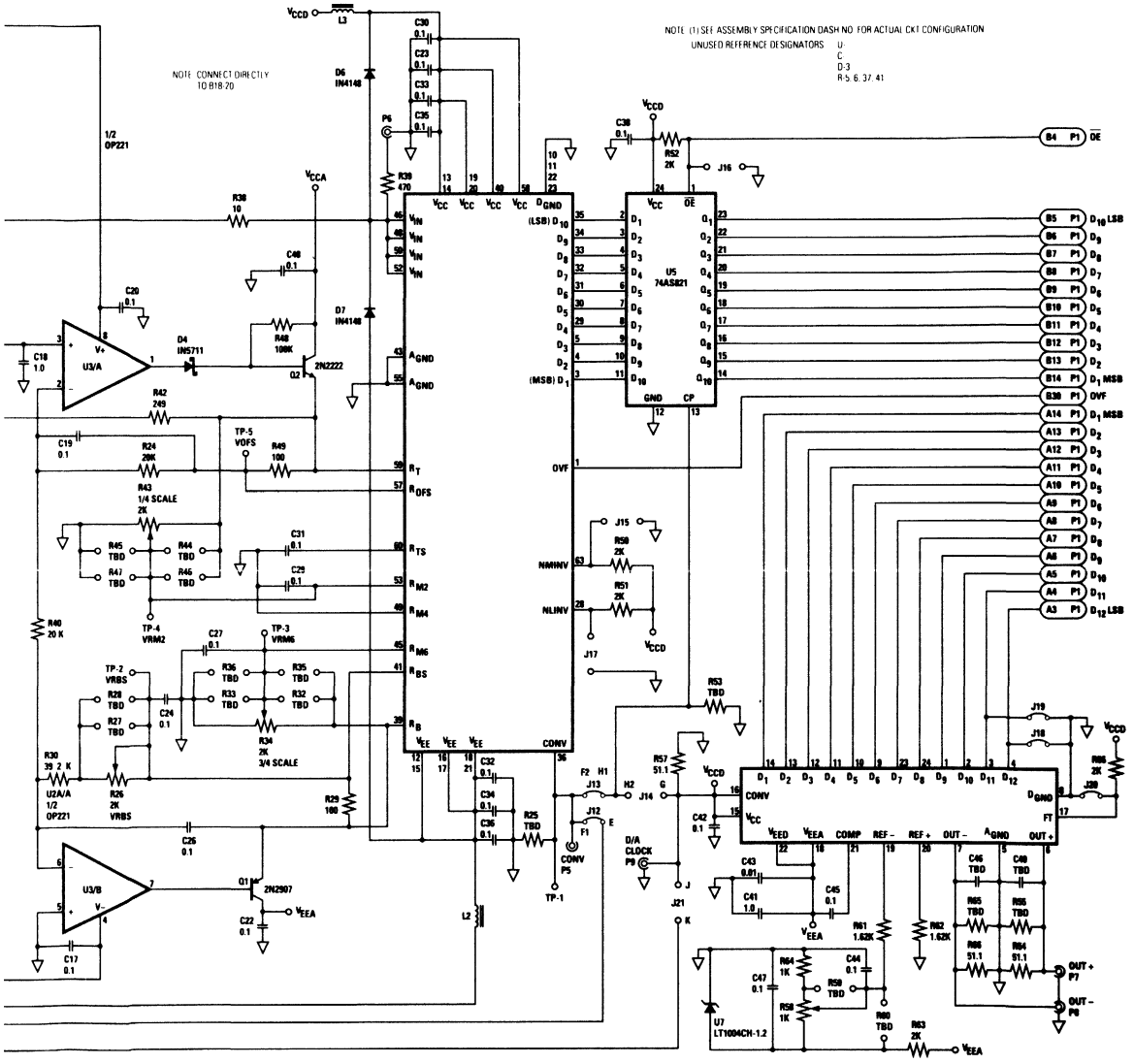


TDC1020E1C Circuit Side Layout



TDC1020E1C A/D Converter Schematic Diagram




NOTE (1) SEE ASSEMBLY SPECIFICATION DASH NO. FOR ACTUAL CKT CONFIGURATION
UNUSED REFERENCE DESIGNATORS U-
C-
D-3
R-5, 6, 37, 41
NOTE CONNECT DIRECTLY TO B18-20
U5 74AS821
U3/A
U3/B
U2A/A
1/2 OP221
2N2222
2N2907
IN5711
IN4148
LT1004CH-1.2
TP-1
TP-2 VRBS
TP-3 VRMS
TP-4 VRM2
TP-5 VOFS
D/A CLOCK
CONV
OVF
NMINV
NLINV
OUT+
OUT-

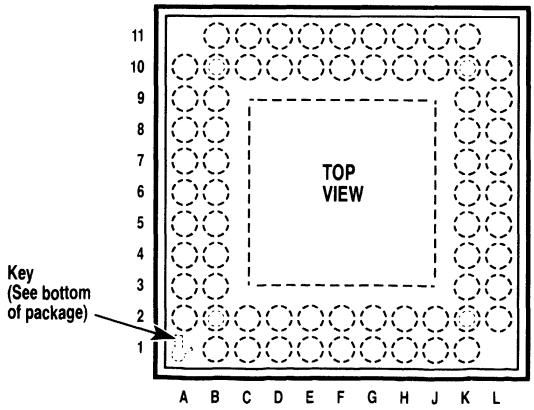
Ordering Information

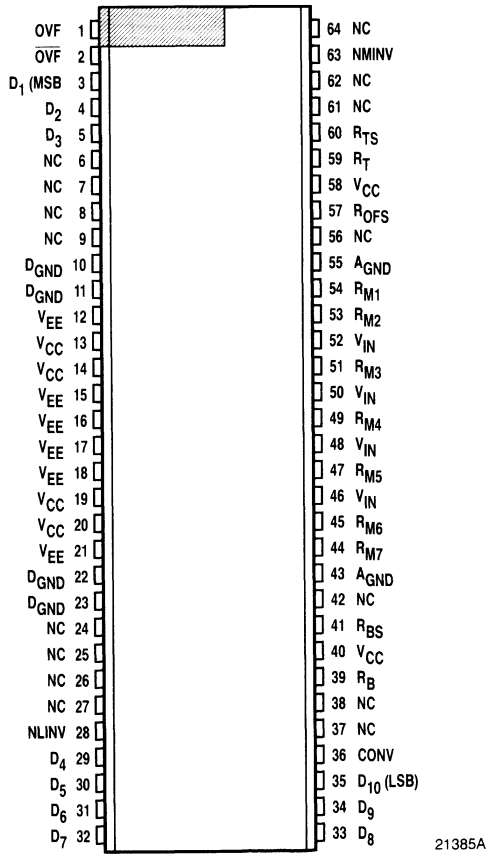
Product Number	Temperature Range	Screening	Package	Package Marking
TDC1020J1C	STD – T_A = 0°C to 70°C	Commercial	64 Pin Hermetic Ceramic DIP	1020J1C
TDC1020J1V	EXT – T_C = –55°C to 125°C	Military	64 Pin Hermetic Ceramic DIP	1020J1V
TDC1020G0C	STD – T_A = 0°C to 70°C	Commercial	68 Pin PGA	1020G0C
TDC1020G0V	EXT – T_C = –55°C to 125°C	Military	68 Pin PGA	1020G0V
TDC1020E1C	STD – T_A = 0°C to 70°C	– –	Eurocard Format Board With A/D Converter	TDC1020E1C

Pin Assignments

68 Pin Grid Array – G0 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A2	NC	B9	R_{M7}	F10	D_7	K4	V_{CC}
A3	A_{GND}	B10	NC	F11	D_8	K5	V_{CC}
A4	R_{M2}	B11	R_{BS}	G1	D_3	K6	V_{EE}
A5	R_{M3}	C1	R_{TS}	G2	D_2	K7	V_{EE}
A6	NC	C2	R_T	G10	NC	K8	V_{CC}
A7	NC	C10	R_B	G11	D_6	K9	NC
A8	R_{M5}	C11	V_{CC}	H1	NC	K10	D_{GND}
A9	R_{M6}	D1	NC	H2	NC	K11	NC
A10	A_{GND}	D2	NC	H10	D_4	L2	D_{GND}
B1	V_{CC}	D10	D_{10} LSB	H11	D_5	L3	V_{EE}
B2	R_{OFS}	D11	CONV	J1	NC	L4	NC
B3	R_{M1}	E1	OVF	J2	NC	L5	V_{EE}
B4	V_{IN}	E2	NMINV	J10	NC	L6	V_{EE}
B5	V_{IN}	E10	NC	J11	NLINV	L7	V_{CC}
B6	R_{M4}	E11	D_9	K1	NC	L8	V_{EE}
B7	V_{IN}	F1	D_1 MSB	K2	NC	L9	NC
B8	V_{IN}	F2	$\overline{OVF}$	K3	D_{GND}	L10	D_{GND}





64 Pin Hermetic Ceramic DIP – J1 Package

TDC1021

Use TDC1044 for New Designs

Monolithic A/D Converter

4-Bit, 25MSPS

The TRW TDC1021 is a 25 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting signals with full-power frequency components up to 10MHz into 4-bit digital words. A sample-and-hold circuit is not required. All digital inputs and outputs are TTL compatible.

The TDC1021 consists of 15 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs, in binary or offset two's complement coding.

Note: TRW recommends the use of the TDC1044 for new designs.

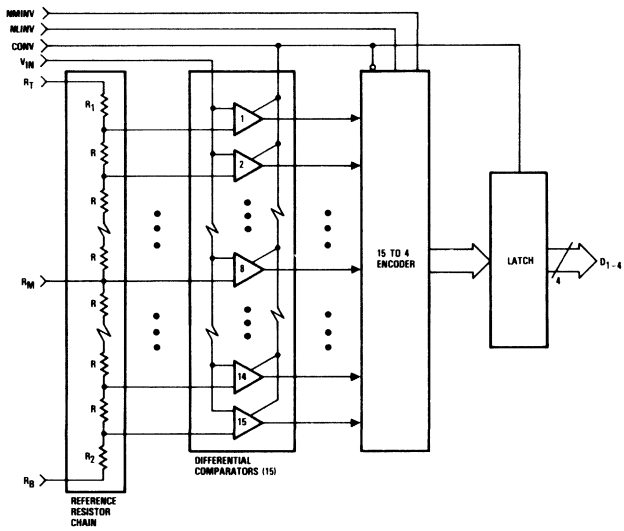
Features

- 4-Bit Resolution
- ±1/4 LSB Linearity
- Sample-And-Hold Circuit Not Required
- TTL Compatible
- 25MSPS Conversion Rate
- Selectable Output Format
- Available In 16 Lead DIP
- Standard/Extended Temperature Range

Applications

- Video Special Effects
- Radar Data Conversion
- High-Speed Multiplexed Data Acquisition
- Medical Imaging
- Image Processing

Functional Block Diagram



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Printed in the U.S.A.

TDC1025

Monolithic A/D Converter

8-Bit, 50Msps

The TRW TDC1025 is a 50Msps (MegaSample Per Second) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 12MHz into 8-bit digital words. A sample-and-hold circuit is not necessary. All digital inputs and outputs are ECL compatible.

The TDC1025 consists of 255 latching comparators, combining logic, and an output register. A differential ECL convert signal controls the conversion operation. The digital outputs will interface with differential or single-ended ECL. The device requires a single −5.2V power supply.

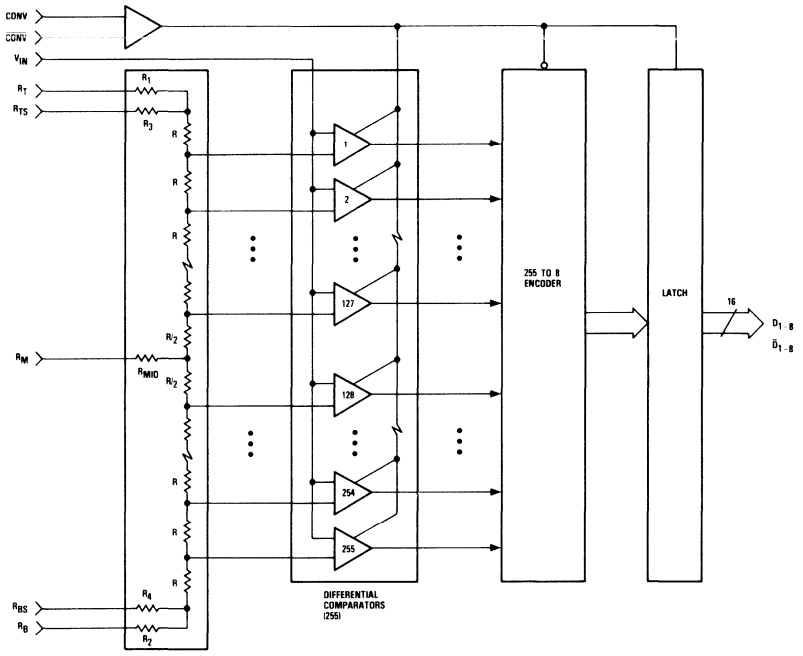
Features

- 8-Bit Resolution
- 50Msps Conversion Rate
- Sample-And-Hold Circuit Not Required
- Differential Or Single-Ended ECL Compatible
- Single −5.2V Power Supply
- Available In 68 Contact Or Leaded Chip Carrier

Applications

- Medical Electronics
- Fluid Flow Analysis
- Seismic Analysis
- Radar/Sonar
- Transient Analysis
- High-Speed Image Processing

Functional Block Diagram



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40G01330 Rev. F – 11/90
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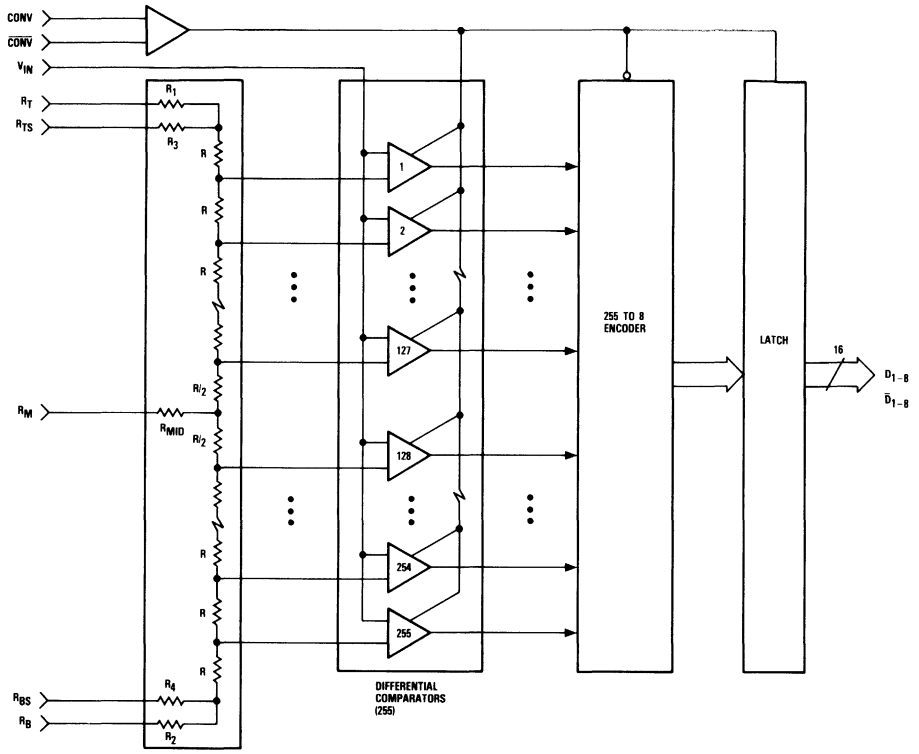
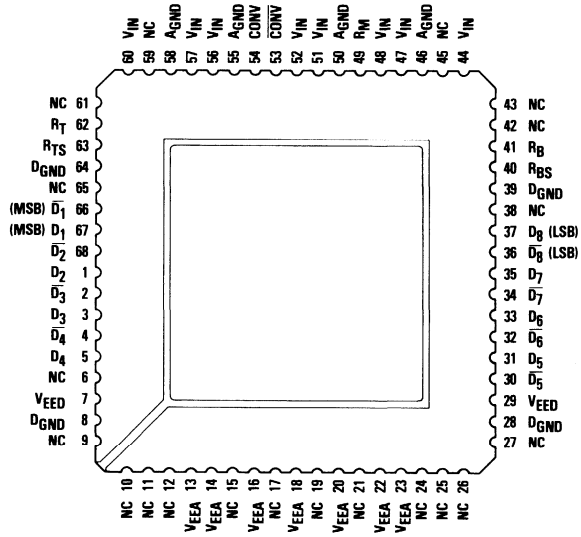
Functional Block Diagram



Pin Assignments



68 Contact Or Leaded Chip Carrier – C1, L1 Package

Functional Description

General Information

The TDC1025 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 255 reference voltages to produce an N-of-255 code (sometimes referred to as a "thermometer" code, as all the comparators below the signal will be on, and all those above the signal will be off). The encoding logic converts the N-of-255 code into binary format. The output latch holds the output constant between updates.

A

Power

The TDC1025 operates from a single -5.2V power supply. The separate analog and digital power pins, V_{EEA} and V_{EED}, both require -5.2V, and may be connected to the same power supply. However, separate decoupling of the analog and digital power pins is recommended (refer to Figure 5 for a typical decoupling circuit). The return for I_{EED}, the current drawn from the V_{EED} supply, is D_{GND}. The return for I_{EEA}, the current drawn from the V_{EEA} supply, is A_{GND}. The analog and digital ground planes should be separated to minimize ground noise and prevent ground loops, and connected back at the power supply. All power and ground pins must be connected.

Name	Function	Value	C1, L1 Package
V_{EED}	Digital Supply Voltage	-5.2V	Pins 7, 29
V_{EEA}	Analog Supply Voltage	-5.2V	Pins 13, 14, 16, 18, 20, 22, 23
D_{GND}	Digital Ground	0.0V	Pins 8, 28, 39, 64
A_{GND}	Analog Ground	0.0V	Pins 46, 50, 55, 58

Reference

The TDC1025 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and -2.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain ($V_{RT}-V_{RB}$) must be between 1.8V and 2.2V. The nominal voltages are V_{RT} = 0.0V, V_{RB} = -2.0V.

Two sense points, R_{TS} and R_{BS}, may be used to minimize the offset errors and temperature sensitivity. With sensing, resistors R_1 and R_2 (as shown in the Functional Block Diagram) are contained within the feedback loop, and no longer contribute to the offset error. The remaining offset errors, E_{OTS} and E_{OBS}, can be eliminated by the calibration method discussed under Calibration. The temperature sensitivity of this remaining offset error is specified by t_{COS}, Temperature Coefficient, Sensed. The sense resistors, R_3 and R_4 (as shown in the Functional Block Diagram) are approximately 1 kOhm. These resistors are not designed to carry the total reference current, and should not be used as reference inputs. If the sensed points are not used, these pins should be left open. The circuit in Figure 5 shows a typical sensing configuration.

A midpoint tap, R_M, allows the converter to be adjusted for optimum linearity, although adjustment is not necessary to meet the linearity specification. It can also be used to achieve a non-linear transfer function. The circuit shown in Figure 7 will provide approximately 1/2 LSB adjustment of the linearity midpoint. The characteristic impedance at this node is approximately 75 Ohms, and should be driven from a low-impedance source. Note that any load applied to this node will affect linearity. Noise introduced at this point, as well as the reference inputs and sense points may degrade the quantization process, resulting in encoding errors.

Due to the variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically, (as in an Automatic Gain Control circuit), a low-impedance reference source is required. The reference voltages may be varied dynamically at rates up to 10MHz.

Reference (Cont.)

Name	Function	Value	C1, L1 Package
R_T	Reference Resistor (Top)	0.0V	Pin 62
R_{TS}	Reference Resistor Sense (Top)		Pin 63
R_M	Reference Resistor (Middle)	-1.0V	Pin 49
R_B	Reference Resistor (Bottom)	-2.0V	Pin 41
R_{BS}	Reference Resistor Sense (Bottom)		Pin 40

Convert

The TDC1025 requires a differential ECL Convert (CONV) signal. Both convert inputs must be connected, with $\overline{CONV}$ being the complement of CONV. A sample is taken (the comparators are latched) within 10ns after the rising edge on the CONV pin. This time is t_{STO}, Sampling Time Offset. This delay may vary from part to part and as a function of temperature, but the short-term uncertainty (jitter) in sampling time offset is less than 50 picoseconds. The 255 to 8 encoding is performed on the falling edge of the CONV signal. The coded output is transferred to the output latches on the next rising edge. Data is held valid at the output register for at least t_{HO}, Output Hold Time, after the rising edge of CONV. New data becomes valid after a Digital Output Delay, t_D. This permits the previous conversion result to be acquired by external circuitry on that rising edge, i.e. data for sample N is acquired by the external circuitry while the TDC1025 is taking input sample N + 2. Note that there are minimum pulse width (t_{PWL} and t_{PWH}) requirements on the waveshape of the CONV signal. (Refer to Figure 1)

Name	Function	Value	C1, L1 Package
CONV	Convert	ECL	Pin 54
$\overline{CONV}$	Convert Complement	ECL	Pin 53

Analog Input

The TDC1025 comparator array causes the input impedance to vary slightly with the signal level, as comparator input transistors are cut-off or become active. For optimal performance, the source impedance driving the device must be less than 25 Ohms. The input signal will not damage the TDC1025 if it remains within the range of +0.5V to V_{EEA}. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 255, proportional to the magnitude of the analog input. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction. All eight analog input pins should be connected through resistors near the chip to provide a balanced analog input to all portions of the comparator array. The optimized values are shown in Figure 6.

The analog input bandwidth, specified for a full-power input, is limited by the slew rate capabilities of the internal comparators. Decreasing the analog input amplitude will reduce the slew rate, and thus increase the effective bandwidth. Note that other system performance characteristics are specified for the recommended 2V p-p amplitude, and may degrade with the decreased analog input signal. A sample-and-hold circuit at the analog input will also extend performance beyond the specified bandwidth.

Name	Function	Value	C1, L1 Package
V_{IN}	Analog Signal Input	0V to -2V	Pins 44, 47, 48, 51, 52, 56, 57, 60

Outputs

The outputs of the TDC1025 are both differential and single-ended ECL compatible. The outputs should be terminated with a 1.5 kOhm impedance into a −5.2V source to meet the specified logic levels. Using the outputs in a differential mode will provide increased noise immunity.

Name	Function	Value	C1, L1 Package
$\overline{D_1}$	MSB Output, Complement	ECL	Pin 66
D_1	MSB Output	ECL	Pin 67
$\overline{D_2}$		ECL	Pin 68
D_2		ECL	Pin 1
$\overline{D_3}$		ECL	Pin 2
D_3		ECL	Pin 3
$\overline{D_4}$		ECL	Pin 4
D_4		ECL	Pin 5
$\overline{D_5}$		ECL	Pin 30
D_5		ECL	Pin 31
$\overline{D_6}$		ECL	Pin 32
D_6		ECL	Pin 33
$\overline{D_7}$		ECL	Pin 34
D_7		ECL	Pin 35
$\overline{D_8}$	LSB Output, Complement	ECL	Pin 36
D_8	LSB Output	ECL	Pin 37

No Connects

There are several pins labeled No Connect (NC), which have no connections to the chip. These pins should be left open.

Name	Function	Value	C1, L1 Package
NC	No Connect	Open	Pins 6, 9, 10, 11, 12, 15, 17, 19, 21, 24, 25, 26, 27, 38, 42, 43, 45, 59, 61, 65

Thermal Design

The case temperature must be limited to a maximum of 80°C for the standard temperature range and 125°C for the extended temperature range. For ambient temperatures above 45°C, 500 L.F.P.M. moving air is required for specified performance. In addition to moving air, heat sinking is an efficient method to optimize thermal management.

Figure 1. Timing Diagram

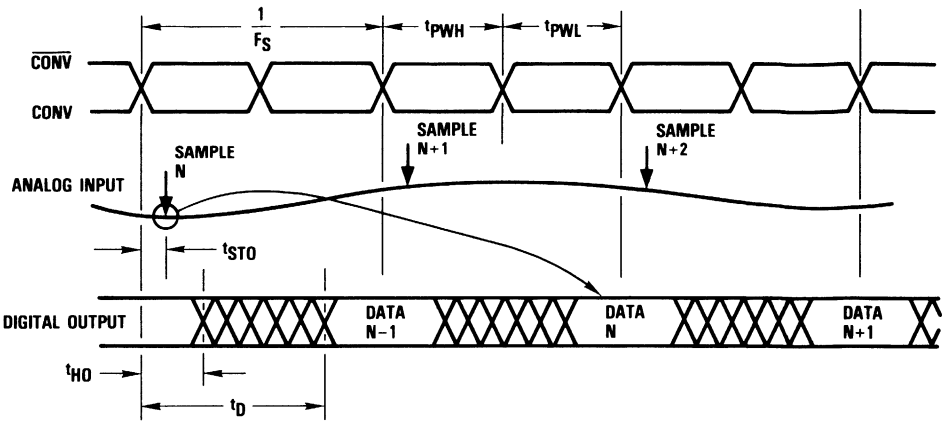
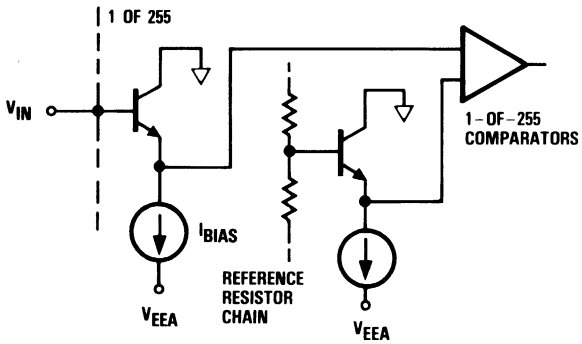
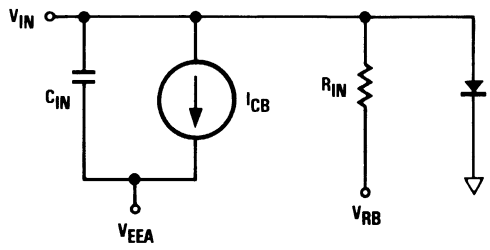


Figure 2. Simplified Analog Input Equivalent Circuit





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Convert Input Equivalent Circuit

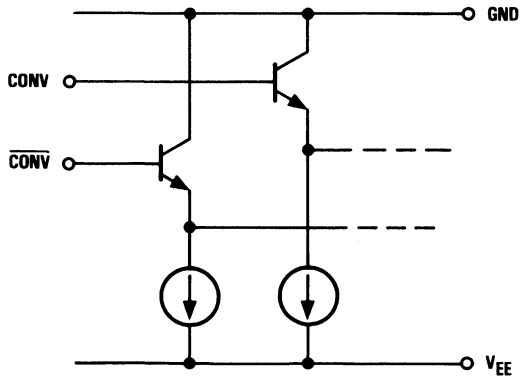
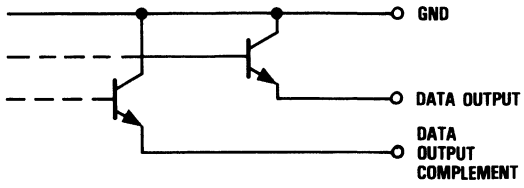
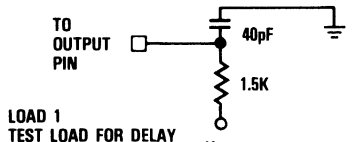


Figure 4. Output Circuits

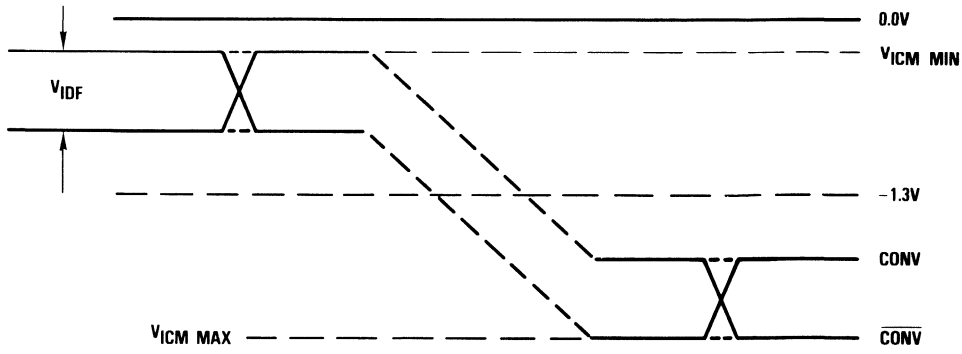


OUTPUT EQUIVALENT CIRCUIT



LOAD 1
TEST LOAD FOR DELAY MEASUREMENTS

Figure 5. CONVert, $\overline{\text{CONV}}$ert Switching Levels



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltages

V_{EED} (measured to D_{GND})	+0.5 to -7.0V
V_{EEA} (measured to A_{GND})	+0.5 to -7.0V
A_{GND} (measured to D_{GND})	+0.5 to -0.5V
V_{EEA} (measured to V_{EED})	+0.5 to -0.5V

Input Voltages

CONV, $\overline{\text{CONV}}$ (measured to D_{GND})	+0.5 to V_{EED}V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EEA}V
V_{RT} (measured to V_{RB})	0 to +2.5V

Output

Short-circuit duration (single output in high state to ground)	Indefinite

Temperature

Operating, ambient	-55 to +125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	-65 to +150°C

Note:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{EED}	Digital Supply Voltage	-4.9	-5.2	-5.5	-4.9	-5.2	-5.5	V
V_{EEA}	Analog Supply Voltage	-4.9	-5.2	-5.5	-4.9	-5.2	-5.5	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential	-0.1	0.0	+0.1	-0.1	0.0	+0.1	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	-0.1	0.0	+0.1	-0.1	0.0	+0.1	V
t_{PWL}	CONV Pulse Width, LOW	8			8			ns
t_{PWH}	CONV Pulse Width, HIGH	12			12			ns
V_{ICM}	CONV Input Voltage, Common Mode	-0.5		-2.5	-0.5		-2.5	V
V_{IDF}	CONV Input Voltage, Differential	0.3		1.2	0.3		1.2	V
V_{RT}	Most Positive Reference Input [1]	-0.1	0.0	+0.1	-0.1	0.0	+0.1	V
V_{RB}	Most Negative Reference Input [1]	-1.9	-2.0	-2.1	-1.9	-2.0	-2.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature [2]	0		70				°C
T_C	Case Temperature [2]	0		100	-55		+125	°C

Notes:

1. V_{RT} Must be more positive than V_{RB}, and voltage reference differential must be within specified range.
2. 500 L.F.P.M. moving air required above 45°C ambient.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{EE}	Supply Current	V_{EEA}, V_{EED} = MAX					
		T_A = 0°C to 70°C		-725			mA
		T_A = 70°C		-575			mA
		T_C = -55°C to 125°C				-1000	mA
		T_C = 125°C				-500	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM	10	35	10	45	mA
R_{REF}	Total Reference Resistance		57	200	44	200	Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	4		4		kOhms
C_{IN}	Input Capacitance			160		160	pF
I_{CB}	Input Constant Bias Current	V_{EEA}, V_{EED} = MAX, V_{IN} = 0.0V		750		1200	μA
I_I	Digital Input Current	V_{EEA}, V_{EED} = MAX, V_I = -0.7V		160		240	μA
V_{OL}	Output Voltage, Logic LOW	V_{EEA}, V_{EED} = NOM, I_{OL} = Test Load [1]		-1.6		-1.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{EEA}, V_{EED} = NOM, I_{OH} = Test Load [1]	-0.95		-1.1		V
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		20		20	pF

Note:

1. Test Load = 1.5 kOhms to -5.2V, C = 40pF.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{EEA}, V_{EED} = MIN	50		50		MSPS
t_{STO}	Sampling Time Offset	V_{EEA}, V_{EED} = MIN		10		10	ns
t_D	Digital Output Delay	V_{EEA}, V_{EED} = MIN, Load [1]		20		23	ns
t_{HO}	Digital Output Hold Time	V_{EEA}, V_{EED} = MIN, Load [1]	2		2		ns

Note:

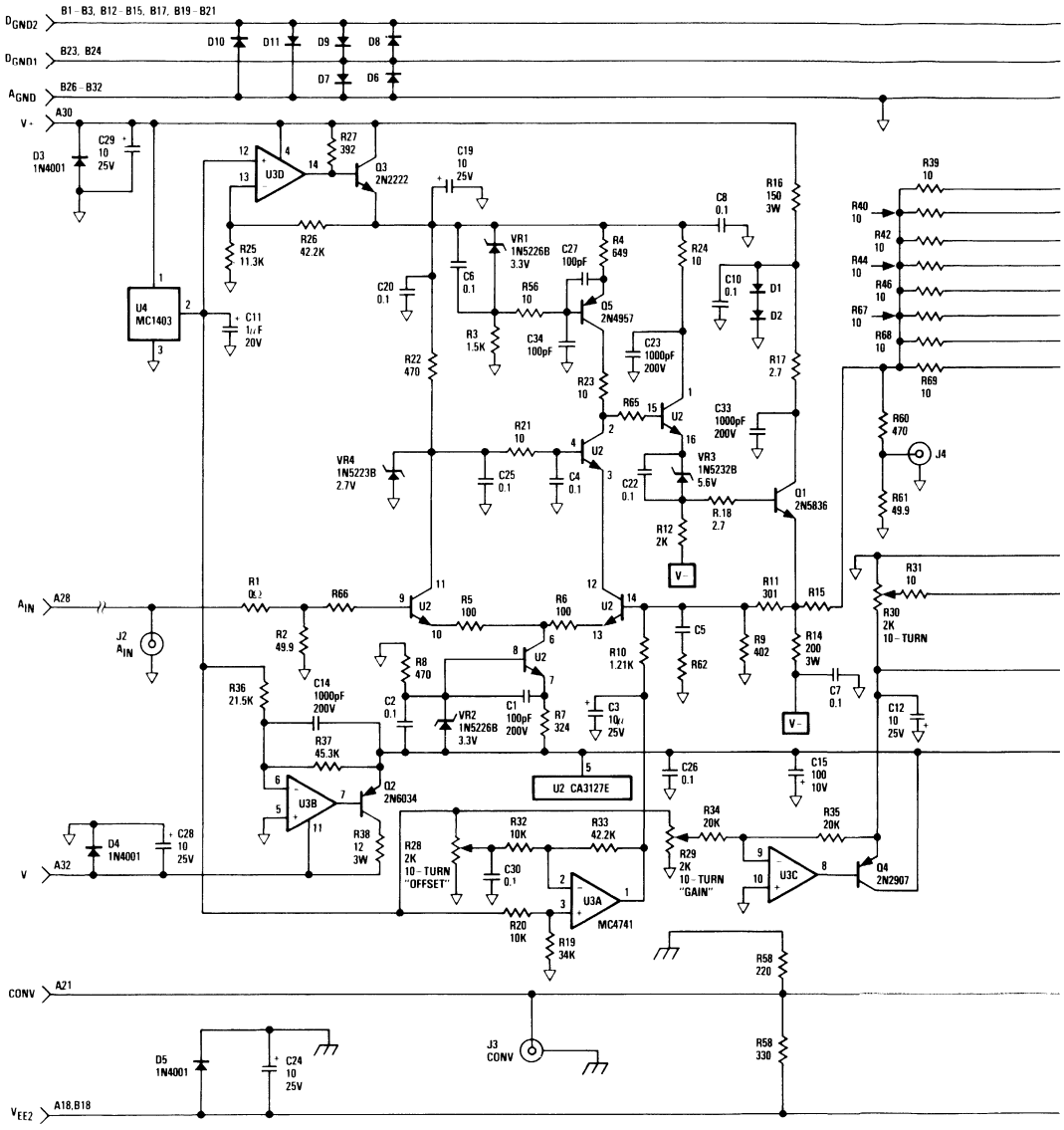
1. Test load = 1.5 kOhms to -5.2V, C = 40pF.

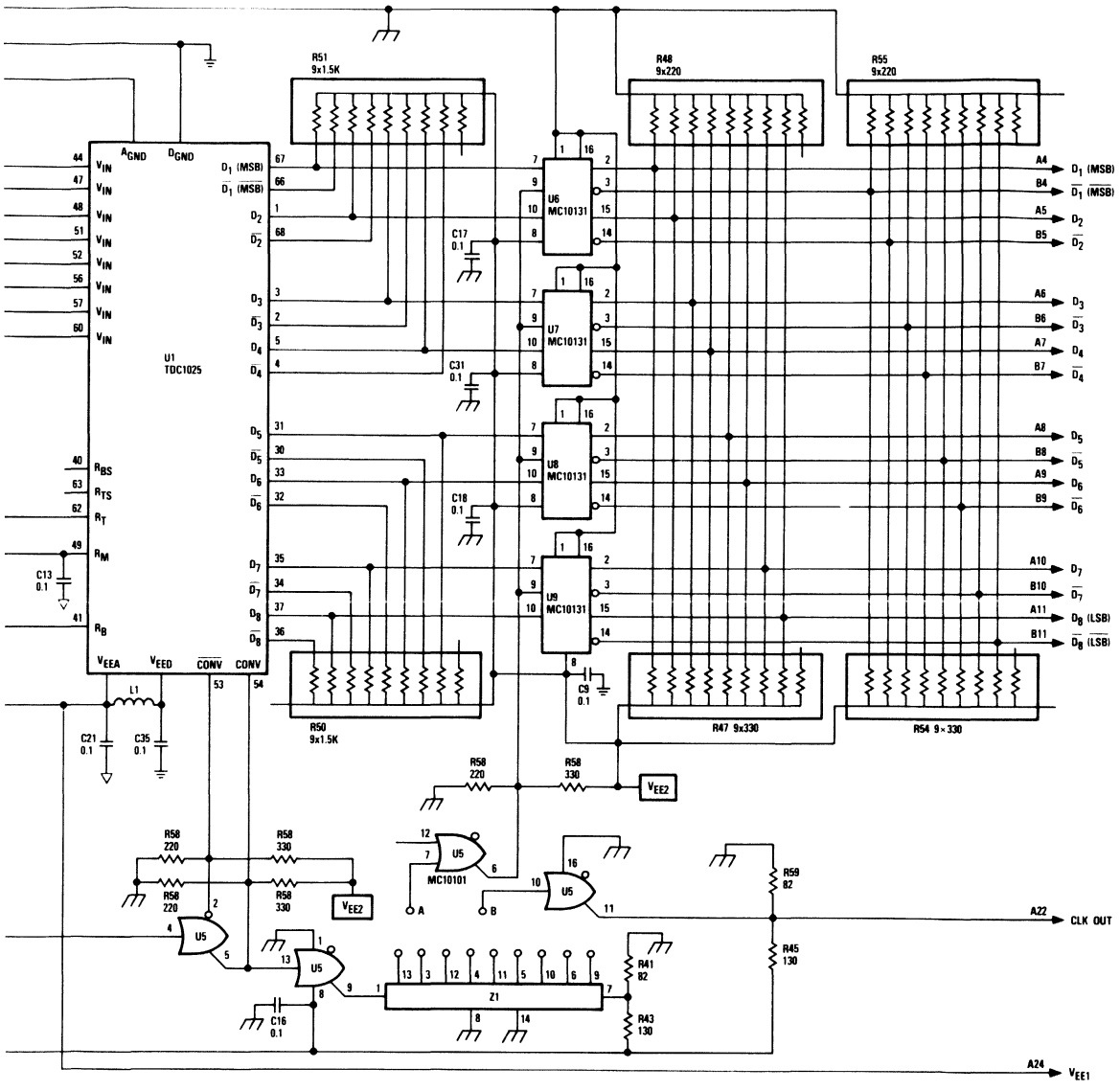
A

System performance characteristics within specified operating conditions

Parameter			Test Conditions	Temperature Range				Units
				Standard		Extended		
				Min	Max	Min	Max	
E_{LI}	Linearity	Integral, Independent	V_{RT}, V_{RB} = NOM		0.3		0.3	%
E_{LD}	Linearity	Differential			0.3		0.3	%
Q	Code Size		V_{RT}, V_{RB} = NOM	15	185	15	185	% Nominal
E_{OT}	Offset Error	Top	V_{IN} = V_{RT}		+40		+45	mV
E_{OTS}	Offset Error	Top, Sensed			±10		±10	mV
E_{OB}	Offset Error	Bottom	V_{IN} = V_{RB}		-40		-45	mV
E_{OBS}	Offset Error	Bottom, Sensed			±10		±15	mV
T_{COS}	Offset Error	Temperature Coefficient, Sensed			80		80	µV/°C
BW	Bandwidth, Full Power Input			12.5		12.5		MHz
t_{TR}	Transient Response, Full Scale Input Change				10		10	ns
SNR	Signal-to-Noise Ratio		20MHz Bandwidth, 50MSPS Conversion Rate					
		Peak Signal/RMS Noise	1.25MHz Input	53		53		dB
			5.34MHz Input	51		51		dB
			10.0MHz Input			47		dB
			12.0MHz Input	47				dB
		RMS Signal/RMS Noise	1.25MHz Input	44		44		dB
			5.34MHz Input	42		42		dB
			10.0MHz Input			38		dB
			12.0MHz Input	38				dB
EAP	Aperture Error				40		40	ps

Figure 6. Typical Interface Schematic




U1
TDC1025
R51
9x1.5K
R48
9x220
R55
9x220
R50
9x1.5K
R47 9x330
R54 9x330
U6
MC10131
U7
MC10131
U8
MC10131
U9
MC10131
C17
0.1
C31
0.1
C18
0.1
C9
0.1
C13
0.1
C21
0.1
C35
0.1
L1
R58
220
R58
330
U5
MC10101
R59
82
R45
130
R41
82
R43
130
Z1
C16
0.1
A4
B4
A5
B5
A6
B6
A7
B7
A8
B8
A9
B9
A10
B10
A11
B11
A22
CLK OUT
A24

A

Notes for Figure 6

1. All resistor values are in Ohms.
2. All resistors are 1/8W unless otherwise noted.
3. All capacitor values are in microFarads unless otherwise noted.
4. All capacitors are 50WVDC unless otherwise noted.
5. All diodes are 1N4148 unless otherwise noted.
6. R58 is a quad 220/330 Ohm terminator SIP.
7. Z1 is a digital delay line, 2ns per tap, 20ns total Rhombus TZB12-5.
8. L1 is a ferrite bead inductor, Fair-rite part number 2743001112.
9. A_{GND} pins on the TDC1025L1 are: 46, 50, 55, 58.
10. D_{GND} pins on the TDC1025L1 are: 8, 28, 39, 64.
11. V_{EEA} pins on the TDC1025L1 are: 13, 14, 16, 18, 20, 22, 23.
12. V_{EED} pins on the TDC1025L1 are: 7, 29.
13. Values for components C5, R15, R62, R65, R66 are determined during the manufacturing process.
14. Component designators C32, R49, R57, R63, R64, J1 are not used on the TDC1025E1C board.
15. Components R30, R31, R45, R47, R48, R54, R55, R59, R60, R61, J4, are user options and are not included with the board.

Typical Interface

Figure 6 shows an example of a typical interface circuit for the TDC1025. The analog input amplifier is a discrete differential amplifier followed by an NPN transistor. The transistor satisfies the input drive requirement of the A/D converter. The analog input resistors, attached close to the V_{IN} pins, provide frequency stability and a balanced analog input to all portions of the comparator array. All eight V_{IN} pins are connected together close to the device package, and the feedback loop should be closed at that point. Bipolar inputs may be used by adjusting the offset control. The amplifier has a gain of two, increasing a 1 Volt p-p input signal to the recommended 2 Volt p-p input for the A/D.

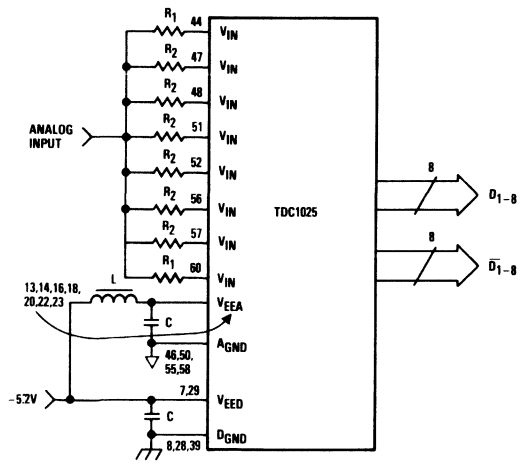
The top reference, R_T, is grounded, with the sense point, R_{TS}, left open. The offset error introduced at the top of the reference chain is cancelled by the offset adjustment. The bottom reference voltage, V_{RB} is supplied by an amplifier, and a PNP transistor. The feedback loop through the sense, R_{BS}, minimizes the offset error and related temperature variations at the bottom of the resistor chain. Additional gain adjustment can be made by varying the input voltage to the sensing op-amp.

The differential clock is provided by an ECL gate, with termination close to the TDC1025 to minimize ringing or overshoot. The convert clock is delayed by approximately 5-10ns to latch the data at the output. The data outputs are terminated with 1.5 kOhms to -5.2V. The standard Thevenin equivalent (220 Ohms-330 Ohms to -5.2V) is used where additional termination is required.

The analog and digital ground planes are separated to minimize ground noise and prevent ground loops, and are connected back at the power supply. The independent ECL digital ground aids in maintaining the chip digital ground, especially in a system with high-speed ECL logic. Protective diodes between all three ground planes avoid damage due to excessive differences in ground potential.

A

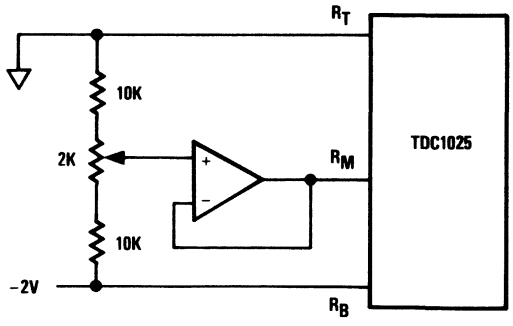
Figure 7. Power Decoupling and Input Network



L = FERRITE BEAD INDUCTOR
R_1 = 10Ω, 1% CARBON COMPOSITION OR CERAMIC CHIP RESISTOR
R_2 = 10Ω, 1% CARBON COMPOSITION OR CERAMIC CHIP RESISTOR
C = 0.1μF CERAMIC DISC CAPACITOR
⏚ = ANALOG GROUND
⏚ = DIGITAL GROUND

Note: Pins are shown for L1, C1 packages

Figure 8. Typical Reference Midpoint Adjust Circuit



Output Coding

Step	Range		Binary		Offset Two's Complement	
			True	Inverted	True	Inverted
	−2.0000V FS 7.8431 mV Step	−2.0480V FS 8.000 mV Step		All Outputs Inverted	D_1 Inverted	D_2−D_9 Inverted
000	0.0000V	0.0000V	000000000	111111111	100000000	011111111
001	−0.0078V	−0.0080V	000000001	111111110	100000001	011111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	−0.9961V	−1.0160V	011111111	100000000	111111111	000000000
128	−1.0039V	−1.0240V	100000000	011111111	000000000	111111111
129	−1.0118V	−1.0320V	100000001	011111110	000000001	111111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
254	−1.9921V	−2.0392V	111111110	000000001	011111110	100000001
255	−2.0000V	−2.0400V	111111111	000000000	011111111	100000000

Note:

1. Voltages are code midpoints after calibration.
2. Any output may be inverted by interchanging connections to the true (D_N) and complement ($\overline{D_N}$) output pins.

Calibration

To calibrate the TDC1025, adjust V_{RT} and V_{RB} to set the 1st and 255th thresholds to the desired voltages. Note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −2V desired range, continuously strobe the converter with −0.0039V (1/2 LSB from 0V) on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −1.996V (1/2 LSB from −2V) and adjust V_{RB} for toggling between codes 254 and 255.

The degree of required adjustment is indicated by the offset errors, E_{OT} and E_{OB}. Offset errors are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the integrated circuit. These parasitic resistors are shown as R_1 and R_2 in the Functional Block Diagram. Calibration will cancel all offset voltages, eliminating offset and gain errors.

The above method of calibration requires that both ends of the resistor chain, R_T and R_B, are driven by buffered operational amplifiers. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error, which can be compensated for by varying the voltage applied to R_B. The bottom reference is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in Figure 5.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1025C1C	STD – T_C = 0°C to 80°C	Commercial	68 Contact Chip Carrier	1025C1C
TDC1025C1A	EXT – T_C = – 55°C to 125°C	High Reliability	68 Contact Chip Carrier	1025C1A
TDC1025L1C	STD – T_C = 0°C to 80°C	Commercial	68 Contact Chip Carrier	1025L1C
TDC1025L1A	EXT – T_C = – 55°C to 125°C	High Reliability	68 Leaded Chip Carrier	1025L1A

A

TDC1029

Monolithic A/D Converter

6-Bit, 100Msps

The TRW TDC1029 is a 100Msps (MegaSample Per Second) fully-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full power frequency components up to 50MHz into 6-bit digital words. A sample-and-hold circuit is not required. All digital inputs and outputs are ECL compatible.

The TDC1029 consists of 63 latching comparators, combining logic, and an output register. A differential convert (CONV) signal controls the conversion operation. The digital outputs are single-ended ECL with the exception of the MSB which is differential enabling binary or offset two's complement output format.

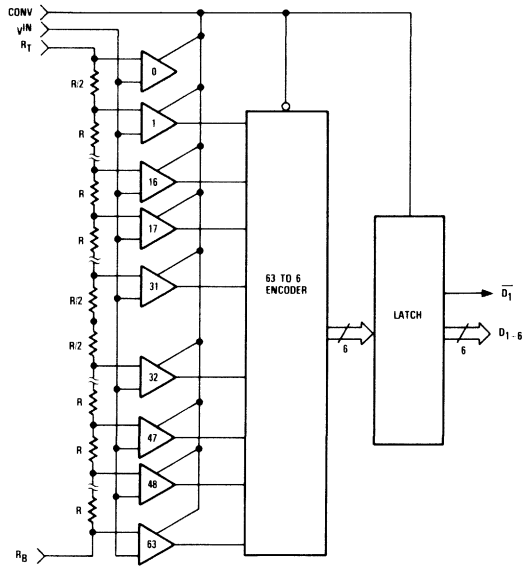
Features

- 6-Bit Resolution
- 100Msps Conversion Rate
- 50MHz Input Bandwidth
- Low Cost
- 1/2 LSB Linearity
- Sample-And-Hold Circuit Not Required
- 1V Input Range
- Binary Or Two's Complement Output Format
- 1/4, 1/2 And 3/4 Scale Reference Resistor Taps On J6 Package
- Available In A 24 Pin CERDIP

Applications

- Transient Digitizers
- Direct Digital Receivers
- Radar Data Conversion
- Data Acquisition
- Telecommunications
- Medical Imaging
- High-Energy Physics Experimentation

Functional Block Diagram



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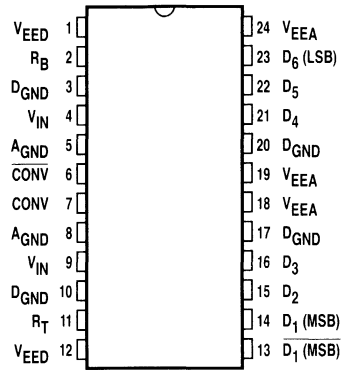
La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

40G01198 Rev. F–11/90
Printed in the U.S.A.

Pin Assignments



24 Pin CERDIP – B7 Package

Functional Description

General Information

The TDC1029 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 63 reference voltages to produce an N-of-63 code (sometimes referred to as a "thermometer" code, as all the comparators biased more positive than the input signal will be on, and all the rest will be off.) The encoding logic converts the N-of-63 code into binary data, with the complement of the MSB available for offset two's complement output format. The output latch holds the output data constant between updates.

Power

The TDC1029 operates from separate analog and digital power supplies, V_{EEA} and V_{EED}. Since the required voltage for both V_{EEA} and V_{EED} is $-5.2V$, these should ultimately be connected to the same power source, but separate decoupling for each is recommended. A typical decoupling network is shown in the *Typical Interface Circuit*. The return path for I_{EED}, the current drawn from the V_{EED} supply is D_{GND}. The return path for I_{EEA}, the current drawn from the V_{EEA} supply, is A_{GND}. All power and ground pins must be connected.

Thermal Design

The TDC1029 has thermal characteristics similar to other high-performance ECL devices and is rated for a maximum ambient temperature of 70°C. For ambient temperatures above 40°C, 500 L.F.P.M. moving air is required for specified performance. The maximum case temperature should be no greater than 110°C.

Reference

The TDC1029 reference voltage is applied between R_T and R_B. TDC1029 converts analog signals in the range $V_{RB} \geqslant V_{IN} \geqslant V_{RT}$ into digital form. The voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 0.9V and 1.1V. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between $-0.2V$ and $-1.4V$. V_{RT} should be more positive than V_{RB} within that range. The nominal voltages are: $V_{RT} = -0.3V$, $V_{RB} = -1.3V$. These voltages may be varied dynamically up to 25MHz. Due to slight variations in the reference current with changes in clock and input signals, R_T and R_B should be low-impedance points. For circuits in which the reference is not varied, a bypass capacitor to A_{GND} is recommended. If the reference inputs are varied dynamically (as in an AGC circuit), a low-impedance reference source is required.

Convert

The TDC1029 requires a differential ECL CONVert (CONV) signal. A sample is taken (the comparators are latched) t_{STO} after a rising edge on the CONV pin. The result from the encoding logic is transferred to the output latches on the next rising edge. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONVert signal. New data becomes valid after a maximum delay time t_D. Both convert inputs must be connected, with CONV being the complement of $\overline{CONV}$.

Analog Input

The TDC1029 uses latching comparators which cause the input impedance to vary slightly with the signal level. For optimal performance, the source impedance driving the device must be less than 25 Ohms. The input signal will not damage the TDC1029 if it remains within the range of $+0.5V$ to V_{EEA}. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 63 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction. Both analog input pins MUST be connected through 15 Ohm resistors as shown in the *Typical Interface Circuit*.

Outputs

The outputs of the TDC1029 are ECL compatible. Outputs $D_{2\text{-}6}$ are single-ended, while the MSB (D_1) is differential. Offset two's complement format is available by cross-wiring the MSB, i.e., interchanging D_1 and $\overline{D_1}$. The outputs should be terminated with a 100 Ohm (or greater) impedance into a −2.0V source.

Package Interconnections

Signal Type	Signal Name	Function	Value	B7 Package Pins
Power	V_{EEA}	Analog Supply Voltage	−5.2V	18, 19, 24
	V_{EED}	Digital Supply Voltage	−5.2V	1, 12
	D_{GND}	Digital Ground	0.0V	3, 10, 17, 20
	A_{GND}	Analog Ground	0.0V	5, 8
Reference	R_T	Reference Resistor (Top)	−0.30V	11
	R_B	Reference Resistor (Bottom)	−1.30V	2
Convert	CONV	Convert	ECL	7
	$\overline{CONV}$	Convert Complement	ECL	6
Analog Input	V_{IN}	Analog Signal Input	See Text	4, 9
Outputs	$\overline{D_1}$	MSB Output Complement	ECL	13
	D_1	MSB Output	ECL	14
	D_2		ECL	15
	D_3		ECL	16
	D_4		ECL	21
	D_5		ECL	22
	D_6	LSB Output	ECL	23

A

Figure 1. Timing Diagram

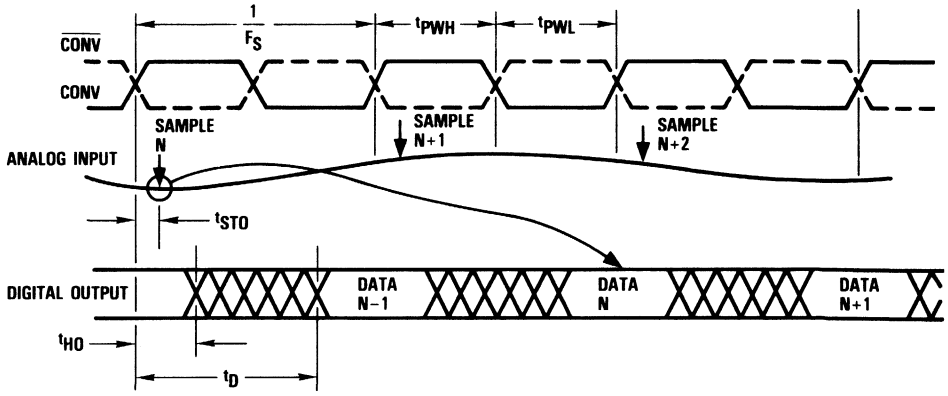


Figure 2. Simplified Analog Input Equivalent Circuit

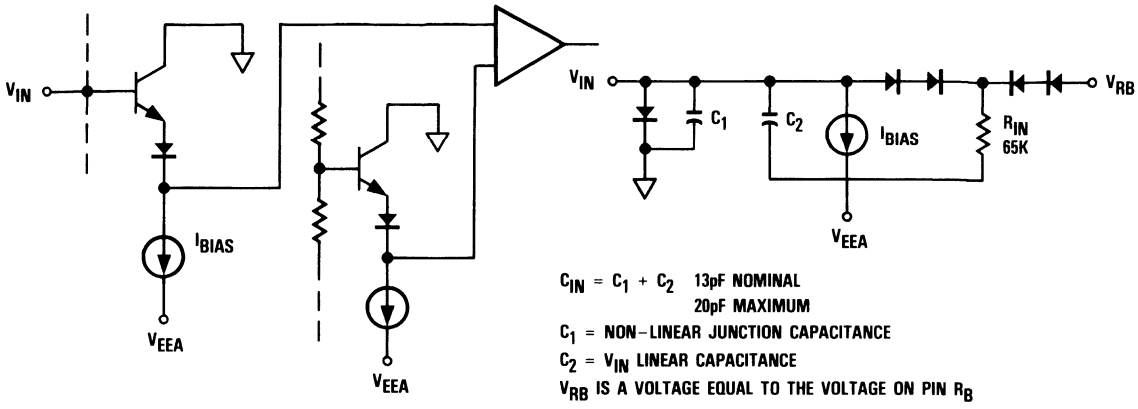


Figure 3. Convert Input Equivalent Circuit

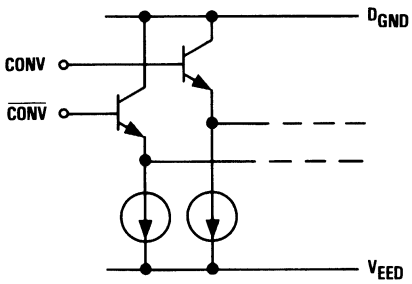


Figure 4. Output Circuits

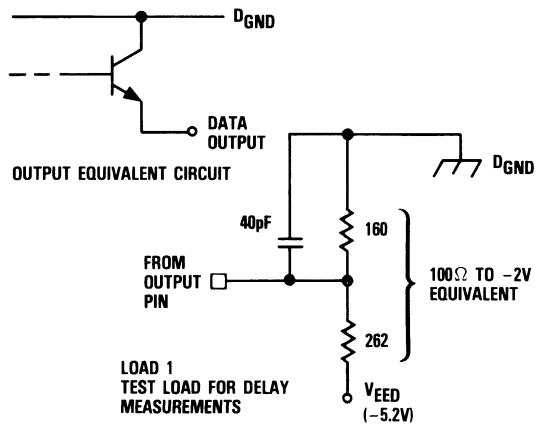
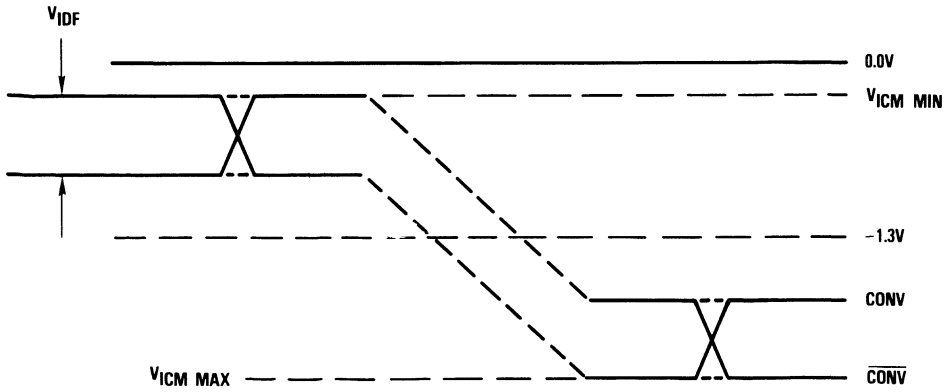


Figure 5. CONVert, $\overline{\text{CONV}}$ert Switching Levels



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltages

V_{EED} (measured to D_{GND})	0.5 to −7.0V
V_{EEA} (measured to A_{GND})	0.5 to −7.0V
A_{GND} (measured to D_{GND})	1.0 to −1.0V
V_{EEA} (measured to V_{EED})	0.5 to −0.5V

Input Voltages

CONV, $\overline{CONV}$ (measured to D_{GND})	+0.5 to V_{EED}V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EEA}V
V_{RT} (measured to V_{RB})	+1.5 to −1.5V

Output

Short circuit duration (single output to ground)	Indefinite

Temperature

Operating, ambient	−60 to +115°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Note:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{EED}	Digital Supply Voltage	−4.9	−5.2	−5.5	V
V_{EEA}	Analog Supply Voltage	−4.9	−5.2	−5.5	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential	−0.1	0.0	0.1	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	3	4		ns
t_{PWH}	CONV Pulse Width, HIGH	5	6		ns
V_{ICM}	CONV Input Voltage, Common Mode Range (Figure 6)	−0.5		−2.5	V
V_{IDF}	CONV Input Voltage, Differential (Figure 6)	0.4		1.2	V
V_{RT}	Most Positive Reference Input [1]	−0.2	−0.3	−0.4	V
V_{RB}	Most Negative Reference Input [1]	−1.2	−1.3	−1.4	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.9	1.0	1.1	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V
T_A	Ambient Temperature [2]	0		70	°C

Notes:

1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.
2. 500 L.F.P.M. moving air required above 40°C.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
$I_{EEA}+I_{EED}$	Supply Current	V_{EEA}, V_{EED} = MAX			
		T_A = 0°C to 70°C		-450	mA
		T_A = 70°C		-375	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM	10	35	mA
R_{REF}	Total Reference Resistance		29	100	Ohm
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}, V_{EE} = MAX	6		kOhm
C_{IN}	Input Equivalent Capacitance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}		20	pF
I_{CB}	Input Constant Bias Current	V_{EEA}, V_{EED} = MAX, V_{IN} = -0.3V		500	μA
I_I	Input Current	V_{EEA}, V_{EED} = MAX, V_I = -0.5V		250	μA
V_{OL}	Output Voltage, Logic LOW	V_{EEA}, V_{EED} = NOM, Test Load 1		-1.650	V
V_{OH}	Output Voltage, Logic HIGH	V_{EEA}, V_{EED} = NOM, Test Load 1	-0.950		V
C_I	Digital Input Capacitance	T_A = 25°C		15	pF

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Conversion Rate	V_{EEA}, V_{EED} = MIN	100		MSPS
t_{STO}	Sampling Time Offset	V_{EEA}, V_{EED} = MIN		6	ns
t_D	Output Delay	V_{EEA}, V_{EED} = MIN, Load 1		8	ns
t_{HO}	Output Hold Time	V_{EEA}, V_{EED} = MIN, Load 1	1.5		ns

System performance characteristics within specified operating conditions

Parameter			Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error	Integral, Terminal Based	V_{RT}, V_{RB} = NOM		±0.8	%
E_{LD}	Linearity Error	Differential			±0.8	%
Q	Code Size		V_{RT}, V_{RB} = NOM	50	150	% Nominal
E_{OT}	Offset Error	Top	V_{IN} = V_{RT}		20	mV
E_{OB}	Offset Error	Bottom	V_{IN} = V_{RB}	-8	+8	mV
T_{CO}	Offset Error	Temperature Coefficient			±35	µV/°C
BW	Bandwidth, Full Power Input [1]		F_S = 100MSPS	50		MHz
t_{TR}	Transient Response, Full-Scale Input Change				6	ns
SNR	Signal-To-Noise-Ratio [2]		100MSPS Conversion Rate			
		Peak Signal/RMS Noise	25MHz Input	42		dB
			50MHz Input	39		dB
		RMS Signal/RMS Noise	25MHz Input	33		dB
			50MHz Input	30		dB
E_{AP}	Aperture Error				30	ps

Notes:

1. Beat frequency sinusoidal reconstruction producing no errors greater then 3 LSBs, t_{PWH} = 6ns.
2. Single frequency sinusoidal input attenuated 3dB at 1/2 sampling frequency (anti-alias prefilter).

Output Coding [1]

Step	Range		Binary	Offset Two's Complement
	-1.3000V FS 15.8730mV STEP	-1.3080V FS 16.0000mV STEP	MSB LSB	MSB LSB
00	-0.3000V	-0.3000V	000000	100000
01	-0.3159V	-0.3160V	000001	100001
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
31	-0.7921V	-0.7960V	011111	111111
32	-0.8079V	-0.8120V	100000	000000
33	-0.8238V	-0.8280V	100001	000001
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
62	-1.2841V	-1.2920V	111110	011110
63	-1.3000V	-1.3080V	111111	011111

Note:

1. Voltages are code midpoints after calibration.

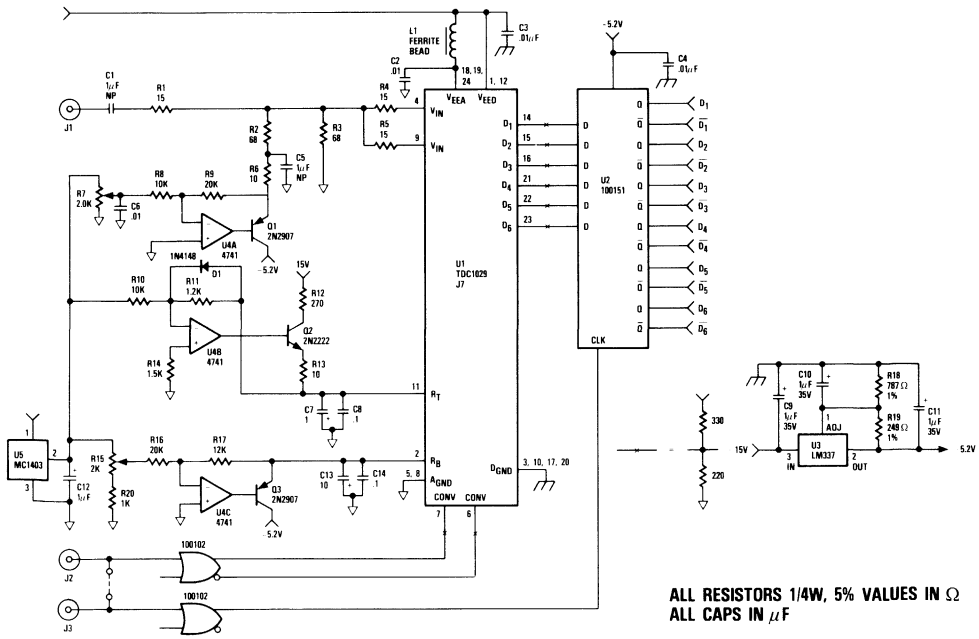
Calibration

To calibrate the TDC1029, adjust V_{RT} and V_{RB} to set 1st and 63rd thresholds to the desired voltages. Assuming a −0.3V to −1.3V desired range, continuously strobe the converter with −0.3079V (1/2 LSB from −0.300V) on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −1.2921V (1/2 LSB from −1.300V) and adjust V_{RB} for toggling between codes 62 and 63. Instead of adjusting V_{RT}, R_T can be connected to a fixed voltage and the most positive end of the range calibrated with an offset control. R_B is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in *Figure 6*.

Typical Interface Circuit

Figure 6 shows an example of a typical interface circuit for the TDC1029. The analog input is AC coupled with a 1μF non polar capacitor, then offset by −0.8V with a 741 type operational amplifier and an emitter follower. System offset is adjusted via a variable resistor which alters the gain of the amplifier that provides the offset to the analog input signal. The reference voltages for the TDC1029 are both supplied by 741 type operational amplifiers configured as inverting amplifiers with emitter followers. The reference bottom is adjustable via a variable resistor to allow the system gain to be adjusted. The power supply to the TDC1029 has been regulated with an LM337 three-terminal regulator, then V_{EEA} has a ferrite bead inductor in series with the supply and a parallel bypass capacitor to ground. The purpose of the inductor is to isolate the analog supply from the noise and voltage spikes that might be present on the digital supply. The digital data that is generated by the TDC1029 is latched with a 100151 ECL latch.

Figure 6. Typical Interface Circuit



ALL RESISTORS 1/4W, 5% VALUES IN Ω
ALL CAPS IN μF

Typical Interface Circuit

Figure 6 shows an example of a typical interface circuit for the TDC1029. The analog input is AC coupled with a 1μF non polar capacitor, then offset by −0.8V with a 741 type operational amplifier and an emitter follower. System offset is adjusted via a variable resistor which alters the gain of the amplifier that provides the offset to the analog input signal. The reference voltages for the TDC1029 are both supplied by 741 type operational amplifiers configured as inverting amplifiers with emitter followers. The reference bottom is adjustable via a variable resistor to allow the system gain to be adjusted. The power supply to the TDC1029 has been regulated with an LM337 three-terminal regulator, then V_{EEA} has a ferrite bead inductor in series with the supply and a parallel bypass capacitor to ground. The purpose of the inductor is to isolate the analog supply from the noise and voltage spikes that might be present on the digital supply. The digital data that is generated by the TDC1029 is latched with a 100151 ECL latch.

Applications

The TDC1029J6 (28 lead DIP) has three additional reference resistor taps available. These may be used in a variety of ways. Below are depicted two possible applications of these taps (Figures 7 and 8). In Figure 7 the potential at the reference middle point is sensed and fed back as an offset to the input amplifier so that the input voltage is automatically offset the proper amount for accurate conversion. In Figure 8 the reference taps are driven at different potentials so that the dynamic range of the converter is similar to that of an 8-bit converter. The dynamic range is expanded because the quantization steps are not of equal size. Figure 9 is an illustration of the transfer function of the circuit in Figure 8.

Figure 7. Midpoint Feedback

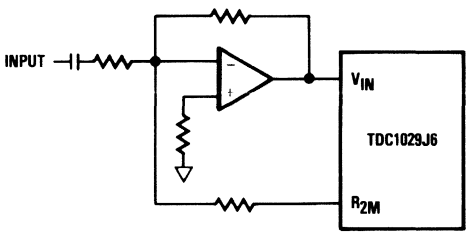


Figure 8. External Voltage Divider

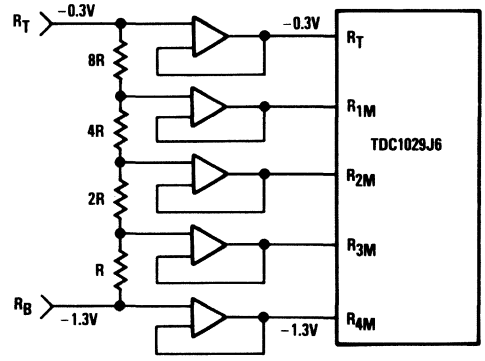
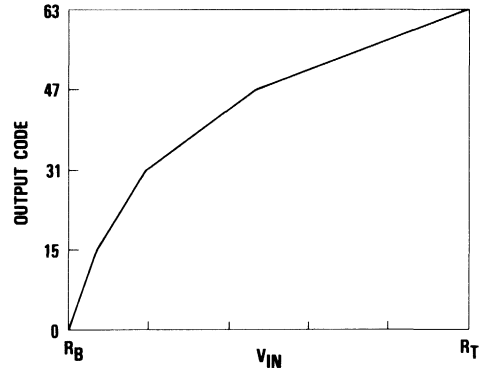


Figure 9. Piecewise Linear Transfer Function



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1029B7C	STD – T_A = 0°C to 70°C	Commercial	24 Pin CERDIP	1029B7C

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TDC1035

Monolithic Peak Digitizer

8-Bit, 30ns Full Response Peak Width

The TDC1035 is a unique variant of the full-parallel ("flash") analog-to-digital converter, capable of capturing the maximum peak amplitude of one or more pulses applied to its input between asynchronous reset pulses. Multiple "peak read" operations can be performed between resets. Peaks are detected digitally, so operation is stable and predictable. Packaged in a 24 pin CERDIP, the TDC1035 features lower power consumption and smaller size than an analog peak detector/ADC combination. All digital inputs and outputs are TTL compatible, and all outputs are registered and three-state.

Features

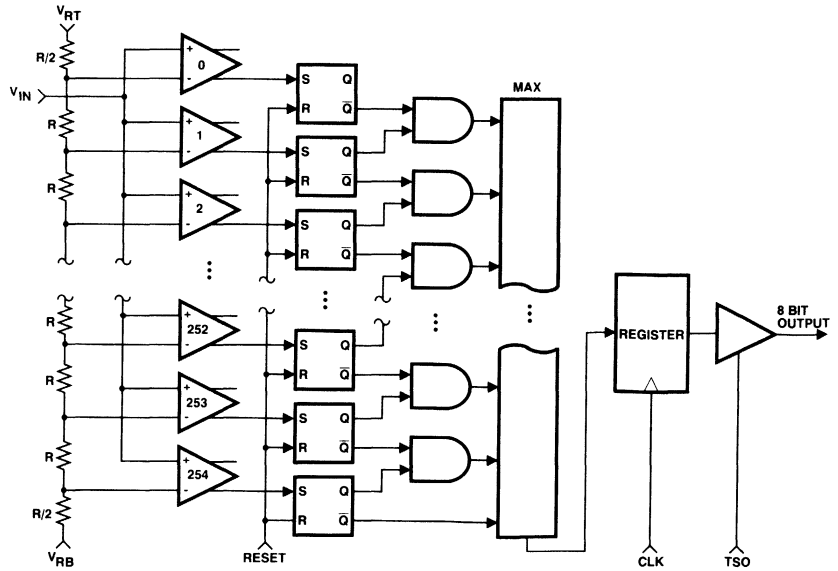
- 8-Bit Resolution
- Full DC Linearity For Pulses 30ns Wide
- Does Not Require Analog Peak-Hold Circuit
- Continuous Peak Capture Between Resets
- Multiple Read Operations Between Resets
- 1/2 LSB Linearity
- Narrow Ambiguity Region Around Reset
- Detects Pulses As Small As 12ns Wide
- Guaranteed Monotonic
- Selectable Data Format
- Available In A 24 Pin CERDIP Package
- 1.0W Power Consumption
- Three-State Registered Outputs

Applications

- Radar Pulse Classification
- Electronic Countermeasures
- Radiation Measurement
- Instrumentation

A

Functional Block Diagram



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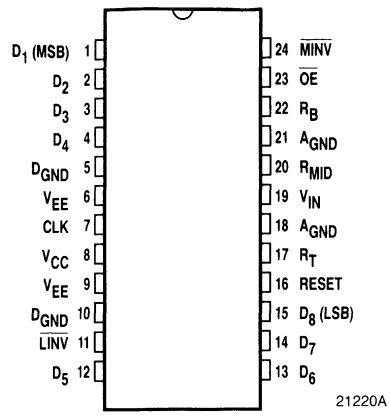
Pin Assignments



24 Pin CERDIP – B7 Package

Functional Description

General Information

The TDC1035 peak detector operates on ground-referenced negative-going signals. Within t_{RP} nanoseconds after the rising edge of the clock signal CLK, it outputs the most negative value reached since the previous RESET pulse. The active-HIGH RESET control is independent of CLK, but may be connected to CLK to provide a single-control peak detector. Multiple output cycles are permitted between reset operations.

The TDC1035 contains parallel array of comparators, an array of latches, and an encoder which outputs the location of the highest-valued latch which is set. The TDC1035's response characteristics are determined by its comparator array. A comparator's response time is determined by the degree of overdrive, since the output changes only when the area above threshold reaches a characteristic value. Therefore, the digitization accuracy of a pulse's peak value depends on the shape of the pulse.

To permit accurate, repeatable characterization, the TDC1035 is tested with a slew-rate limited "square" pulse. It will digitize (to its DC accuracy) the peak value of a square pulse having a minimum duration of 30ns. The accuracy degrades gracefully as the duration decreases from 30 down to 12ns, where it understates the applied amplitude by 15% (*Figure 7*). Production characterization of the TDC1035 uses "square" pulses with controlled rise and fall times of 8ns.

Performance of the TDC1035 with other pulse shapes (such as Gaussian or bandwidth-limited square pulse) can be estimated by applying an energy above threshold model, with area of 120 picoVolt-seconds.

The operation of all asynchronous sequential logic circuits involves some temporal ambiguity. The most common form of this ambiguity, metastability, occurs in data synchronizers. In a peak digitizer such as the TDC1035, this ambiguity comes in the form of periods during which the accuracy of the measurement of a pulse may be affected, or the pulse may not even be detected. There is a 10ns (t_{RP}) ambiguity period after the falling edge of the RESET signal, during which detection or accuracy of detection of any pulse is not guaranteed. There is also a region of 40ns (t_{PC}) before the rising edge of the (output) clock (CLK) where a pulse may be missed or detected inaccurately. These regions are shown in the timing diagrams, *Figures 1 and 2*. During the latter period, if the input signal increases to a new peak larger than the previously-latched value, the value loaded into the output register may be incorrect (and will most likely be zero); nonetheless, the peak detection latches will hold the (correct) new peak value.

As shown in *Figure 3*, the TDC1035's comparator inputs have emitter-follower buffers, which limit the permissible input signal slew rate to 250V/μs. This corresponds to a full-scale transition time of 8ns.

Power

The TDC1035 operates from two supply voltages: +5.0V and −5.2V. The current return for the positive supply is D_{GND}, and the return for the negative (analog) supply is A_{GND}. All power and ground pins MUST be connected.

Reference

The reference for the TDC1035 is a negative voltage applied across a chain of 255 resistors. The top of this chain is connected to the RT pin, and the voltage applied to the R_T pin (V_{RT}) should be within 0.1V of the analog ground. Note that the difference between the voltage applied to the pin and the voltage at the reference chain is the offset specification (E_{OT} and E_{OB}). The bottom of the reference resistor chain is connected to the RB pin, and the voltage applied to the R_B pin (V_{RB}) should be between 1.8 and 2.2V negative with respect to the R_T pin for full-specification operation. Reduced reference voltage operation is possible at reduced accuracy (for example, for generating a non-linear transfer function). The $R_T - R_B$ reference source should be able to deliver at least 45mA.

Due to the variation in the reference currents with clock and input signals, R_T and R_B should be connected to circuit nodes with a low impedance to ground. For circuits in which the reference is not varied at a high rate, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically (e.g., for AGC or nonlinear operation), a low-impedance reference source is required. The reference voltages may be varied dynamically; contact the factory for information on limitations when the device is used in this mode. The performance of the TDC1035 is specified with DC references of $V_{RT} = 0.0V$ and $V_{RB} = -2.0V$.

Control

Two function control pins, $\overline{MINV}$ and $\overline{LINV}$, are provided. These names stand for active-LOW Most significant bit INVert and active-LOW Least significant bits INVert, respectively. These controls are for DC (i.e., steady-state), not dynamic, use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. A single output state control pin, $\overline{OE}$, is provided. The three-state outputs may be placed in a high-impedance state by applying a logic HIGH to the $\overline{OE}$ control pin, and enabled by driving $\overline{OE}$ LOW.

The function control pins may be tied to V_{CC} for a logic HIGH, and D_{GND} for a logic LOW; however, a 2.2 kOhm pull-up resistor is preferred over direct connection to V_{CC}. If a pull-up resistor is not used, the absolute maximum voltage rating for the part becomes that of the TTL input, 5.5V, rather than the higher value for the V_{CC} terminal.

Command

Two pins, RESET and CLK, control the TDC1035. When brought HIGH, the level-sensitive RESET control resets the peak-storing latches. The edge-sensitive CLK control causes the peak value to be loaded into the output register when a rising-edge (LOW-to-HIGH) signal is applied. As noted above, there is a data ambiguity period associated with the operation of each of these inputs.

Analog Input

Although the TDC1035's 255 comparators have emitter-follower isolated inputs, the input impedance can vary up to 25 percent with the signal level, as comparator input transistors switch on or off. As a result, for optimal performance, the source impedance of the driving device must be less than 25 Ohms. The input signal will not damage the TDC1035 if it remains in the range $V_{EE} - 0.5V$ to $V_{AGND} + 0.5V$. If the input signal stays between the V_{RT} and V_{RB} reference voltages, the 8-bit digital equivalent of the most negative voltage reached will be latched into the array of latches, subject to the dynamic effects mentioned above. A transient more negative than V_{RB} will cause a full-scale output t_{DO} after the CLK line rises.

Outputs

The outputs of the TDC1035 are TTL compatible, capable of driving four low-power Schottky TTL (54LS/74LS) unit loads or the equivalent. The outputs hold the previous data a minimum time t_{HO} after the rising edge of the CLK input, and are guaranteed to have the new output value after a maximum time t_{DO}. Under light DC load conditions (such as driving CMOS loads or base-input low-power Schottky such as the 74L5374) 2.2k pull-up resistors to +5.0V are recommended.

Package Interconnections

Name	Function	Value	B7 Package Pins
V_{CC}	Positive Supply Voltage	+5.0V	8
V_{EE}	Negative Supply Voltage	−5.2V	6, 9
D_{GND}	Digital Ground	0.0V	5, 10
A_{GND}	Analog Ground	0.0V	18, 21
R_T	Reference Resistor, Top	0.0V	17
R_B	Reference Resistor, Bottom	−2.0V	22
$\overline{MINV}$	MSB Invert	TTL (Active LOW)	24
$\overline{LINV}$	LSB Invert	TTL (Active LOW)	11
$\overline{OE}$	Output Enable	TTL (Active LOW)	23
RESET	Resets Peak Value to Zero	TTL (Active HIGH)	16
CLK	Loads Output Register	TTL (Rising Edge)	7
V_{IN}	Analog Input Signal	0.0V to −2.0V	19
D_1	MSB Output	TTL	1
D_2		TTL	2
D_3		TTL	3
D_4		TTL	4
D_5		TTL	12
D_6		TTL	13
D_7		TTL	14
D_8	LSB Output	TTL	15

Figure 1. Timing with Separate RESET and CLK

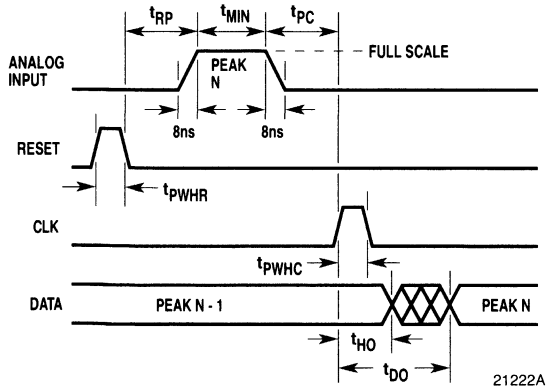


Figure 2. Timing with Common RESET and CLK

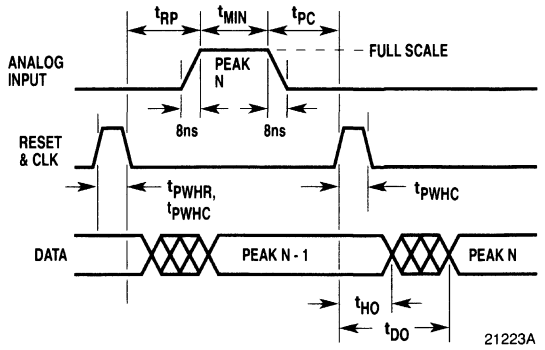
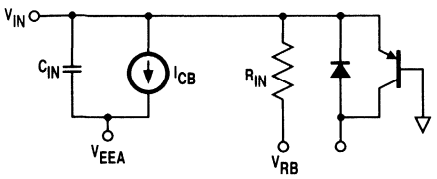
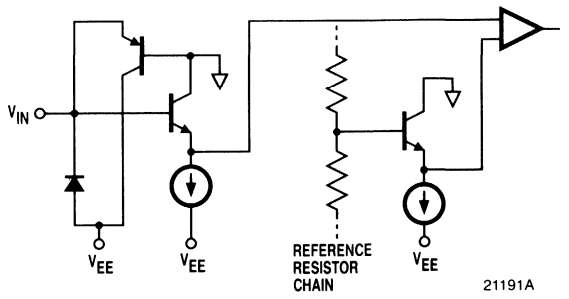


Figure 3. Simplified Analog Input Equivalent Circuits



C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B



A

Figure 4. Digital Input Equivalent Circuit

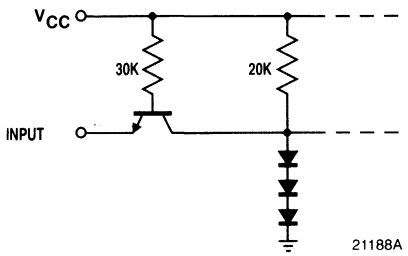


Figure 5. Output Circuits

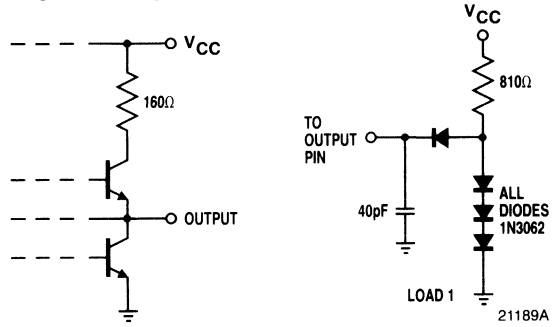


Figure 6. Recommended Input Circuit

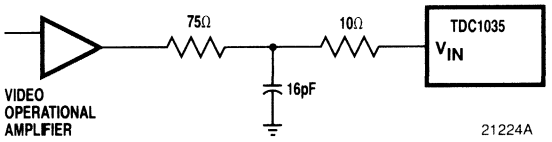
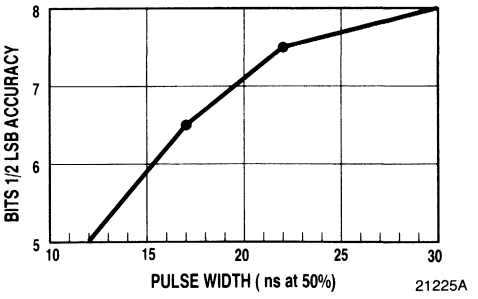


Figure 7. Variation of Accuracy as a Function of Width, "Square" Input Pulse



Output Coding

Step	Range		Binary		Offset Two's Complement	
			True	Inverted	True	Inverted
	−2.0000V FS	−2.0480V FS	$\overline{MINV}$ = 1	0	0	1
	7.8431mV Step	8.000mV Step	$\overline{LINV}$ = 1	0	1	0
000	0.0000V	0.0000V	00000000	11111111	10000000	01111111
001	−0.0078V	−0.0080V	00000001	11111110	10000001	01111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	−0.9922V	−1.0160V	01111111	10000000	11111111	00000000
128	−1.0000V	−1.0240V	10000000	01111111	00000000	11111111
129	−1.0078V	−1.0320V	10000001	01111110	00000001	11111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
254	−1.9844V	−2.0240V	11111110	00000001	01111110	10000001
255	−1.9922V	−2.0320V	11111111	00000000	01111111	10000000

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND}) ..... −0.5 to +7.0V
V_{EE} (measured to D_{GND}) ..... −7.0 to +0.5V
A_{GND} (measured to D_{GND}) ..... −0.5 to +0.5V

Input Voltages

RESET, CLK, $\overline{OE}$, $\overline{MINV}$, $\overline{LINV}$ (measured to A_{GND}) ..... −0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND}) ..... (V_{EE} − 0.5) to +0.5V
V_{RT} (measured to V_{RB}) ..... −2.2 to +2.2V

Outputs

Applied voltage (measured to D_{GND}) ..... −0.5 to +0.5V [2]
Applied current (externally forced) ..... −1.0 to 6.0mA [3,4]
Short-circuit duration (single output HIGH to shorted to ground) ..... 1 Second

Temperature

Operating, ambient ..... −55 to +125°C
junction ..... +175°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance is guaranteed only if specified operating conditions are met.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.5	V
V_{EE}	Negative Supply Voltage	−4.90	−5.2	−5.5	−4.90	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWHR}	Reset Minimum Pulse Width, HIGH	20			20			ns
t_{PWLC}	CLK Minimum Pulse Width, LOW	20			20			ns
t_{PWHC}	CLK Minimum Pulse Width, HIGH	20			20			ns
S_R	Input Signal Slew Rate			250			250	V/μS
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{RT}	Reference Voltage, Top	−0.1	0.0	0.1	−0.1	0.0	0.1	V
V_{RB}	Reference Voltage, Bottom	−1.8	−2.0	−2.2	−1.8	−2.0	−2.2	V
$V_{RT}-V_{RB}$	Reference Voltage Span	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{IN}	Input Voltage Range	V_{RT}		V_{RB}	V_{RT}		V_{RB}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = Max, Static		35		35	mA
I_{EE}	Negative Supply Current	V_{EE} = Max, Static		−160		−160	mA
I_{REF}	Reference Current	$V_{RT}-V_{RB}$ = Nom		35		35	mA
R_{REF}	Reference Resistance	Total, R_T to R_B	57		57		Ohms
R_{IN}	Input Equivalent Resistance (DC)	V_{RT}, V_{RB} = Nom, $V_{IN}=V_{RB}$	50		50		kOhms
C_{IN}	Input Capacitance, Analog	V_{RT}, V_{RB} = Nom, $V_{IN}=V_{RB}$		50		50	pF
I_{CB}	Input Constant Bias Current	V_{EE} = Max		250		350	μA
I_{IL}	Input Current Logic LOW	V_{CC} = Max, V_{IL} = 0.4V		−500		−500	μA
I_{IH}	Input Current Logic HIGH	V_{CC} = Max, V_{IH} = 2.4V		50		50	μA
I_{IM}	Input Current, V_{IN} = Max	V_{CC} = Max, V_{IH} = 5.5V		1		1	mA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = Max, V_O = 0V	−30	30	−30	30	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = Max, V_O = 5V	−30	30	−30	30	μA
I_{OS}	Short-Circuit Output [1]	V_{CC} = Max, Output HIGH, one output tied to D_{GND} for 1 second.		−50		−50	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Max, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
C_{IN}	Input Capacitance, Digital			10		10	pF

Note: 1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{PC}	CLK Setup Time	V_{CC}=Min, V_{EE}=Min, Load 1		30		30	ns
t_{RP}	RESET Delay	V_{CC}=Min, V_{EE}=Min, Load 1		5		5	ns
t_{DO}	Output Delay	V_{CC}=Min, V_{EE}=Min, Load 1		35		35	ns
t_{HO}	Output Hold Time	V_{CC}=Min, V_{EE}=Min, Load 1	5		5		ns
t_{DIS}	Output Disable Time	V_{CC}=Min, V_{EE}=Min, Load 1		20		20	ns
t_{ENA}	Output Enable Time	V_{CC}=Min, V_{EE}=Min, Load 1		70		90	ns

Note: 1. t_{RP} and t_{PC} are the guaranteed maximum lengths of the ambiguity periods.

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error, Integral, Independent	V_{RT}, V_{RB}=Nom		0.2		0.2	%FS
E_{LD}	Linearity Error, Differential	V_{RT}, V_{RB}=Nom		0.2		0.2	%FS
CS	Code Size	V_{RT}, V_{RB}=Nom	30	170	30	170	% Nominal
t_{MIN}	Analog Input Pulse Width	Square Pulse,					
		15% Accuracy	12		12		ns
		DC Accuracy	30		30		ns
E_{OT}	Offset Error, Top	V_{IN}=V_{RT}		±8		±8	mV
E_{OB}	Offset Error, Bottom	V_{IN}=V_{RB}		±15		±15	mV
T_{CO}	Offset Error, Temperature Coefficent	V_{RT}, V_{RB}, V_{CC}, V_{EE}=Nom		±20		±20	μV/°C

Applications Discussion

Under certain conditions, the real component of the input impedance may go negative at frequencies near 100MHz. To prevent oscillation at the input signal port, TRW recommends connecting the input signal to the TDC1035 via a series-connected resistor of at least 10 Ohms located close to the device. Further, if the signal bandwidth is not already limited so that the input slew rate limit is not exceeded, external circuitry is also recommended. The circuit shown in *Figure 6* accomplishes both goals.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1035B7C	STD – T_A=0°C to 70°C	Commercial	24 Pin CERDIP	1035B7C
TDC1035B7V	EXT – T_C= – 55°C to 125°C	MIL-STD-883	24 Pin CERDIP	1035B7V

TDC1038

Monolithic Video A/D Converter

8-Bit, 20Msps, Low Power

The TRW TDC1038 is a flash analog-to-digital converter capable of converting a video-speed signal into a stream of 8-bit digital words at 20Msps (MegaSamples Per Second). It is pin-for-pin compatible with the industry-standard TDC1048 but uses half the power. Since the TDC1038 is a flash converter, a sample-and-hold circuit is not required.

The TDC1038 consists of 255 clocked latching comparators, combining logic, and an output register. A single convert clock controls the conversion operation. The unit can be configured to give either true or inverted outputs, in binary or offset two's complement coding. All digital I/O is TTL compatible.

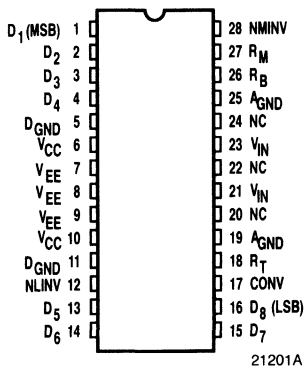
Features

- 8-Bit Resolution
- DC To 20Msps Conversion Rate
- 7MHz Full-Power Bandwidth
- 30MHz Small Signal −3dB Bandwidth
- 1/2 LSB Linearity
- 700mW Power Dissipation
- +5V, −5.0V (Or −5.2V) Supply Operation
- Low Cost
- Drop-In Replacement For TDC1048
- Sample-And-Hold Circuit Not Required
- Analog Input Range 0 To −2V
- Differential Phase 0.3°
- Differential Gain 0.7%
- Selectable Data Format
- Available In Plastic DIP, CERDIP, And PLCC

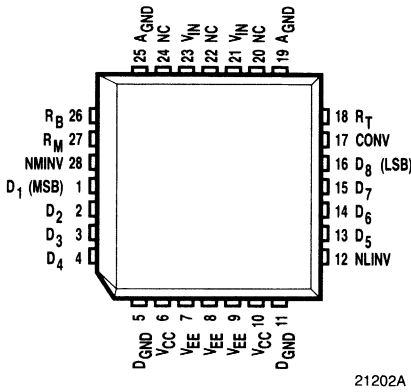
Applications

- Digital Television
- Electronic Warfare
- Low Power Upgrade For TDC1048
- Video Digitizing
- Medical Imaging
- High Energy Physics
- Low Cost, Low Power, High-Speed Data Conversion

Pin Assignments



28 Pin CERDIP – B6 Package
28 Pin Plastic DIP – N6 Package



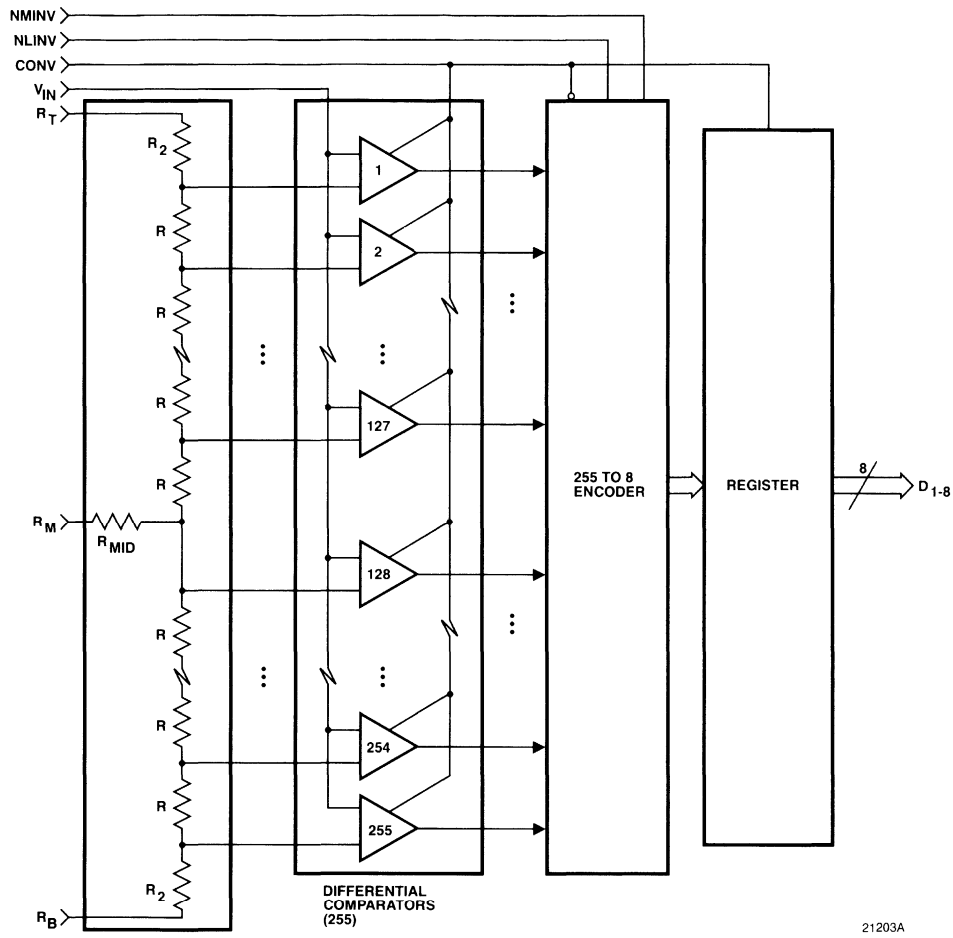
28 Lead Plastic J-Leaded Chip Carrier – R3 Package

TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

40G06121 Rev C–11/90
Printed in the U.S.A.

Functional Block Diagram



Functional Description

General Information

The TDC1038 has three functional sections: a comparator array, encoding logic, and output registers. The comparator array compares the input signal with 255 reference voltages to produce an N-of-255 code (or thermometer code, since all the comparators whose reference is more negative than the input signal will be on, and all those whose reference is more positive will be off). The encoding logic converts the N-of-255 code into the user's choice of coding. The output register holds the output constant between updates.

Power

The TDC1038 operates from two supply voltages: +5.0V and −5.0V. −5.2V may be used with a slight increase in power dissipation. The return path for I_{CC}, the current from the +5.0V supply, is D_{GND}. The return for path I_{EE}, the current from the −5.0V supply, is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1038 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. The specifications of

Reference (cont.)

the TDC1038 are guaranteed with V_{RT} (the voltage applied to the top of the reference resistor chain) at 0.0 ± 0.1V and V_{RB} (the voltage applied to the bottom of the reference resistor chain) at −2.0 ± 0.1V.

Linearity is guaranteed with no adjustment; however, a midpoint tap, R_M, allows trimming of converter integral linearity as well as the creation of a nonlinear transfer function. This is explained in the Application Note ***TP-19 "Non-Linear A/D Conversion"***. The circuit shown in ***Figure 6*** will provide approximately a 1/2 LSB adjustment of the linearity at midscale. The characteristic impedance seen at this node is approximately 220 Ohms and should be driven from a low-impedance source. Note that any load applied to this node will affect linearity, and any noise introduced at this point will degrade the overall quantization SNR. Due to the slight variation in the reference current with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor (0.01 to 0.1μF) to ground is recommended. If the reference inputs are exercised dynamically (as in an automatic gain control circuit) a low-impedance reference source is required. The reference voltages may be varied dynamically up to 5MHz; however, device performance is specified with fixed reference voltages as defined in the ***Operating Conditions Table***.

Analog Input

For precise quantization, the TDC1038 uses latching comparators. For optimum overall system performance the source impedance of the driving circuit must be less than 25 Ohms. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number from 0 to 255. When a signal outside the recommended input voltage range (0 to −2V) is applied, the output will remain at either full-scale value. The input signal will not damage the TDC1038 if it remains within the range specified in the ***Absolute Maximum Ratings Table***. Both analog input pins are connected together internally and therefore either one or both may be used.

Convert

The TDC1038 requires an external convert (CONV) signal. Because the TDC1038 is a flash converter it does not require a track-and-hold circuit. A sample is taken (the outputs of the comparators are latched) within t_{STO} (Sampling Time Offset) after a rising edge on the CONV pin. The result is encoded and then transferred to the output registers on the next rising edge. The digital output for sample N becomes valid t_D after the rising edge of clock N+1 and remains valid until t_{HO} after the rising edge of clock N+2. (See ***Figure 1, Timing Diagram***.)

Output Format Control

Two output format control pins, NMINV and NLINV, are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. These active LOW pins may be tied to V_{CC} (through a 4.7 kOhm resistor) for a logic 1 or D_{GND} for a logic 0.

Outputs

The outputs of the TDC1038 are TTL compatible, capable of driving four low-power Schottky TTL (54/74 LS) loads or the equivalent. The outputs hold the previous data for a minimum of t_{HO} after the rising edge of the CONVert signal.

Not Connected

There are several pins that have no internal connection to the chip. They should be left open.

Package Interconnections

Signal Type	Signal Name	Function	Value	B6, N6, R3 Package Pins
Power	V_{CC}	Digital Supply Voltage	+5.0V	6, 10
	V_{EE}	Analog Supply Voltage	−5.0V	7, 8, 9
	A_{GND}	Analog Ground	0.0V	19, 25
	D_{GND}	Digital Ground	0.0V	5, 11
Reference	R_T	Reference Resistor (Top)	0.0V	18
	R_M	Reference Resistor (Middle)	−1.0V	27
	R_B	Reference Resistor (Bottom)	−2.0V	26
Analog Input	V_{IN}	Analog Signal Input	0V to −2V	21, 23
Convert	CONV	Convert	TTL	17
Format Control	NMINV	Not Most Significant Bit Invert	TTL	28
	NLINV	Not Least Significant Bit Invert	TTL	12
Data Output	D_1	Most Significant Bit Output	TTL	1
	D_2		TTL	2
	D_3		TTL	3
	D_4		TTL	4
	D_5		TTL	13
	D_6		TTL	14
	D_7		TTL	15
	D_8	Least Significant Bit Output	TTL	16
Not Connected	NC	Not Connected	Open	20, 22, 24

Figure 1. Timing Diagram

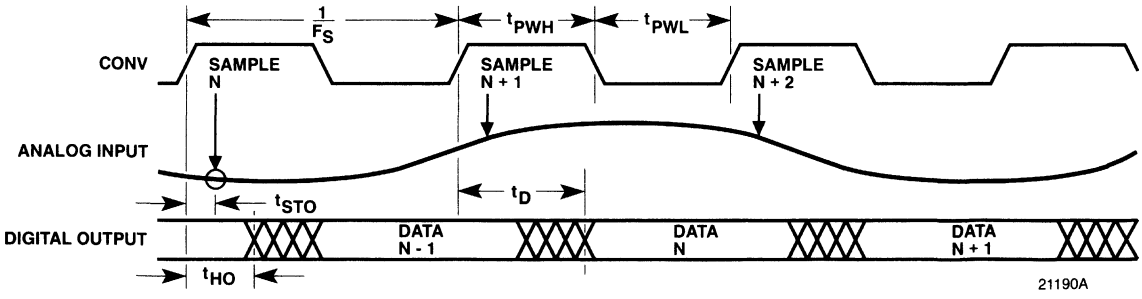
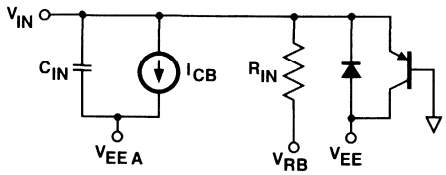


Figure 2. Simiplified Input Circuits



C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

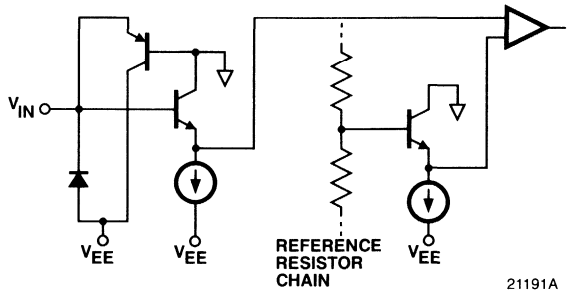


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Figure 3. Convert Input Equivalent Circuit

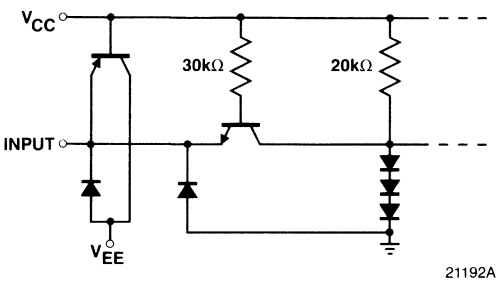

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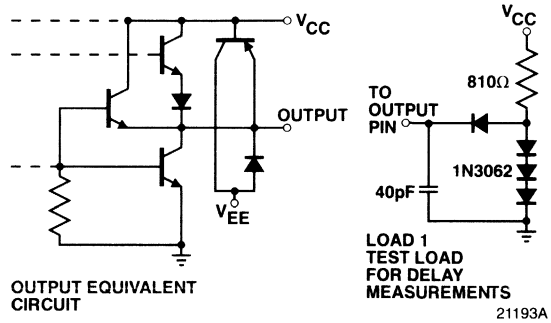
Figure 4. Output Circuit



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Output Coding Table

Input Voltage	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
	NMINV = HIGH NLINV = HIGH	NMINV = LOW NLINV = LOW	NMINV = LOW NLINV = HIGH	NMINV = HIGH NLINV = LOW
0.0000V	0000 0000	1111 1111	1000 0000	0111 1111
−0.0078V	0000 0001	1111 1110	1000 0001	0111 1110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.9922V	0111 1111	1000 0000	1111 1111	0000 0000
−1.0000V	1000 0000	0111 1111	0000 0000	1111 1111
−1.0078V	1000 0001	0111 1110	0000 0001	1111 1110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−1.9844V	1111 1110	0000 0001	0111 1110	1000 0001
−1.9922V	1111 1111	0000 0000	0111 1111	1000 0000

Notes: 1. NMINV and NLINV are to be considered DC controls. They may be tied to +5V for a logic 1 or tied to ground for a logic 0.
2. Voltages are code midpoints.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input Voltages [2]

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to (V_{CC} + 0.5V)
V_{IN}, V_{RT} V_{RB} (measured to A_{GND})	V_{EE} to +0.5V
V_{RT} (measured to V_{RB})	−2.2 to +2.2V

Input Currents [3]

CONV, NMINV, NLINV	−50 to +50mA
V_{IN}, V_{RT}, V_{RB}	−100 to +100mA

Output

Applied voltage [2] (measured to D_{GND})	−0.5 to (V_{CC} + 0.5V)
Applied current [3], externally forced	−20 to +20mA
Short circuit duration (single output in HIGH state to ground)	1 Second

Temperature

Operating, ambient (all packages except N6 and R3)	−55 to +125°C
(N6 and R3 packages only)	−20 to +90°C
junction (all packages)	+175°C
Lead, soldering, all packages (10 seconds)	+300°C
Storage, all packages	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. A condition applied individually that exceeds the Operating Conditions specification but is less than the Absolute Maximum Ratings will not cause immediate device failure. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{CC}	Digital Supply Voltage	4.75	5.0	5.25	V
V_{EE}	Analog Supply Voltage	−4.75	−5.0	−5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0	+0.1	V
t_{PWL}	CONVert Pulse Width, LOW	19			ns
t_{PWH}	CONVert Pulse Width, HIGH	27			ns
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
I_{OL}	Output Current, Logic LOW			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400	μA
V_{RT}	Most Positive Reference Input [1]	−0.1	0.0	0.1	V
V_{RB}	Most Negative Reference Input [1]	−1.9	−2.0	−2.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	1.8	2.0	2.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70	°C

Note: 1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Thermal characteristics (approximate)

Parameter		Package	Typical	Units
Θ_{ja}	Thermal Resistance, Junction to Ambient	N6	45	°C/W
		R3	65	°C/W
		B6	50	°C/W
Θ_{jc}	Thermal Resistance, Junction to Case	N6	17	°C/W
		R3	14	°C/W
		B6	12	°C/W

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{CC}	Positive Supply Current	V_{CC} = Max [1]		45	mA
I_{EE}	Negative Supply Current	V_{EE} = Max [1]		−165	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = Nom		30	mA
R_{REF}	Total Reference Resistance		67		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}	80		kOhms
C_{IN}	Input Capacitance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}		50	pF
I_{CB}	Input Constant Bias Current	V_{CCA} = Max		250	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.4V		−0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V	−200	50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = Max, V_I = V_{CC} = Max		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		V
I_{OS}	Short-Circuit Output Current	V_{CC} = Max, Output HIGH, one pin to ground, one second duration max.		−40	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15	pF

Note: 1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Conversion Rate		20		Msps
t_{STO}	Sampling Time Offset		−2	10	ns
t_D	Output Delay	V_{CC} = Min, Load 1, Figure 4		30	ns
t_{HO}	Output Hold Time	V_{CC} = Max, Load 1, Figure 4	5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Temperature Range: Standard Max	Units
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = Nom		0.2	%
E_{LD}	Linearity Error Differential			0.2	%
CS	Code Size		25	175	% Nom
E_{OT}	Offset Error, Top	$V_{IN} = V_{RT}$		+15	mV
E_{OB}	Offset Error, Bottom	$V_{IN} = V_{RB}$		−15	mV
T_{CO}	Offset Error, Temperature Coefficient		−20	+20	μV/°C
BW	Bandwidth, Full Scale Input	No Spurious or Missing Codes	7		MHz
BW_{SS}	−3dB Bandwidth, Small Signal	−20dBFS Input	30		MHz
t_{TR}	Transient Response, Full Scale		40		ns
SNR	Signal-to-Noise Ratio	10MHz Bandwidth, 20Msps Conversion Rate			
	Peak Signal/RMS Noise	1.248MHz Input	54		dB
		2.438MHz Input	53		dB
	RMS Signal/RMS Noise	1.248MHz Input	45		dB
		2.438MHz Input	44		dB
E_{AP}	Aperture Error			60	ps
DP	Differential Phase Error	$F_S = 4 \times NTSC$		1.0	Degree
DG	Differential Gain Error	$F_S = 4 \times NTSC$		2.0	%

A

Figure 5. Typical Interface Circuit

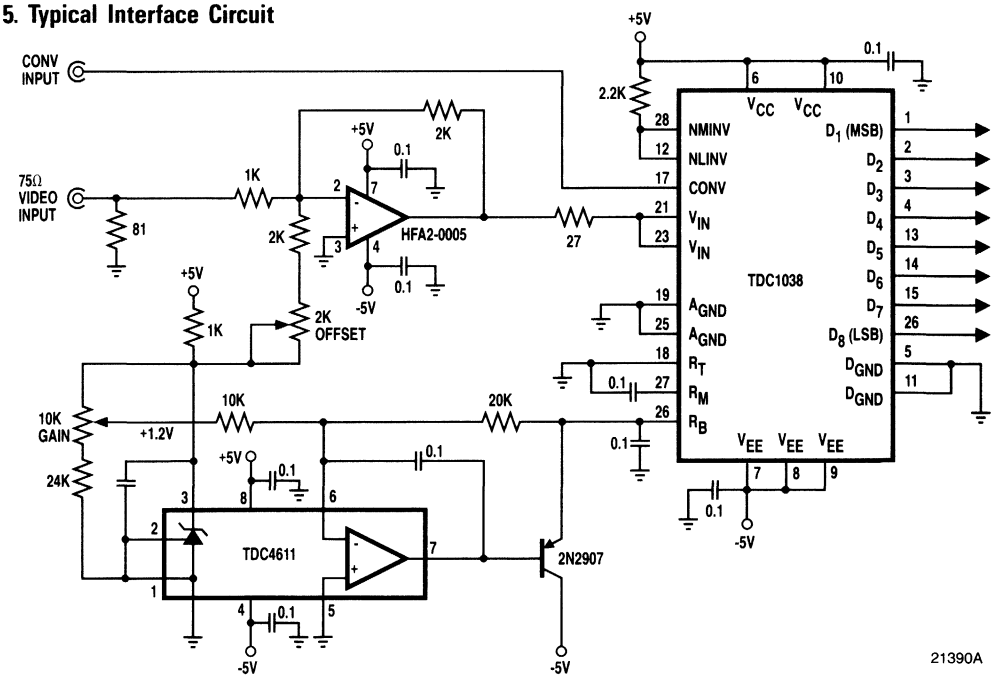


Figure 6. Optional Midscale Linearity Adjust

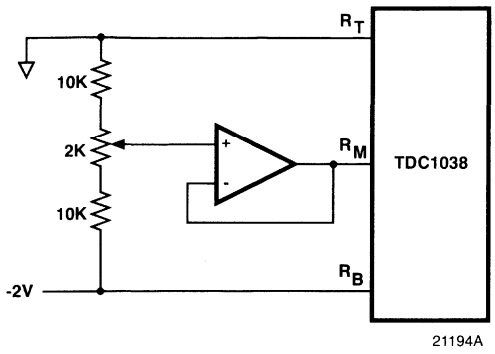
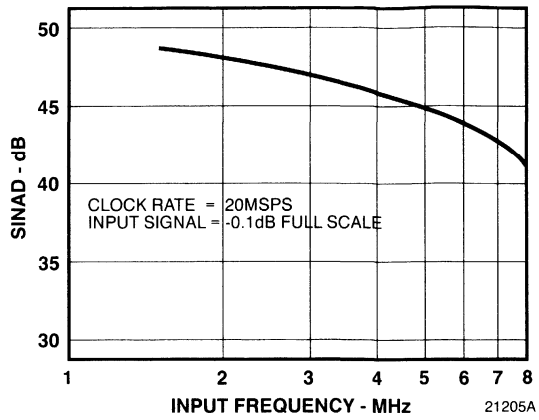


Figure 7. Typical SINAD vs. Input Frequency



Typical Interface Circuit

The *Typical Interface Circuit (Figure 5)* shows a wideband operational amplifier driving the A/D converter directly. Bipolar inputs to the op amp can be accommodated by adjusting the offset control. TRW's TDC4611 provides a stable reference for the offset and gain controls. All V_{IN} pins are connected close to the device package and the input amplifier's feedback loop should be closed at that point. The buffer has an inverting gain of two, increasing a 1Vp-p video input signal to the recommended 2Vp-p input for the TDC1038. Proper decoupling is recommended for all systems.

The bottom reference voltage (V_{RB}) is supplied by an inverting amplifier or the TDC4611, buffered with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain.

Evaluation Board

The TDC1038E1C is a Eurocard-style printed circuit board designed to optimize the performance of, and to aid in the evaluation of, the TDC1038 A/D converter. The board dimensions are 100mm x 160mm with a standard 64 pin double-row DIN male connector installed. A complementary 64 pin double-row DIN female connector is included with the board. The circuitry on the board includes reference voltage generator, wideband video input amplifier, and a TDC1012 12-bit D/A converter which may be used in evaluating certain parameters of the TDC1038.

The board employs only two conducting sides. Most of the circuit interconnections are on the bottom of the board while the top is mostly solid ground plane. SMA connectors are installed on the board to facilitate analog I/O and clocks. The board is calibrated and tested at the factory and is supplied complete with TDC1038 and TDC1012 installed.

Power and Ground

Four power supply voltages are required for the operation of the TDC1038E1C: $V_{CC} = +5V$, $V_{EE} = -5.2V$, $V+ = +15V$ and $V- = -15V$. All power inputs are decoupled to a single solid ground plane, GND. All GND pins of the board are connected to the ground plane and it is recommended that all GND pins be used.

Voltage Reference Generator

The TDC1038E1C has a voltage reference generator circuit for driving the RB terminal of the TDC1038. With RT grounded, a variable $-2V$ is supplied to RB from U2 and Q2. The GAIN potentiometer provides $\pm 10\%$ adjustment range on the RB voltage. Diodes D3 through D6 act as clamps which protect the TDC1038 from power-on conditions that might violate absolute maximum ratings and damage the TDC1038.

Video Input Amplifier

The input amplifier of the TDC1038E1C, U3, has been designed to accept a ±0.5V input range and translate that signal to the 0V to −2V range of the TDC1038. The output of this amplifier can be monitored at the AOUT SMA connector which is connected to the V_{IN} terminals of the TDC1038 through a 470Ω resistor. The OFFSET potentiometer, R29, gives a ±0.5V offset adjustment range to the board.

A/D Converter Inputs

The clock to the TDC1038, CONV, is normally brought onto the board through the SMA connector labeled "CONV." By installing jumper J1, this signal is routed through the edge connector pin B2. A location for a terminating resistor, R14 is available on the board for terminating a clock cable. The NMINV and NLINV inputs to the TDC1038 are pulled HIGH with resistors and may be pulled LOW by installing jumpers J2 and J3.

The analog signal input to the TDC1038E1C is brought onto the board by way of the SMA connector labeled "A_{IN}" near pin 28 of the TDC1038. A terminating resistor, R23, is included on the board for terminating a 50Ω analog input signal cable.

A/D Converter Data Outputs and D/A Converter Data Inputs

The eight data outputs of the TDC1038 are brought to edge connector pins B13 through B21 (excluding B18). These pins are located directly across the edge connector from the corresponding data inputs of the TDC1012 D/A converter to simplify connection of A/D outputs to D/A inputs.

D/A Converter Inputs

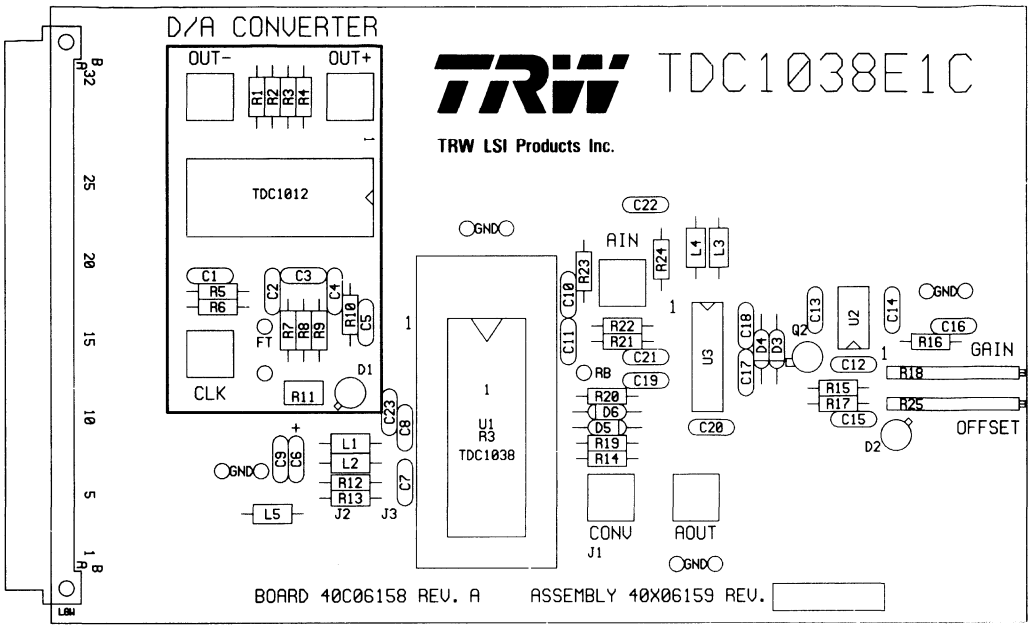
The clock to the TDC1012, CLK, is normally brought onto the board through an SMA connector labeled "CLK" near pin 16 of the TDC1012. A location for a terminating resistor, R6 is provided for clock cable termination. The clock to the TDC1012 is also brought to the edge connector pin B24.

D/A converter outputs are brought to SMA connectors labeled OUT+ and OUT− as well as edge connector pins B28 and B27. Load resistors of 51.1Ω are provided on the board to facilitate 50Ω cable connection to the board.

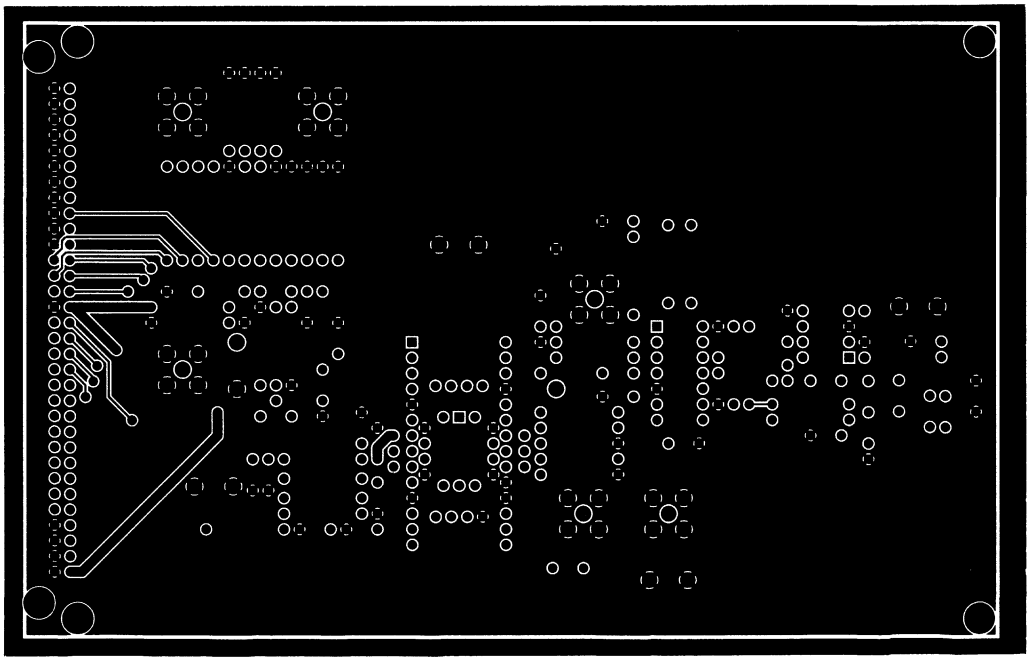
Potentiometer R11 is used to adjust the reference voltage to the TDC1012. This voltage is adjusted to −1.0V as part of the factory test and calibration procedure.

Removing the jumper in the location labeled "FT" will put the TDC1012 into feedthrough (unclocked) mode. This eliminates the requirement for a D/A clock signal, but will degrade the fidelity of the TDC1012 reconstruction.

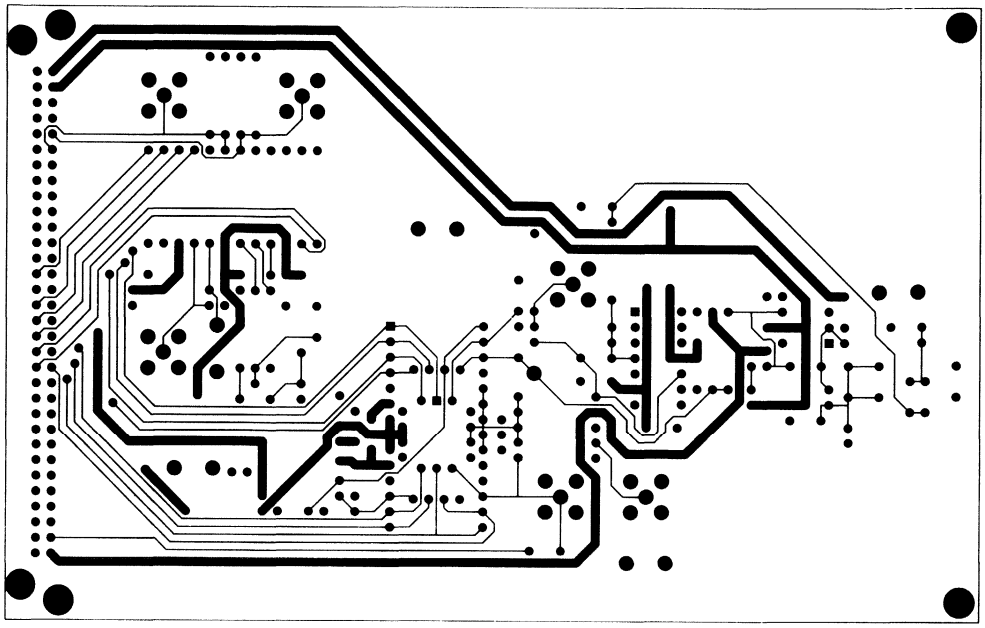
TDC1038E1C Silkscreen Layout



TDC1038E1C Component Side Layout



TDC1038E1C Circuit Side Layout



A

TDC1038E1C Eurocard Edge Connector Pinout

GND	A32	B32	V– (–15V)
GND	A31	B31	V+ (+15V)
GND	A30	B30	NC
GND	A29	B29	NC
GND	A28	B28	D/A OUT+
GND	A27	B27	D/A OUT–
GND	A26	B26	NC
GND	A25	B25	NC
GND	A24	B24	D/A CLK
GND	A23	B23	NC
GND	A22	B22	NC
D/A D_1 MSB	A21	B21	A/D D_1 MSB
D/A D_2	A20	B20	A/D D_2
D/A D_3	A19	B19	A/D D_3
GND	A18	B18	V_{CC} (+5V)
D/A D_4	A17	B17	A/D D_4
D/A D_5	A16	B16	A/D D_5
D/A D_6	A15	B15	A/D D_6
D/A D_7	A14	B14	A/D D_7
D/A D_8 LSB	A13	B13	A/D D_8 LSB
NC	A12	B12	NC
NC	A11	B11	NC
NC	A10	B10	NC
NC	A9	B9	NC
NC	A8	B8	NC
NC	A7	B7	NC
NC	A6	B6	NC
NC	A5	B5	NC
GND	A4	B4	NC
GND	A3	B3	NC
GND	A2	B2	A/D CONV
GND	A1	B1	V_{EE} (–5.2V)

Mating Connectors for TDC1038E1C

AMP	532507-2	Wire-wrap
AMP	532507-1	Solder tail
Robinson-Nugent	RNE-64BS-W-TG30	Wire-wrap
Robinson-Nugent	RNE-64BS-S-TG30	Solder tail
Souriau	8609-264-6115-7550E1	Wire-wrap
Souriau	8609-264-6114-7550E1	Solder tail
Souriau	8609-264-6813-7550E1	Solder tail, right-angle bend

Figure 8. TDC1038E1C A/D Converter Schematic Diagram

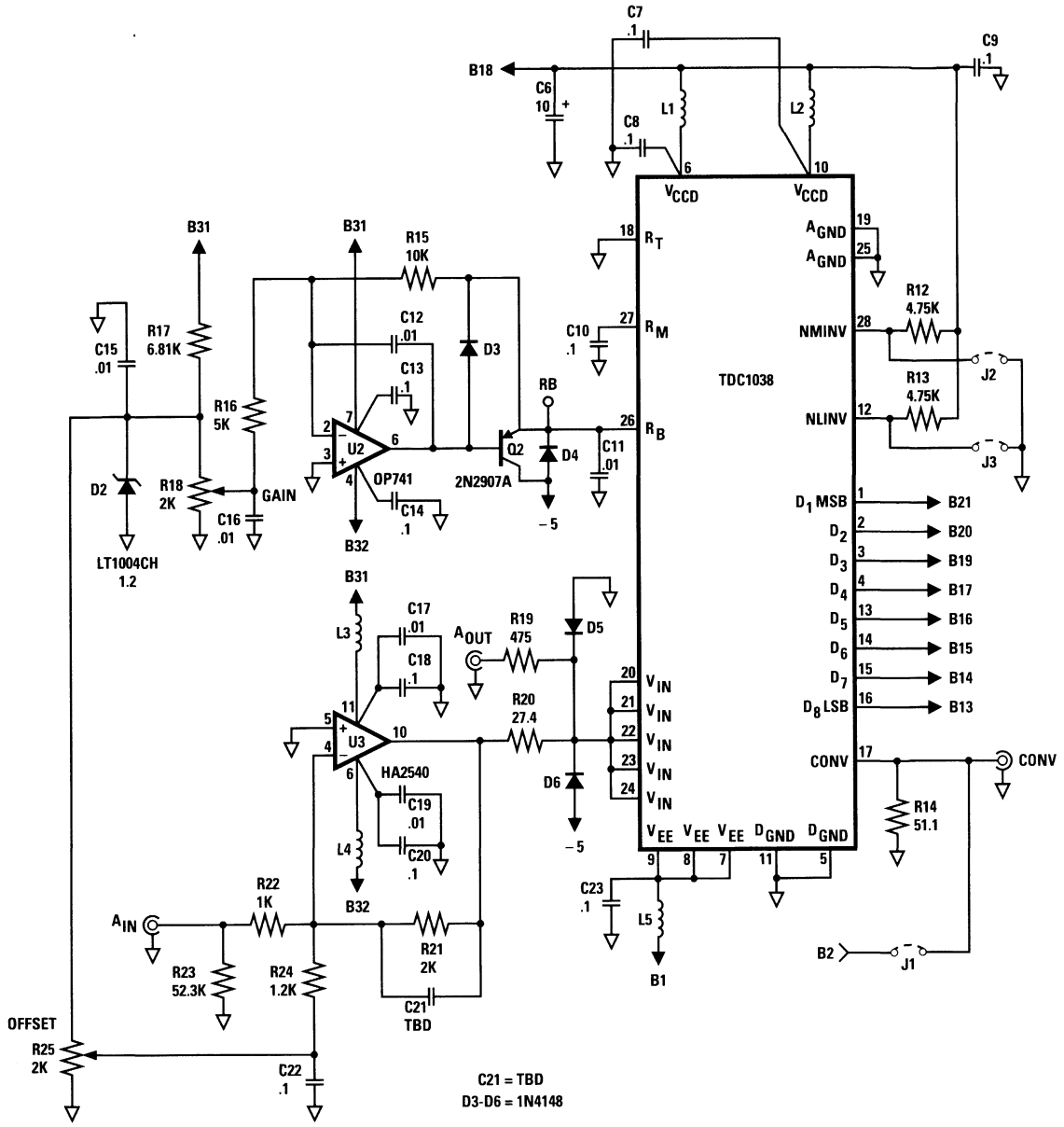
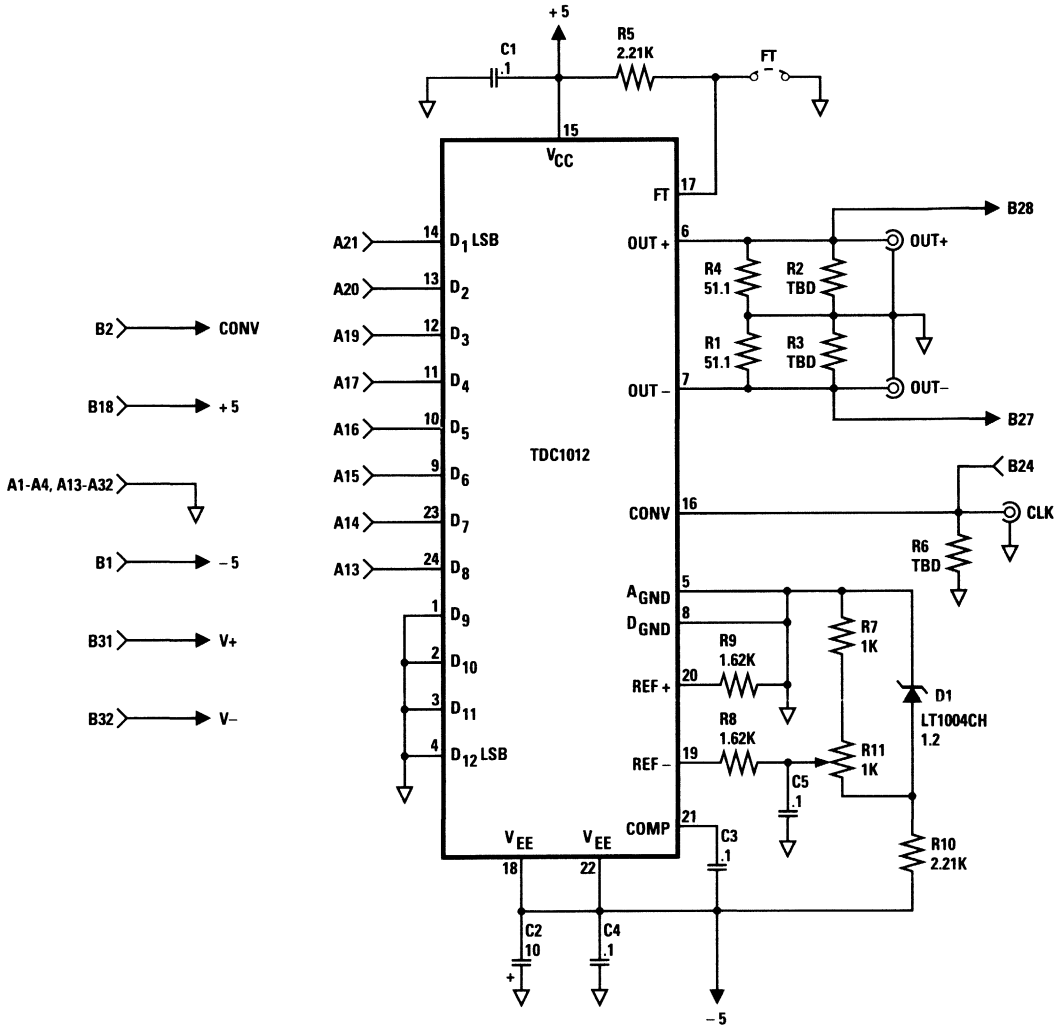


Figure 9. TDC1038E1C D/A Converter Schematic Diagram



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1038B6C	STD – T_A = 0°C to 70°C	Commercial	28 Pin CERDIP	1038B6C
TDC1038N6C	STD – T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	1038N6C
TDC1038R3C	STD – T_A = 0°C to 70°C	Commercial	28 Lead Plastic J-Leaded Chip Carrier	1038R3C
TDC1038E1C	STD – T_A = 0°C to 70°C	– –	Eurocard PC Board	TDC1038E1C

TDC1044

Monolithic Video A/D Converter

4-Bit, 25Msps

The TRW TDC1044 is a 25Msps (MegaSample Per Second) fully parallel analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 12.5MHz into 4-bit digital words. Use of a sample-and-hold circuit is not necessary for operation of the TDC1044. All digital inputs and outputs are TTL compatible.

The TDC1044 consists of 15 latching comparators, encoding logic, and an output register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

Features

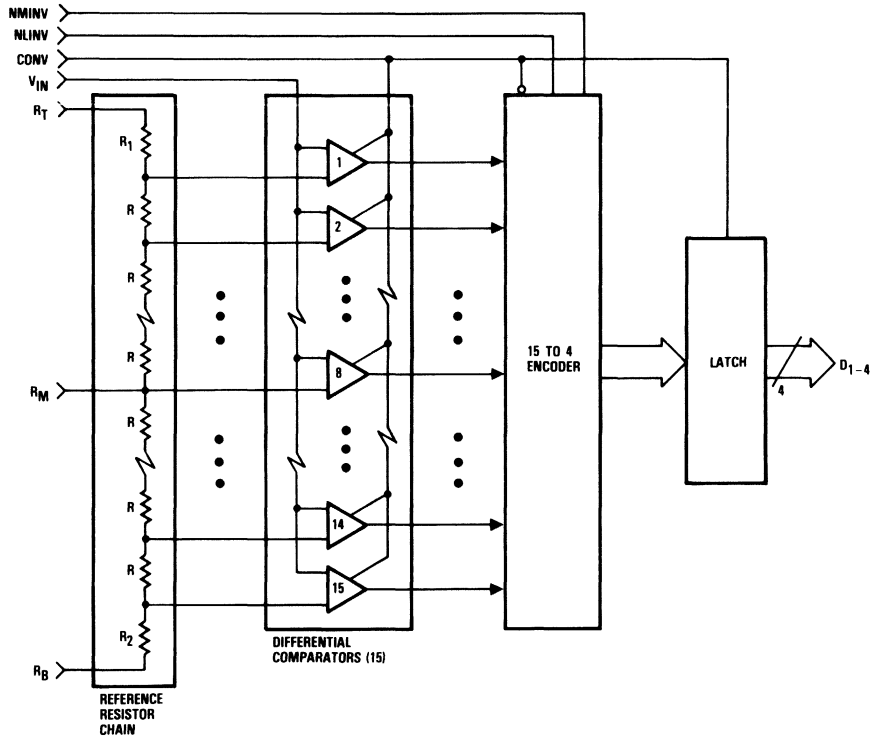
- 4-Bit Resolution
- 1/4 LSB Non-Linearity
- Sample-And-Hold Circuit Not Required
- 25Msps Conversion Rate
- Selectable Output Format
- Available In A 16 Pin DIP

Applications

- Video Special Effects
- Radar Data Conversion
- Medical Imaging
- Image Processing

A

Functional Block Diagram



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La Jolla, CA 92038

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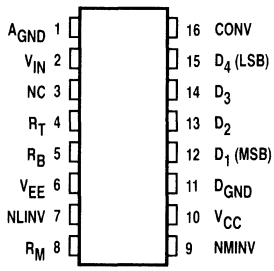
40G01899 Rev. D – 11/90
Printed in the U.S.A.

Pin Assignments



16 Pin DIP – B9 Package
16 Pin Plastic DIP – N9 Package

Functional Description

General Information

The TDC1044 has three functional sections: a comparator array, encoding logic, and an output register. The comparator array compares the input signal with 15 reference voltages to produce an N-of-15 code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-15 code into binary or two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output register holds the output constant between updates.

Power

The TDC1044 operates from two power supply voltages, +5.0V and −5.2V. The return for I_{CC} (the current drawn from the +5.0V supply) is D_{GND}. The return for I_{EE} (the current drawn from the −5.2V supply) is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1044 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RB}$ into digital form. V_{RB} (the voltage applied to R_B at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to R_T at the top of the reference resistor chain) should be between +0.1V and −1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 0.4V and 1.3V. The nominal voltages are V_{RT}=0.00V and V_{RB}=−1.00V. These voltages may be varied dynamically up to 10MHz. Due to slight variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are varied dynamically (as in an Automatic Gain Control circuit), a low-impedance reference source is required. A reference middle, R_M, is also provided; this may be used as an input to adjust the mid-scale point in order to improve integral linearity. This point may also be used as a tap to supply a mid-scale voltage to offset the analog input. If V_{RM} is used as an output, it must be connected to a high input impedance device which has small input current. Noise at this point may adversely affect the performance of the device.

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. These pins are active LOW as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Convert

The TDC1044 requires a CONVert (CONV) signal. A sample is taken (the comparators are latched) within t_{STO} after a rising edge of CONV. The coded result is translated to the output latches on the next rising edge. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. New data becomes valid after a maximum delay time, t_D.

Analog Input

The TDC1044 uses latching comparators which cause the input impedance to vary slightly with the signal level. For optimal performance, the source impedance of the driving circuit must be less than 25 Ohms. The input signal will not damage the device if it remains within the range of V_{EE} to +0.5V. If the input signal is at a voltage between V_{RT} and V_{RB}, the output will be a binary code between 0 and 15 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Outputs

The outputs of the TDC1044 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. Data becomes valid after a maximum delay time (t_D) after the rising edge of CONV. For optimum performance, 2.2 kOhm pull-up resistors are recommended.

No Connects

Pin 3 of the TDC1044 is labeled No Connect (NC), and has no connection to the chip. Connect this pin to A_{GND} for best noise performance.

Package Interconnections

Signal Type	Signal Name	Function	Value	B9, N9 Package Pins
Power	V_{CC}	Positive Supply Voltage	+5.0V	10
	V_{EE}	Negative Supply Voltage	−5.2V	6
	D_{GND}	Digital Ground	0.0V	11
	A_{GND}	Analog Ground	0.0V	1
Reference	R_T	Reference Resistor Top	0.0V	4
	R_M	Reference Resistor Middle	−0.5V	8
	R_B	Reference Resistor Bottom	1.0V	5
Controls	NMINV	Not Most Significant Bit INVert	TTL	9
	NLINV	Not Least Significant Bit INVert	TTL	7
Convert	CONV	Convert	TTL	16
Analog Input	V_{IN}	Analog Signal Input	0V to −1V	2
Outputs	D_1	Most Significant Bit Output	TTL	12
	D_2		TTL	13
	D_3		TTL	14
	D_4	Least Significant Bit Output	TTL	15
No Connects	NC	No Connect	A_{GND}	3

Figure 1. Timing Diagram

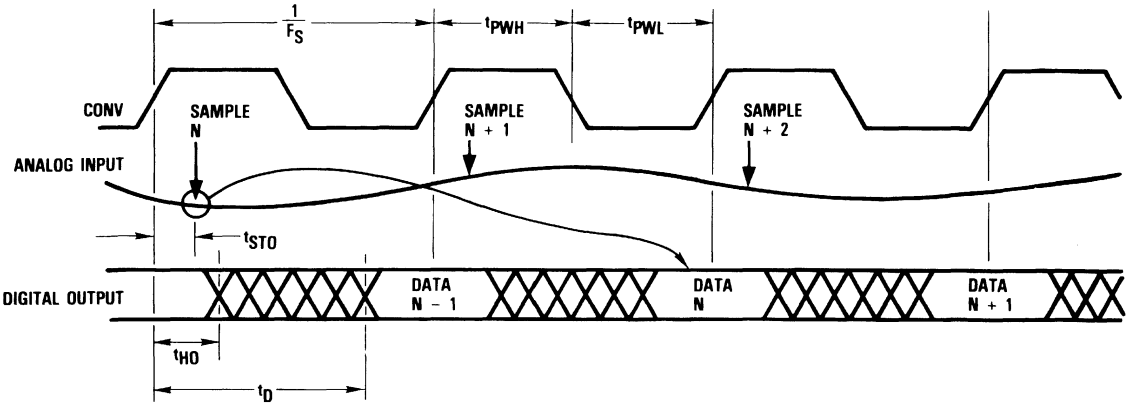


Figure 2. Simplified Analog Input Equivalent Circuit

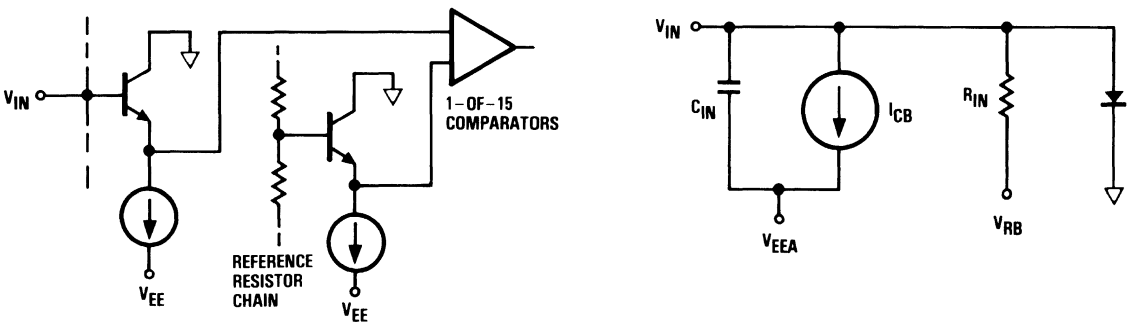


Figure 3. Digital Input Equivalent Circuit

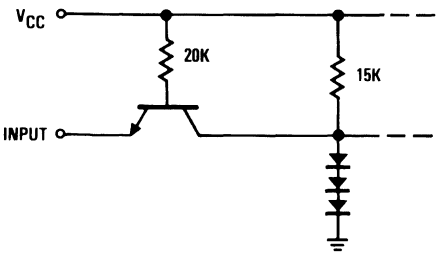
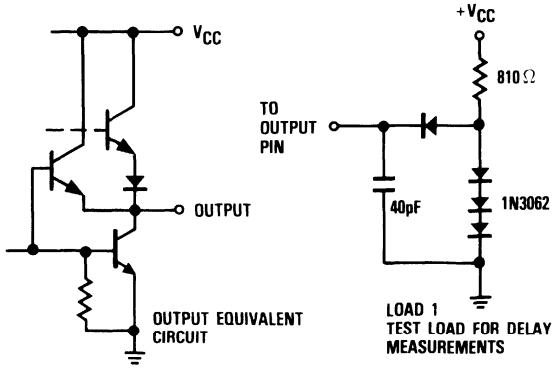


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}V
V_{RT} (measured to V_{RB})	−2.2 to +2.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to +5.5V [2]
Applied current, externally forced	−1.0 to +6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, ambient	−55 to +125°C
junction	+150°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (Measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage (Measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	17			17			ns
t_{PWH}	CONV Pulse Width, HIGH	17			17			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			2.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{RT}	Most Positive Reference	−1.9	0.0	0.1	−1.9	0.0	0.1	V
V_{RB}	Most Negative Reference	−2.1	−1.0	−0.1	−2.1	−1.0	−0.1	V
$V_{RT}-V_{RB}$	Reference Differential	0.2	1.0	2.0	0.2	1.0	2.0	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = MAX, static [1]		15		20	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, static [1]					
		T_A = 0°C to 70°C		-50			mA
		T_A = 70°C		-40			mA
		T_C = -55°C to 125°C				-65	mA
		T_C = -125°C				-35	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM		2		2	mA
R_{REF}	Total Reference Resistance		500		500		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	300		100		kOhms
C_{IN}	Input Capacitance			25		25	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		25		50	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V CONV		-0.4		-0.6	mA
		NMINV, NLINV		-0.6		-0.8	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, One pin to ground, one second duration, Output HIGH.		-30		-30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case: all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	25		25		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN		10		15	ns
t_D	Digital Output Delay	V_{CC} = MIN, V_{EE} = MIN, Load 1		30		35	ns
t_{HO}	Digital Output Hold Time	V_{CC} = MAX, V_{EE} = MAX, Load 1	5		5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error Integral, Independent	V_{RB} - NOM		1.6		1.6	%
E_{LD}	Linearity Error Differential			1.6		1.6	%
CS	Code Size	V_{RT}, V_{RB} - NOM	75	125	75	125	% Nominal
E_{OT}	Offset Error Top	V_{IN} - V_{RT}		+30		+30	mV
E_{OB}	Offset Error Bottom	V_{IN} - V_{RB}		+40		+40	mV
T_{CO}	Offset Error Temperature Coefficient			±20		±20	μV/°C
BW	Bandwidth, Full Power Input		12.5		12.5		MHz
t_{TR}	Transient Response, Full Scale			10		10	ns
E_{AP}	Aperture Error			30		30	ps

A

Output Coding Table[1]

Range	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
-1.00V FS	NMINV - 1 NLINV - 1	0 0	0 1	1 0
0.000V	0000	1111	1000	0111
-0.067V	0001	1110	1001	0110
-0.133V	0010	1101	1010	0101
-0.200V	0011	1100	1011	0100
-0.267V	0100	1011	1100	0011
-0.333V	0101	1010	1101	0010
-0.400V	0110	1001	1110	0001
-0.467V	0111	1000	1111	0000
-0.533V	1000	0111	0000	1111
-0.600V	1001	0110	0001	1110
-0.667V	1010	0101	0010	1101
-0.733V	1011	0100	0011	1100
-0.800V	1100	0011	0100	1011
-0.867V	1101	0010	0101	1010
-0.933V	1110	0001	0110	1001
-1.000V	1111	0000	0111	1000

Note:

1. Input voltages are at code centers.

Calibration

To calibrate the TDC1044, adjust V_{RT} and V_{RB} to set the 1st and 15th thresholds to the desired voltages. Assuming a 0V to −1V desired range, continuously strobe the converter with −0.0033V (1/2 LSB from 0.000V) on the analog input, and adjust V_{RT} for output toggling between codes 0000 and 0001. Then apply −0.967V (1/2 LSB from −1.000V) and adjust V_{RB} for toggling between codes 1110 and 1111. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with an amplifier offset control. R_B is a convenient point for gain adjustment that is not in the analog signal path.

Typical Interface Circuit

The TDC1044 does not require a special input buffer amplifier to drive the analog input because of its low input capacitance. A terminated low-impedance transmission line (<100 Ohms) connected to the V_{IN} terminal of the device is sufficient if the input voltage levels match those of the A/D converter.

However, many driver circuits lack sufficient offset control, drive current, or gain stability. The ***Typical Interface Circuit*** in ***Figure 5*** shows a simple amplifier and voltage reference circuit that may be used with the device. U2 is a wide-band operational amplifier with a gain factor of −1. A small value resistor, R12, serves to isolate the small input capacitance of the A/D converter from the amplifier output and insure frequency stability. The pulse and frequency response of the amplifier are optimized by variable capacitor C12. The reference voltage for the TDC1044 is generated by amplifier U3. System gain is adjusted by varying R9 which controls the reference voltage level to the A/D converter.

Input voltage range and input impedance for the circuit are determined by resistors R1 and R2. Formulas for calculating values for these input resistors are:

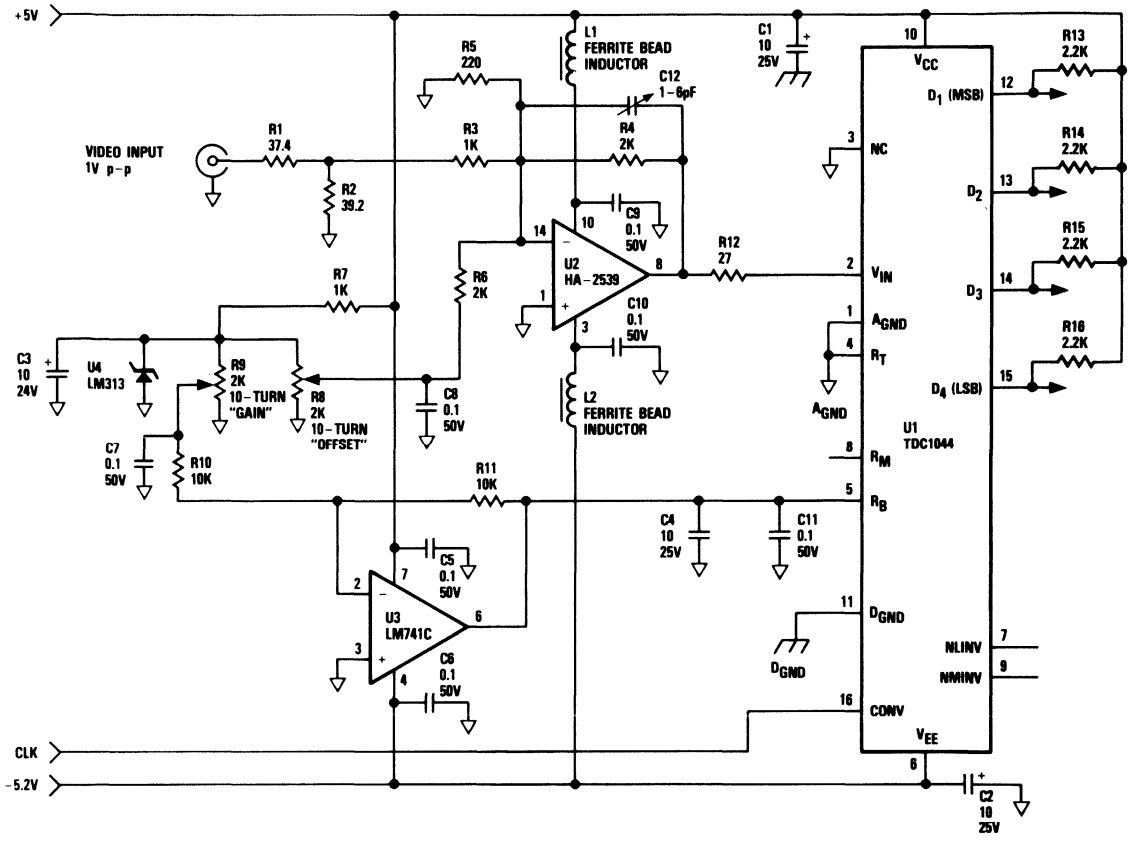
$$R1 = \frac{1}{\left(\frac{2VR}{Z_{IN}}\right) - \frac{1}{1000}}$$

and

$$R2 = Z_{IN} - \left(\frac{1000\ R1}{1000 + R1}\right)$$

where VR is the input voltage range of the circuit, Z_{IN} is the input impedance of the circuit, and the constant 1000 comes from the value of R3. As shown, the circuit is set up for 1Vp-p 75 Ohm video input.

Figure 5. Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1044B9C	STD–T_A=0°C to 70°C	Commercial	16 Pin DIP	1044B9C
TDC1044B9V	EXT–T_C= –55°C to 125°C	MIL-STD-883	16 Pin DIP	1044B9V
TDC1044N9C	STD–T_A=0°C to 70°C	Commercial	16 Pin Plastic DIP	1044N9C

TDC1046

Monolithic Video A/D Converter

6-Bit, 25Msps

The TRW TDC1046 is a 25Msps (MegaSample Per Second) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 12.5MHz into 6-bit digital words. Use of a sample-and-hold circuit is not necessary for operation of the TDC1046. All digital inputs and outputs are TTL compatible.

The TDC1046 consists of 63 clocked latching comparators, encoding logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

Features

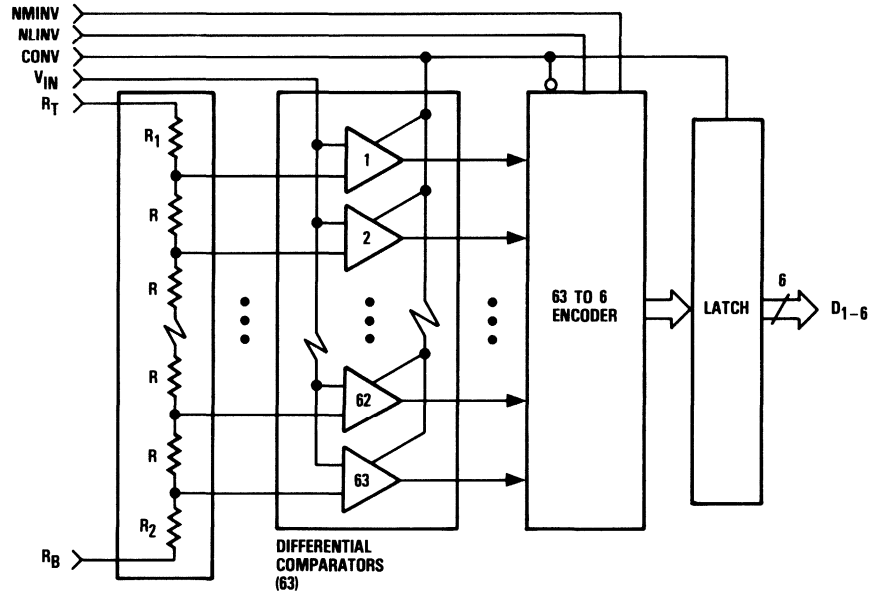
- 6-Bit Resolution
- 1/4 LSB Linearity
- Sample-And-Hold Circuit Not Required
- TTL Compatible
- 25Msps Conversion Rate
- Selectable Output Format
- Available In An 18 Pin CERDIP
- Low Cost
- Low Analog Input Capacitance
- Available Per Standard Military Drawing

Applications

- Low Cost Video Digitizing
- Medical Imaging
- Data Acquisition
- TV Special Effects
- Video Simulators
- Radar Data Conversion

A

Functional Block Diagram

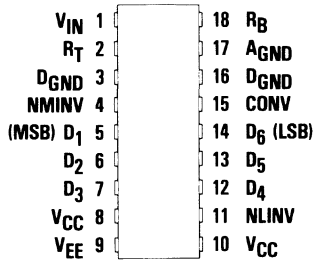


TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

40G01719 Rev. E–11/90
Printed in the U.S.A.

Pin Assignments



18 Pin CERDIP – B8 Package

Functional Description

General Information

The TDC1046 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 63 reference voltages to produce an N-of-63 code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-63 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

Power

The TDC1046 operates from two supply voltages, +5.0V and −5.2V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return for I_{EE}, the current drawn from the −5.2V supply, is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1046 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied to R_B at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to R_T at the top of the reference resistor chain) should be between +0.1V and −1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain ($V_{RT} - V_{RB}$) must be between 0.8V and 1.2V. The nominal voltages are $V_{RT} = 0.00V$ and $V_{RB} = -1.00V$. These voltages may be varied dynamically up to 12.5MHz. Due to variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically (as in an Automatic Gain Control circuit), a low-impedance reference source is required.

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. These pins are active LOW as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Convert

The TDC1046 requires a CONVert (CONV) signal. A sample is taken (the comparators are latched) within 5ns (t_{STO}) after a rising edge on the CONV pin. This time is t_{STO}, Sampling Time Offset. The 63 to 6 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal.

Analog Input

The TDC1046 uses strobed latching comparators which cause the input impedance to vary with the signal level, as comparator input transistors are cut-off or become active. For optimal performance, the source impedance of the driving circuit must be less than 50 Ohms. The input signal will not damage the TDC1046 if it remains within the range of V_{EE} to +0.5V. If the input signal is at a voltage between V_{RT} and V_{RB}, the output will be a binary number between 0 and 63 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Outputs

The outputs of the TDC1046 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. Data is guaranteed to be valid after a maximum delay time (t_D) after the rising edge of CONV. For optimum performance, 2.2 kOhm pull-up resistors are recommended.

Package Interconnections

Signal Type	Signal Name	Function	Value	B8 Package Pins
Power	V_{CC}	Positive Supply Voltage	+5.0V	8, 10
	V_{EE}	Negative Supply Voltage	−5.2V	9
	D_{GND}	Digital Ground	0.0V	3, 16
	A_{GND}	Analog Ground	0.0V	17
Reference	V_{RT}	Reference Resistor (Top)	0.0V	2
	V_{RB}	Reference Resistor (Bottom)	−1.0V	18
Controls	NMINV	Not Most Significant Bit INVert	TTL	4
	NLINV	Not Least Significant Bit INVert	TTL	11
Convert	CONV	Convert	TTL	15
Analog Input	V_{IN}	Analog Signal Input	0V to −1V	1
Outputs	D_1	MSB Output	TTL	5
	D_2		TTL	6
	D_3		TTL	7
	D_4		TTL	12
	D_5		TTL	13
	D_6	LSB Output	TTL	14

Output Coding Table [1]

Range	Binary		Two's Complement	
	True	Inverted	True	Inverted
	NMINV = 1	0	0	1
15.8730mV Step	NLINV = 1	0	1	0
0.0000V	000000	111111	100000	011111
−0.0159V	000001	111110	100001	011110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.4921V	011111	100000	111111	000000
−0.5079V	100000	011111	000000	111111
−0.5238V	100001	011110	000001	111110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.9841V	111110	000001	011110	100001
−1.0000V	111111	000000	011111	100000

Note: 1. Voltages are code midpoints when calibrated (see *Calibration* section).

Figure 1. Timing Diagram

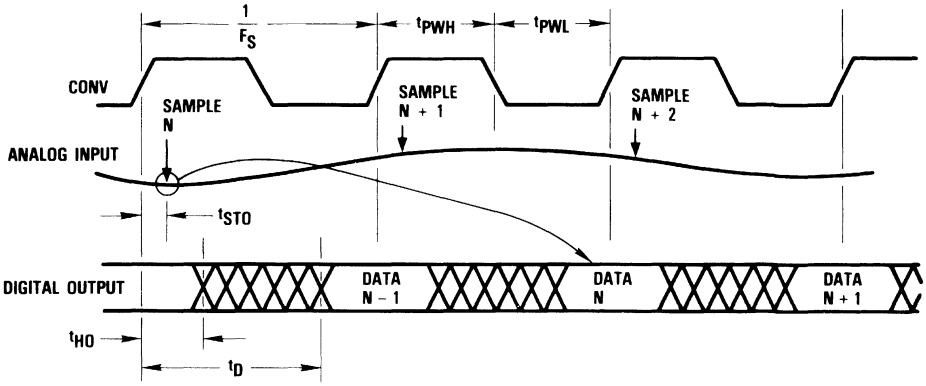
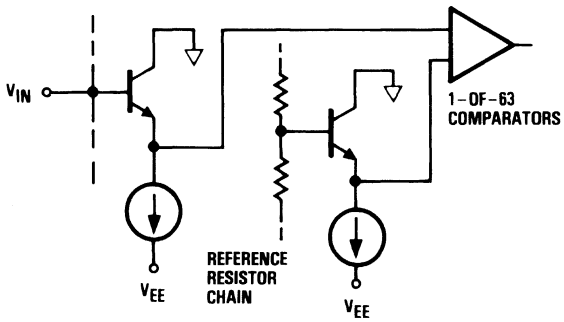
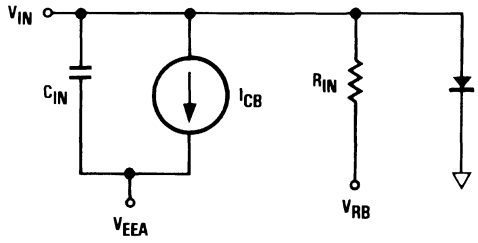


Figure 2. Simplified Analog Input Equivalent Circuit





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Digital Input Equivalent Circuit

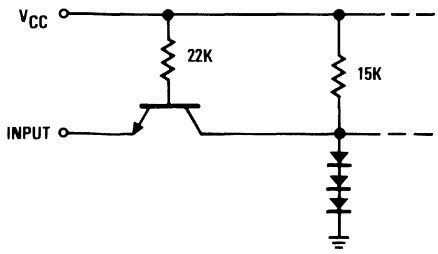
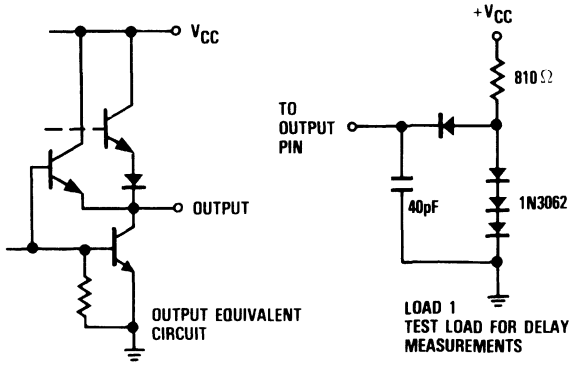


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}
V_{RT} (measured to V_{RB})	+1.2 to −1.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to 5.5V [2]
Applied current, externally forced	−1.0 to 6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, case	−55 to +125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width (LOW)	15			15			ns
t_{PWH}	CONV Pulse Width (HIGH)	17			17			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			2.0	mA
I_{OH}	Output Current, Logic HIGH			−0.4			−0.4	mA
V_{RT}	Most Positive Reference Input [1]	−0.1	0.0	0.1	−0.1	0.0	0.1	V
V_{RB}	Most Negative Reference Input [1]	−0.9	−1.0	−1.1	−0.9	−1.0	−1.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.8		1.2	0.8		1.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				
T_C	Case Temperature				−55		125	°C

Note:

1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = MAX, static[1]		20		25	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, static[1]					
		T_A = 0°C to 70°C		-95			mA
		T_A = 70°C		-75			mA
		T_C = -55°C to 125°C				-150	mA
		T_C = 125°C				-75	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM		10		15	mA
R_{REF}	Total Reference Resistance	V_{RT} - V_{RB} = MAX	100		66		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	40		40		kOhms
C_{IN}	Input Capacitance			30		30	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		105		180	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V CONV		-0.4		-0.6	mA
		NMINV, NLINV		-0.6		-0.8	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = 2 mA		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, One pin to ground, one second duration, output HIGH		-30		-30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	25		25		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN		5		10	ns
t_D	Output Delay	V_{CC} = MIN, V_{EE} = MIN, Load 1		30		35	ns
t_{HO}	Output Hold Time	V_{CC} = MAX, V_{EE} = MAX, Load 1	5		5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = Nom		0.4		0.4	%
E_{LD}	Linearity Error Differential			0.4		0.4	%
CS	Code Size	V_{RT}, V_{RB} = Nom	50	150	50	150	% Nominal
E_{OT}	Offset Error, Top	$V_{IN} = V_{RT}$		+50		+50	mV
E_{OB}	Offset Error, Bottom	$V_{IN} = V_{RB}$		−30		−30	mV
T_{CO}	Temperature Coefficient (Offset Voltage)			±20		±20	μV/°C
BW	Bandwidth, Full Power Input		12.5		12.5		MHz
t_{TR}	Transient Response, Full-Scale			10		10	ns
SNR	Signal-to-Noise Ratio	12.5MHz Bandwidth, 25Msps Conversion Rate					
	Peak Signal/RMS Noise	1MHz Input	42		36		dB
		12.5MHz Input	40		32		dB
	RMS Signal/RMS Noise	1MHz Input	33		33		dB
		12.5MHz Input	31		29		dB
E_{AP}	Aperture Error			30		30	ps

A

Calibration

To calibrate the TDC1046, adjust V_{RT} and V_{RB} to set the 1st and 63rd thresholds to the desired voltages. In the *Functional Block Diagram*, note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −1V desired range, continuously strobe the converter with −0.0079V on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −0.9921V and adjust V_{RB} for toggling between codes 62 and 63. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. R_B is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in *Figure 5*.

Typical Interface Circuit

The TDC1046 does not require a special input buffer amplifier to drive the analog input because of its low analog input capacitance. A terminated low-impedance transmission line (<100 Ohms) connected to the V_{IN} terminals of the TDC1046 is sufficient if the input voltage levels match those of the A/D converter.

However, many driver circuits lack sufficient offset control, drive current, or gain control. The *Typical Interface Circuit (Figure 5)* shows a simple buffer amplifier and voltage reference circuit that may be used with the TDC1046. U2 is a wide-band operational amplifier with a gain factor of −2. A small value resistor, R12, serves to help isolate the input capacitance of the A/D converter from the amplifier output and insure frequency stability. The pulse and frequency response of the buffer amplifier are optimized by variable capacitor C12.

The reference voltage for the TDC1046 is generated by amplifier U3 and PNP transistor Q1 which supplies the reference current. System gain is adjusted by varying R9 which controls the reference voltage level to the A/D converter.

Input voltage range and input impedance for the circuit are determined by resistors R1 and R2. Formulas for calculating values for these input resistors are:

$$R1 = \frac{1}{\left(\frac{2VR}{Z_{IN}}\right) - \frac{1}{1000}}$$

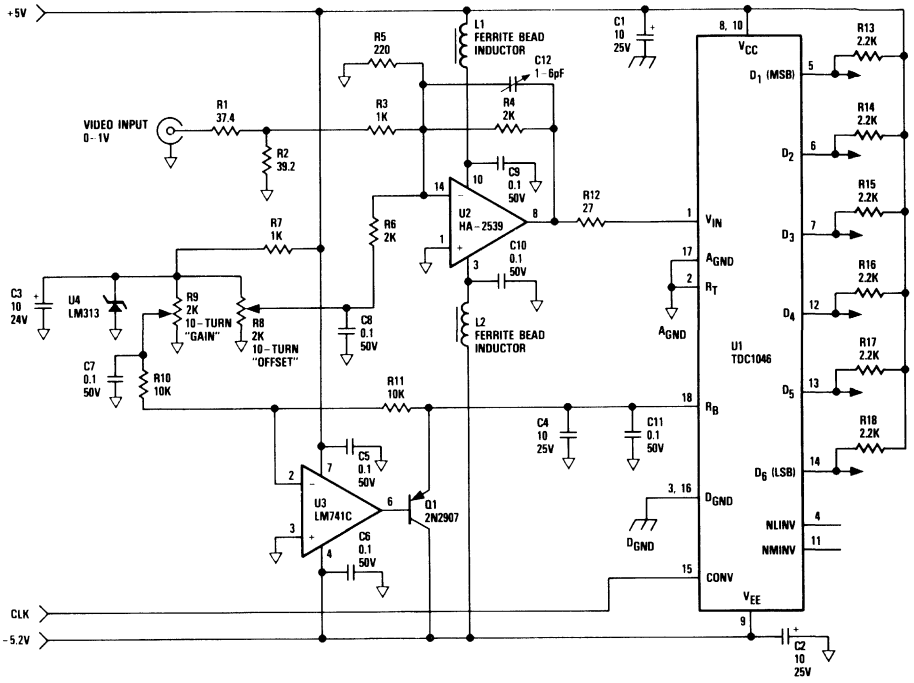
Typical Interface Circuit (cont.)

and

$$R2 = Z_{IN} - \left(\frac{1000\ R1}{1000 + R1}\right)$$

where VR is the input voltage range of the circuit, Z_{IN} is the input impedance of the circuit, and the constant 1000 comes from the value of R3. As shown, the circuit is set up for 1Vp-p 75 Ohm video input.

Figure 5. Typical Interface Circuit



Standard Military Drawing

These devices are also available as products manufactured, tested, and screened in compliance with Standard Military Drawings (SMDs). The nearest vendor equivalent product is shown below; however, the applicable SMD is the sole controlling document defining the SMD product.

Standard Military Drawing	Nearest Equivalent TRW Product No.	Package
5962-87786-01VA	TDC1046B8V	18 Pin CERDIP

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1046B8C	STD – T_A = 0°C to 70°C	Commercial	18 Pin CERDIP	1046B8C
TDC1046B8V	EXT – T_C = –55°C to 125°C	MIL-STD-883	18 Pin CERDIP	1046B8V
5962-87786-01VC	EXT – T_C = –55°C to 125°C	Per Standard Military Drawing	18 Pin CERDIP	5962-87786-01VC

TDC1047

Monolithic Video A/D Converter

7-Bit, 20Msps

The TRW TDC1047 is a 20Msps (MegaSample Per Second) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 7MHz into 7-bit digital words. A sample-and-hold circuit is not necessary. All digital inputs and outputs are TTL compatible.

The TDC1047 consists of 127 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

The TDC1047 is pin and function compatible with TRW's TDC1027, and offers increased performance with lower power dissipation.

Features

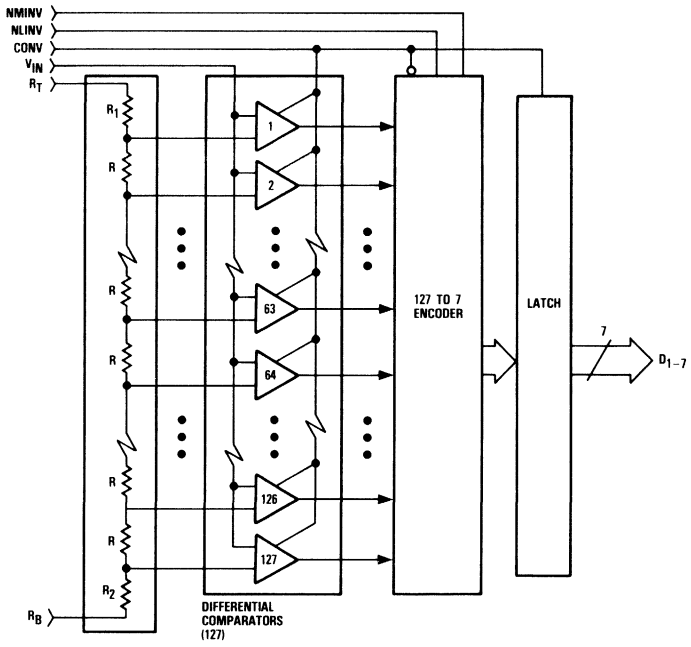
- 7-Bit Resolution
- 1/2 LSB Linearity
- Sample-And-Hold Circuit Not Required
- 20Msps Conversion Rate
- Selectable Output Format
- Available In 24 Pin CERDIP

Applications

- Low-Cost Video Digitizing
- Medical Imaging
- TV Special Effects
- Video Simulators
- Radar Data Conversion

A

Functional Block Diagram



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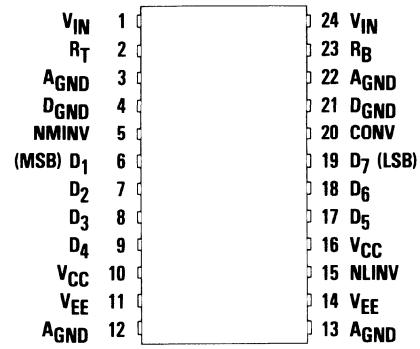
40G01393 Rev. E–11/90
Printed in the U.S.A.

Pin Assignments



24 Pin CERDIP – B7 Package

Functional Description

General Information

The TDC1047 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 127 reference voltages to produce an N-of-127 code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-127 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

Power

The TDC1047 operates from two supply voltages, +5.0V and −5.2V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return for I_{EE}, the current drawn from the −5.2V supply, is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1047 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and −1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 0.8V and 1.2V. The nominal voltages are V_{RT} = 0.00V and V_{RB} = −1.00V. These voltages may be varied dynamically up to 7MHz. Due to variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically as in an Automatic Gain Control (AGC) circuit, a low-impedance reference source is recommended.

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. These pins are active LOW as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Convert

The TDC1047 requires a CONVert (CONV) signal. A sample is taken (the comparators are latched) within the Sampling Time Offset (t_{STO}) of a rising edge on the CONV pin. The 127 to 7 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. This permits the previous conversion result to be acquired by external circuitry at that rising edge, i.e., data for sample N is acquired by the external circuitry while the TDC1047 is taking input sample N+2.

Analog Input

The TDC1047 uses strobed latching comparators which cause the input impedance to vary with the signal level, as comparator input transistors are cut-off or become active. For optimal performance, both V_{IN} pins must be used and the source impedance of the driving circuit must be less than 30 Ohms. The input signal will not damage the TDC1047 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 127 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Outputs

The outputs of the TDC1047 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal.

Package Interconnections

Signal Type	Signal Name	Function	Value	B7 Package Pins
Power	V_{CC}	Positive Supply Voltage	+5.0V	10, 16
	V_{EE}	Negative Supply Voltage	−5.2V	11, 14
	D_{GND}	Digital Ground	0.0V	4, 21
	A_{GND}	Analog Ground	0.0V	3, 12, 13, 22
Reference	R_T	Reference Resistor (Top)	0.00V	2
	R_B	Reference Resistor (Bottom)	−1.00V	23
Controls	NMINV	Not Most Significant Bit INVert	TTL	5
	NLINV	Not Least Significant Bit INVert	TTL	15
Convert	CONV	Convert	TTL	20
Analog Input	V_{IN}	Analog Signal Input	0V to −1V	1, 24
Outputs	D_1	MSB Output	TTL	6
	D_2		TTL	7
	D_3		TTL	8
	D_4		TTL	9
	D_5		TTL	17
	D_6		TTL	18
	D_7	LSB Output	TTL	19

Figure 1. Timing Diagram

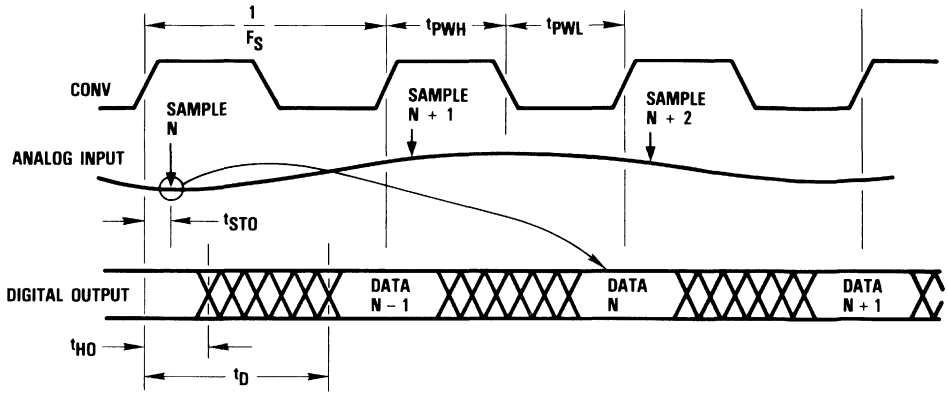
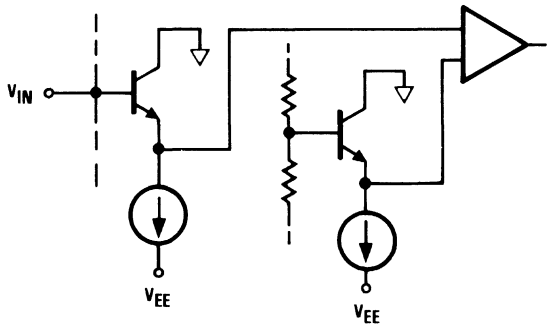
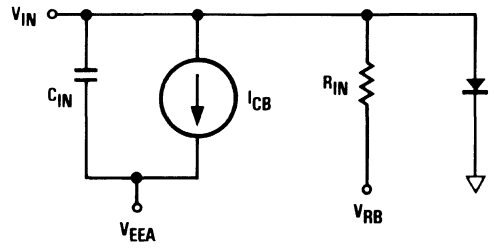


Figure 2. Simplified Analog Input Equivalent Circuit





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Digital Input Equivalent Circuit

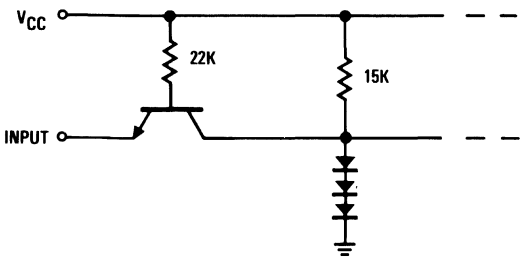
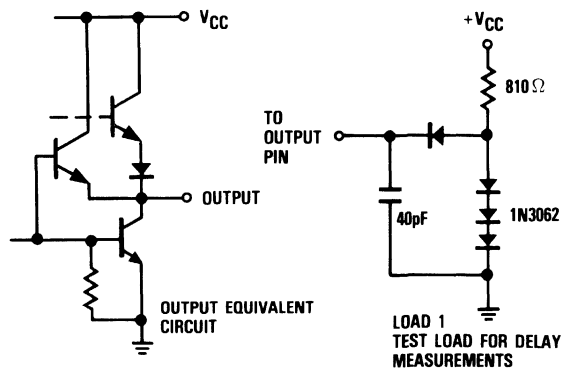


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device will be damaged)[1]

Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}
V_{RT} (measured to V_{RB})	+2.2 to −2.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to 5.5V[2]
Applied current, externally forced	−1.0 to 6.0mA[3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, case	−55 to + 125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter	Test Conditions	Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	14			14			ns
t_{PWH}	CONV Pulse Width, HIGH	16			16			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			2.0	mA
I_{OH}	Output Current, Logic HIGH			−0.4			−0.4	mA
V_{RT}	Most Positive Reference Input[1]	−0.1	0.0	0.1	−0.1	0.0	0.1	V
V_{RB}	Most Negative Reference Input[1]	−0.9	−1.0	−1.1	−0.9	−1.0	−1.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.8	1.0	1.2	0.8	1.0	1.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note:

1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = Max, static [1]		25		30	mA
I_{EE}	Negative Supply Current	V_{EE} = Max, static [1]					
		T_A = 0°C to 70°C		-170			mA
		T_A = 70°C		-135			mA
		T_C = -55°C to 125°C				-220	mA
		T_C = 125°C				-130	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = Nom		35		50	mA
R_{REF}	Total Reference Resistance		28		20		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}	100		40		kOhms
C_{IN}	Input Capacitance			60		60	pF
I_{CB}	Input Constant Bias Current	V_{EE} = Max		150		300	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.5V CONV		-0.4		-0.6	mA
		NMINV, NLINV		-0.6		-0.8	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = Max, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = Max, one pin to ground, one second duration.		-30		-30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = Min, V_{EE} = Min	20		20		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = Min, V_{EE} = Min		7		10	ns
t_D	Output Delay	V_{CC} = Min, V_{EE} = Min, Load 1		30		35	ns
t_{HO}	Output Hold Time	V_{CC} = Max, V_{EE} = Max, Load 1	5		5		ns

System performance characteristics within specified operating conditions

Parameter			Test Conditions	Temperature Range				Units
				Standard		Extended		
				Min	Max	Min	Max	
E_{LI}	Linearity Error	Integral, Independent	V_{RT}, V_{RB} = Nom		0.4		0.4	%
E_{LD}	Linearity Error	Differential			0.4		0.4	%
CS	Code Size		V_{RT}, V_{RB} = Nom	30	170	30	170	% Nominal
V_{OT}	Offset Voltage	Top	V_{IN} = V_{RT}		+50		+50	mV
V_{OB}	Offset Voltage	Bottom	V_{IN} = V_{RB}		−30		−30	mV
T_{CO}	Temperature Coefficient				±20		±20	μV/°C
BW	Bandwidth, Full Power Input			7		7		MHz
t_{TR}	Transient Response, Full Scale				10		10	ns
SNR	Signal-to-Noise Ratio		7MHz Bandwidth,					
			20MSPS Conversion Rate					
		Peak Signal/RMS Noise	1MHz Input	48		46		dB
			7MHz Input	46		44		dB
		RMS Signal/RMS Noise	1MHz Input	39		37		dB
			7MHz Input	37		35		dB
E_{AP}	Aperture Error				50		50	ps
DP	Differential Phase Error[1]		F_S = 4 x NTSC		1.5		1.5	Degree
DG	Differential Gain Error[1]		F_S = 4 x NTSC		2.5		2.5	%

Note:
1. In excess of quantization.

Output Coding

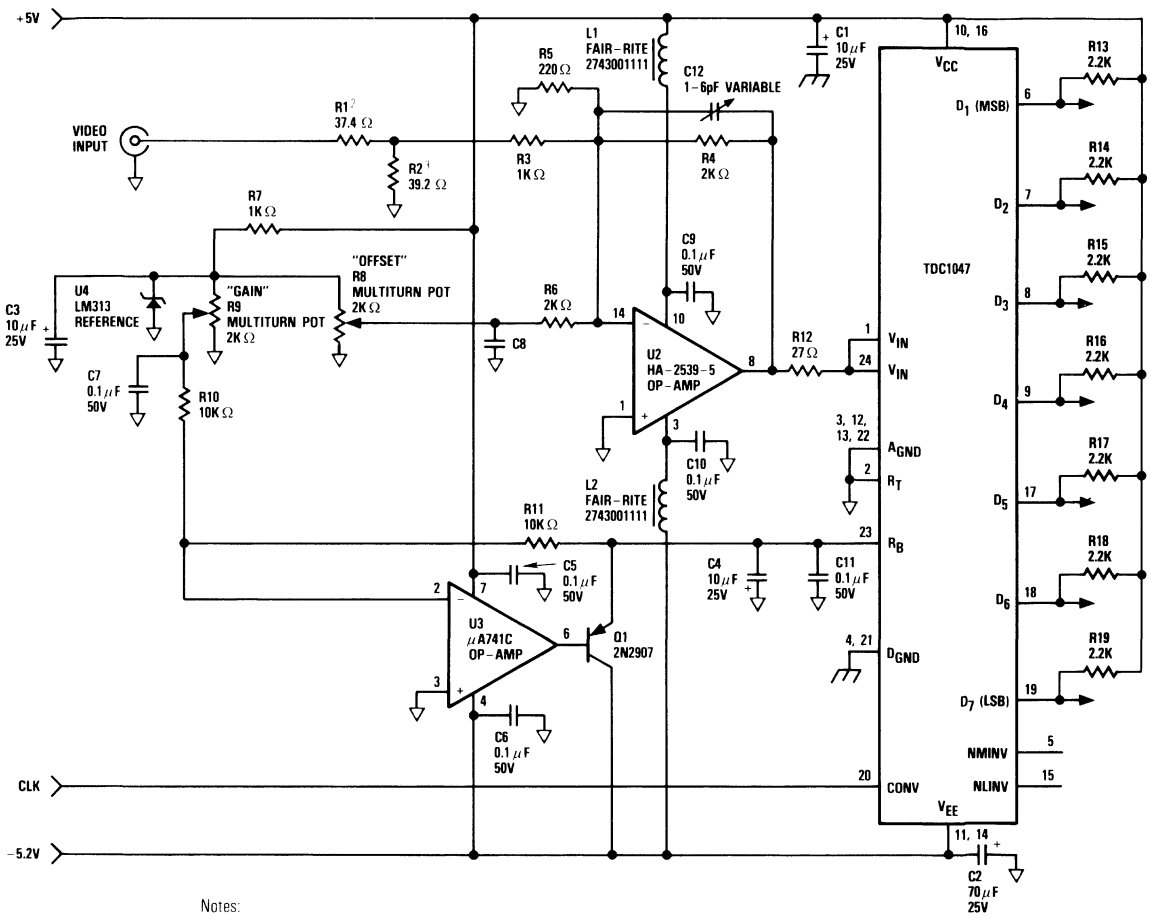
Step		Binary		Offset Two's Complement	
	Range	True	Inverted	True	Inverted
	−1.0000V FS	NMINV = 1	0	0	1
	7.874mV STEP	NLINV = 1	0	1	0
000	0.0000V	0000000	1111111	1000000	0111111
001	−0.0078V	0000001	1111110	1000001	0111110
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
063	−0.4960V	0111111	1000000	1111111	0000000
064	−0.5039V	1000000	0111111	0000000	1111111
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
126	−1.9921V	1111110	0000001	0111110	1000001
127	−1.0000V	1111111	0000000	0111111	1000000

Note:
1. Voltages are code midpoints when calibrated (see Calibration Section).

Calibration

To calibrate the TDC1047, adjust V_{RT} and V_{RB} to set the 1st and 127th thresholds to the desired voltages in the block diagram. Note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −1V desired range, continuously strobe the converter with −0.0039V on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −0.9961V and adjust V_{RB} for toggling between codes 126 and 127. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. R_B is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in Figure 5.

Figure 5. Typical Interface Circuit



Notes:

1. Unless otherwise specified, all resistors are 1/4W, 2%.
2. $R1 = Z_{IN} - \left(\frac{1000\ R2}{1000 + R2}\right)$
3. $R2 = \frac{1}{\left(\frac{2V_{Range}}{V_{REF}\ Z_{IN}}\right) - 0.001}$

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1047B7C	STD – T_A = 0°C to 70°C	Commercial	24 Pin CERDIP	1047B7C
TDC1047B7V	EXT – T_C = – 55°C to 125°C	MIL-STD-883	24 Pin CERDIP	1047B7V

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TDC1048

Monolithic Video A/D Converter

8-Bit, 20Msps

The TRW TDC1048 is a 20Msps (MegaSample Per Second) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 7MHz into 8-bit digital words. A sample-and-hold circuit is not necessary. Low power consumption eases thermal considerations, and board space is minimized with a 28 pin package. All digital inputs and outputs are TTL compatible.

The TDC1048 consists of 255 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

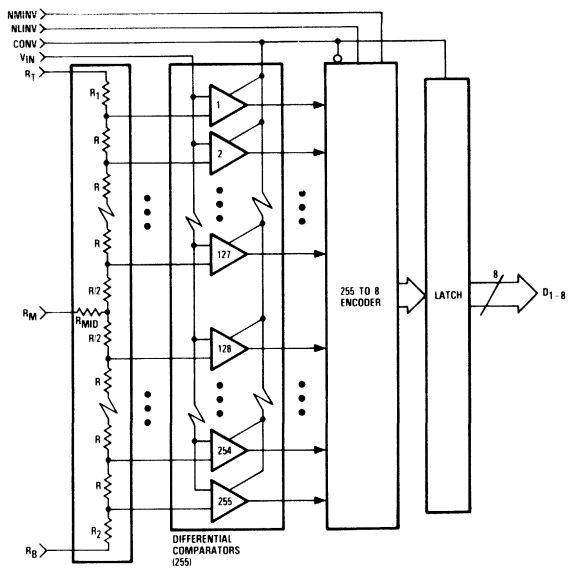
Features

- 8-Bit Resolution
- 20Msps Conversion Rate
- Sample-And-Hold Circuit Not Required
- Differential Phase 1 Degree
- Differential Gain 2%
- 1/2 LSB Linearity
- Guaranteed Monotonic
- TTL Compatible Outputs
- Selectable Data Format
- Available In 28 Pin Plastic DIP, CERDIP, Or LCC
- MIL-STD-883 Compliant Screening Available
- Available Per Standard Military Drawing
- Evaluation Board – TDC1048E1C
- Also Available As A Complete Hybrid – THC1068

Applications

- Low-Cost Video Digitizing
- Radar Data Conversion
- Data Acquisition
- Medical Imaging

Functional Block Diagram



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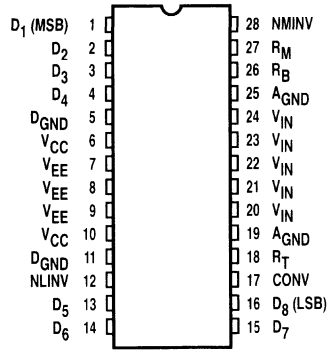
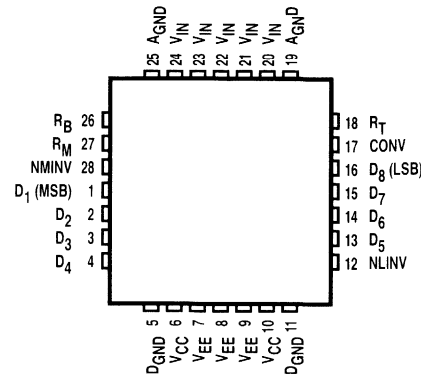
Pin Assignments



28 Pin CERDIP – B6 Package
28 Pin Plastic DIP – N6 Package



28 Contact Chip Carrier – C3 Package
28 Leaded Plastic Chip Carrier – R3 Package

Functional Description

General Information

The TDC1048 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 255 reference voltages to produce an N-of-255 code (sometimes referred to as a "thermometer" code, as all the comparators below the signal will be on, and all those above the signal will be off). The encoding logic converts the N-of-255 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

Power

The TDC1048 operates from two supply voltages, +5.0V and −5.2V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return for I_{EE}, the current drawn from the −5.2V supply, is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1048 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and −2.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 1.8V and 2.2V. The nominal voltages are V_{RT} = 0.0V, V_{RB} = −2.0V.

A midpoint tap, R_M, allows the converter to be adjusted for optimum linearity, although adjustment is not necessary to meet the linearity specification. It can also be used to achieve a nonlinear transfer function. The circuit shown in ***Figure 5*** will provide approximately 1/2 LSB adjustment of the linearity midpoint. The characteristic impedance seen at this node is approximately 220Ω, and should be driven from a low-impedance source. Note that any load applied to this node will affect linearity, and noise introduced at this point will degrade the quantization process.

Due to the variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically, (as in an automatic gain control circuit), a low-impedance reference source is required. The reference voltages may be varied dynamically up to 5MHz.

Control

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. These pins are active LOW, as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Convert

The TDC1048 requires a convert (CONV) signal. A sample is taken (the comparators are latched) within 15ns after a rising edge on the CONV pin. This time is t_{STO}, Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a function of temperature, but the short-term uncertainty (jitter) in sampling offset time is less than 100 picoseconds. The 255 to 8 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. Data is held valid at the output register for at least t_{HO}, Output Hold Time, after the rising edge of CONV. New data becomes valid after a Digital Output Delay, t_D, time. This permits the previous conversion result to be acquired by external circuitry at that rising edge, i.e., data for sample N is acquired by the external circuitry while the TDC1048 is taking input sample N+2.

Analog Input

The TDC1048 uses strobed latching comparators which cause the input impedance to vary with the signal level, as comparator input transistors are cut-off or become active. As a result, for optimal performance, the source impedance of the driving device must be less than 25Ω. The input signal will not damage the TDC1048 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 255 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction. All five analog input pins must be connected together.

Outputs

The outputs of the TDC1048 are TTL compatible, capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONVert signal. For optimum performance, 2.2 kΩ pull-up resistors are recommended.

Package Interconnections

Signal Type	Signal Name	Function	Value	B6, N6, C3, R3 Package Pins
Power	V_{CC}	Positive Supply Voltage	+5.0V	6, 10
	V_{EE}	Negative Supply Voltage	−5.2V	7, 8, 9
	D_{GND}	Digital Ground	0.0V	5, 11
	A_{GND}	Analog Ground	0.0V	19, 25
Reference	R_T	Reference Resistor (Top)	0.0V	18
	R_M	Reference Resistor (Middle)	−0.996V	27
	R_B	Reference Resistor (Bottom)	−2.0V	26
Controls	NMINV	Not Most Significant Bit INVert	TTL	28
	NLINV	Not Least Significant Bit INVert	TTL	12
Convert	CONV	Convert	TTL	17
Analog Input	V_{IN}	Analog Signal Input	0V to −2V	20, 21, 22, 23, 24

Package Interconnections (cont.)

Signal Type	Signal Name	Function	Value	B6, N6, C3, R3 Package Pins
Outputs	D_1	MSB Output	TTL	1
	D_2		TTL	2
	D_3		TTL	3
	D_4		TTL	4
	D_5		TTL	13
	D_6		TTL	14
	D_7		TTL	15
	D_8	LSB Output	TTL	16

Figure 1. Timing Diagram

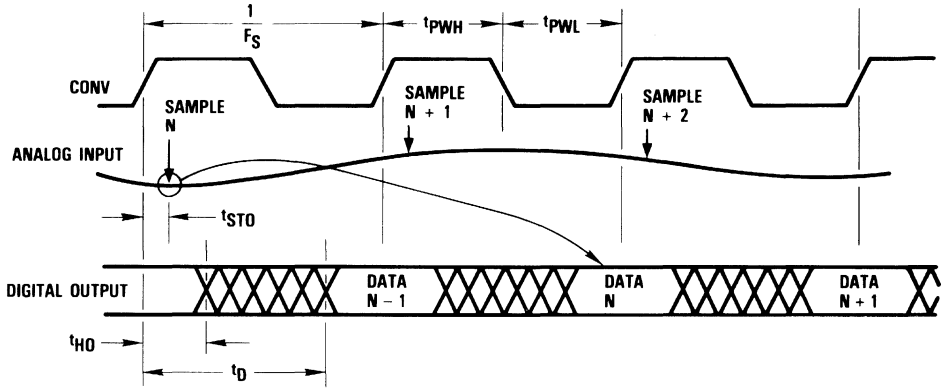
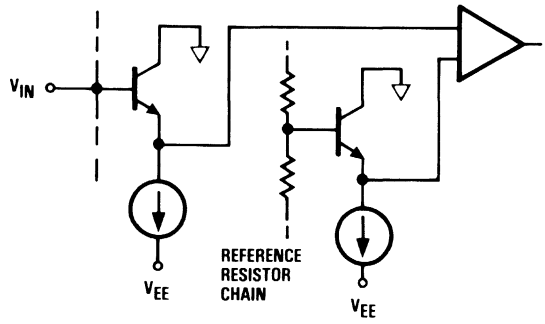
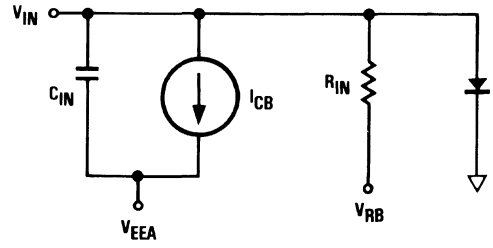


Figure 2. Simplified Analog Input Equivalent Circuit





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Convert Input Equivalent Circuit

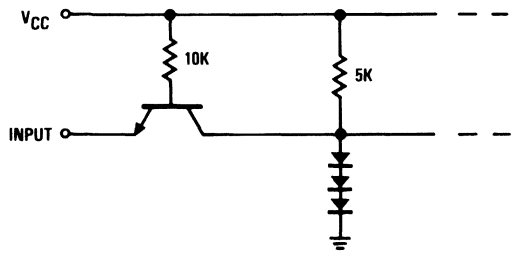
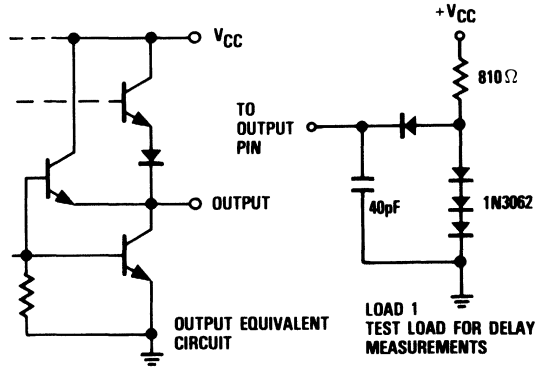


Figure 4. Output Circuits



A

Output Coding Table

Step	Range		Binary		Offset Two's Complement	
			True	Inverted	True	Inverted
	−2.0000V FS 7.8431mV Step	−2.0480V FS 8.000mV Step	NMINV=1 NLINV=1	0 0	0 1	1 0
000	0.0000V	0.0000V	00000000	11111111	10000000	01111111
001	−0.0078V	−0.0080V	00000001	11111110	10000001	01111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	−0.9961V	−1.0160V	01111111	10000000	11111111	00000000
128	−1.0039V	−1.0240V	10000000	01111111	00000000	11111111
129	−1.0118V	−1.0320V	10000001	01111110	00000001	11111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
254	−1.9921V	−2.0320V	11111110	00000001	01111110	10000001
255	−2.0000V	−2.0400V	11111111	00000000	01111111	10000000

Notes:
1. NMINV and NLINV are to be considered DC controls. They may be tied to +5V for a logical "1" and tied to ground for a logical "0."
2. Voltages are code midpoints when calibrated by the procedure given below.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND}) ..... −0.5 to +7.0V
V_{EE} (measured to A_{GND}) ..... +0.5 to −7.0V
A_{GND} (measured to D_{GND}) ..... −0.5 to +0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND}) ..... −0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND}) ..... +0.5 to V_{EE}
V_{RT} (measured to V_{RB}) ..... +2.2 to −2.2V

Output

Applied voltage (measured to D_{GND}) ..... −0.5 to +5.5V [2]
Applied current, externally forced ..... −1.0 to +6.0mA [3,4]
Short circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, ambient ..... −55 to +125°C
junction ..... +175°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.50	V
V_{EE}	Negative Supply Voltage	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0	+0.1	−0.1	0	+0.1	V
t_{PWL}	CONV Pulse Width, LOW	18			18			ns
t_{PWH}	CONV Pulse Width, HIGH	22			22			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
V_{RT}	Most Positive Reference Input [1]	−0.1	0.0	0.1	−0.1	0.0	+0.1	V
V_{RB}	Most Negative Reference Input [1]	−1.9	−2.0	−2.1	−1.9	−2.0	−2.1	V
V_{RT}-V_{RB}	Voltage Reference Differential	1.8	2.0	2.2	1.8	2.0	2.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note: 1. V_{RT} Must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = Max, static [1]		35		40	mA
I_{EE}	Negative Supply Current	V_{EE} = Max, static [1]					
		T_A = 0°C to 70°C		−260			mA
		T_A = 70°C		−185			mA
		T_C = −55°C to 125°C				−320	mA
		T_C = 125°C				−180	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = Nom		40		50	mA
R_{REF}	Total Reference Resistance		50		40		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}	10		10		kOhms
C_{IN}	Input Capacitance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}		100		100	pF
I_{CB}	Input Constant Bias Current	V_{EE} = Max		200		550	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.5V					
		CONV		−0.4		−0.4	mA
		NMINV, NLINV		−0.6		−0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = Max, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = Max, Output HIGH, one pin to ground, one second duration max.		−30		−30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note: 1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = Min, V_{EE} = Min	20		20		Msps
t_{STO}	Sampling Time Offset	V_{CC} = Min, V_{EE} = Min	0	10	0	15	ns
t_D	Digital Output Delay	V_{CC} = Min, V_{EE} = Min, Load 1		30		35	ns
t_{HO}	Digital Output Hold Time	V_{CC} = Max, V_{EE} = Max, Load 1	5		5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = Nom		0.2		0.2	%
E_{LD}	Linearity Error Differential			0.2		0.2	%
CS	Code Size		25	175	25	175	% Nominal
E_{OT}	Offset Error, Top	$V_{IN}=V_{RT}$		+40		+40	mV
E_{OB}	Offset Error, Bottom	$V_{IN}=V_{RB}$		−30		−30	mV
T_{CO}	Offset Error, Temperature Coefficient			±20		±20	μV/°C
BW	Bandwidth, Full Power Input		7		5		MHz
t_{TR}	Transient Response, Full-Scale			20		20	ns
SNR	Signal-to-Noise Ratio	20Msps Conversion Rate, 10MHz Bandwidth					
	Peak Signal/RMS Noise	1.248MHz Input	54		53		dB
		2.438MHz Input	53		52		dB
	RMS Signal/RMS Noise	1.248MHz Input	45		44		dB
		2.438MHz Input	44		43		dB
E_{AP}	Aperture Error			60		60	ps
DP	Differential Phase Error	F_S = 4 x NTSC		1.0		1.0	Degree
DG	Differential Gain Error	F_S = 4 x NTSC		2.0		2.0	%
NPR	Noise Power Ratio	DC to 8MHz White Noise Bandwidth 4 Sigma Loading 1.248MHz Slot 20Msps Conversion Rate	36.5		36.5		dB

Calibration

To calibrate the TDC1048, adjust V_{RT} and V_{RB} to set the 1st and 255th thresholds to the desired voltages. Note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −2V desired range, continuously strobe the converter with −0.0039V (1/2 LSB from 0V) on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −1.996V (1/2 LSB from −2V) and adjust V_{RB} for toggling between codes 62 and 63.

The degree of required adjustment is indicated by the offset error, E_{OT} and E_{OB}. Offset errors are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the integrated circuit. These parasitic resistors are shown as R_1 and R_2 in the *Functional Block Diagram*. Calibration will cancel all offset voltages, eliminating offset and gain errors.

The above method of calibration requires that both ends of the resistor chain, R_T and R_B, are driven by buffered operational amplifiers. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error, which can be compensated for by varying the voltage applied to R_B. The bottom reference is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in *Figure 6*.

Typical Interface

Figure 6 shows an example of a typical interface circuit for the TDC1048. The analog input amplifier is a bipolar wideband operational amplifier, which is used to directly drive the A/D converter. Bipolar inputs may be accommodated by adjusting the offset control. TRW's TDC4611 provides a stable reference for both the offset and gain control. All five V_{IN} pins are connected close to the device package, and the buffer amplifier feedback loop should be closed at that point. The buffer has a gain of minus two, increasing a 1Vp-p video input signal to the recommended 2Vp-p input for the A/D converter. Proper decoupling is recommended for all systems.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier on the TDC4611, buffered with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain. The bottom reference voltage can be adjusted to cancel the gain error introduced by the offset voltage, E_{OB}, as discussed in the *Calibration* section.

Figure 5. Typical Reference Midpoint Adjust Circuit

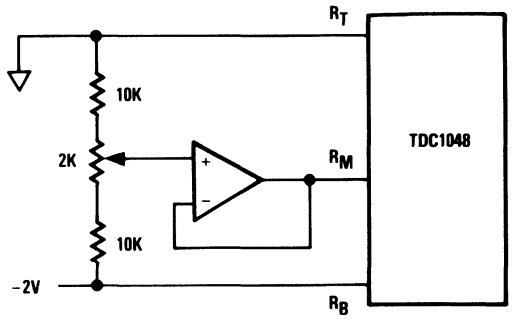
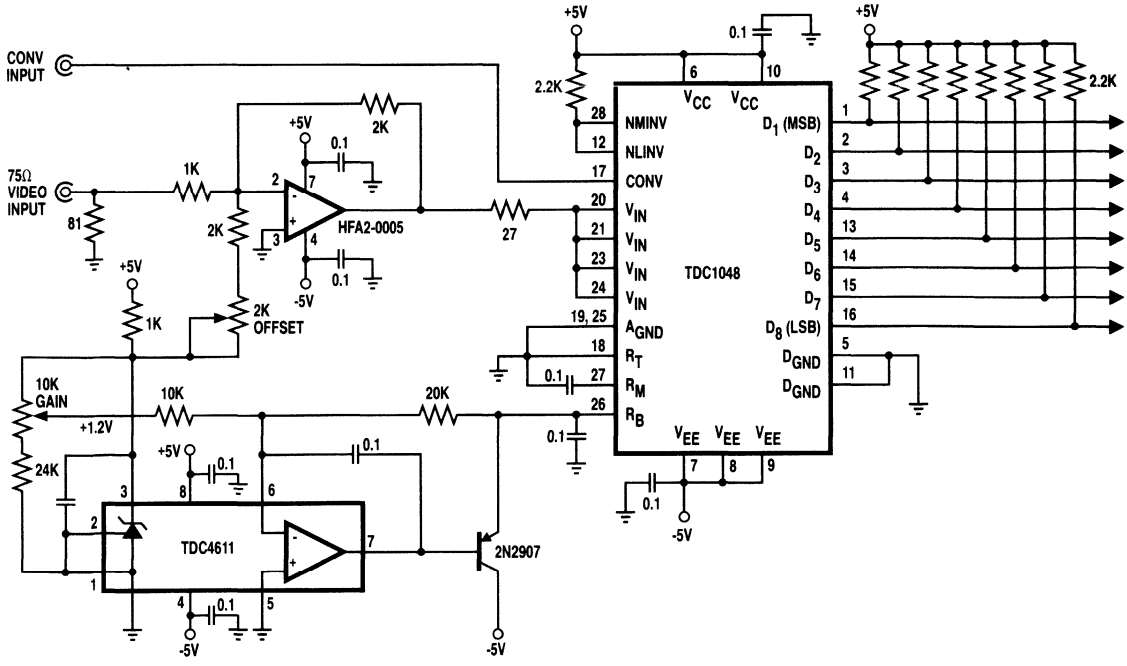


Figure 6. Typical Interface Circuit



Evaluation Board

The TDC1048E1C is a Eurocard-style printed circuit board designed to optimize the performance of, and to aid in the evaluation of, the TDC1048 A/D converter. The board dimensions are 100mm x 160mm with a standard 64 pin double-row DIN male connector installed. A complementary 64 pin double-row DIN female connector is included with the board. The circuitry on the board includes reference voltage generator, wideband video input amplifier, and TDC1048 8-bit A/D converter.

The board employs only two conducting sides. Most of the circuit interconnections are on the bottom of the board while the top is mostly solid ground plane. SMA connectors are installed on the board to facilitate analog I/O and clocks. The board is calibrated and tested at the factory.

Power and Ground

Two power supply voltages are required for the operation of the TDC1048E1C: $V_{CC} = +5V$ and $V_{EE} = -5.2V$. All power inputs are decoupled to a solid ground planes, A_{GND} and D_{GND}. For best performance, all A_{GND} ad D_{GND} pins of the board are connected to power supply ground and all ground pins be should be used.

Voltage Reference Generator

The TDC1048E1C has a voltage reference generator circuit for driving the RB terminal of the TDC1048. With RT grounded, a variable $-2V$ is supplied to RB from U3 and Q1. The GAIN potentiometer provides $\pm 10\%$ adjustment range on the RB voltage. Diodes D1 through D4 act as clamps which protect the TDC1048 from power-on conditions that might violate absolute maximum ratings and damage the TDC1048.

Video Input Amplifier

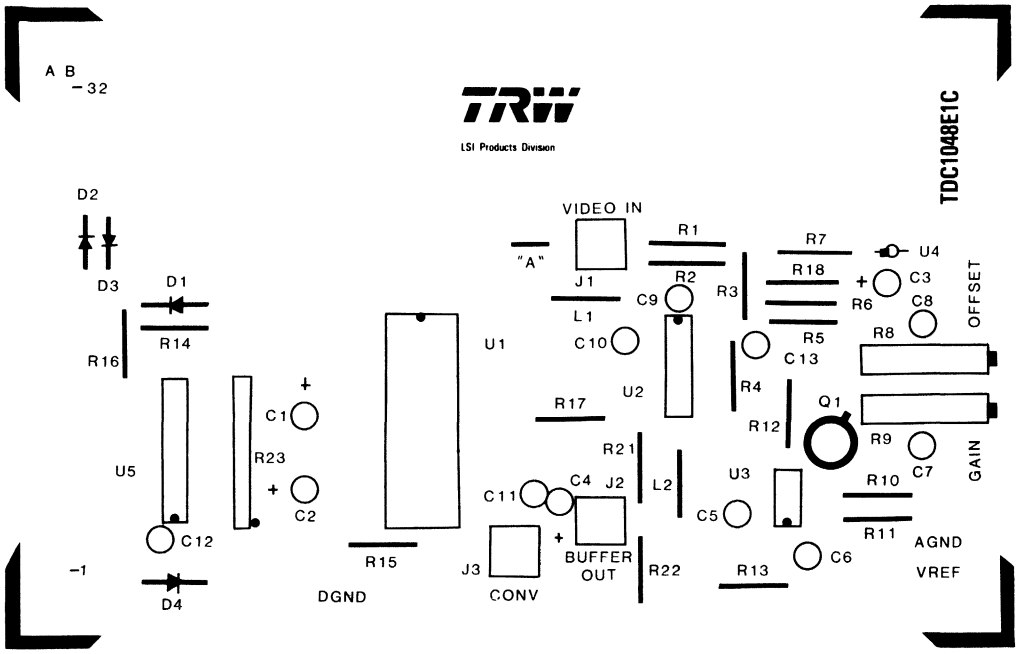
The input amplifier of the TDC1048E1C, U2, has been designed to accept a $\pm 0.5V$ input range and translate that signal to the 0V to $-2V$ range of the TDC1048. The output of this amplifier can be monitored at the J2 SMA connector which is connected to the V_{IN} terminals of the TDC1048 through a 470Ω resistor. The OFFSET potentiometer, R29, gives a $\pm 0.5V$ offset adjustment range to the board.

A/D Converter Inputs

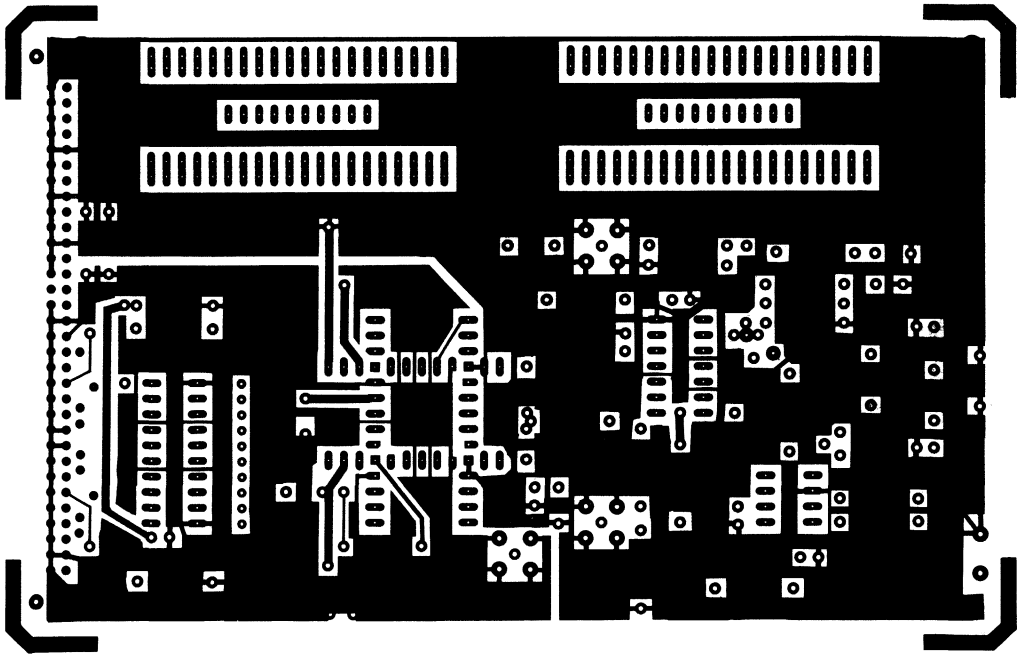
The clock to the TDC1048, CONV, is normally brought onto the board through the SMA connector labeled "CONV." It is also routed to the edge connector pin B15. The NMINV and NLINV inputs to the TDC1048 are pulled HIGH with resistors R14 and R15 and are routed to edge connector pins B13 and B6.

The analog signal input to the TDC1048E1C is brought onto the board by way of the SMA connector labeled "A_{IN}" near pin 28 of the TDC1048. A terminating resistor network, R1 and R2, is included on the board for terminating analog input signal cable. The eight data outputs of the TDC1048 are brought to edge connector pins after registering data in U5.

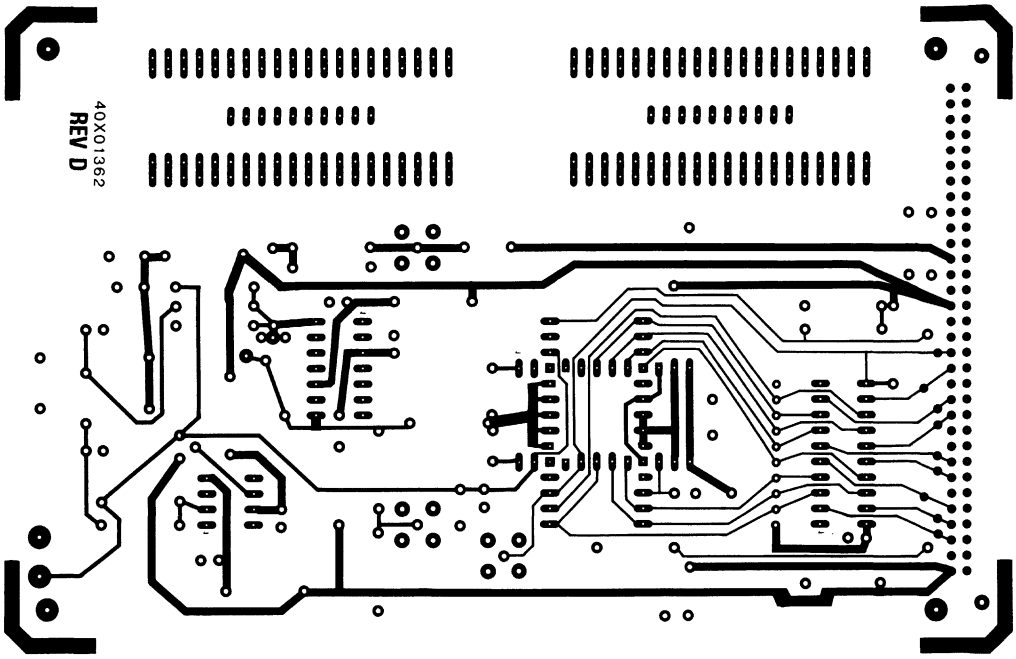
TDC1048E1C Silkscreen Layout



TDC1048E1C Component Side Layout



TDC1048E1C Circuit Side Layout



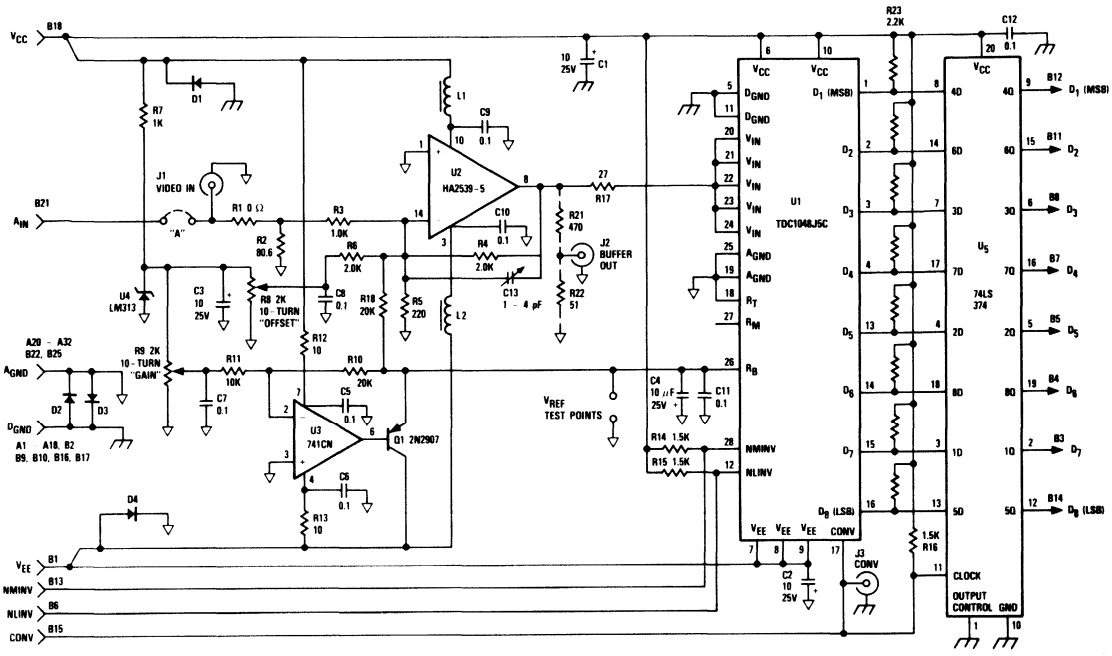
TDC1048E1C Eurocard Edge Connector Pinout

A_{GND}	A32	B32	NC
A_{GND}	A31	B31	NC
A_{GND}	A30	B30	NC
A_{GND}	A29	B29	NC
A_{GND}	A28	B28	NC
A_{GND}	A27	B27	NC
A_{GND}	A26	B26	NC
A_{GND}	A25	B25	A_{GND}
A_{GND}	A24	B24	NC
A_{GND}	A23	B23	NC
A_{GND}	A22	B22	A_{GND}
A_{GND}	A21	B21	A_{IN}
A_{GND}	A20	B20	NC
NC	A19	B19	NC
D_{GND}	A18	B18	V_{CC}
D_{GND}	A17	B17	D_{GND}
D_{GND}	A16	B16	D_{GND}
D_{GND}	A15	B15	CONV
D_{GND}	A14	B14	D8 LSB
D_{GND}	A13	B13	NMINV
D_{GND}	A12	B12	D_1 MSB
D_{GND}	A11	B11	D_2
D_{GND}	A10	B10	D_{GND}
D_{GND}	A9	B9	D_{GND}
D_{GND}	A8	B8	D_3
D_{GND}	A7	B7	D_4
D_{GND}	A6	B6	NLINV
D_{GND}	A5	B5	D_5
D_{GND}	A4	B4	D_6
D_{GND}	A3	B3	D_7
D_{GND}	A2	B2	D_{GND}
D_{GND}	A1	B1	V_{EE}

Mating Connectors for TDC1048E1C

AMP	532507-2	Wire-wrap
AMP	532507-1	Solder tail
Robinson-Nugent	RNE-64BS-W-TG30	Wire-wrap
Robinson-Nugent	RNE-64BS-S-TG30	Solder tail
Souriau	8609-264-6115-7550E1	Wire-wrap
Souriau	8609-264-6114-7550E1	Solder tail
Souriau	8609-264-6813-7550E1	Solder tail, right-angle bend

Figure 7. Schematic of Evaluation Board



Notes for Figure 7. Schematic of Evaluation Board

1. All capacitor values are in microfarads (μF).
2. All capacitor voltage ratings are 50WVDC unless otherwise noted.
3. All resistors are 1/8W unless otherwise noted.
4. All resistor values are in Ohms.
5. All diodes are 1N4001.

Miscellaneous Evaluation Board Parts

Eurocard Connector DIN 41612B 2-Row 64-Contact Board Mount Male	Winchester 64P-6033-0430
Eurocard Connector DIN 41612B 2-Row 64-Contact Wire-Wrap Female	Winchester 64S-6033-0422-1
J1-J3 SMA Coax Connector (J2, J3 not included)	Sealectro 50-651-0000-31 or Omni-Spectra 2062-0000-00
L1, L2 Ferrite Bead Inductors	Fair-Rite Products Corp. 2743001112

Input Resistor Selection Table (Values in Ohms)

Z_{IN}	Input Voltage Range									
	1V		2V		4V		5V		10V	
	R1	R2	R1	R2	R1	R2	R1	R2	R1	R2
50	0	52.3	24.9	24.3	37.4	12.7	40.2	10	45.3	4.99
75	0	80.6	37.4	39.2	56.2	19.1	60.4	15.4	68.1	7.5
93	0	102	46.4	48.7	69.8	23.7	75	19.1	84.5	9.31
1k	0	Open	499	1k	750	332	806	249	909	110

For input voltage ranges and input impedances not covered by the *Input Resistor Selection Table*, the following formulas may be used to calculate R1 and R2:

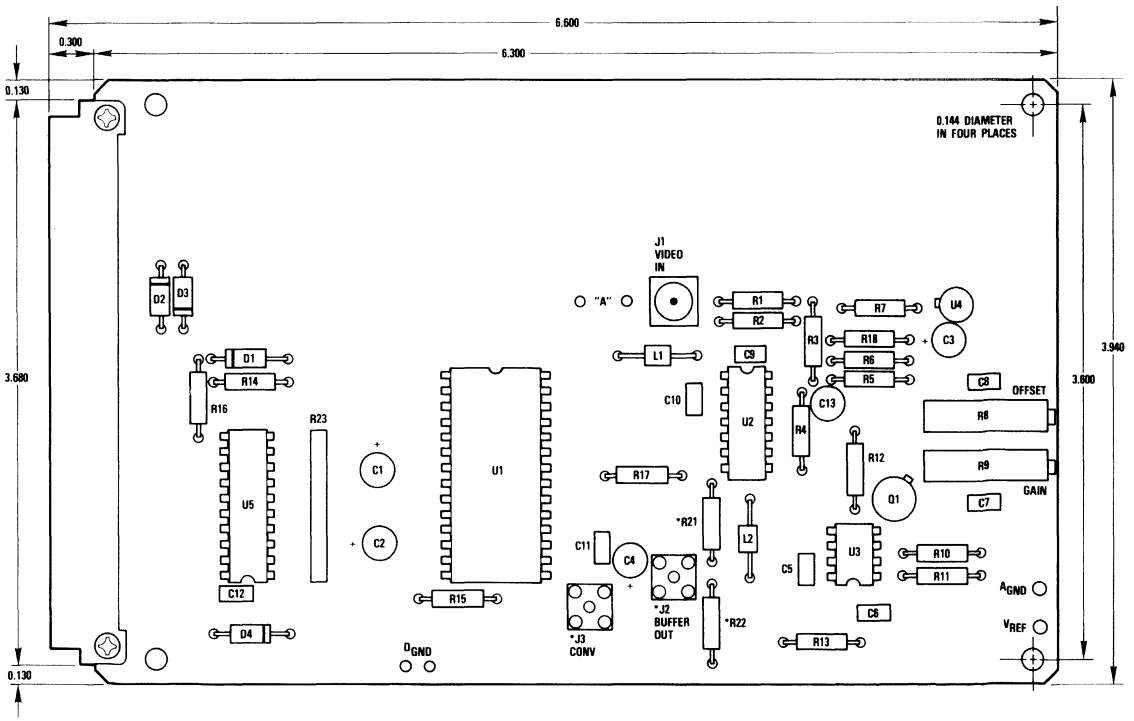
$$R2 = \frac{1}{\frac{VR}{Z_{IN}} + \frac{1}{1000}}$$

and

$$R1 = Z_{IN} - \frac{1000\ R2}{R2 + 1000}$$

where VR is the desired input voltage range of the board, Z_{IN} is the desired input impedance of the board, and the constant value 1000 is given by the value of R3.

Assembly for TDC1048E1C



Note:

1. * not supplied.
2. Dimensions in inches.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
5962-87600 01XC	EXT–T_C = –55°C to 125°C	Per Standard Military Drawing	28 Pin Ceramic DIP	5962-87600 01XC
TDC1048C3C	STD–T_A = 0°C to 70°C	Commercial	28 Contact LCC	1048C3C
TDC1048C3V	EXT–T_C = –55°C to 125°C	MIL-STD-883	28 Contact LCC	1048C3V
5962-87600 013A	EXT–T_C = –55°C to 125°C	Per Standard Military Drawing	28 Contact LCC	5962-87600 013A
TDC1048R3C	STD–T_A = 0°C to 70°C	Commercial	28 Leaded PLCC	1048R3C
TDC1048B6C	STD–T_A = 0°C to 70°C	Commercial	28 Pin CERDIP	1048B6C
TDC1048B6V	EXT–T_C = –55°C to 125°C	MIL-STD-883	28 Pin CERDIP	1048B6V
TDC1048N6C	STD–T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	1048N6C
TDC1048E1C	STD–T_A = 0°C to 70°C	– –	Eurocard Format Board with A/D Converter	TDC1048E1C

A

TDC1049

High-Speed A/D Converter
9-Bit, 30Msps

The TDC1049 is a flash (full-parallel) analog-to-digital converter capable of converting analog signals with full-power frequency components up to 15MHz into 9-bit words at rates up to 30Msps (Megasamples Per Second). A sample-and-hold circuit is not required. All digital inputs and outputs are differential ECL.

The TDC1049 consists of 512 latching comparators, encoding logic and an output register. A differential convert signal controls the conversion operation. The outputs can be connected to give either true or inverted binary or offset two's complement formats.

Features

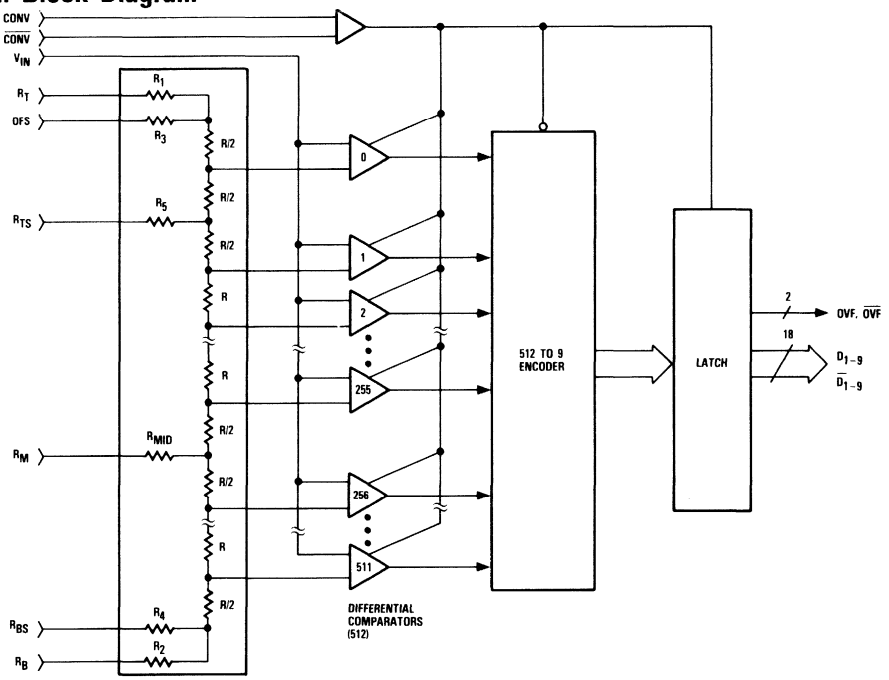
- 30Msps Conversion Rate, 15MHz Analog Bandwidth
- 9-Bit Resolution And Linearity
- Sample-And-Hold Circuit Not Required
- Differential Phase 0.5 Degrees
- Differential Gain 1.0%
- Overflow Flag
- Single −5.2V Power Supply
- Differential ECL Outputs
- Available In A 64 Pin DIP, 68 Contact LCC And 68 Pin Ceramic Pin Grid Array
- Available Per Standard Military Drawing

Applications

- Video Data Conversion
- Radar Data Conversion
- High-Speed Data Acquisition

A

Functional Block Diagram



TRW LSI Products Inc.
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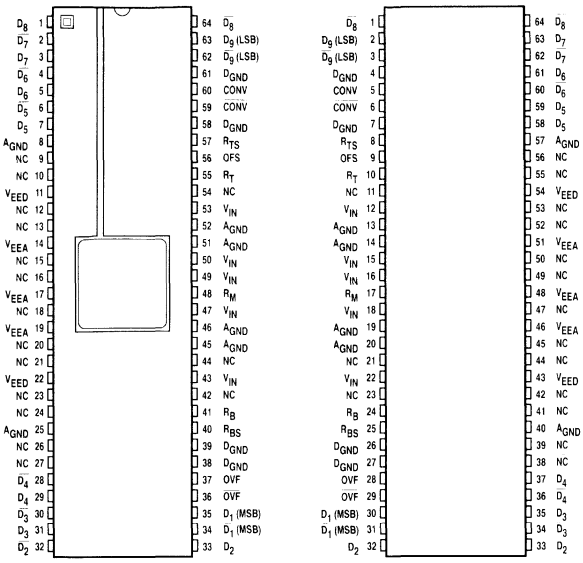
La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

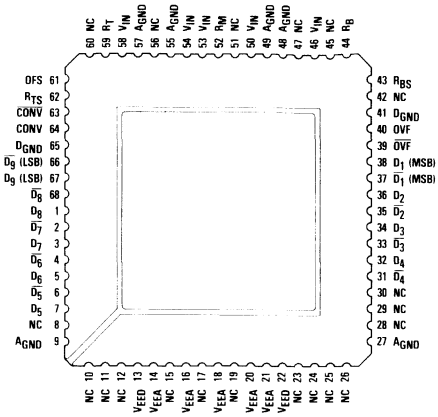
40G03657 Rev. D – 11/90
Printed in the U.S.A.

Pin Assignments



64 Pin DIP – J0 Package

64 Pin DIP – J3 Package

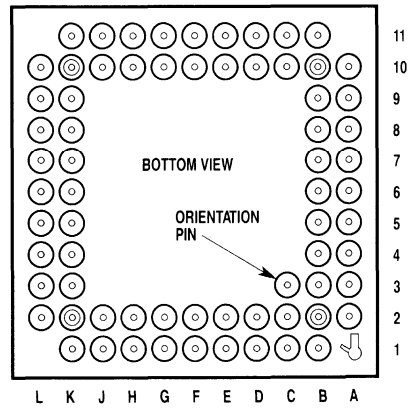


68 Contact LCC – C1 Package

Pin Assignments

68 Pin Ceramic Pin Grid Array, G8 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A2	NC	B9	V_{EEA}	F10	D_8	K4	A_{GND}
A3	V_{EED}	B10	NC	F11	$\overline{D_7}$	K5	V_{IN}
A4	NC	B11	A_{GND}	G1	D_1	K6	V_{IN}
A5	NC	C1	NC	G2	$\overline{D_1}$	K7	NC
A6	NC	C2	NC	G10	D_9	K8	A_{GND}
A7	NC	C10	D_5	G11	$\overline{D_8}$	K9	V_{IN}
A8	NC	C11	NC	H1	$\overline{OVF}$	K10	R_{TS}
A9	NC	D1	D_4	H2	OVF	K11	$\overline{CONV}$
A10	V_{EED}	D2	$\overline{D_4}$	H10	D_{GND}	L2	NC
B1	NC	D10	D_6	H11	D_9	L3	NC
B2	A_{GND}	D11	$\overline{D_5}$	J1	NC	L4	A_{GND}
B3	V_{EEA}	E1	D_3	J2	D_{GND}	L5	R_M
B4	V_{EEA}	E2	$\overline{D_3}$	J10	CONV	L6	NC
B5	V_{EEA}	E10	D_7	J11	D_{GND}	L7	V_{IN}
B6	V_{EEA}	E11	$\overline{D_6}$	K1	R_{BS}	L8	A_{GND}
B7	V_{EEA}	F1	D_2	K2	R_B	L9	R_T
B8	NC	F2	$\overline{D_2}$	K3	V_{IN}	L10	OVS



Functional Description

General Information

The TDC1049 has three functional sections: a comparator array, encoding logic and output register. The comparator array compares the input signal with 512 reference voltages to produce an N-of-512 code or "thermometer" code. The comparators referenced to voltages less than the input signal will be on and those referenced to voltages greater than the input signal will be off. The encoding logic converts the N-of-512 code into 9-bit binary data. The output register holds the output between updates.

Power

For optimum performance, separate analog and digital power, V_{EEA} and V_{EED} should be supplied to the TDC1049. Separate analog and digital power supplies or a common supply with separate analog and digital paths and high-frequency decoupling can be used. The return path for the current drawn from V_{EEA} and V_{EED} is A_{GND} and D_{GND}, respectively. The returns A_{GND} and D_{GND} should also be kept separate and connected together at the power supply terminals. It is recommended that provisions be made on the printed circuit board for shorting jumpers between analog and digital ground as close to the A/D converter as possible. The installation of the jumpers depends upon the printed circuit board layout and overall system performance once the system is in operation. The voltage difference between V_{EEA} and V_{EED} must be less than ± 0.1V. The same voltage difference limit applies to the difference between A_{GND} and D_{GND}. All power and ground inputs to the converter must be connected.

Reference

The TDC1049 converts analog signals in the range $V_{RB} < V_{IN} < V_{RT}$ into digital form. V_{RB} (the voltage applied to R_B) at the bottom of the reference resistor chain, and V_{RT} (the voltage applied to R_T) at the top of the reference resistor chain, should both be between $+0.1$V and -2.1V. Within that range, V_{RT} must be more positive than V_{RB}. The linearity specification is based upon a 2.0V difference between V_{RT} and V_{RB}. The nominal voltages are $V_{RT} = 0.0$V and $V_{RB} = -2.0$V. To avoid damage to the converter, the voltage across V_{RT} and V_{RB} must not exceed 2.2V. A decoupling capacitor is recommended between R_B and A_{GND}. Noise introduced at this point, as well as the other reference inputs (R_T, R_{TS}, R_M, R_{BS}, OFS), may result in encoding errors.

A midpoint tap, R_M, allows the converter to be adjusted for optimum integral linearity. It can also be used to achieve a nonlinear transfer function, but adjustment of R_M is not required to meet 9-bit linearity. If this node is driven by external circuitry, it should be driven from a low-impedance source; if not used, it must be left open.

Parasitic resistances, R1 and R2, introduce offset errors at the top and bottom of the reference resistor chain. Sense points, R_{TS}, R_{BS} and OFS, may be used to reduce the effect of these offset errors. Overflow Sense (OFS) may be used to reduce the effect of the offset at the overflow (most positive) comparator whenever the Overflow (OVF, $\overline{OVF}$) flags are used. Sense points are not required for 9-bit linearity and, if not used, they must be left open.

Convert

The TDC1049 requires a differential ECL clock (CONV and $\overline{CONV}$) signal. The conversion occurs (the comparators are latched) within t_{STO} (Sampling Time Offset) of the rising edge of CONV. The 512 to 9 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output register on the next rising edge of CONV. Data for sample N is available at the output t_D (Output Delay Time) after the rising edge of sample N + 1.

Analog Input

The TDC1049 uses latching comparators which are connected to the analog inputs V_{IN}. For optimal performance, the source impedance of the driver amplifier should be less than 25Ω. The input signal will not damage the TDC1049 if it remains within the range of V_{EEA} to $+0.5$V. If the input signal is between the V_{RT} and V_{RB}, the output will be a binary number between 0 and 511 inclusive. All five analog inputs must be connected.

Outputs

The outputs of the TDC1049 are differential ECL. The recommended pull-down resistance is 500Ω to -2V, or a 220/330Ω termination between D_{GND} and V_{EED}. The OVF signal indicates that the analog input has exceeded the threshold of the most positive comparator. Data is held valid at the output register for at least t_{HO} (Output Hold Time) after the rising edge of CONV. New data becomes valid t_D after the rising edge of CONV.

No Connects

There are several pins labeled NC (No Connect). These pins are not connected internally and may be either left open or connected to analog ground to aid heat transfer from the package and to reduce electrical noise.

Package Interconnections

Signal Name	Function	Value	J0 Package Pins	J3 Package Pins	C1 Package Pins	G8 Package Pins
V_{EEA}	Analog Supply Voltage	−5.2V	46, 48, 51	14, 17, 19	14, 16, 18, 20, 21	B9, B7, B6, B5, B4
V_{EED}	Digital Supply Voltage	−5.2V	43, 54	11, 22	13, 22	A3, A10
D_{GND}	Digital Ground	0.0V	4, 7, 26, 27	38, 39, 58, 61	41, 65	J2, J11, H10
A_{GND}	Analog Ground	0.0V	13, 14, 19, 20, 40, 57	8, 25, 45, 46, 51, 52	9, 27, 48, 49, 55, 57	B2, K4, L4, K8, L8, B11
R_T	Reference Resistor, Top	0.0V	10	55	59	L9
R_{TS}	Reference Resistor, Top Sense	0.0V	8	57	62	K10
R_B	Reference Resistor, Bottom	−2.0V	24	41	44	K2
R_{BS}	Reference Resistor, Bottom Sense	−2.0V	25	40	43	K1
R_M	Reference Resistor, Midpoint	−1.0V	17	48	52	L5
OFS	Overflow Sense	0.0V	9	56	61	L10
CONV	Convert	ECL	5	60	64	J10
$\overline{CONV}$	Convert, Complement	ECL	6	59	63	K11
V_{IN}	Analog Signal Input	0V to −2V	12, 15, 16, 18, 22	43, 47, 49, 50, 53	46, 50, 53, 54, 58	K3, K5, K6, L7, K9
D_1 MSB	Most Significant Bit	ECL	30	35	38	G1
$\overline{D_1}$ $\overline{MSB}$	Most Significant Bit Complement	ECL	31	34	37	G2
D_2		ECL	32	33	36	F1
$\overline{D_2}$		ECL	33	32	35	F2
D_3		ECL	34	31	34	E1
$\overline{D_3}$		ECL	35	30	33	E2
D_4		ECL	36	29	32	D1
$\overline{D_4}$		ECL	37	28	31	D2
D_5		ECL	58	7	7	C10
$\overline{D_5}$		ECL	59	6	6	D11
D_6		ECL	60	5	5	D10
$\overline{D_6}$		ECL	61	4	4	E11
D_7		ECL	62	3	3	E10
$\overline{D_7}$		ECL	63	2	2	F11
D_8		ECL	64	1	1	F10
$\overline{D_8}$		ECL	1	64	68	G11
D_9 LSB	Least Significant Bit	ECL	2	63	67	G10
$\overline{D_9}$ $\overline{LSB}$	Least Significant Bit Complement	ECL	3	62	66	H11
OVF	Overflow Output	ECL	28	37	40	H2
$\overline{OVF}$	Overflow Output Complement	ECL	29	36	39	H1
NC	No Connect	Open	11, 21, 23, 38, 39, 41, 42, 44, 45, 47, 49, 50, 52, 53, 55, 56	9, 10, 12, 13, 15, 16, 18, 20, 21, 23, 24, 26, 27, 42, 44, 54	8, 10, 11, 12, 15, 17, 19, 23, 24, 25, 26, 28, 29, 30, 42, 45, 47, 51, 56, 60	B1, C2, C1, J1, L2, L3, L6, K7, C11, B10, A9, B8, A8, A7, A6, A5, B4, A4, A2

Output Coding Table [1]

V_{IN}	OVF	D_1 MSB ... D_9 LSB
+0.0039V	1	000000000
0.0000V	0	000000000
−0.0039V	0	000000001
•	•	•
•	•	•
•	•	•
−0.9980V	0	011111111
−1.0020V	0	100000000
−1.0059V	0	100000001
•	•	•
•	•	•
•	•	•
−1.9961V	0	111111110
−2.0000V	0	111111111

Note: 1. Voltages are code midpoints.

Figure 1. Timing Diagram

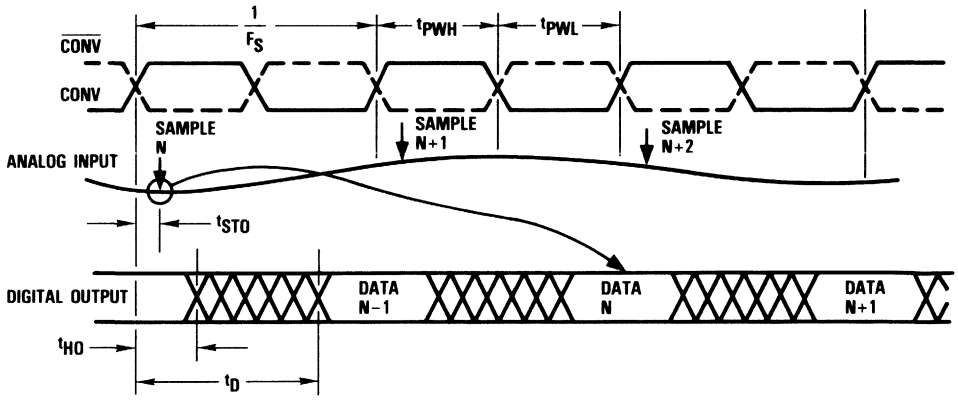
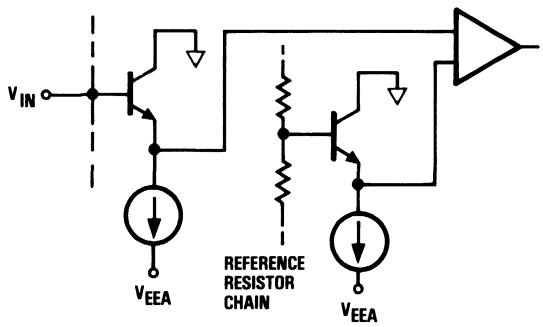
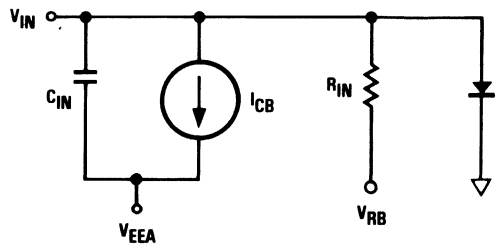


Figure 2. Simplified Analog Input Equivalent Circuits





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Digital Input Equivalent Circuit

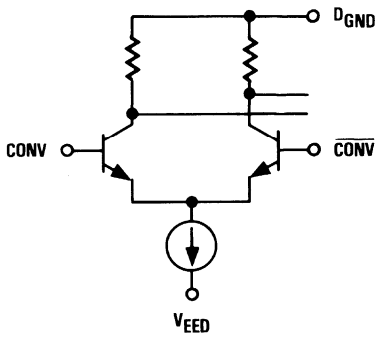


Figure 4. Output Circuits

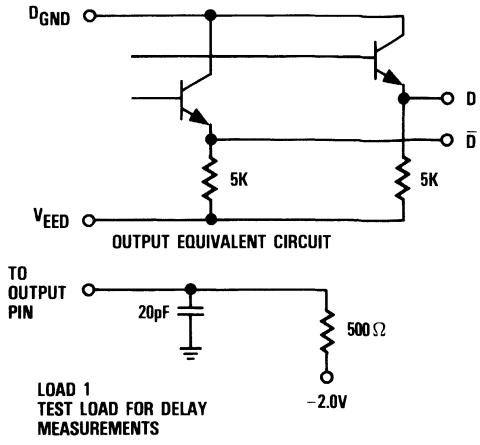
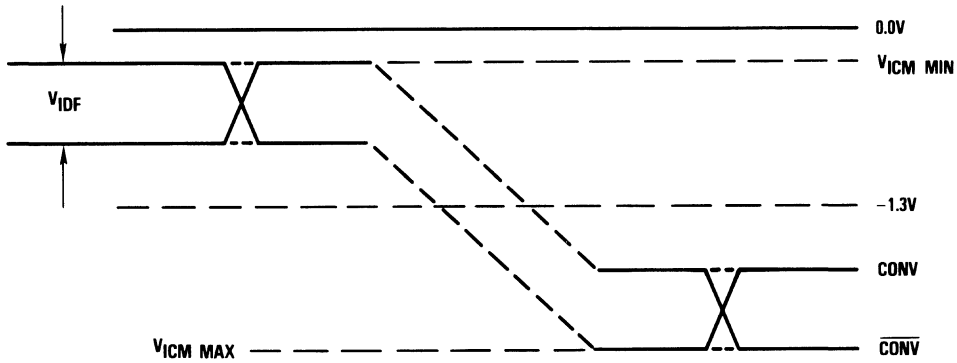


Figure 5. CONVert, CONVert Switching Levels



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{EED} (measured to D_{GND}) ..... +0.5 to −7.0V
V_{EEA} (measured to A_{GND}) ..... +0.5 to −7.0V
A_{GND} (measured to D_{GND}) ..... +1.0 to −1.0V
V_{EEA} (measured to V_{EED}) ..... +0.5 to −0.5V

Input Voltages [2]

CONV, $\overline{CONV}$ (measured to D_{GND}) ..... +0.5 to V_{EE}
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND}) ..... +0.5 to V_{EE}
V_{RT} (measured to V_{RB}) ..... +2.5 to −2.5V

Output

Short-circuit duration (single output in HIGH state to ground) ..... Infinite

Temperature

Operating, case ..... −60 to +140°C
junction ..... +175°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Extended Min	Extended Nom	Extended Max	Units
V_{EED}	Digital Supply Voltage (measured to D_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{EEA}	Analog Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	+0.1	−0.1	0.0	+0.1	V
$V_{EEA} - V_{EED}$	Supply Voltage Differential	−0.1	0.0	+0.1	−0.1	0.0	+0.1	V
t_{PWL}	CONV Pulse Width, LOW	12			12			ns
t_{PWH}	CONV Pulse Width, HIGH	15			15			ns
V_{ICM}	Input Voltage, Common Mode	−0.5		−2.5	−0.5		−2.5	V
V_{IDF}	Input Voltage, Differential	0.3		1.2	0.3		1.2	V
V_{IN}	Input Voltage Range	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
V_{RT}	Most Positive Reference Input [1]	−0.1	0.0	0.1	−0.1	0.0	+0.1	V
V_{RB}	Most Negative Reference Input [1]	−1.9	−2.0	−2.1	−1.9	−2.0	−2.1	V
$V_{RT} - V_{RB}$	Voltage Reference Differential	1.8	2.0	2.2	1.8	2.0	2.2	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note: 1. V_{RT} Must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{EE}	Supply Current	V_{EED}, V_{EEA} = Max					
		T_A = 0°C to 70°C		−950			mA
		T_A = 70°C		−750			mA
		T_C = −55°C to 125°C				−1090	mA
		T_C = 125°C				−750	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = Nom	10	36	10	36	mA
R_{REF}	Total Reference Resistance		56	200	56	200	Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}	16		16		kOhms
C_{IN}	Analog Input Capacitance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}		160		160	pF
I_{CB}	Input Constant Bias Current	V_{EEA} = Max, V_{IN} = 0V		500		750	μA
I_I	Input Current, CONV, $\overline{CONV}$	V_{EED} = Max, V_I = −0.7V		150		180	μA
V_{OL}	Output Voltage, Logic LOW [1]	V_{EED} = Nom		−1.6		−1.5	V
V_{OH}	Output Voltage, Logic HIGH [1]	V_{EED} = Nom	−0.95		−1.1		V
C_I	Digital Input Capacitance	T_A = 25°C, f = 1MHz		20		20	pF

Note: 1. Test Load = 500Ω to −2V on each output.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{EED}, V_{EEA} = Min	30		30		Msps
t_{STO}	Sampling Time Offset	V_{EED}, V_{EEA} = Min	−2	6	−2	6	ns
t_D	Output Delay [1]	V_{EED}, V_{EEA} = Min		27		27	ns
t_{HO}	Output Hold Time [1]	V_{EED}, V_{EEA} = Min	3		3		ns

Note: 1. Test Load = 500Ω to −2V on each output, C_{LOAD} = 20pF.

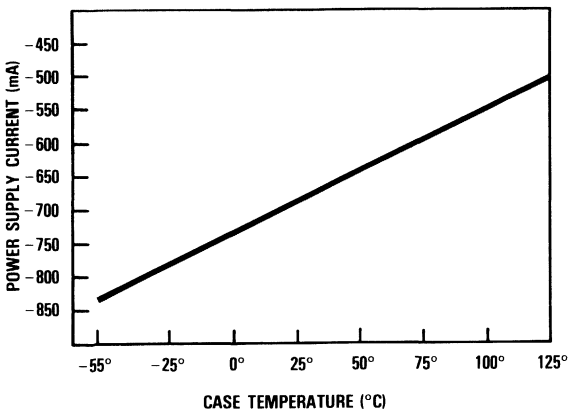
System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = Nom		0.15		0.20	%
		V_{RT}, V_{RB} = Nom, V_{RM} Adjusted		0.10		0.10	%
E_{LD}	Linearity Error Differential	V_{RT}, V_{RB} = Nom		0.1		0.1	%
Q	Code Size	V_{RT}, V_{RB} = Nom	15	185	15	185	% Nominal
E_{OTS}	Offset Error, Top	V_{IN} = V_{RT}, R_{TS} Connected		±4		±4	mV
E_{OT}	Offset Error, Top	V_{IN} = V_{RT}		30		30	mV
E_{OBS}	Offset Error, Bottom	V_{IN} = V_{RB}, R_{BS} Connected		±4		±4	mV
E_{OB}	Offset Error, Bottom	V_{IN} = V_{RB}		−30		−30	mV
T_{CO}	Offset Error, Temperature Coefficient			20		20	µV/°C
t_{TR}	Transient Response, Full-Scale			20		20	ns
BW	Bandwidth, Full Power Input	±0.9dB Frequency Response	15		15		MHz
SNR	Signal-to-Noise Ratio	30Msps Conversion Rate, 10MHz Bandwidth					
	Peak Signal/RMS Noise	1.25MHz Input	57		57		dB
		5.0MHz Input	53		53		dB
	RMS Signal/RMS Noise	1.25MHz Input	48		48		dB
		5.0MHz Input	44		44		dB
E_{AP}	Aperture Error			50		50	ps
DP	Differential Phase Error	F_S = 4 x NTSC		0.5		0.5	Degree
DG	Differential Gain Error	F_S = 4 x NTSC		1.5		1.5	%

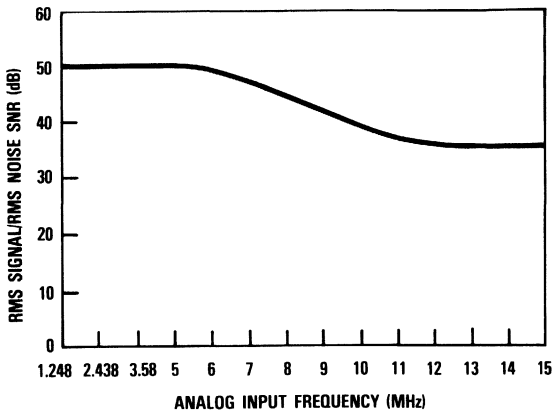
A

Typical Performance Curves

A. Power Supply Current vs. Temperature



B. SNR vs. Analog Input Frequency



Evaluation Board

The TDC1049E1C1 is a Eurocard-style printed circuit board designed to optimize the performance of, and to aid in the evaluation of, the TDC1049 A/D converter. The board dimensions are 100mm x 160mm with a standard 64 pin double-row DIN male connector installed. A complementary 64 pin double-row DIN female connector is included with the board. The circuitry on the board includes reference voltage generator, wideband video input amplifier, AC-coupled differential clock generators for the A/D converter and output register, and a TDC1112 12-bit D/A converter which may be used in evaluating certain parameters of the TDC1049.

The board employs only two conducting sides. Most of the circuit interconnections are on the bottom of the board while the top is mostly solid ground plane. SMA connectors are installed on the board to facilitate analog I/O and clocks. The board is calibrated and tested at the factory and is supplied complete with TDC1049 and TDC1112 installed.

The TDC1049E1C1 is based upon the TDC1049G8C integrated circuit packaged in a 68 pin ceramic pin grid array style package. It supersedes the TDC1049E1C which is based upon the TDC1049J0C 64 pin DIP package.

Power and Ground

Four power supply voltages are required for the operation of the TDC1049E1C: $V_{CC} = +5V$, $V_{EE} = -5.2V$, $V+ = +15V$ and $V- = -15V$. All power inputs are decoupled to a single solid ground plane, GND. All GND pins of the board are connected to the ground plane and it is recommended that all GND pins be used.

Voltage Reference Generator

The TDC1049E1C1 has two voltage reference generator circuits for driving the RT and RB terminal of the TDC1049. The RT generator, U5D-Q1, drive the RT terminal to 0.0V. A variable $-2V$ is supplied to RB from U5C and Q2. The GAIN potentiometer provides $\pm 10\%$ adjustment range on the RB voltage. Diodes D3 through D10 act as clamps which protect the TDC1049 from power-on conditions that might violate absolute maximum ratings and damage the TDC1049.

Video Input Amplifier

The input amplifier of the TDC1049E1C, U4, has been designed to accept a $\pm 0.5V$ input range and translate that signal to the 0V to $-2V$ range of the TDC1049. The output of this amplifier can be monitored at the AOUT SMA connector which is connected to the V_{IN} terminals of the TDC1049 through a 470Ω resistor. The OFFSET potentiometer, R27, gives a $\pm 0.5V$ offset adjustment range to the board.

A/D Converter Inputs

The clock to the TDC1049, CONV, is normally brought onto the board through the SMA connector labeled "CONV." By installing jumper J1, this signal is routed through the edge connector pin B2. A terminating resistor, R41 is installed on the board for terminating a 50Ω clock signal cable. The clock generator accept virtually any waveform and provides differential ECL signals to the TDC1049. The duty-cycle of the TDC1049 clock may be adjusted by installing the 2 kΩ "PW" potentiometer, R42.

The analog signal input to the TDC1049E1C1 is brought onto the board by way of the SMA connector labeled "A_{IN}." A terminating resistor, R17, is included on the board for terminating a 50Ω analog input signal cable.

A/D Converter Data Outputs and D/A Converter Data Inputs

The nine data outputs of the TDC1049 (after registers U2 and U3) are brought to edge connector pins B3 through B11. These pins are located directly across the edge connector from the corresponding data inputs of the TDC1112 D/A converter to simplify connection of A/D outputs to D/A inputs.

D/A Converter Inputs

The clock to the TDC1112, CLK, is normally brought onto the board through an SMA connector labeled "CLK" near pin 16 of the TDC1112. The clock input to the TDC1112 is also brought to the edge connector pin B24. Resistors, R7 and R8, provide a Thevenin equivalent 130Ω termination for the CONV signal. R5 and R6 bias the $\overline{\text{CONV}}$ input to the TDC1112 near the ECL threshold level.

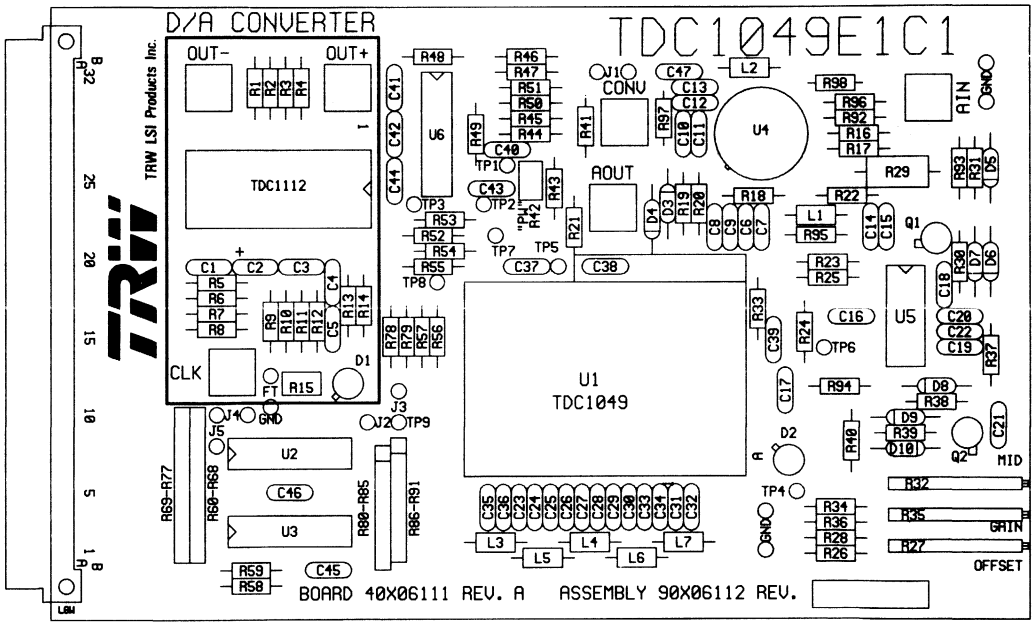
D/A converter outputs are brought to SMA connectors labeled OUT+ and OUT– as well as edge connector pins B27 and B26. Load resistors of 51.1Ω are provided on the board to facilitate 50Ω cable connection to the board.

Potentiometer R11 is used to adjust the reference voltage to the TDC1112. This voltage is adjusted to –1.0V as part of the factory test and calibration procedure.

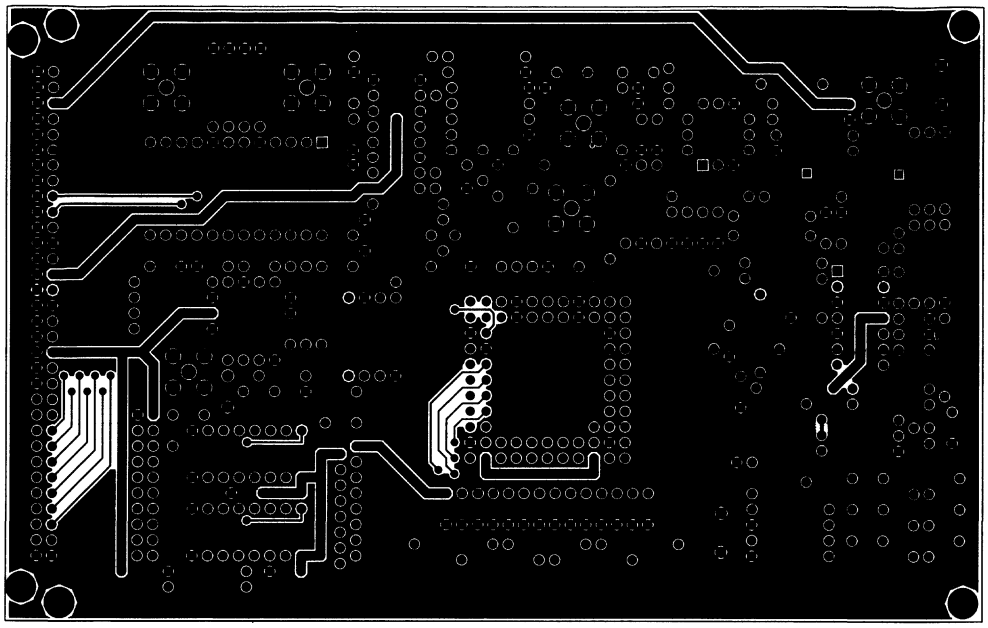
Placing a jumper in the location labeled "FT" will put the TDC1112 into feedthrough (unclocked) mode. This eliminates the requirement for a D/A clock signal, but will degrade the fidelity of the TDC1112 reconstruction.

A

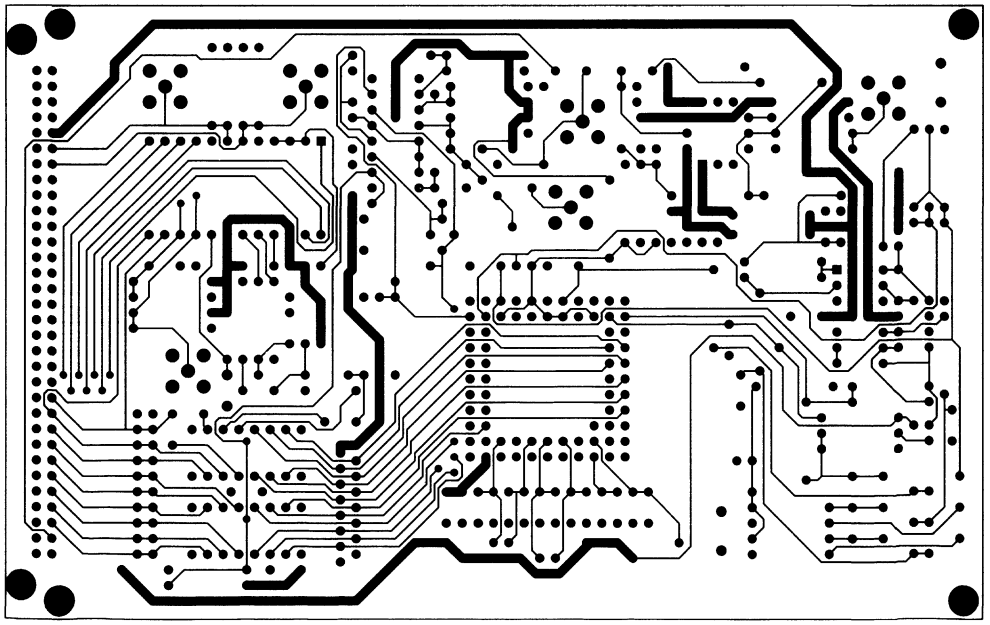
TDC1049E1C Silkscreen Layout



TDC1049E1C Component Side Layout



TDC1049E1C Circuit Side Layout



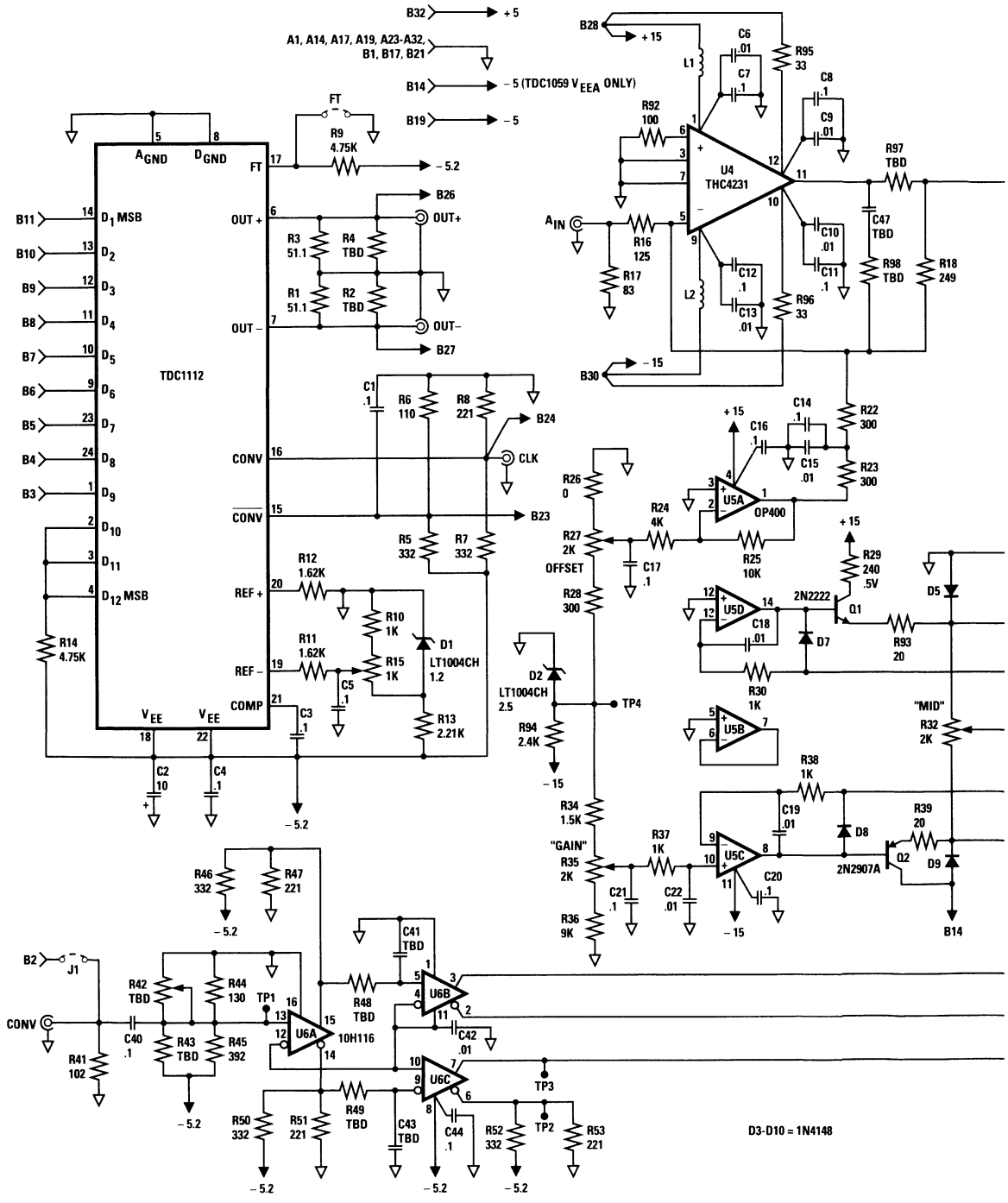
TDC1049E1C Eurocard Edge Connector Pinout

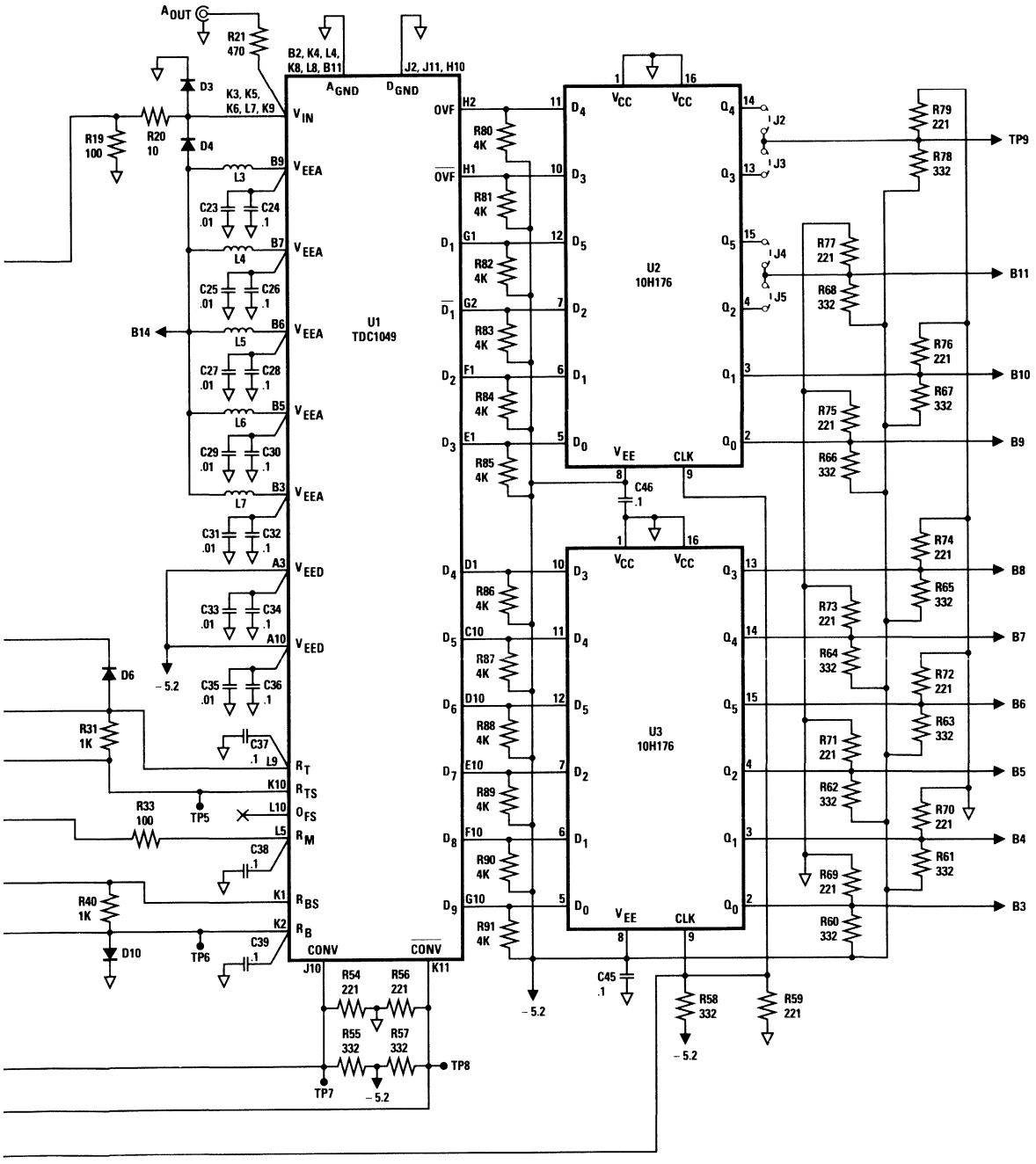
GND	A32	B32	V_{CC} (+5V)
GND	A31	B31	NC
GND	A30	B30	V− (−15V)
GND	A29	B29	NC
GND	A28	B28	V+ (+15V)
GND	A27	B27	D/A OUT−
GND	A26	B26	D/A OUT+
GND	A25	B25	NC
GND	A24	B24	D/A CONV
GND	A23	B23	D/A $\overline{\text{CONV}}$
GND	A22	B22	NC
GND	A21	B21	GND
GND	A20	B20	NC
GND	A19	B19	V_{EE} (−5.2V)
GND	A18	B18	NC
GND	A17	B17	GND
GND	A16	B16	NC
GND	A15	B15	NC
GND	A14	B14	V_{EE} (−5.2V)
GND	A13	B13	NC
GND	A12	B12	NC
D/A D_1 MSB	A11	B11	A/D D_1 MSB
NCD/A D_2	A10	B10	A/D D_2
D/A D_3	A9	B9	A/D D_3
D/A D_4	A8	B8	A/D D_4
D/A D_5	A7	B7	A/D D_5
D/A D_6	A6	B6	A/D D_6
D/A D_7	A5	B5	A/D D_7
D/A D_8	A4	B4	A/D D_8
D/A D_9 LSB	A3	B3	A/D D_9 LSB
A/D $\overline{\text{CONV}}$	A2	B2	A/D CONV
GND	A1	B1	GND

Mating Connectors for TDC1049E1C

AMP	532507-2	Wire-wrap
AMP	532507-1	Solder tail
Robinson-Nugent	RNE-64BS-W-TG30	Wire-wrap
Robinson-Nugent	RNE-64BS-S-TG30	Solder tail
Souriau	8609-264-6115-7550E1	Wire-wrap
Souriau	8609-264-6114-7550E1	Solder tail
Souriau	8609-264-6813-7550E1	Solder tail, right-angle bend

Figure 6. TDC1049E1C A/D Converter Schematic Diagram




A_OUT
R21 470
D3
D4
R19 100
R20 10
K3, K5, K6, L7, K9
B2, K4, L4, K8, L8, B11
J2, J11, H10
A_GND
D_GND
V_IN
V_EEA
V_EED
U1 TDC1049
B14
B9
B7
B6
B5
B3
A3
A10
L3
L4
L5
L6
L7
C23 .01
C24 .1
C25 .01
C26 .1
C27 .01
C28 .1
C29 .01
C30 .1
C31 .01
C32 .1
C33 .01
C34 .1
C35 .01
C36 .1
C37 .1
C38 .1
C39 .1
-5.2
D6
R31 1K
L9
L10
L5
K10
K1
K2
R33 100
TP5
R40 1K
D10
TP6
R_T
R_TS
O_FS
R_M
R_BS
R_B
CONV
CONV
J10
K11
OVF
OVF
H2
H1
G1
G2
F1
E1
D1
C10
D10
E10
F10
G10
R80 4K
R81 4K
R82 4K
R83 4K
R84 4K
R85 4K
R86 4K
R87 4K
R88 4K
R89 4K
R90 4K
R91 4K
U2 10H176
U3 10H176
V_CC
V_EE
CLK
C46 .1
C45 .1
R58 332
R59 221
R54 221
R56 221
R55 332
R57 332
TP7
TP8
J2
J3
J4
J5
R79 221
R78 332
R77 221
R68 332
R76 221
R67 332
R75 221
R66 332
R74 221
R65 332
R73 221
R64 332
R72 221
R63 332
R71 221
R62 332
R70 221
R61 332
R69 221
R60 332
TP9
B11
B10
B9
B8
B7
B6
B5
B4
B3

Standard Military Drawing

These devices are also available as products manufactured, tested, and screened in compliance with Standard Military Drawings (SMDs). The nearest vendor equivalent product is shown below; however, the applicable SMD is the sole controlling document defining the SMD product.

Standard Military Drawing	Nearest Equivalent TRW Product No.	Package
5962-88532-01XC	TDC1049J0V	64 Pin Ceramic DIP
5962-88532-01YC	TDC1049J3V	64 Pin Ceramic DIP
5962-88532-01ZA	TDC1049C1V	68 Contact Chip Carrier

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1049J0C	STD – T_A = 0°C to 70°C	Commercial	64 Pin Ceramic DIP	1049J0C
TDC1049J0V	EXT – T_C = –55°C to 125°C	MIL-STD-883	64 Pin Ceramic DIP	1049J0V
5962-88532 01XC	EXT – T_C = –55°C to 125°C	Per Standard Military Drawing	64 Pin Ceramic DIP	5962-88532 01XC
TDC1049C1C	STD – T_A = 0°C to 70°C	Commercial	68 Contact Ceramic LCC	1049C1C
TDC1049C1V	EXT – T_C = –55°C to 125°C	MIL-STD-883	68 Contact Ceramic LCC	1049C1V
5962-88532 01ZA	EXT – T_C = –55°C to 125°C	Per Standard Military Drawing	68 Contact Ceramic LCC	5962-88532 01ZA
TDC1049G8C	STD – T_A = 0°C to 70°C	Commercial	68 Pin Ceramic PGA	1049G8C
TDC1049G8V	EXT – T_C = –55°C to 125°C	MIL-STD-883	68 Pin Ceramic PGA	1049G8V
TDC1049E1C	STD – T_A = 0°C to 70°C	– –	Eurocard PC Board	TDC1049E1C

TDC1058

Monolithic Video A/D Converter

8-Bit, 20Msps, Low Power

The TRW TDC1058 is a flash analog-to-digital converter capable of converting a video-speed signal into a stream of 8-bit digital words at 20Msps (MegaSamples Per Second). Since the TDC1058 is a flash converter, a sample-and-hold circuit is not required.

The TDC1058 consists of 255 clocked latching comparators, combining logic, and an output register. A single convert clock controls the conversion operation. The unit can be configured to give either true or inverted outputs in binary or offset two's complement coding. All digital I/O is TTL compatible.

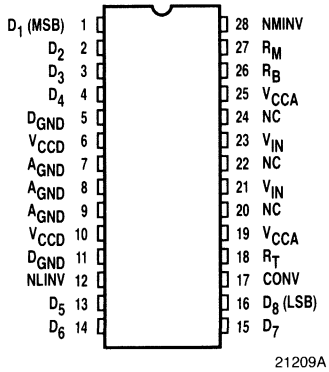
Features

- 8-Bit Resolution
- DC To 20Msps Conversion Rate
- 7MHz Full-Power Bandwidth
- 60MHz Small Signal −3dB Bandwidth
- 1/2 LSB Linearity
- 600mW Power Dissipation
- +5V Single Supply Operation
- Lowest Cost
- Pin Compatible With CXA1096P, ADC-304
- Sample-And-Hold Circuit Not Required
- Analog Input Range +3V To +5V
- Differential Phase 0.5°
- Differential Gain 1%
- Selectable Data Format
- Available In Plastic DIP, CERDIP And PLCC

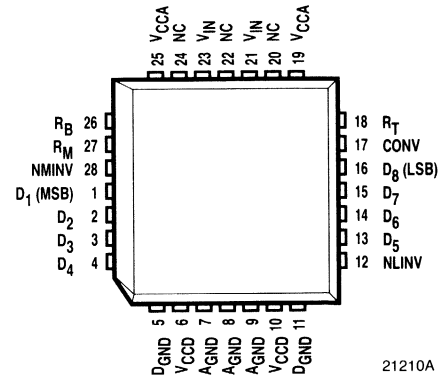
Applications

- Digital Television
- PC-Based Data Acquisition
- Video Digitizing
- Medical Imaging
- High Energy Physics
- Low Cost, Low Power, High-Speed Data Conversion

Pin Assignments



28 Pin CERDIP – B6 Package
28 Pin Plastic DIP – N6 Package



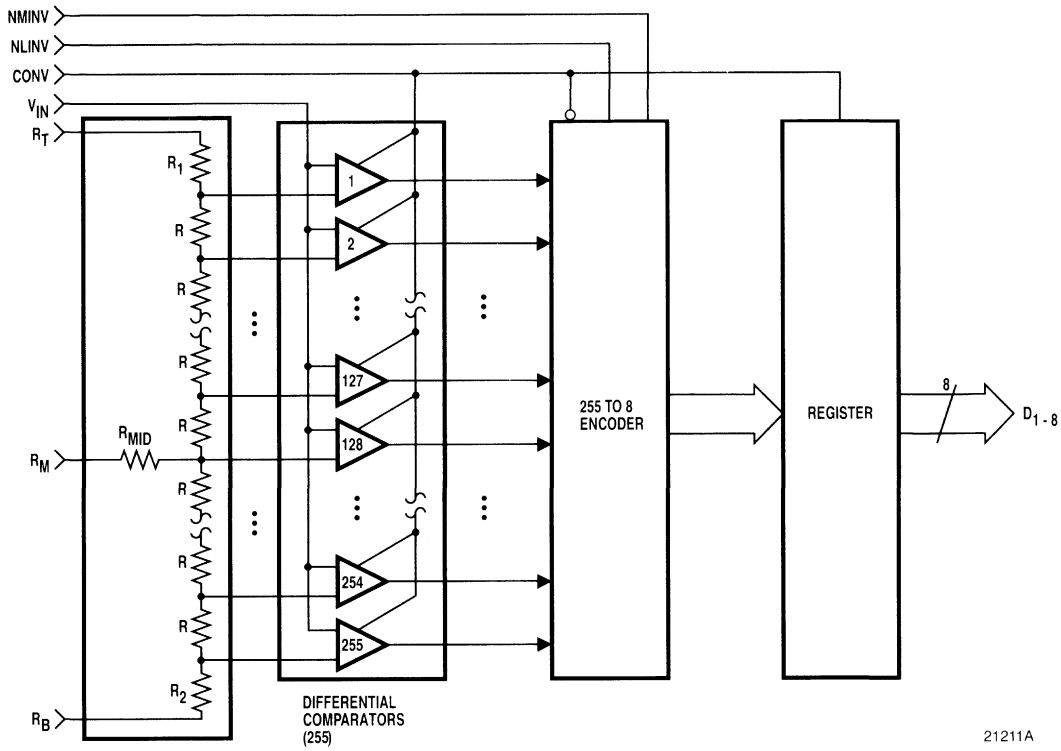
28 Leaded Plastic Chip Carrier – R3 Package

TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

40G05738 Rev. D – 11/90
Printed in the U.S.A.

Functional Block Diagram



Functional Description

General Information

The TDC1058 has three functional sections: a comparator array, encoding logic, and output registers. The comparator array compares the input signal with 255 reference voltages to produce an N-of-255 code (or thermometer code, since all the comparators whose reference is more negative than the input signal will be on, and all those whose reference is more positive will be off). The encoding logic converts the N-of-255 code into the user's choice of coding. The output register holds the output constant between updates.

Power

The TDC1058 operates from a single supply voltage: +5.0V. All power and ground pins must be connected.

Reference

The TDC1058 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. Nominally, V_{RB} is set to 3V and V_{RT} is set to 5V. However, the specifications of the TDC1058 are guaranteed as long as the following three reference operating conditions are met: 1.) the voltage applied across the reference resistor

Reference (cont.)

chain (V_{RT}-V_{RB}) is within the range of 1.8 to 2.2V, 2.) $V_{RT} \leq (V_{CCA}+0.1V)$ and 3.) $V_{RB} \geq 2.65V$. Therefore, if the supply voltage is expected to drop below 4.9V, the reference voltages should be lowered accordingly. For instance, if the system design allows the supply voltage to drop to the minimum recommended value of 4.75V, V_{RT} should be set to 4.65V and V_{RB} should be set to 2.65V. These reference voltages will allow the TDC1058 to give fully guaranteed performance over the full supply voltage range. See the ***Operating Conditions Table*** for further information.

Linearity is guaranteed with no adjustment; however, a midpoint tap, R_M, allows for the optional trimming of converter integral linearity as well as the creation of a nonlinear transfer function. This is explained in the ***Application Note TP-19 "Non-Linear A/D Conversion."*** The circuit shown in ***Figure 7*** will provide approximately a 1/2 LSB adjustment of the linearity at midscale. The characteristic impedance seen at this node is approximately 220 Ohms and should be driven from a low-impedance source. Note that any load applied to this node will affect linearity and any noise introduced at this point will degrade the overall SNR. Due to the slight variation in the reference current with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor (0.01 to 0.1μF) to ground is recommended. If the reference inputs are exercised dynamically (as in an automatic gain control circuit) a low-impedance reference source is required. The reference voltages may be varied dynamically at up to 5MHz; however, device performance is specified with fixed reference voltages as defined in the ***Operating Conditions Table***.

Analog Input

For precise quantization, the TDC1058 uses latching comparators. The source impedance of the driving circuit must be less than 25 Ohms, for optimum overall system performance. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number from 0 to 255. When a signal outside the recommended input voltage range (V_{RB} to V_{RT}) is applied, the output will remain at either full-scale value. The input signal will not damage the TDC1058 if it remains within the range specified in the ***Absolute Maximum Ratings Table***. Both analog input pins are connected together internally and therefore either one or both may be used.

Convert

The TDC1058 requires an external convert (CONV) signal. Because the TDC1058 is a flash converter it does not require a track-and-hold circuit. A sample is taken (the outputs of the comparators are latched) within t_{STO} (Sampling Time Offset) after a rising edge on the CONV pin. The result is encoded on the falling edge, and then transferred to the output registers on the next rising edge. The output becomes valid t_D (Output Delay Time) after the rising edge of CONVert and remains valid for at least t_{HO} (Output Hold Time) after the rising edge of CONVert. Therefore, the value of sample N becomes valid t_D after the rising edge of clock N+1 and remains valid until t_{HO} after the rising edge of clock N+2. (See ***Figure 1, Timing Diagram***.)

Output Format Control

Two output format control pins, NMINV and NLINV, are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. These pins are active LOW, as signified by the N prefix in the signal name. They may be tied to V_{CC} (through a 4.7 kOhm resistor) for a logic HIGH or D_{GND} for a logic LOW.

Outputs

The outputs of the TDC1058 are TTL compatible and capable of driving four low-power Schottky TTL (54/74 LS) loads or the equivalent. The outputs hold the previous data for a minimum of t_{HO} after the rising edge of the CONVert signal.

Not Connected

There are several pins that have no internal connection to the chip. They should be left open.

Package Interconnections

Signal Type	Signal Name	Function	Value	B6, N6, R3 Package Pins
Power	V_{CCD}	Digital Supply Voltage	+5.0V	6, 10
	V_{CCA}	Analog Supply Voltage	+5.0V	19, 25
	A_{GND}	Analog Ground	0.0V	7, 8, 9
	D_{GND}	Digital Ground	0.0V	5, 11
Reference	R_T	Reference Resistor (Top)	5.0V	18
	R_M	Reference Resistor (Middle)	4.0V	27
	R_B	Reference Resistor (Bottom)	3.0V	26
Analog Input	V_{IN}	Analog Signal Input	See Text	21, 23
Convert	CONV	Convert	TTL	17
Format Control	NMINV	Not Most Significant Bit Invert	TTL	28
	NLINV	Not Least Significant Bit Invert	TTL	12
Data Output	D_1	Most Significant Bit Output	TTL	1
	D_2		TTL	2
	D_3		TTL	3
	D_4		TTL	4
	D_5		TTL	13
	D_6		TTL	14
	D_7		TTL	15
	D_8	Least Significant Bit Output	TTL	16
Not Connected	NC	Not Connected	Open	20, 22, 24

Figure 1. Timing Diagram

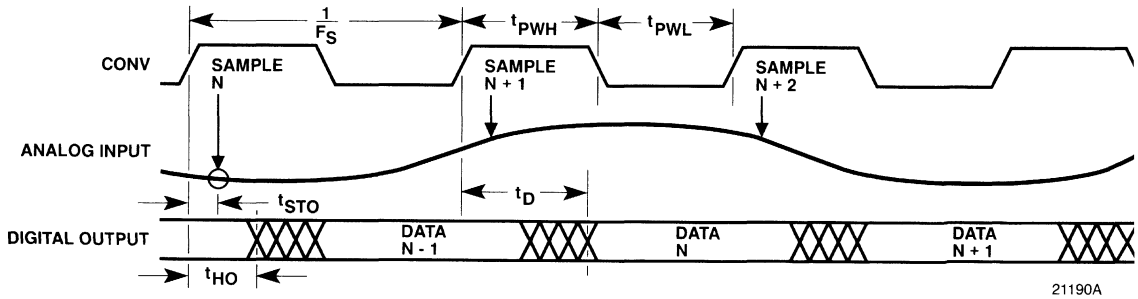
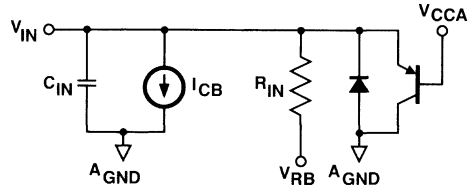


Figure 2. Simplified Analog Input Equivalent Circuit



C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

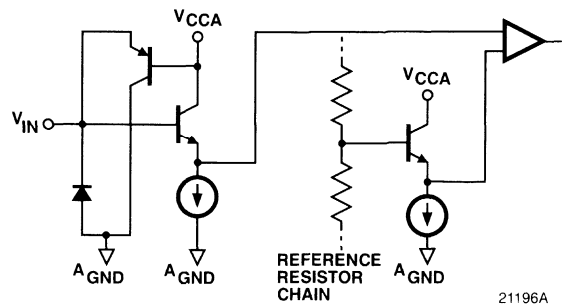


Figure 3. Convert Input Equivalent Circuit

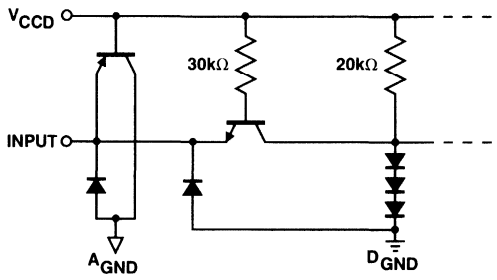
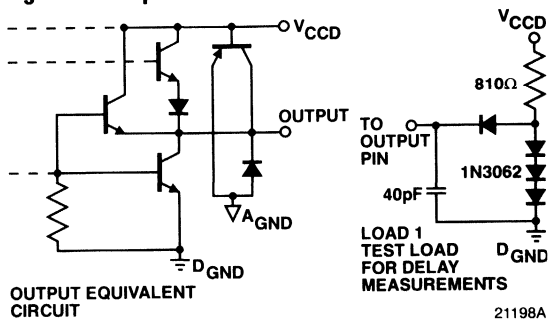


Figure 4. Output Circuit



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Output Coding Table

Input Voltage	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
	NMINV = HIGH NLINV = HIGH	NMINV = LOW NLINV = LOW	NMINV = LOW NLINV = HIGH	NMINV = HIGH NLINV = LOW
5.0000V	0000 0000	1111 1111	1000 0000	0111 1111
4.9922V	0000 0001	11111110	1000 0001	0111 1110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
4.0078V	0111 1111	1000 0000	1111 1111	0000 0000
4.0000V	1000 0000	0111 1111	0000 0000	1111 1111
3.9922V	1000 0001	0111 1110	0000 0001	1111 1110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3.0156V	1111 1110	0000 0001	0111 1110	1000 0001
3.0078V	1111 1111	0000 0000	0111 1111	1000 0000

Notes:
1. NMINV and NLINV are to be considered DC controls. They may be tied to +5V through a 4.7 kOhm resistor for a logic HIGH or tied to ground for a logic LOW.
2. Voltages are code midpoints.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CCD} (measured to D_{GND})	−0.5 to +7.0V
V_{CCA} (measured to A_{GND})	−0.5 to +7.0V
V_{CCA} (measured to V_{CCD})	−0.5 to +0.5V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input Voltages [2]

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT} V_{RB} (measured to A_{GND})	−0.5 to +5.5V
V_{RT} (measured to V_{RB})	−2.2 to +2.2V

Input Currents [3]

CONV, NMINV, NLINV	−50 to +50mA
V_{IN}, V_{RT}, V_{RB}	−100 to +100mA

Output

Applied voltage [2] (measured to D_{GND})	−0.5 to (V_{CC} + 0.5V)
Applied current [3], externally forced	−50 to +50mA
Short-circuit duration (single output in HIGH state to ground)	1 Second

Temperature

Operating, ambient (all packages except N6 and R3)	−55 to +125°C
(N6 and R3 packages only)	−20 to +90°C
junction	+175°C
Lead, soldering, all packages (10 seconds)	+300°C
Storage, all packages	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. A condition applied individually that exceeds the Operating Conditions specification but is less than the Absolute Maximum Ratings will not cause immediate device failure. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{CCA}	Analog Supply Voltage	4.75	5.0	5.25	V
V_{CCD}	Digital Supply Voltage	4.75	5.0	5.25	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	−0.1	0	+0.1	V
t_{PWL}	CONV Pulse Width, LOW	19			ns
t_{PWH}	CONV Pulse Width, HIGH	27			ns
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
I_{OL}	Output Current, Logic LOW			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400	μA
V_{RT}	Most Positive Reference Input [1]		5.0	V_{CCA} + 0.1	V
V_{RB}	Most Negative Reference Input [1]	2.65	3.0		V
$V_{RT}-V_{RB}$	Voltage Reference Differential	1.8	2.0	2.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70	°C

Note: 1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Thermal characteristics (approximate)

Parameter		Package	Typical	Units
Θ_{ja}	Thermal Resistance, Junction to Ambient	N6	45	°C/W
		R3	65	°C/W
		B6	50	°C/W
Θ_{jc}	Thermal Resistance, Junction to Case	N6	17	°C/W
		R3	14	°C/W
		B6	TBD	°C/W

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Temperature Range: Standard Max	Units
$I_{CCA}+I_{CCD}$	Total Supply Current	V_{CC} = Max [1]		160	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = Nom		30	mA
R_{REF}	Total Reference Resistance		67		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}	80		kOhms
C_{IN}	Input Capacitance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}		50	pF
I_{CB}	Input Constant Bias Current	V_{CCA} = Max		250	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.4V		−0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V	−200	50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = Max, V_I = V_{CC} = Max		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		V
I_{OS}	Short-Circuit Output Current	V_{CC} = Max, Output HIGH, one pin to ground, one second duration max.		−40	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15	pF

Note: 1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

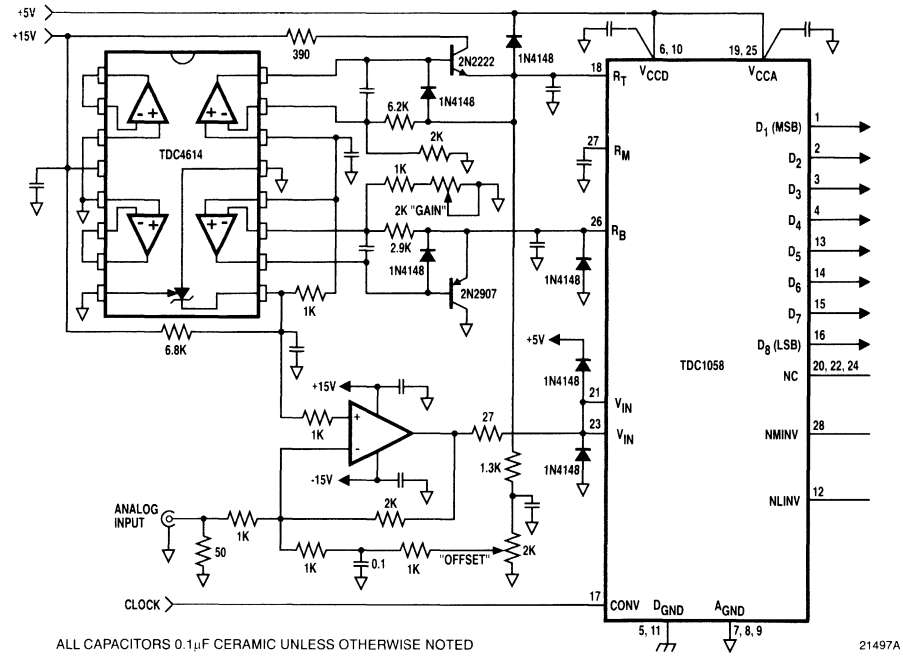
Parameter		Test Conditions	Temperature Range: Standard Min	Temperature Range: Standard Max	Units
F_S	Maximum Conversion Rate	V_{CC} = Min	20		Msps
t_{STO}	Sampling Time Offset	V_{CC} = Min	−2	10	ns
t_D	Output Delay	V_{CC} = Min, Load 1, Figure 4		35	ns
t_{HO}	Output Hold Time	V_{CC} = Max, Load 1, Figure 4	5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = Nom		0.2	%
E_{LD}	Linearity Error Differential			0.2	%
CS	Code Size		25	175	% Nom
E_{OT}	Offset Error, Top	$V_{IN} = V_{RT}$	−10	+10	mV
E_{OB}	Offset Error, Bottom	$V_{IN} = V_{RB}$		−15	mV
T_{CO}	Offset Error, Temperature Coefficient		−20	±20	μV/°C
BW	Bandwidth, Full Scale Input	No Spurious or Missing Codes	7		MHz
BW_{SS}	−3dB Bandwidth, Small Signal	−20dBFS Input	60		MHz
t_{TR}	Transient Response, Full Scale		70		ns
SNR	Signal-to-Noise Ratio	10MHz Bandwidth, 20Msps Conversion Rate			
	Peak Signal/RMS Noise	1.248MHz Input	54		dB
		2.438MHz Input	53		dB
	RMS Signal/RMS Noise	1.248MHz Input	45		dB
		2.438MHz Input	44		dB
E_{AP}	Aperture Error			60	ps
DP	Differential Phase Error	F_S = 4 × NTSC		1.0	Degree
DG	Differential Gain Error	F_S = 4 × NTSC		2.0	%

A

Figure 5. Typical Interface Circuit



ALL CAPACITORS 0.1μF CERAMIC UNLESS OTHERWISE NOTED

21497A

Figure 6. Inexpensive Interface Circuit

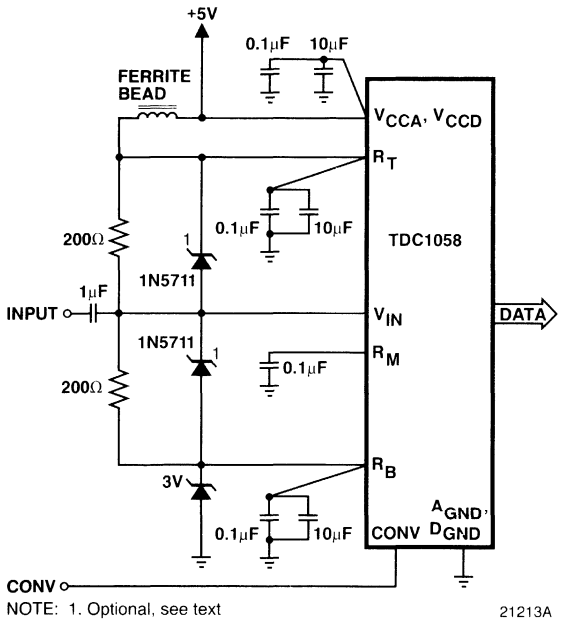
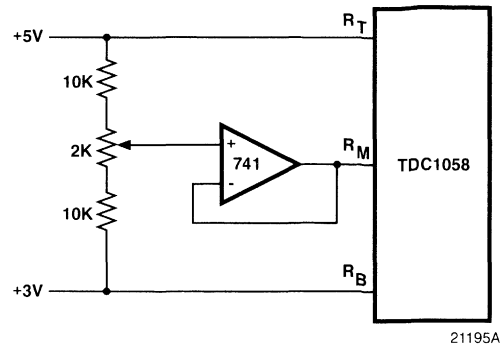


Figure 7. Optional Midscale Linearity Adjust



Typical Interface Circuit

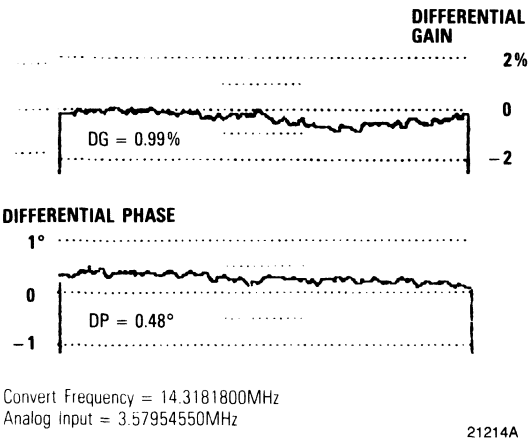
The *Typical Interface Circuit (Figure 5)* shows an example of a high-performance application circuit for the TDC1058. The wideband analog input amplifier drives the A/D converter directly. Bipolar inputs to the amplifier can be accommodated by adjusting the offset control. TRW's TDC4614 provides a stable reference for both the offset and gain control. All V_{IN} pins are con-nected close to the device package and the input ampli-fier's feedback loop should be closed at that point. The buffer has an inverting gain of two, increasing a 1Vp-p video input signal to the recommended 2Vp-p input for the TDC1058. Proper decoupling is recommended for all systems.

The bottom reference voltage (V_{RB}) is supplied by an inverting amplifier or the TDC4614, buffered with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain.

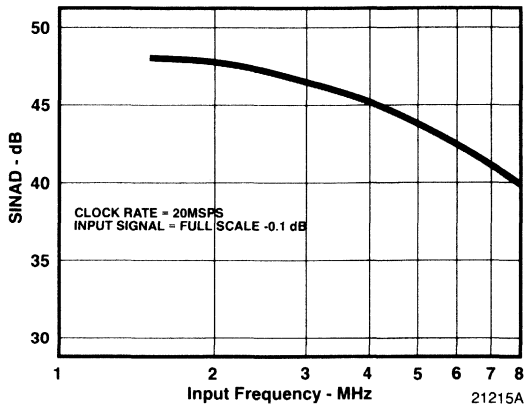
The *Inexpensive Interface Circuit* shown in *Figure 6* offers considerable parts reduction for cost-sensitive applications where DC response is not required and loss of some power supply rejection is tolerable. The 200 Ohm resistors bias the input to +4V and provide the current to the zener diode to provide the reference bottom voltage. The 1μF capacitor decouples the input signal from the DC voltage present at the input of the TDC1058. The 10μF and 0.1μF capacitors, as well as the ferrite bead, provide power supply decoupling. The 1N5711 Schottky diodes are for protection against overvoltages at the input and are not required if these precautions are taken elsewhere in the circuit.

Typical Performance Curves

A. Typical Differential Phase and Gain



B. Typical SINAD (SNR + Distortion) vs. Input Frequency



A

Evaluation Board

The TDC1058E1C is a Eurocard-style printed circuit board designed to optimize the performance of, and to aid in the evaluation of the TDC1058 A/D converter. The board dimensions are 100mm x 160mm with a standard 64 pin double-row DIN male connector installed. A complementary 64 pin double-row DIN female connector is included with the board. The circuitry on the board includes reference voltage generators, wideband video input amplifier, and a TDC1012 12-bit D/A converter which may be used in evaluating certain parameters of the TDC1058.

The board employs only two conducting sides. Most of the circuit interconnections are on the bottom of the board while the top is mostly solid ground plane. SMA connectors are installed on the board to facilitate analog I/O and clocks. The board is calibrated and tested at the factory and is supplied complete with TDC1058 and TDC1012 installed.

Power and Ground

Four power supply voltages are required for the operation of the TDC1058E1C: $V_{CC} = +5V$, $V_{EE} = -5.2V$, $V+ = +15V$ and $V- = -15V$. All power inputs are decoupled to a single solid ground plane, GND. All GND pins of the board are connected to the ground plane and it is recommended that all GND pins be used.

Voltage Reference Generator

The TDC1058E1C has two voltage reference generator circuits for driving the RT and RB terminals of the TDC1058. A fixed +5.0V is applied to RT from U2 and Q1. A variable +3V is supplied to RB from U3 and Q2. The GAIN potentiometer provides ±10% adjustment range on the RB voltage. Diodes D3 through D8 act as clamps which protect the TDC1058 from power-on conditions that might violate absolute maximum ratings and damage the TDC1058.

Video Input Amplifier

The input amplifier of the TDC1058E1C, U4, has been designed to accept a ±0.5V input range and translate that signal to the +3V to +5V range of the TDC1058. The output of this amplifier can be monitored at the AOUT SMA connector which is connected to the V_{IN} terminals of the TDC1058 through a 470Ω resistor. The OFFSET potentiometer, R29, gives a ±0.5V offset adjustment range to the board.

A/D Converter Inputs

The clock to the TDC1058, CONV, is normally brought onto the board through the SMA connector labeled "CONV." By installing jumper J1, this signal is routed through the edge connector pin B2. A terminating resistor location, R32 is available on the board for terminating clock signal cable. The NMINV and NLINV inputs to the TDC1058 are pulled HIGH with resistors and may be pulled LOW by installing jumpers J2 and J3.

The analog signal input to the TDC1058E1C is brought onto the board by way of the SMA connector labeled "A_{IN}" near pin 28 of the TDC1058. A terminating resistor, R25, is included on the board for terminating a 50Ω analog input signal cable.

A/D Converter Data Outputs and D/A Converter Data Inputs

The eight data outputs of the TDC1058 are brought to edge connector pins B13 through B21 (excluding B18). These pins are located directly across the edge connector from the corresponding data inputs of the TDC1012 D/A converter to simplify connection of A/D outputs to D/A inputs.

D/A Converter Inputs

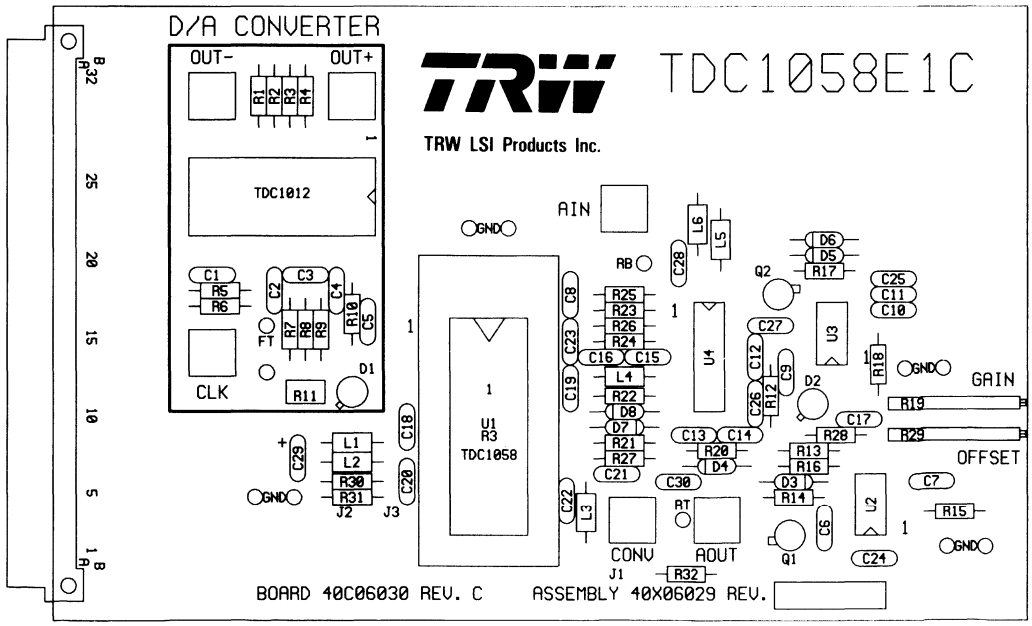
The clock to the TDC1012, CLK, is normally brought onto the board through an SMA connector labeled "CLK" near pin 16 of the TDC1012. A location for a terminating resistor, R6 is provided for clock cable termination. The clock to the TDC1012 is also brought to the edge connector pin B24.

D/A converter outputs are brought to SMA connectors labeled OUT+ and OUT– as well as edge connector pins B28 and B27. Load resistors of 51.1Ω are provided on the board to facilitate 50Ω cable connection to the board.

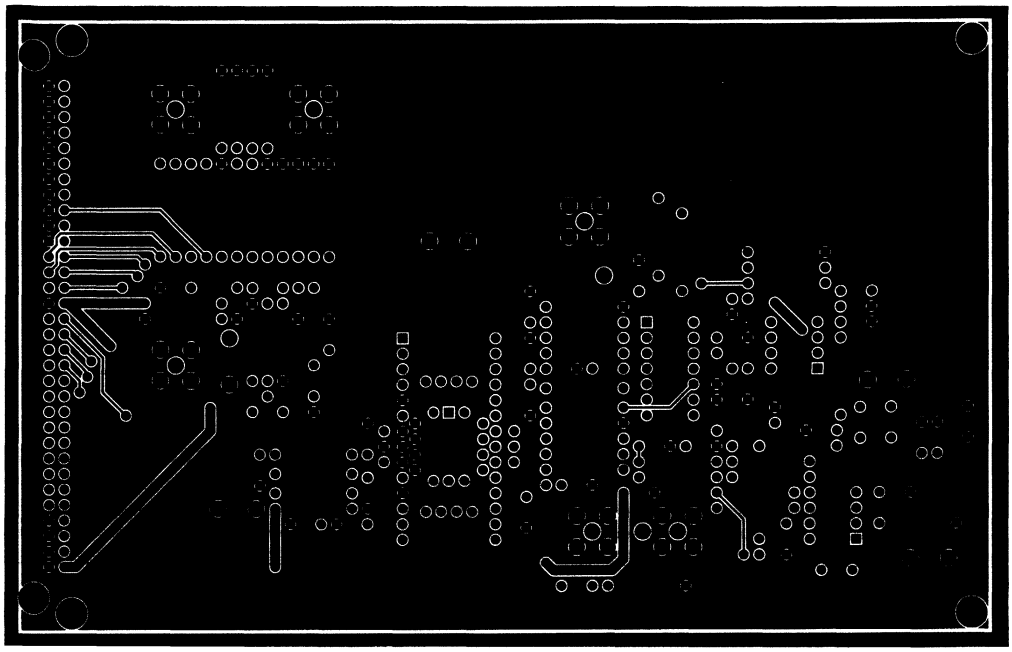
Potentiometer R11 is used to adjust the reference voltage to the TDC1012. This voltage is adjusted to –1.0V as part of the factory test and calibration procedure.

Removing the jumper in the location labeled "FT" will put the TDC1012 into feedthrough (unclocked) mode. This eliminates the requirement for a D/A clock signal, but will degrade the fidelity of the TDC1012 reconstruction.

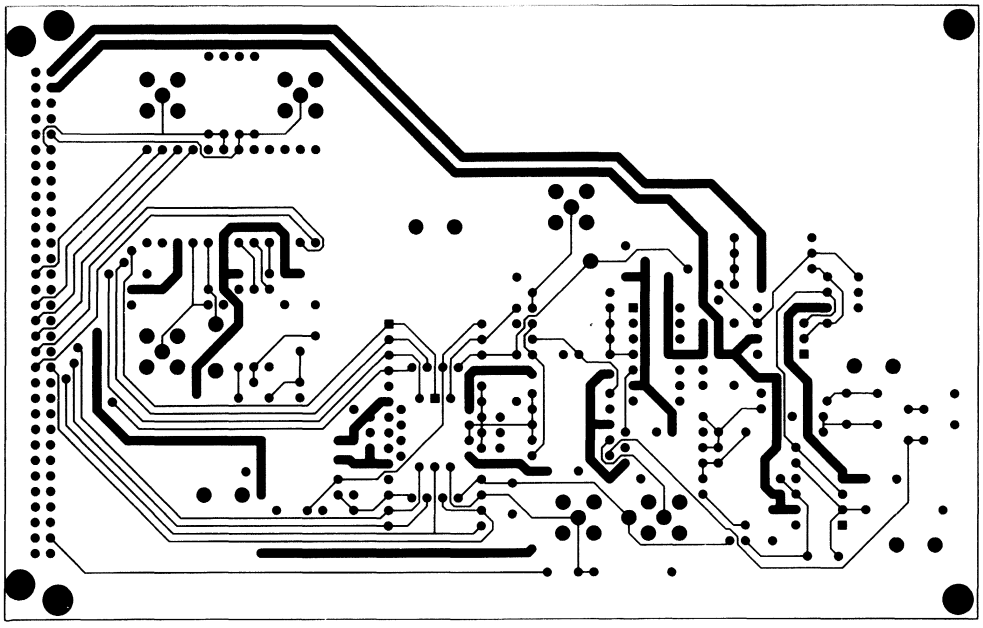
TDC1058E1C Silkscreen Layout



TDC1058E1C Component Side Layout



TDC1058E1C Circuit Side Layout



TDC1058E1C Eurocard Edge Connector Pinout

GND	A32	B32	V− (−15V)
GND	A31	B31	V+ (+15V)
GND	A30	B30	NC
GND	A29	B29	NC
GND	A28	B28	D/A OUT+
GND	A27	B27	D/A OUT−
GND	A26	B26	NC
GND	A25	B25	NC
GND	A24	B24	D/A CLK
GND	A23	B23	NC
GND	A22	B22	NC
D/A D_1 MSB	A21	B21	A/D D_1 MSB
D/A D_2	A20	B20	A/D D_2
D/A D_3	A19	B19	A/D D_3
GND	A18	B18	V_{CC} (+5V)
D/A D_4	A17	B17	A/D D_4
D/A D_5	A16	B16	A/D D_5
D/A D_6	A15	B15	A/D D_6
D/A D_7	A14	B14	A/D D_7
D/A D_8 LSB	A13	B13	A/D D_8 LSB
NC	A12	B12	NC
NC	A11	B11	NC
NC	A10	B10	NC
NC	A9	B9	NC
NC	A8	B8	NC
NC	A7	B7	NC
NC	A6	B6	NC
NC	A5	B5	NC
GND	A4	B4	NC
GND	A3	B3	NC
GND	A2	B2	A/D CONV
GND	A1	B1	V_{EE} (−5.2V)

Mating Connectors for TDC1058E1C

AMP	532507-2	Wire-wrap
AMP	532507-1	Solder tail
Robinson-Nugent	RNE-64BS-W-TG30	Wire-wrap
Robinson-Nugent	RNE-64BS-S-TG30	Solder tail
Souriau	8609-264-6115-7550E1	Wire-wrap
Souriau	8609-264-6114-7550E1	Solder tail
Souriau	8609-264-6813-7550E1	Solder tail, right-angle bend

Figure 8. TDC1058E1C A/D Converter Schematic Diagram

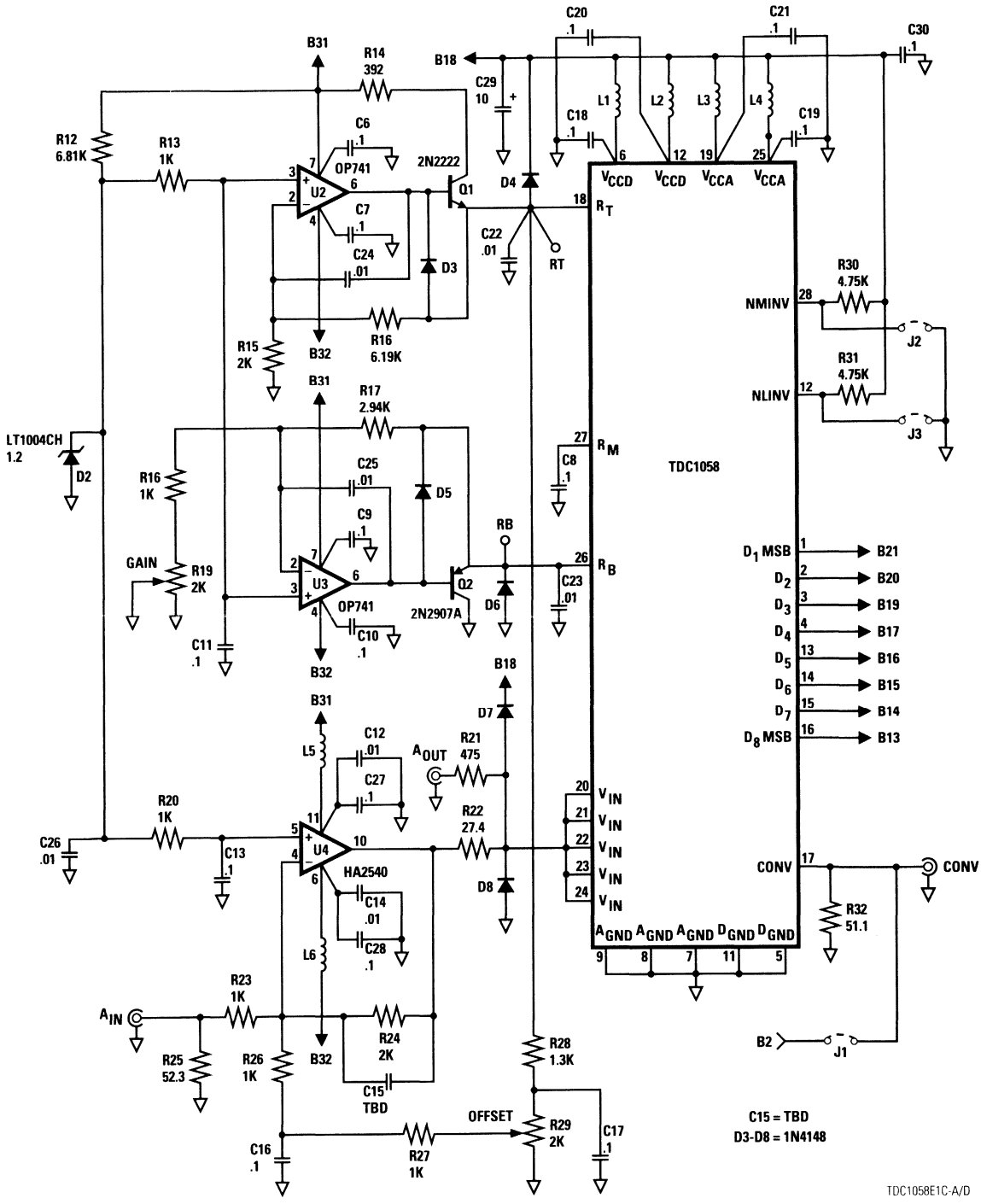
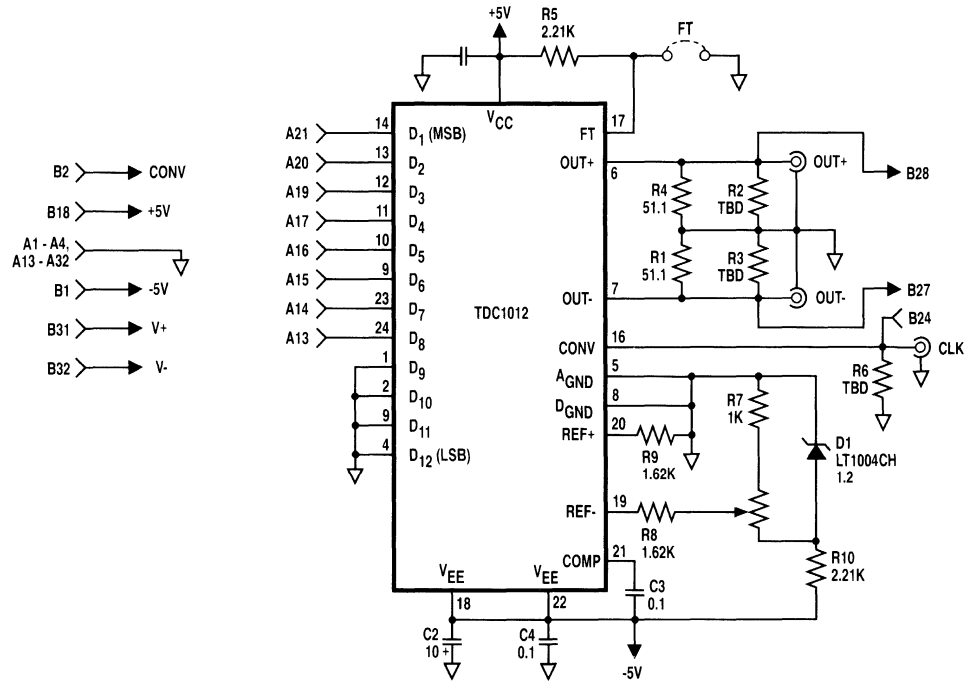


Figure 9. TDC1058E1C D/A Converter Schematic Diagram



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1058B6C	STD – T_A = 0°C to 70°C	Commercial	28 Pin CERDIP	1058B6C
TDC1058N6C	STD – T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	1058N6C
TDC1058R3C	STD – T_A = 0°C to 70°C	Commercial	28 Leaded Plastic Chip Carrier	1058R3C
TDC1058E1C	STD – T_A = 0°C to 70°C	– –	Eurocard PC Board	TDC1058E1C

TMC1061

10-Bit High-Speed Microprocessor-Compatible A/D Converter with Track/Hold

Employing a "half-flash" A/D conversion technique, the TMC1061 CMOS 10-bit A/D converter offers high-speed conversions while dissipating only 235 milliwatts. The analog input signal to the TMC1061 is tracked and held by an internal sampling circuit. Input signals from DC to greater than 200kHz can be digitized accurately without the need for an external track/hold stage.

For convenient interface to microprocessors, the TMC1061 has been designed to function as a TTL compatible memory device or I/O port without the need for additional interface logic, clocks, or timing generators.

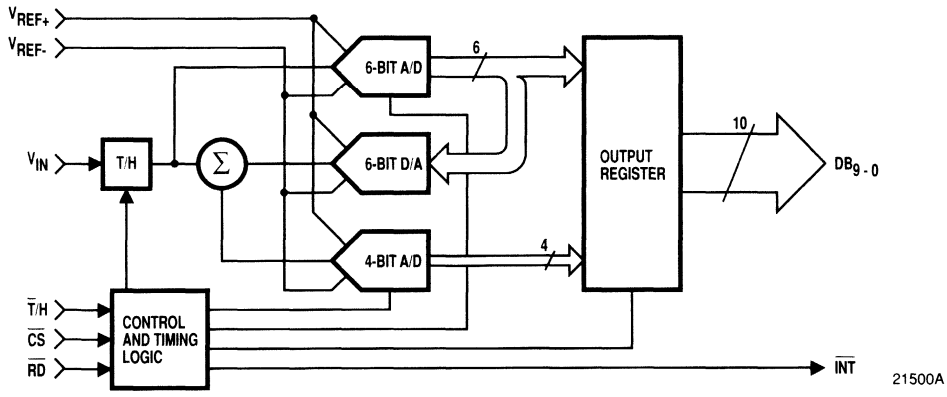
Features

- 1.8µs Maximum Conversion Time
- Includes Track/Hold Input Stage
- No External Clock Or Timer Required
- Single +5 Volt Power Supply Operation
- No Missing Codes, Guaranteed
- Power Dissipation Less Than 235mW

Applications

- Waveform Digitizers
- Disk Drives
- Digital Signal Processing
- Mobile Telecommunications

Functional Block Diagram

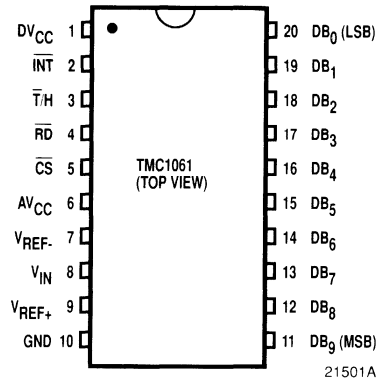


TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

40G06707 Rev. A – 8/90
Printed in the U.S.A.

Pin Assignments



20 Pin CERDIP – B3 Package
20 Pin Plastic DIP – N3 Package
20 Pin Plastic SOIC – M3 Package

Functional Description

The TMC1061 accurately converts an analog input signal to 10-bit data by performing two low-resolution flash A/D conversions. The first A/D conversion provides the six Most Significant Bits (MSBs) of the final result while the second A/D conversion produces the four Least Significant Bits (LSBs) of the 10-bit result.

The sixteen comparators used in the first flash conversion are used again for the second flash. Thus, the half-flash conversion techniques used in the TMC1061 needs only a small fraction of the number of comparators that would be required for a traditional flash converter, and far fewer than would be used in a conventional half-flash approach. This allows the TMC1061 to perform high- speed conversions with minimal power drain.

Power and Grounding

The TMC1061 is designed to operate from a single +5 Volt power supply. There are two power supply input pins, AV_{CC} and DV_{CC}. These pins allow separate external decoupling capacitors for the analog and digital sections of the TMC1061. To ensure optimum performance, the two power supply pins should be connected to the same voltage source, and each should be decoupled with a 0.1µF ceramic capacitor in parallel with a 10µF tantalum capacitor. Depending on the circuit board layout and other system considerations such as power supply noise and proximity of noisy circuit elements, more decoupling may be necessary.

It is important to ensure that none of the TMC1061's input or output pins are driven to voltages more than 300mV above AV_{CC} and DV_{CC}, or more than 300mV below GND. If these limitations are exceeded, the current into or out of any pin on the TMC1061 must be limited to less than 5mA, and no more than a total of 20mA into or out of all overdriven pins can be allowed. In systems with multiple power supplies where the TMC1061's voltage reference source and input amplifiers are powered separately from the A/D converter, careful attention to power supply sequencing must be paid and clamp diodes used to prevent damage to the CMOS A/D converter. The TMC1061's power supply pins should be at the proper voltage before other signals are applied.

To ensure fast, accurate A/D conversions from the TMC1061, it is necessary to use good circuit board layout techniques. The analog ground return path must have low-impedance and be free of noise from other circuits in the system. Noise from neighboring digital circuitry can degrade performance. The digital ground plane should be separate from the analog ground plane.

All decoupling capacitors should be located as close to the TMC1061 as possible. The analog input should be isolated from noisy signal traces to avoid cross-coupling unwanted noise into the input. All external components (e.g., filter capacitors) connected from the converter input to GND should be connected to a low-noise ground return point. Improper grounding may result in degraded A/D converter performance.

Voltage Reference

The TMC1061 has two reference voltage inputs, V_{REF+} and V_{REF-}, which define the zero to full-scale input range of the TMC1061. The reference inputs can be connected to cover the entire power supply voltage range for ratiometric applications by connecting V_{REF-} to GND and V_{REF+} to V_{CC}. They can be connected to any other voltages between GND and V_{CC} to accommodate other input voltage ranges. When the overall V_{REF} is reduced to less than 5 Volts, the sensitivity of the TMC1061 is increased (if $V_{REF+} - V_{REF} = 2$ Volts, then 1LSB = 1.953mV). When the input voltage range is decreased, however, linearity and offset errors become larger with respect to the range. The *Typical Performance Curves* give more information on the performance of the TMC1061 as reference voltage is varied. A reference voltage range ($V_{REF+} - V_{REF}$) of less than 2 Volts is not recommended.

Voltage Reference

V_{REF-} is usually connected to GND. It is occasionally useful to use an input voltage range which is offset from ground. The TMC1061 can easily be set up to accommodate this requirement. V_{REF-} can be driven to a voltage more positive than ground as long as the voltage source applied to V_{REF-} is capable of sinking the necessary reference current. V_{REF-} should be properly decoupled to reduce noise injection when driven to a voltage other than GND.

Since the resistance between the two voltage reference inputs (V_{REF+} and V_{REF-}) can be as low as 400Ω, the voltage source driving these inputs should have low output impedance. Noise on either voltage reference inputs will degrade the performance of the TMC1061. The circuits that are connected to V_{REF+} and V_{REF-} must be stable, low noise voltage sources. Each voltage reference input should be decoupled with a 10μF tantalum and a 0.1μF ceramic capacitor. Additional decoupling may be necessary where power supply and ground noise may be excessive.

The choice of reference voltage source depends upon the requirements of the system. In ratiometric data acquisition applications, where the magnitude of the system parameter being digitized is proportional to or depends upon the power supply voltage level, the reference inputs are normally connected to V_{CC} and GND, and no other reference voltage is used. In absolute measurement applications, where absolute 10-bit accuracy is required, a voltage reference source with better than 0.1% accuracy and temperature drift characteristics is recommended.

The Analog Input

The internal track/hold stage of the TMC1061 samples the analog input voltage every A/D conversion cycle. During the acquisition time period, t_{ACQ}, the analog input is connected to a network comprising a 600Ω resistor in series with a capacitor of 35pF. Short-duration current spikes can be seen at the analog input during normal operation. These spikes are the natural result of switching a fixed voltage onto a capacitor charged to a different voltages level. These observed spikes do not affect the operation or the accuracy of the A/D converter.

High source impedances of amplifiers or buffers driving the TMC1081 can slow the charging of the sampling capacitors and degrade conversion accuracy. Therefore, only signal sources with low output impedances (< 500Ω) used. If the system requirements allow for increased sampling time, the source impedance can be higher. If a signal source has a high output impedance, its output should be buffered with an operational amplifier. The operational amplifier's output should be frequency-stable when driving a 35pF capacitive load. Ringing or voltage shifts at the TMC1061 input during the sampling period can result in degraded performance.

The TMC1061 can correctly convert analog input signals from (GND - 50mV) to (V_{CC} + 50 mV). The signal source must not drive the analog input pin more than 300mV more positive than AV_{CC} and DV_{CC} or more negative than 300mV GND. If it is possible for the analog input pin to be forced beyond these voltages, the current flowing into or out of V_{IN} should be limited to 5mA to avoid damage to to the TMC1061.

The TMC1061 can perform accurate conversions of input signals at frequencies from DC to greater than 200kHz without external sampling circuitry.

Modes of Operation

The TMC1061 has two digital interface modes illustrated in the *Timing Diagrams*.

In Mode 1, the $\overline{T}/H$ input determines the start of the conversion process. When $\overline{T}/H$ is driven LOW for a minimum of 20ns, the comparators that determine the upper 6-bits of the final result become active. When $\overline{T}/H$ goes HIGH, the 6-bit partial result is stored and the final 4-bit conversion begins. After t_{CONV} (approximately 1.2μs, 1.8μs maximum) $\overline{INT}$ goes LOW, indicating that the conversion is complete and that the final results can be read when $\overline{RD}$ goes LOW. $\overline{CS}$ must be LOW in order to enable $\overline{T}/H$ or $\overline{RD}$. $\overline{CS}$ is logically ANDed with $\overline{T}/H$ and $\overline{RD}$. The input voltage is sampled when $\overline{CS}$ and $\overline{T}/H$ are LOW, and the result is read when $\overline{CS}$ and $\overline{RD}$ are LOW.

In Mode 2 ("RD mode"), the $\overline{T}/H$ and $\overline{RD}$ inputs are connected together. A conversion is initiated when both inputs are LOW. The TMC1061 samples the input voltage and causes the comparators to become active and to determine the upper 6-bits of the final result. An internal timer terminates the conversion of the upper 6-bits and initiates the conversion of the four LSBs. In this mode, t_{CONV} lasts approximately 1.8μs (2.4μs maximum) after $\overline{T}/H$ and $\overline{RD}$ are brought LOW. After t_{CONV}, $\overline{INT}$ goes LOW indicating that the conversion is complete. The data on the outputs (enabled when $\overline{RD}$ is LOW) becomes valid approximately 20ns after $\overline{INT}$ goes LOW. Data will be enabled on the outputs throughout the conversion process, but are not valid until after $\overline{INT}$ goes LOW.

Signal Definitions

Power

DV_{CC}, AV_{CC} — Digital and analog positive power supply voltage inputs. They should always be connected to the same voltage source, but are separated to allow for individual decoupling capacitors.

GND — This is the power supply ground input to the TMC1061.

Analog Inputs

V_{IN} — The TMC1061 outputs a 10-bit binary word whose magnitude corresponds to magnitude of the voltage on the V_{IN} input with respect to the difference between V_{REF+} and V_{REF-}.

V_{REF-}, V_{REF+} — The reference voltage inputs determine the input voltage range of the TMC1061. V_{REF+} must be more positive than V_{REF-}. An input voltage equal to V_{REF-} produces an output code of 0, and an input voltage equal to one LSB less than V_{REF+} produces an output code of 1023.

Digital Inputs

$\overline{CS}$ — The Chip Select control input enables the $\overline{T/H}$ and $\overline{RD}$ inputs when LOW.

$\overline{T}/H$ — This is the Track/Hold control input. When this pin is LOW, it causes the analog input signal to be sampled and initiates a new A/D conversion cycle.

$\overline{RD}$ — When LOW, the $\overline{RD}$ control input enables the ten data outputs of the TMC1061. When HIGH, the outputs are in a high-impedance state.

Digital Outputs

$\overline{INT}$ — The interrupt output goes LOW at the end of each A/D conversion. $\overline{INT}$ returns HIGH following the rising edge of $\overline{RD}$.

DB_0-DB_9 — These are the ten data output pins. They are enabled when $\overline{RD}$ is LOW.

Package Interconnections

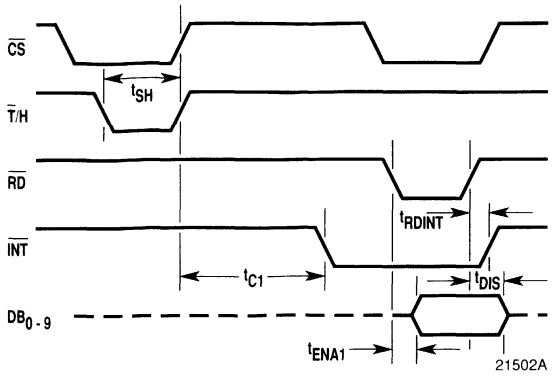
Signal Type	Signal Name	Function	Value	Pin
Power	AV_{CC}	Positive Analog Supply	+5.0V	6
	DV_{CC}	Positive Digital Supply	+5.0V	1
	GND	Ground	0.0V	10
Analog Inputs	V_{IN}	Analog Signal Input	±4.7V	8
	V_{REF+}	Positive Reference Input	+4.7V	9
	V_{REF-}	Negative Reference Input	0.0V	7
Digital Inputs	$\overline{CS}$	Chip Select	TTL	5
	$\overline{T}/H$	Track/Hold Control	TTL	3
	$\overline{RD}$	Read Control	TTL	4
DigitalOutputs	$\overline{INT}$	Interrupt Output	TTL	2
	DB_9 MSB	Most Significant Bit	TTL	11
	DB_8		TTL	12
	DB_7		TTL	13
	DB_6		TTL	14
	DB_5		TTL	15
	DB_4		TTL	16
	DB_3		TTL	17
	DB_2		TTL	18
	DB_1		TTL	19
	DB_0 LSB	Least Significant Bit	TTL	20

Output Coding

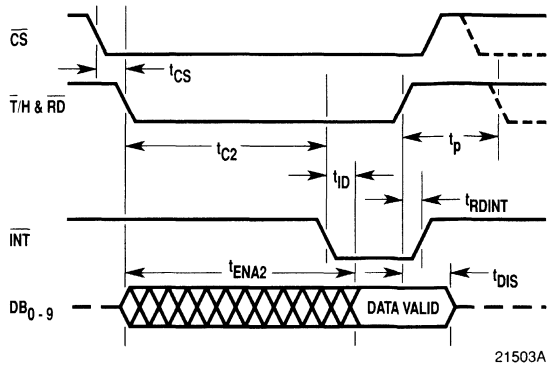
Input Voltage	DB_9 MSB		DB_0 LSB
>4.092	11	1111	1111
+4.092	11	1111	1111
+4.088	11	1111	1110
•		•	
•		•	
•		•	
+0.004	00	0000	0001
0.000	00	0000	0000
<0.000	00	0000	0000

Note: The input voltage range used for this table is from 0.0 to +4.092 Volts. V_{REF-} = GND and V_{REF+} = 4.096 Volts. Input voltages are measured at code centers.

Mode 1. Timing Diagram



Mode 2. Timing Diagram



Absolute maximum ratings (beyond which the device may be damaged) [1,2]

Supply Voltages

DV_{CC}	−0.5 to +6.5V
AV_{CC}	−0.5 to +6.5V
AV_{CC} - DV_{CC} [6]	−0.3 to +0.3V

Input Voltages

Digital Inputs	(DV_{CC} + 0.3) to − 0.3V
Analog Inputs	(AV_{CC} + 0.3) to (GND − 0.3) V

Outputs

Digital Outputs, applied voltage	−0.5 to DV_{CC}
Input current, any pin, externally forced [3]	±5mA
Short-circuit duration (single output to GND)	unlimited

Temperature

Operating, junction	−60 to +135°C
Soldering	
N3 package (10 seconds)	+260°C
B6 package (10 seconds)	+300°C
M3 small outline package	+260°C
Vapor phase (60 seconds)	+215°C
Infrared (15 seconds)	+220°C
Junction	+150°C
Storage	−65 to +150°C

Package input current [3]	±20mA
Package power dissipation at 25°C [4]	875mW
ESD Susceptibility [5]	1500V

Note: Applied voltages must be current limited to specified ranges and that forcing voltages must be limited to specified ranges.

Operating conditions [1,2,8,9]

Parameter		Min	Nom	Max	Min	Nom	Max	Units
AV_{CC}, DV_{CC}	Positive Power Supply Voltages [6]	4.5	5.0	5.5	4.5	5.0	5.5	V
AV_{CC}–DV_{CC}	Power Supply Voltage Differential	–0.1	0.0	0.1	–0.1	0.0	0.1	V
V_{IN}	Input Voltage Range	GND–.050	+4.069	AV_{CC}+.050	GND-.050	+4.069	AV_{CC}+.050	V
SR	Input Slew Rate		1.7			1.7		V/µs
V_{REF}	Reference Voltage [6]	3.5	+4.096	AV_{CC}+.050	3.5	+4.096	AV_{CC}+.050	V
V_{IL}	Input Voltage, Logic LOW, DV_{CC} = 4.75V		1.4	0.8		1.4	0.8	V
V_{IH}	Input Voltage, Logic HIGH, DV_{CC} = 5.25V	2.0	1.4		2.0	1.4		V
I_{OL}	Output Current, Logic LOW	–6.0	–20		–6.0	–20		mA
I_{OH}	Output Current, Logic HIGH	8.0	20		8.0	20		mA
T_J	Junction Temperature, Plastic	–40		+85				°C
T_J	Junction Temperature, CERDIP				–55		+125	°C

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Electrical characteristics within specified operating conditions [8,9]

Parameter		Test Conditions	Temperature Range					Units
				Industrial		Extended		
			Typ	Min	Max	Min	Max	
DI_{CC}	DVCC Supply Current	$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = HIGH	0.1		2.0		2.0	mA
AI_{CC}	AVCC Supply Current	$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = HIGH	30		45		45	mA
C_{IN}	Analog Input Capacitance		35					pF
I_{VIN}	Analog Input Current	$\overline{CS}$ = V_{IN} = +5.0V	0.01		3		3	µA
		V_{IN} = 0.0V, $\overline{CS}$ = +5.0V	–0.01		–3		–3	µA
R_{REF}	Reference Resistance		650	400	900	400	900	Ω
C	Digital Input Capacitance		5					pF
I_{IL}	Input Current, Logic LOW		–0.005		–1.0		–1.0	µA
I_{IH}	Input Current, Logic HIGH		0.005		1.0		1.0	µA
V_{OL}	Output Voltage, Logic LOW	I_{OUT} = 1.6mA, DV_{CC} = 4.75V			0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	I_{OUT} = -360µA, DV_{CC} = 4.75V		2.4		2.4		V
		I_{OUT} = -10µA, DV_{CC} = 4.75V		4.5		4.5		V
I_{OZL}	Output Leakage Current, LOW	V_{OUT} = 0.0V	–0.01		-3.0		–3.0	µA
I_{OZH}	Output Leakage Current, HIGH	V_{OUT} = 5.0V	0.01		3.0		3.0	µA
C_{OUT}	Digital Output Capacitance		5					pF

Switching characteristics within specified operating conditions [8,9,10]

Parameter		Test Conditions	Temperature Range					Units
			Industrial			Extended		
			Typ	Min	Max	Min	Max	
t_{C1}	Conversion Time	Mode 1	1.2		1.8		1.8	µs
t_{C2}	Conversion Time	Mode 2	1.8		2.4		2.4	µs
t_{SH}	Sampling Time [7]	Figure 1, RS = 50Ω			250		250	ns
t_{RDINT}	$\overline{RD}$ to Reset of $\overline{INT}$		10		50		50	ns
t_{ID}	$\overline{INT}$ to Data Delay	CL = 100pF	20		50		50	ns
t_P	Dead Time		10		20		20	ns
t_{ENA1}	Output Enable Time	Mode 1, C_L = 100pF	20		50		50	ns
t_{ENA2}	Output Enable Time	Mode 2, C_L = 100pF			t_{C2} + 50		t_{C2} + 50	ns
t_{DIS}	Output Disable Time	CL = 100pF, R_L = 1kΩ	20		50		50	ns

System performance characteristics within specified operating conditions [8,9]

Parameter		Test Conditions	Temperature Range					Units
			Industrial			Extended		
			Typ	Min	Max	Min	Max	
E_{LIP}	Integral Linearity Error		±0.3		±1.5		±1.5	LSB
E_{LD}	Differential Linearity Error				±1.0		±1.0	LSB
E_{FS}	Full-Scale Error		±0.5		±1.0		±1.0	LSB
E_Z	Zero Error		±0.1		±1.0		±1.0	LSB
E_{TU}	Total Unadjusted Error		±1.0		±2.0		±2.0	LSB
P_{SSF}	Power Supply Sensitivity	AV_{CC} = DV_{CC} = +5.0 ±5% V_{REF+} = +4.75V, V_{REF-} = 0.0V	±0.125					LSB

Notes on Specification Tables

1. *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Conditions* indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the *Electrical Characteristics*. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

2. All voltages are measured with respect to GND, unless otherwise specified.

3. When the voltage applied to any pin exceeds the power supply voltages (i.e., V_{CC}) the absolute value of current flowing into or out of that pin must be limited to 5mA. The total package input current must be limited to 20mA (i.e. four pins at 5mA per pin).

4. The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the *Absolute Maximum Ratings*, whichever is lower. For this device, T_{JMAX} = 150°C, and the typical thermal resistance (θ_{JA}) when board mounted is 47°C/W for the plastic (N) package, 85°C/W for the ceramic (J) package, and 65 °C/W for the small outline (MW) package.

5. Human body model, 100pF discharged through a 1.5kΩ resistor.

6. Typicals are at 25°C and represent the parametric level most likely to occur.

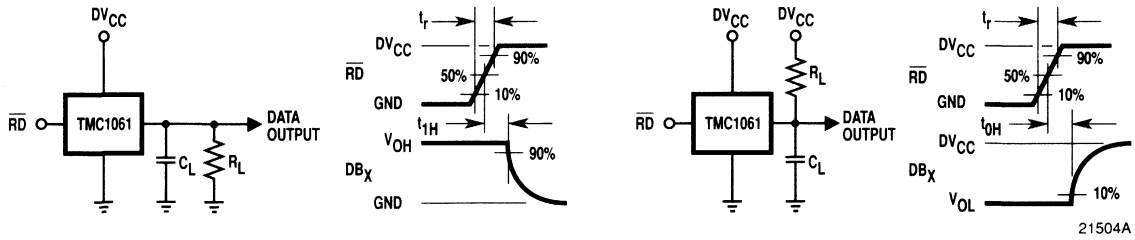
7. TMC1061 performance may degrade if t_{SH} is shorter than the specified value.

8. The following specifications apply for AV_{CC} = DV_{CC} = +5.0 Volts, V_{REF+} = ~5.0V, V_{REF-} = 0.0V unless otherwise specified.

9. Typical performance specifications are for T_J = +25°C.

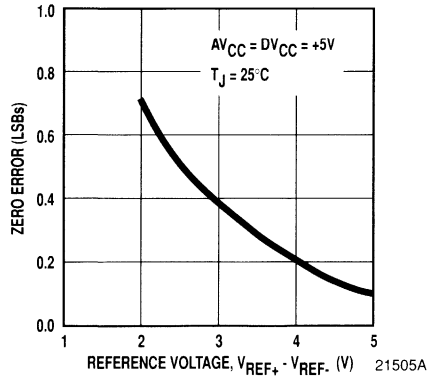
10. Rise and fall times for digital inputs = 20ns, unless otherwise specified.

Figure 3. Output Test Loads

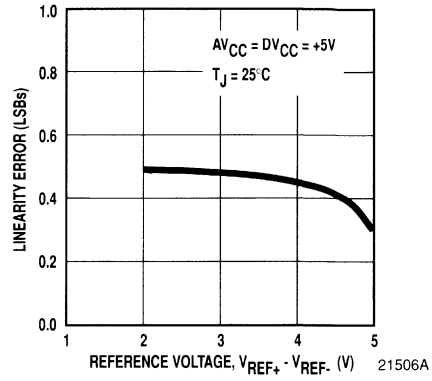


Typical Performance Curves

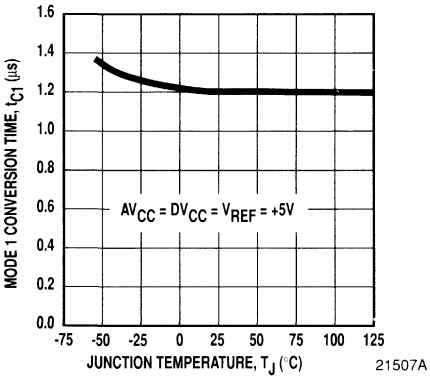
A. Zero (Offset) Error vs Reference Voltage



B. Linearity Error vs Reference Voltage



C. Mode 1 Conversion Time vs Temperature



D. Mode 2 Conversion Time vs Temperature

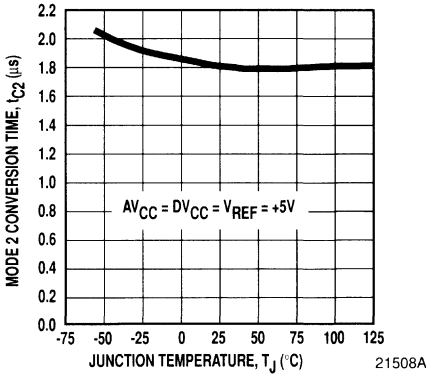
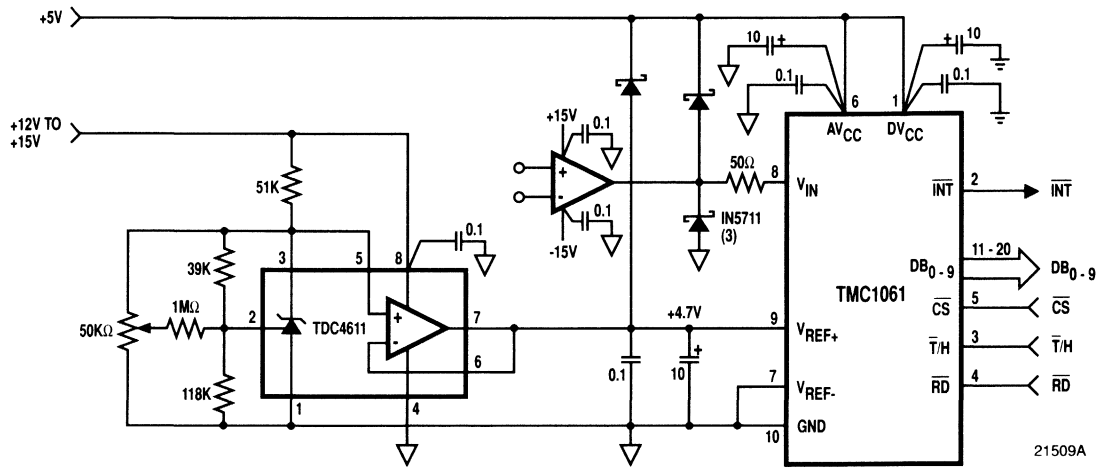


Figure 4. Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC1061B3F	EXT - T_C = -55°C to 125°C	Commercial	20 Pin CERDIP	1061B3F
TMC1061B3B	IND - T_C = -40°C to 85°C	Commercial	20 Pin CERDIP	1061B3B
TMC1061N3B	IND - T_C = -40°C to 85°C	Commercial	20 Pin Plastic	1061N3B
TMC1061M3B	IND - T_C = -40°C to 85°C	Commercial	20 Pin Plastic SOIC	1061M3B
TMC1061E1C	STD - T_A = 0°C to 70°C		Eurocard PC Board	TMC1061E1C

Life Support Policy

TRW LSI PRoducts Inc. components are not designed for use in life support applications, wherein a failure or malfunction of the component can reasonably be expected to result in personal injury. The user of TRW LSI Products Inc. components in life support applications assumes all risk of such use and indemnifies TRW LSI Products Inc. against all damages.

THC1068

Complete High-Speed A/D Converter

8-Bit, 25Msps

Designed to be user-friendly, the THC1068 is a complete flash analog-to-digital converter that combines all circuitry required to convert high-speed analog signals into 8-bit digital data at rates of up to 25Msps (MegaSamples Per Second). Based on the industry standard TDC1048 monolithic flash analog-to- digital converter, the THC1068 contains a wideband analog input amplifier, precision voltage reference and three-state outputs as well as zero-scale and full-scale flags.

The THC1068 offers significant advantages in space efficiency and ease of use. Combining all analog front-end circuitry with the A/D converter in an easy to use package results in savings of board space, component and assembly cost. Furthermore, labor intensive circuit adjustments are eliminated.

The THC1068 is designed to meet the demanding requirements of military applications. It is available in a 24 pin hermetic package and operates with guaranteed performance over the full −55 to +125°C case operating temperature range.

Features

- Complete 8-Bit Analog-To-Digital Converter
- TTL Compatible, Three-State Outputs
- 25Msps Conversion Rate, THC1068-1
- 20Msps Conversion Rate, THC1068
- 10MHz Full Power Analog Input Bandwidth
- Full Performance Is Guaranteed From −55 to 125°C
- Complete Analog Front-End
- Very Low Input Capacitance
- Gain And Offset Internally Trimmed
- Binary And Two's Complement Output Modes
- Zero-Scale And Full-Scale Output Flags
- Operates From +5V And −5.2V Supplies
- 1.6W Typical Power Dissipation
- Hermetically Sealed 24 Pin Package

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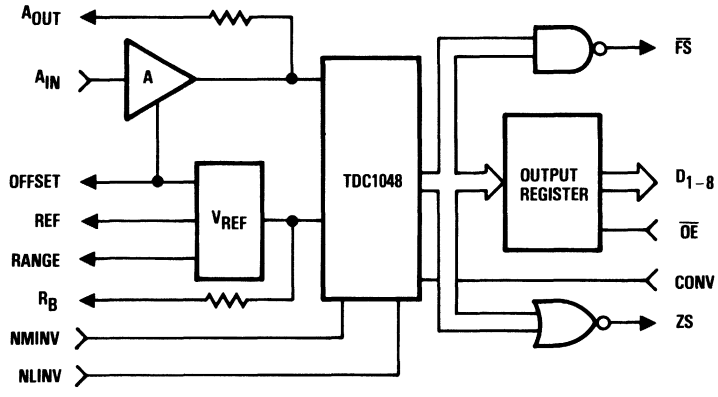
Functional Block Diagram



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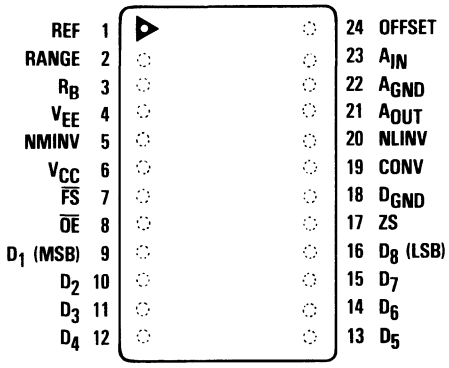
Pin Assignments



24 Pin Hermetic Metal DIP – S7 Package

Functional Description

General Information

The THC1068 is a complete 8-bit A/D converter hybrid in a 24 pin hermetically sealed package. The THC1068 has four functional sections: wideband input amplifier, reference circuitry, monolithic 8-bit flash converter and three-state output register.

The wideband amplifier provides the current necessary to drive the input capacitance of the flash converter while translating the bipolar input to the unipolar range of the flash converter. The input amplifier has a gain of -2 and the stable reference needs no adjustment. The analog input voltage range is -0.5 to 0.5V but can be configured for a 0 to $+1.0$V range by shorting OFFSET to A_{GND}. Likewise, the input can be configured for a 0 to -1.0V range by connecting the OFFSET pin to the REF pin.

The converter portion of the THC1068 is a TDC1048 monolithic 8-bit flash A/D converter. It is made up of a comparator array and encoding logic. The comparator array of the flash converter compares the analog signal from the input amplifier with 255 reference voltages to produce a thermometer code (those comparators referenced to voltages less than the analog input signal will be on and those referenced to voltages greater than the analog signal will be off). The encoding logic of the flash converter then converts the thermometer code into 8 bits of binary data. The TDC1048 data sheet details the operation of the flash portion of the THC1068.

The three-state output register holds the output data between convert cycles and can be set into the high-impedance state with the $\overline{OE}$ control pin.

Power

The THC1068 requires $+5$ and -5.2V for operation. Low-frequency decoupling capacitors of 10μF should be placed as close to the V_{EE} and V_{CC} pins as possible. High-frequency analog and digital power supply decoupling capacitors are included within the THC1068.

For optimum performance, separate analog and digital ground pins are provided on the THC1068. Separate grounds should be maintained on the printed circuit board and connected together at the power supply terminals. However, the voltage difference between A_{GND} and D_{GND} must be within ± 0.1V. It is recommended that provisions be made on the circuit board for shorting jumpers between analog and digital ground as close to the THC1068 as possible. Whether or not the jumpers are required will depend upon the printed circuit board layout and overall system performance.

Reference

A precision voltage reference is used for the flash converter reference as well as for DC level shifting. The REF pin can sink or source up to 2mA but is normally left unconnected.

OFFSET and A_{OUT}

The THC1068 is designed for bipolar (± 0.5V) input operation, but it can also be operated with unipolar positive (0 to $+1$V) and unipolar negative (0 to -1V) inputs. For bipolar input operation, the OFFSET pin must be unconnected. For unipolar positive operation, OFFSET is connected to A_{GND}. For unipolar negative operation, OFFSET is connected to the REF pin. A 2 kOhm potentiometer can be connected between OFFSET, REF and A_{GND} to vary the DC offset of the input amplifier, as shown in ***Figure 5***. A .01μF decoupling capacitor to A_{GND} is located within the THC1068 on the OFFSET pin.

The A_{OUT} pin allows monitoring the analog signal at the input to the flash converter and is normally left unconnected. It has a nominal series resistance of 470 Ohms.

RANGE and R_B

The RANGE pin allows optional adjustment of the reference voltage (gain) of the flash converter and is normally left unconnected. For reference adjustment, a 2 kOhm potentiometer can be connected between REF, RANGE and A_{GND} as shown in ***Figure 5***. The nominal input resistance of RANGE is 300 Ohms with 0.01μF decoupling to A_{GND}. The R_B pin allows monitoring of the full-scale reference voltage to the flash converter through a 470 Ohm series resistor.

Convert

The THC1068 requires a TTL clock (CONV) signal. The conversion occurs within the sampling time offset (t_{STO}) of the rising edge of CONV. The result is transferred to the output of the flash converter on the next rising edge of CONV. Data for sample N is available at the output of the THC1068 t_D (Output Delay Time) after the rising edge of sample N+2, and is shown in ***Figure 1***.

Analog Input

The wideband input amplifier of the THC1068 provides the current necessary to drive the input capacitance of the flash converter. The amplifier provides a gain of −2 and has a nominal input impedance of 1000 Ohms. For lower impedances, a termination resistor should be added as close to the A_{IN} pin as possible. The THC1068 is capable of digitizing sinusoidal signals up to 10MHz. The input amplifier has pulse response as shown in the ***Typical Performance Curves***, with a full-power bandwidth in excess of 20MHz.

Output Controls

The digital output of the THC1068 can be formatted with the NMINV and NLINV control pins. These pins are for D.C. (steady state) use and allow either straight binary or offset two's complement, in either true or inverted sense. The ***Output Coding Table*** shows the output formats possible with these pins. Note that in offset two's complement format, $\overline{FS}$ and ZS indicate midscale codes rather than full and zero-scale codes, as shown in the ***Output Coding Table***. When left unconnected, internal pull-up resistors keep the outputs in true straight binary format.

The data outputs of the THC1068 can be set into the high-impedance state with the $\overline{OE}$ control pin. The outputs become high-impedance points within t_{DIS} after the $\overline{OE}$ is switched HIGH and likewise become valid within t_{ENA} after switching $\overline{OE}$ LOW.

Data

The outputs of the THC1068 are TTL compatible, capable of driving 10 LS loads or their equivalent. New data becomes valid t_D after the rising edge of CONV.

Output Flags

The output flags of the THC1068 are not latched: they are active even when the data outputs are in the high-impedance state. The $\overline{FS}$ (active LOW) flag indicates that the output bits of the flash converter are all HIGH. Likewise, the ZS (active HIGH) flag indicates that the output bits of the flash converter are all LOW. ZS and $\overline{FS}$ represent zero-scale and full-scale analog inputs only when the output code is in the straight binary format. The ***Output Coding Table*** shows the status of the output flags for various input voltages and output code formats. Note that the flags indicate the status of the flash converter output one clock cycle before it appears at the output pins of the THC1068.

Package Interconnections

Signal Type	Signal Name	Function	Value	S7 Package Pins
Power	V_{EE}	Negative Supply Voltage	−5.2V	4
	V_{CC}	Positive Supply Voltage	+5.0V	6
	D_{GND}	Digital Ground	0.0V	18
	A_{GND}	Analog Ground	0.0V	22
Reference	REF	Reference Voltage Output	1.2V	1
OFFSET, A_{OUT}	OFFSET	Input Range Offset Control	0.6V	24
	A_{OUT}	Amplifier Output Monitor Point	0 to −2V	21
RANGE, R_B	RANGE	Reference Gain Control	1.0V	2
	R_B	Reference Voltage Monitor Point	−2.08V	3
Convert	CONV	Convert	TTL	19
Analog Input	A_{IN}	Analog Input	−0.5 to +0.5V	23
Output Controls	NMINV	MSB Invert, Active LOW	TTL	5
	NLINV	All But MSB Invert, Active LOW	TTL	20
	$\overline{OE}$	Output Enable, Active LOW	TTL	8
Data	D_1	MSB Output	TTL	9
	D_2		TTL	10
	D_3		TTL	11
	D_4		TTL	12
	D_5		TTL	13
	D_6		TTL	14
	D_7		TTL	15
	D_8	LSB Output	TTL	16
Output Flags	$\overline{FS}$	Full-Scale Flag	TTL	7
	ZS	Zero-Scale Flag	TTL	17

Output Coding Table

Step	Midpoints 1 LSB = 3.92mV	Binary						Offset Two's Complement					
		True			Inverted			True			Inverted		
		NMINV = 1 NLINV = 1			NMINV = 0 NLINV = 0			NMINV = 0 NLINV = 1			NMINV = 1 NLINV = 0		
		$D_1 \ldots D_8$	$\overline{FS}$	ZS	$D_1 \ldots D_8$	$\overline{FS}$	ZS	$D_1 \ldots D_8$	$\overline{FS}$	ZS	$D_1 \ldots D_8$	$\overline{FS}$	ZS
000	−0.5000V	00000000	1	1	11111111	0	0	10000000	1	0	01111111	1	0
001	−0.4961V	00000001	1	0	11111110	1	0	10000001	1	0	01111110	1	0
•	•	•			•			•			•		
•	•	•			•			•			•		
•	•	•			•			•			•		
126	−0.0059V	01111110	1	0	10000001	1	0	11111110	1	0	00000001	1	0
127	−0.0020V	01111111	1	0	10000000	1	0	11111111	0	0	00000000	1	1
128	+0.0020V	10000000	1	0	01111111	1	0	00000000	1	1	11111111	0	0
129	+0.0059V	10000001	1	0	01111110	1	0	00000001	1	0	11111110	1	0
•	•	•			•			•			•		
•	•	•			•			•			•		
•	•	•			•			•			•		
254	+0.4961V	11111110	1	0	00000001	1	0	01111110	1	0	10000001	1	0
255	+0.5000V	11111111	0	0	00000000	1	1	01111111	1	0	10000000	1	0

Figure 1. Timing Diagram

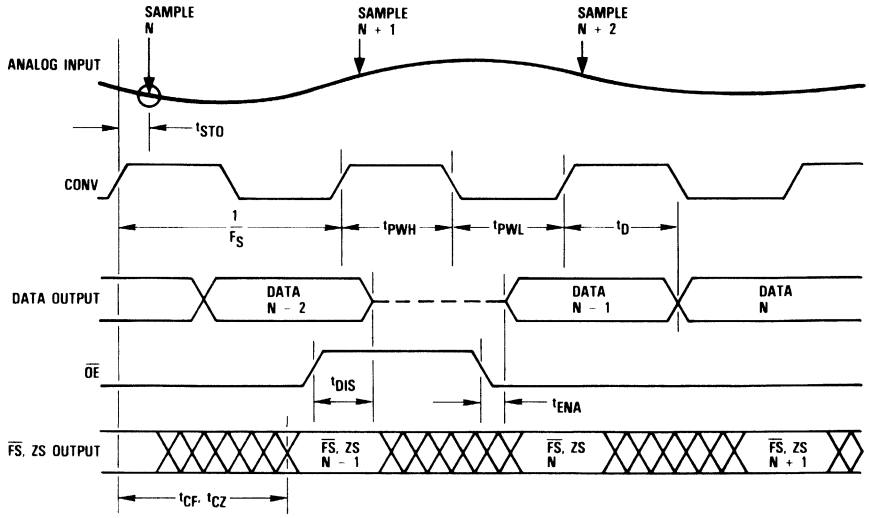


Figure 2. Analog Input Circuit

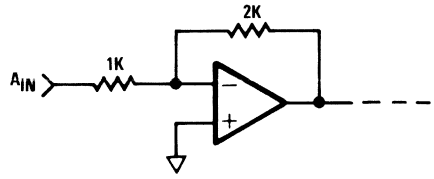


Figure 3. Digital Input Circuits

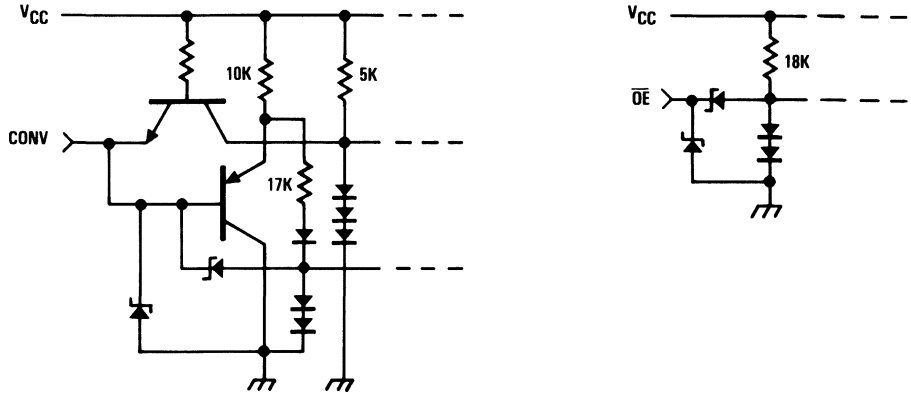


Figure 4. Digital Output Circuits

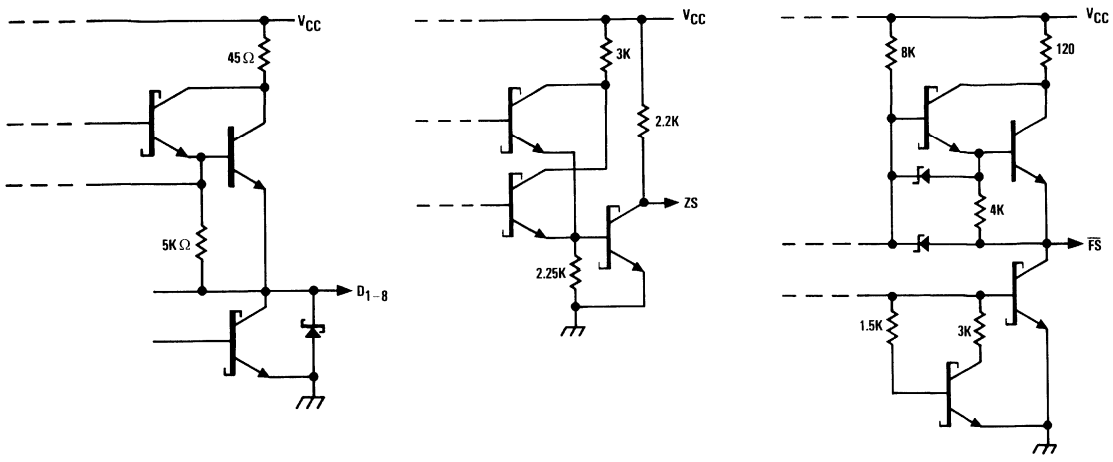


Figure 5. Connection of RANGE, REF and OFFSET

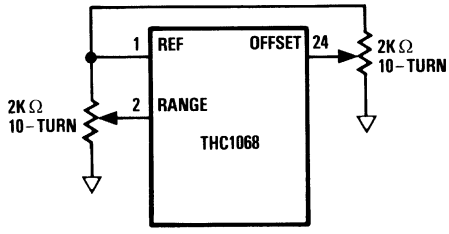
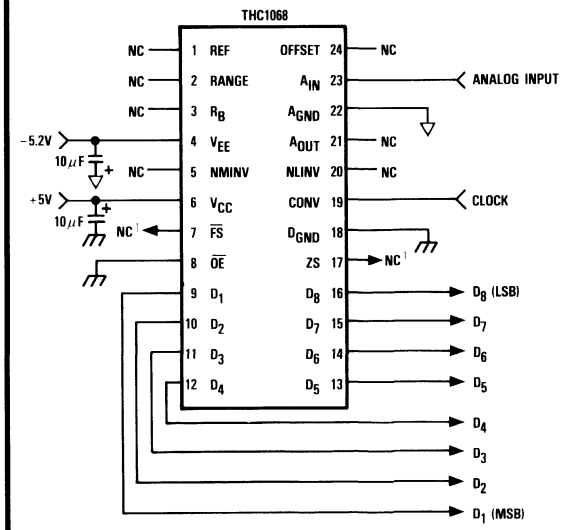


Figure 6. Typical Interface Circuit



Note: 1. Output flags should be NC if not needed.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND}) ..... −0.5 to +7.0V
V_{EE} (measured to A_{GND}) ..... +0.5 to −7.0V
A_{GND} (measured to D_{GND}) ..... −0.5 to +0.5V

Input Voltages [2]

CONV, $\overline{OE}$, NMINV, NLINV (measured to D_{GND}) ..... V_{CC} to −0.5V
A_{IN} (measured to A_{GND}) ..... V_{EE} to V_{CC}

Outputs

Digital outputs, applied voltage (measured to D_{GND}) ..... −0.5 to V_{CC}
Digital outputs, applied current 50mA
Short-circuit duration (single output to GND) ..... Infinite

Temperature

Operating, case ..... −60 to +140°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −65 to +150°C

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the operating conditions are not exceeded.
2. Applied voltage is current limited to specified range.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Digital Supply Voltage (measured to D_{GND})	4.50	5.0	5.50	4.50	5.0	5.50	V
V_{EE}	Analog Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
A_{GND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	+0.1	−0.1	0.0	+0.1	V
t_{PWL}	CONV Pulse Width, LOW	18			18			ns
t_{PWH}	CONV Pulse Width, HIGH	22			22			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.2			2.2			V
V_{IN}	Input Voltage Range, REF and OFFSET Open	−0.5		+0.5	−0.5		+0.5	V
T_A	Ambient Temperature, Still Air	0		+70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Digital Supply Current	V_{CC} = Max, Static[1]		170		170	mA
I_{EE}	Analog Supply Current	V_{EE} = Max, Static[1]		−370		−370	mA
R_{IN}	Analog Input Resistance		970	1030	970	1030	Ohms
C_{IN}	Analog Input Capacitance			5		5	pF
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_{IN} = 0.4V					
		NMINV, NLINV		−3.3		−3.3	mA
		$\overline{OE}$		−0.8		−0.8	mA
		CONV		−1.2		−1.2	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_{IN} = 2.4V					
		NMINV, NLINV		−2.0		−2.0	mA
		$\overline{OE}$		+0.04		+0.04	mA
		CONV		+0.1		+0.1	mA
I_{OZL}	Output Leakage Current, Logic LOW[1]			±50		±50	μA
I_{OZH}	Output Leakage Current, Logic HIGH[1]			±50		±50	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = Max, Output HIGH, one pin to ground, one second duration max.		−200		−200	mA
V_{OL}	Output Voltage, Logic LOW	I_{OL} = 2mA		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	I_{OH} = 250μA	2.4		2.4		V
V_{REF}	Reference Voltage		+1.138	+1.302	+1.138	+1.302	V
C_I	Digital Input Capacitance	T_A = 25°C, f = 1MHz		15		15	pF

Note: 1. Worst case, $\overline{OE}$ = LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC}, V_{EE} = Min					
		THC1068-1	25		25		Msps
		THC1068	20		20		Msps
t_{STO}	Sampling Time Offset	V_{CC}, V_{EE} = Min	−15	0	−15	0	ns
t_D	Digital Output Delay	V_{CC} = Min		20		20	ns
t_{ENA}	HIGH Impedance Enable	V_{CC} = Min		24		24	ns
t_{DIS}	HIGH Impedance Disable	V_{CC} = Min		24		24	ns
t_{CF}	Full-Scale Flag Delay	V_{CC} = Min		55		55	ns
t_{CZ}	Zero-Scale Flag Delay	V_{CC} = Min		100		100	ns

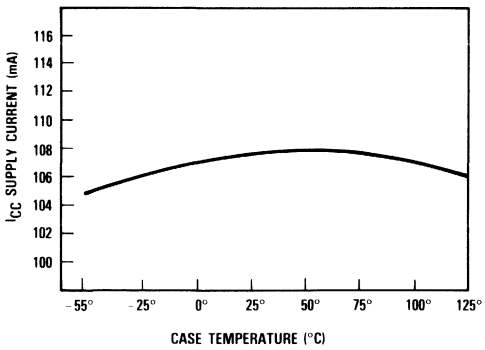
System performance characteristics within specified operating conditions

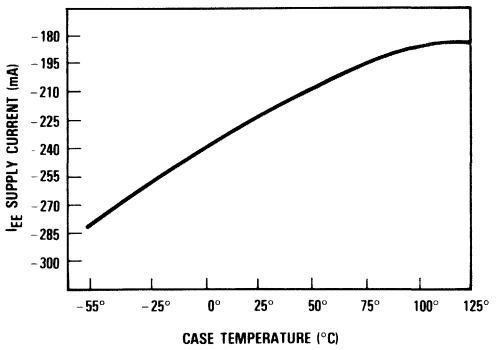
Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error, Integral			0.2		0.2	%
E_{LD}	Linearity Error, Differential			0.2		0.2	%
Q	Code Size		15	185	15	185	% Nominal
t_{TR}	Transient Response, Full-Scale			20		20	ns
BW	Full Power Input Bandwidth		10		10		MHz
SNR	Signal-to-Noise Ratio	10MHz Bandwidth, F_S = 20Msps					
	RMS Signal/RMS Noise	1.248MHz Input	41		41		dB
		2.438MHz Input	40		40		dB
E_{AP}	Aperture Error			60		60	ps
DP	Differential Phase	F_S = 4 x NTSC Subcarrier		1.0		1.0	Degree
DG	Differential Gain	F_S = 4 x NTSC Subcarrier		2.0		2.0	%

A

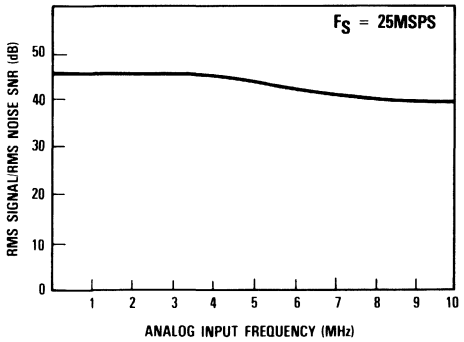
Typical Performance Curves

A. Power Supply Current vs. Temperature

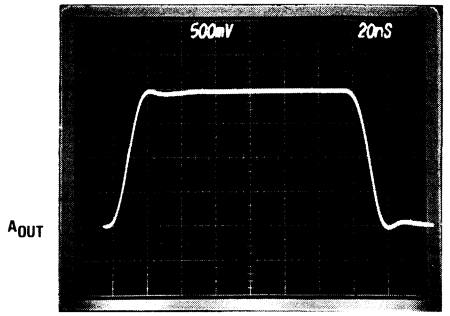




B. SNR vs. Analog Input Frequency



C. Input Amplifier's Pulse Response



Evaluation Board

The THC1068E1C is a Eurocard-style printed circuit board designed to aid in the evaluation of the THC1068 A/D converter. The board dimensions are 100mm x 160mm with a standard 64 pin double-row DIN male connector installed. A complementary 64 pin double-row DIN female connector is included with the board.

The board employs only two conducting sides. Most of the circuit interconnections are on the bottom of the board while the top is mostly solid ground plane. SMA connectors are installed on the board to facilitate analog I/O and clocks. The circuitry on the board includes all power supply decoupling required for the THC1068, and a TDC1012 12-bit D/A converter which may be used in evaluating certain parameters of the THC1068.

The board is calibrated and tested at the factory and is supplied complete with THC1068 and TDC1012 installed.

Power and Ground

Two power supply voltages are required for the operation of the THC1068E1C: $V_{CC} = +5V$ and $V_{EE} = -5.2V$. All power inputs are decoupled to a single solid ground plane, GND. All GND pins of the board are connected to the ground plane and it is recommended that all GND pins be used.

A/D Converter Inputs

The clock to the THC1068, CONV, is brought onto the board by way of edge connector pin B2. A 51.1Ω resistor, R13 may be installed on the board for terminating 50Ω clock signals. The DIP switch controls $\overline{OE}$, NLINV, NMINV and the GAIN and OFFSET adjustment potentiometers. $\overline{OE}$, NLINV and NMINV are pulled to a logic HIGH when their corresponding switch is open.

The analog signal input to the THC1068, A_{IN} is brought onto the board through the SMA connector labeled "A_{IN}" near pin 23 of the THC1068. A terminating resistor, R14, is included on the board for terminating the analog input signal cable.

A/D Converter Data Outputs and D/A Converter Data Inputs

The eight data outputs of the THC1068 are brought to edge connector pins B13 through B21 (excluding B18). These pins are located directly across the edge connector from the corresponding data inputs of the TDC1012 D/A converter to simplify connection of A/D outputs to D/A inputs.

D/A Converter Inputs

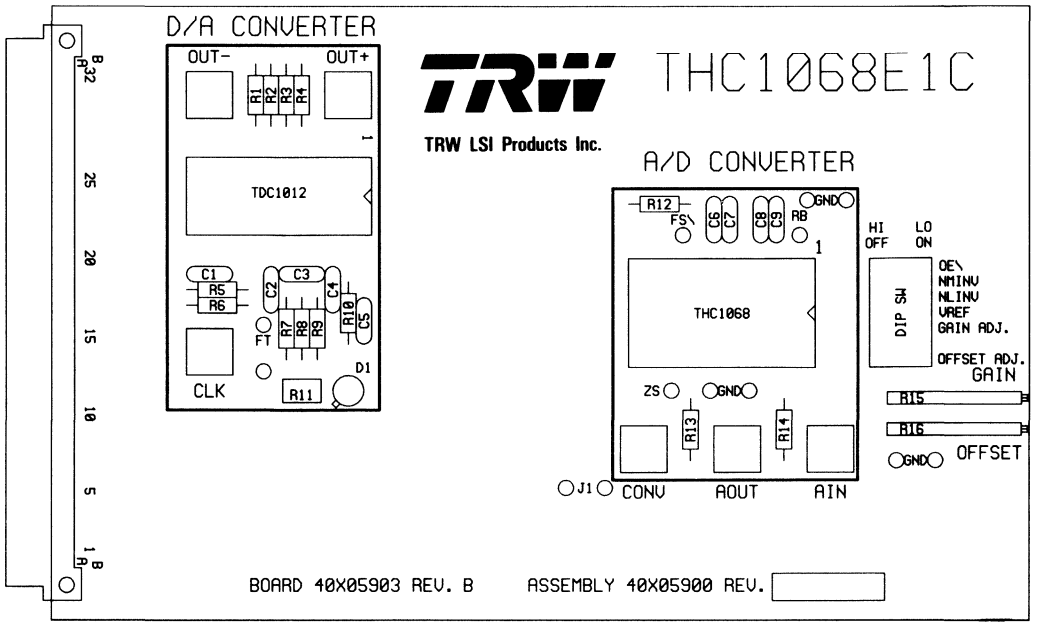
The clock to the TDC1012, CLK, is normally brought onto the board through an SMA connector labeled "CLK" near pin 16 of the TDC1012. A location for a terminating resistor, R6 is provided for clock cable termination. The clock input to the TDC1012 is also brought to the edge connector pin B24.

D/A converter outputs are brought to SMA connectors labeled OUT+ and OUT− as well as edge connector pins B28 and B27. Load resistors of 51.1Ω are provided on the board to source-terminate a 50Ω cable connected to the board.

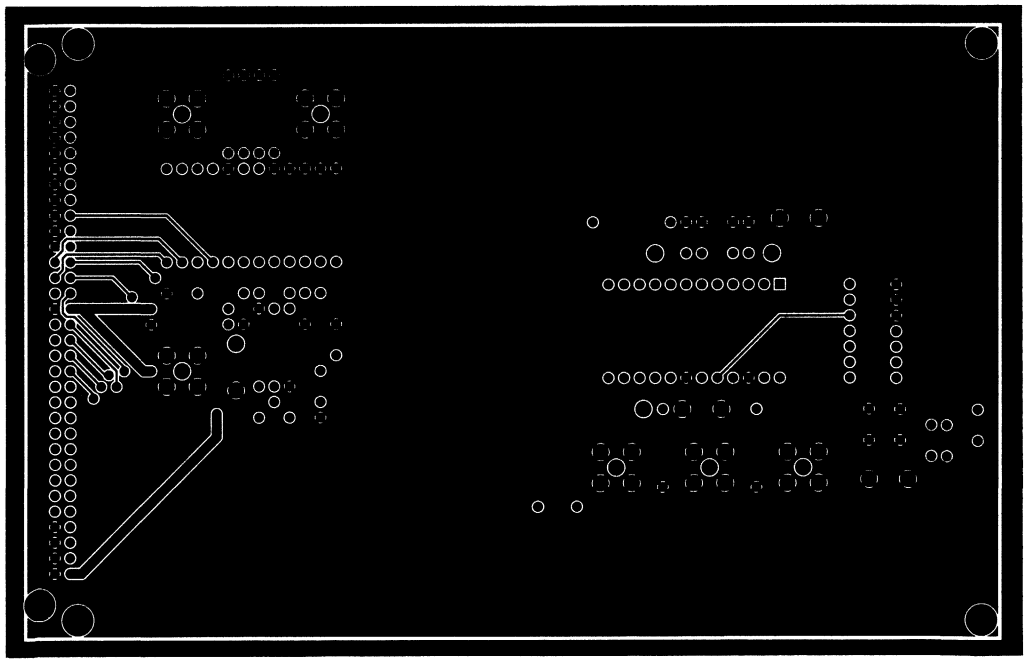
Potentiometer R11 is used to adjust the reference voltage to the TDC1012. This voltage is adjusted to −1.0V as part of the factory test and calibration procedure.

Removing the jumper in the location labeled "FT" will put the TDC1012 into feedthrough (unclocked) mode. This eliminates the requirement for a D/A clock signal, but will degrade the fidelity of the TDC1012 signal reconstruction.

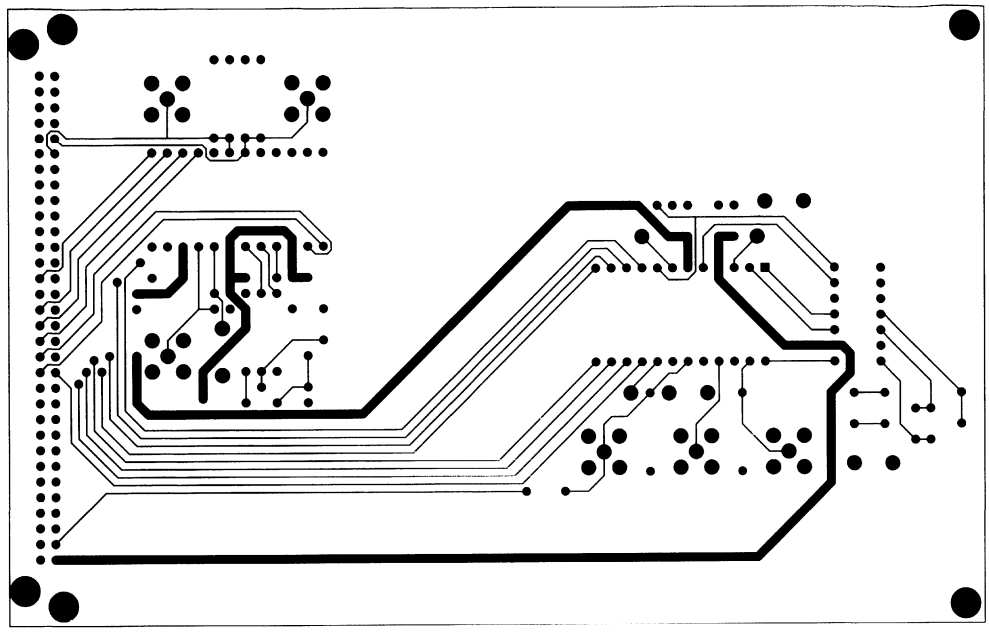
THC1068E1C Silkscreen Layout



THC1068E1C Component Side Layout



THC1068E1C Circuit Side Layout



THC1068E1C Eurocard Edge Connector Pinout

GND	A32	B32	V– (–15V)
GND	A31	B31	V+ (+15V)
GND	A30	B30	NC
GND	A29	B29	NC
GND	A28	B28	D/A OUT+
GND	A27	B27	D/A OUT–
GND	A26	B26	NC
GND	A25	B25	NC
GND	A24	B24	D/A CLK
GND	A23	B23	NC
GND	A22	B22	NC
D/A D_1 MSB	A21	B21	A/D D_1 MSB
D/A D_2	A20	B20	A/D D_2
D/A D_3	A19	B19	A/D D_3
GND	A18	B18	V_{CC} (+5V)
D/A D_4	A17	B17	A/D D_4
D/A D_5	A16	B16	A/D D_5
D/A D_6	A15	B15	A/D D_6
D/A D_7	A14	B14	A/D D_7
D/A D_8	A13	B13	A/D D_8 LSB
NC	A12	B12	NC
NC	A11	B11	NC
NC	A10	B10	NC
NC	A9	B9	NC
NC	A8	B8	NC
NC	A7	B7	NC
NC	A6	B6	NC
NC	A5	B5	NC
GND	A4	B4	NC
GND	A3	B3	NC
GND	A2	B2	A/D CONV
GND	A1	B1	V_{EE} (–5.2V)

Mating Connectors for THC1068E1C

AMP	532507-2	Wire-wrap
AMP	532507-1	Solder tail
Robinson-Nugent	RNE-64BS-W-TG30	Wire-wrap
Robinson-Nugent	RNE-64BS-S-TG30	Solder tail
Souriau	8609-264-6115-7550E1	Wire-wrap
Souriau	8609-264-6114-7550E1	Solder tail
Souriau	8609-264-6813-7550E1	Solder tail, right-angle bend

Figure 7. THC1068E1C A/D Converter Schematic Diagram

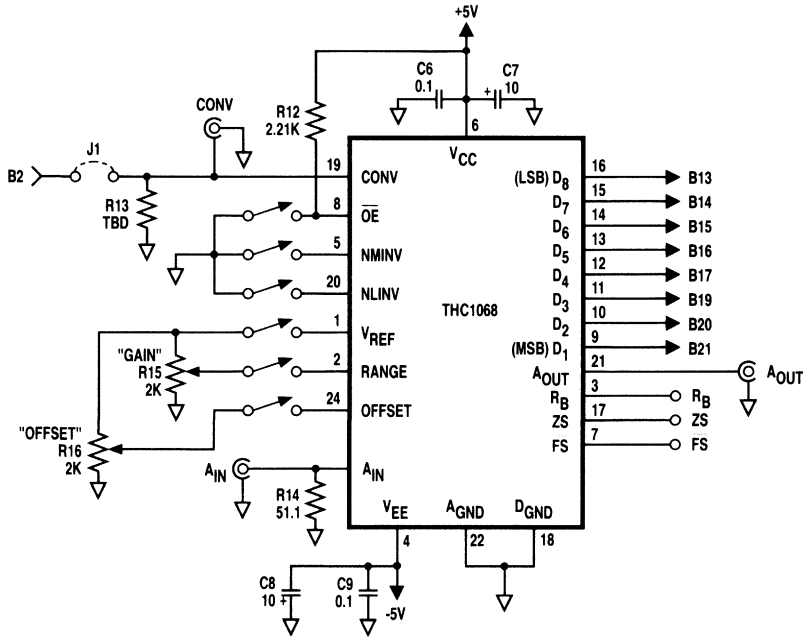
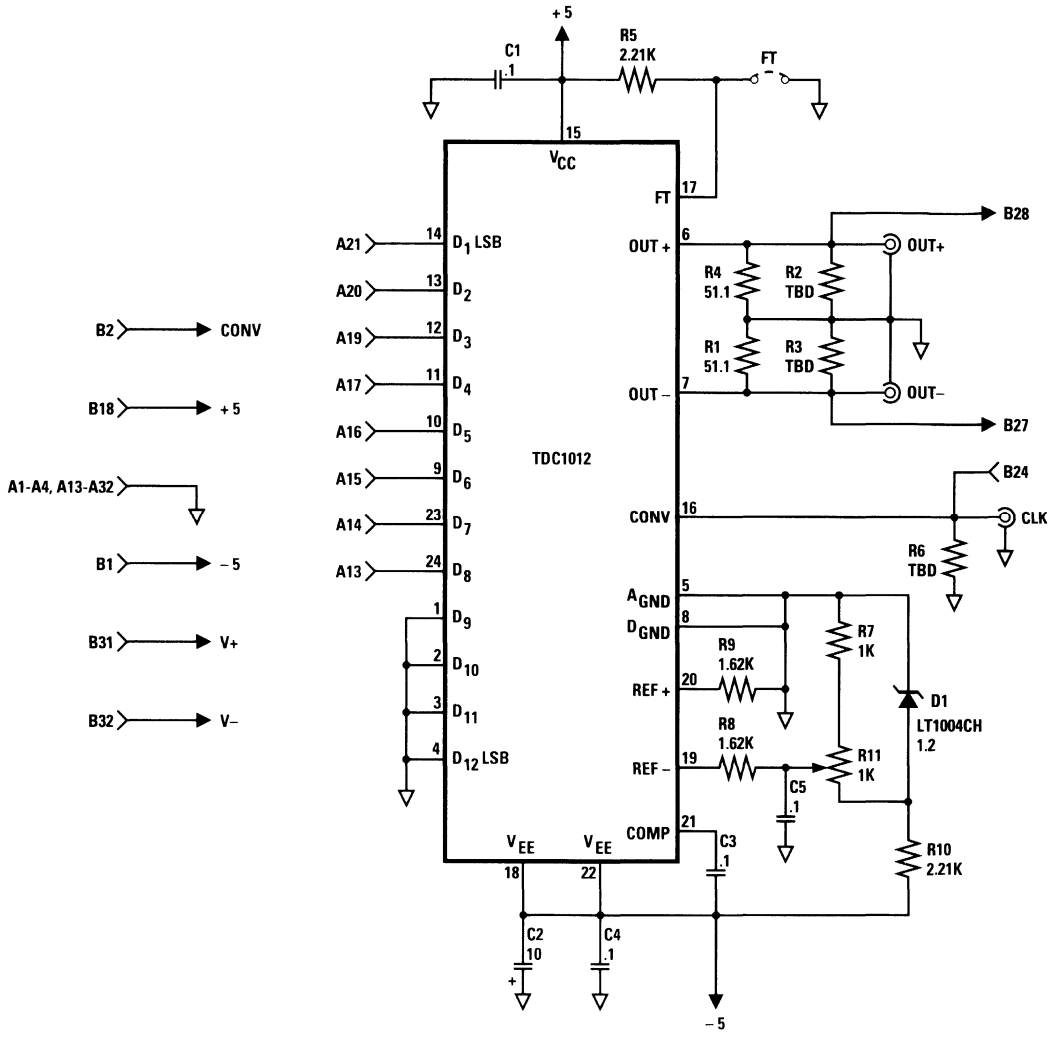


Figure 8. THC1068E1C D/A Converter Schematic Diagram



Ordering Information

Product Number	Temperature Range	Screening	Package[1]	Package Marking
THC1068S7C	STD – T_A = 0°C to 70°C	Commercial	24 Pin Hermetic Metal DIP	1068S7C
THC1068S7C1	STD – T_A = 0°C to 70°C	Commercial	24 Pin Hermetic Metal DIP	1068S7C1
THC1068S7V	EXT – T_C = – 55°C to 125°C	MIL-STD-883	24 Pin Hermetic Metal DIP	1068S7V
THC1068S7V1	EXT – T_C = – 55°C to 125°C	MIL-STD-883	24 Pin Hermetic Metal DIP	1068S7V1
THC1068E1C	STD – T_A = 0°C to 70°C	– –	Eurocard Format PC Board	THC1068E1C

Note: 1. V-grade will only be shipped in military packages.
C-grade will be shipped in commercial packages as available.

A

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THC1069

Complete High-Speed A/D Converter
9-Bit, 37 Msps

The TRW THC1069 is a complete analog-to-digital converter that combines all the circuitry required to convert high-speed analog signals into 9-bit digital data at rates up to 37 Msps (Megasamples per second). The THC1069 comprises a wideband input amplifier stage, stable voltage references, 9-bit flash A/D converter, and output data register which makes the THC1069 very easy to use. The THC1069 offers precision gain, linearity, offset, and outstanding high-speed dynamic performance.

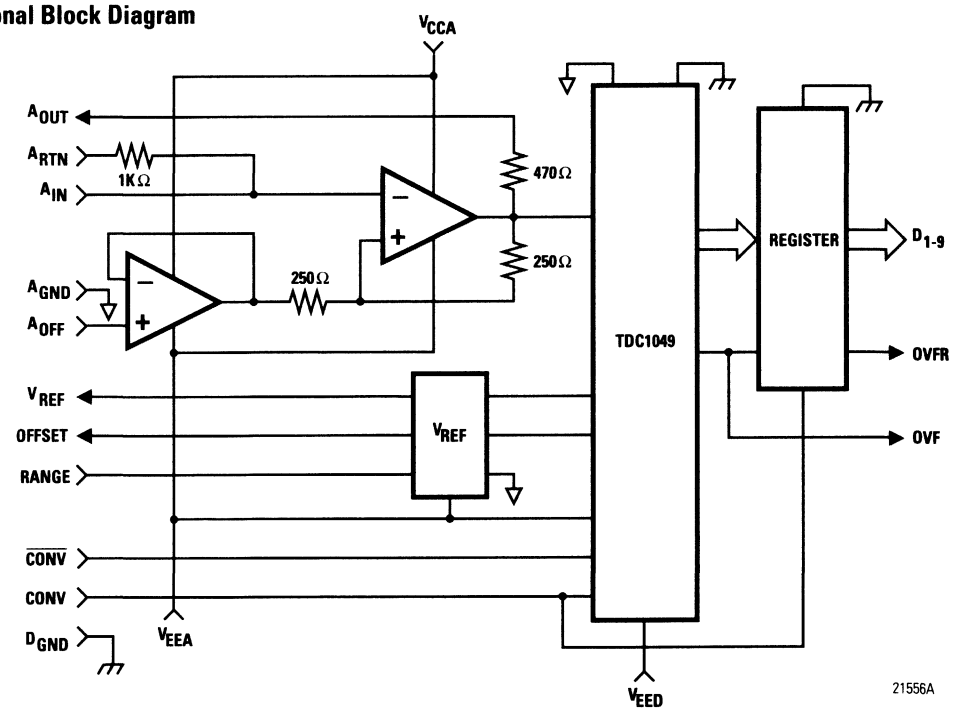
The THC1069 is housed in a 32-pin hermetic package with guaranteed performance over the industrial (–25 to 85°C) or military (–55 to 125°C) case temperature ranges. Military THC1069s are manufactured in compliance with MIL-STD-883C in facilities certified and qualified to MIL-STD-1772.

Features:

- 37 Msps Conversion Rate, Guaranteed
- Guaranteed Performance Over All Operating Conditions
- Complete Analog Front-End
- Requires Only +5 And –5.2 Volt Power Supplies
- ±0.5 Volt Input Range
- Input Capacitance Less Than 10pF
- Range And Offset Externally Adjustable
- Outstanding Overload Recovery
- ECL Compatible
- Overflow Output Flag
- Industrial Or Military Temperature Range
- 32-Pin Hermetic Package

A

Functional Block Diagram



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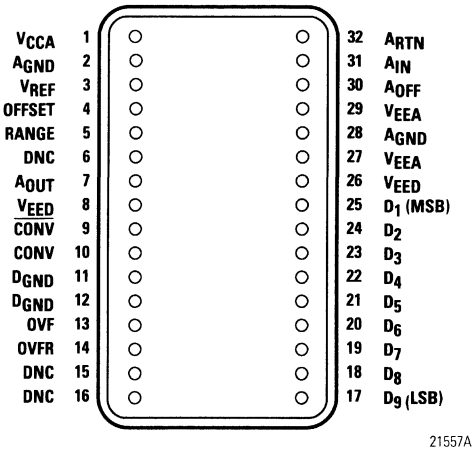
Applications

- Broadcast And Studio Video
- Medical Imaging
- Magnetic Resonance Signal Acquisition
- Radar
- Digital Oscilloscopes
- Spectrum Analysis

Pin Assignments



32 Pin Hermetic Metal DIP – S5 Package

Functional Description

General Information

The THC1069 is a complete 9-bit A/D converter in a hermetically sealed 32-pin package. It has four major functional sections: Wideband input amplifier stage, voltage reference generator, monolithic 9-bit flash A/D converter, and output data register. A/D converter gain, offset, and linearity are calibrated at the factory. Conversion is initiated (i.e., the analog input signal is sampled) by the rising edge of the clock (CONV) signal. Data corresponding to that sample is available three clock cycles later as shown on the *Timing Diagram*.

Power

The THC1069 requires +5 and –5.2 Volts for operation. V_{CCA} (the positive analog power supply voltage) powers analog front-end and reference circuitry on the THC1069. V_{CCA} should be decoupled to analog ground as shown in the *Typical Interface Circuit*. The two negative power supply voltages (V_{EEA} and V_{EED}) may come from the same power source but should be separately decoupled to reduce power supply noise. Decoupling capacitors of 10µF and 0.1µF should be placed as close to the power pins of the THC1069 as possible. Small value (0.01µF) decoupling capacitors are inside the THC1069 on each power supply input.

Analog and digital grounds (A_{GND} and D_{GND}) are isolated from each other inside the THC1069 to minimize crosstalk and achieve optimum performance. It is recommended that the THC1069 be mounted on printed circuit boards with one solid ground plane used for all ground pins. Analog and digital grounds may be kept separate if required by the system grounding plan; however, the voltage difference between A_{GND} and D_{GND} must be kept LOW (within ±0.1 Volt) and noise at the analog input, A_{IN}, referred to A_{GND} must be kept as small as possible in order to realize optimum performance.

Reference

A precision voltage reference is generated within the THC1069. The V_{REF} output has a nominal voltage of –2.0 Volts and can be used to drive external circuitry that may require a stable voltage reference. A potentiometer connected between V_{REF} and A_{GND} with its wiper connected to A_{OFF} provides a stable method of adjusting input offset voltage of the THC1069. Any external loading on the V_{REF} output should be limited to 5 milliamps.

Analog Input

The input amplifier of the THC1069 has a non-inverting gain of two. When the A_{OFF} input is connected to the OFFSET output, the input amplifier is offset so that its output swings from 0.0 to –2.0 Volts, matching the input range requirements of the internal 9-bit flash A/D converter.

A_{RTN} is the ground reference point for the analog input stage and voltage reference generator. It should be connected to a low-noise ground point. The input impedance of the THC1069 is 1kΩ from A_{IN} to A_{GND}. For impedance matching and lower noise in all applications, a termination resistor or low-impedance driver should be located as close to the A_{IN} pin as possible.

Offset Adjustment

The THC1069 is designed for, and its performance guaranteed for, the ±0.5 Volt input range. This input range results when A_{OFF} is connected to OFFSET. A 1 or 10kΩ potentiometer connected between V_{REF} and A_{GND} with its wiper connected to A_{OFF} will provide a variable DC offset. Decoupling capacitors of 0.1 and 0.01μF should be connected from A_{OFF} to A_{RTN} to reduce noise injection into the THC1069. Both unipolar positive (0.0 to +1.0 Volts) and unipolar negative (0.0 to –1.0 Volts) input ranges are possible by varying the DC voltage applied to A_{OFF}.

The A_{OFF} pin is a high-impedance offset adjustment point for the THC1069. This input is connected directly to a wideband amplifier and may be varied at high rates and even used as an alternate analog signal input. Care must be taken (by proper decoupling) in applications where this pin is used for DC offset control to prevent high-frequency noise from being introduced into the THC1069. The voltage present at the A_{OFF} pin is amplified with a gain of –2.

Analog Output

The A_{OUT} pin allows monitoring of the 0.0 to –2.0 Volt analog signal at the flash converter input and is normally left unconnected. A_{OUT} is isolated from the flash A/D converter input with a series resistor of 470Ω.

CONV

The THC1069 requires a differential ECL clock signal, CONV and $\overline{\text{CONV}}$. The analog signal is sampled at t_{STO} (Sampling Time Offset) after the rising edge of CONV. The nine data and two overflow digital outputs are synchronous with respect to the rising edge of CONV. Data for sample N becomes valid t_D after the rising edge of the N+2 CONV pulse and remains valid until t_{HO} after the rising edge of CONV N+3 as shown on the *Timing Diagram*.

Data Outputs

The data and overflow outputs of the THC1069 are ECL-compatible and their operation is synchronous with respect to CONV. The overflow flags, OVFR and OVF, originates from the internal flash A/D converter of the THC1069. It is synchronous with respect to CONV. OVF goes HIGH whenever the voltage at the input of the THC1069 exceeds the most positive full-scale value. OVFR is a registered OVF signal and emerges from the THC1069 one CONV cycle after OVF.

Do Not Connect

DNC (Do Not Connect) pins are connected to internal test points used in the factory calibration of the THC1069. These pins should be left unconnected.

Package Interconnections

Signal Type	Signal Name	Function	Value	Pin
Power, Ground	V_{CCA}	Positive Analog Supply	+5.0V	1
	V_{EEA}	Negative Analog Supply	–5.2V	27, 29
	V_{EED}	Negative Digital Supply	–5.2V	8, 26
	A_{GND}	Analog Ground	0.0V	2, 28
	D_{GND}	Digital Ground	0.0V	11, 12
Analog Inputs	A_{IN}	Analog Signal Input	±0.5V	31
	A_{RTN}	Analog Input Return	0.0V	32
	A_{OFF}	Input Offset Control	text	30
	RANGE	Range Adjust	open	5
Analog Outputs	V_{REF}	Reference Output	–2.0V	3
	A_{OUT}	Amplifier Monitor Point	0 to –2V	7
	OFFSET	Divider output	+1.0V	4
Digital Inputs	CONV	Convert	ECL	10
	$\overline{CONV}$	Convert complement	ECL	9
Digital Outputs	OVF	Overflow Flag	ECL	13
	OVFR	Registered Overflow Flag	ECL	14
	D1 (MSB)	Most Significant Bit	ECL	25
	D_2		ECL	24
	D_3		ECL	23
	D_4		ECL	22
	D_5		ECL	21
	D_6		ECL	20
	D_7		ECL	19
	D_8		ECL	18
	D_9 (LSB)	Least Significant Bit	ECL	17
Not Used	DNC	Do Not Connect	Open	6, 15, 16

Figure 1. Timing Diagram

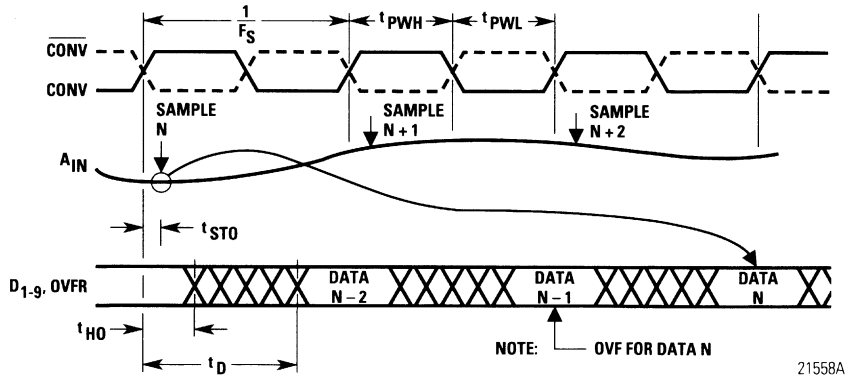


Figure 2. Equivalent V_{REF} Input Circuit

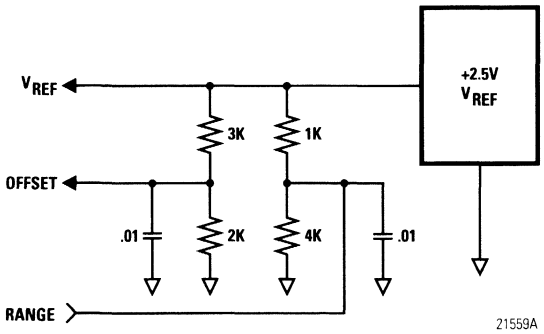


Figure 3. Equivalent Digital Input Circuit

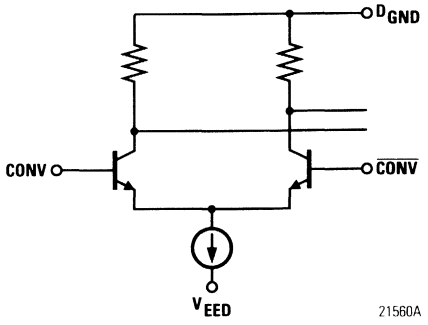
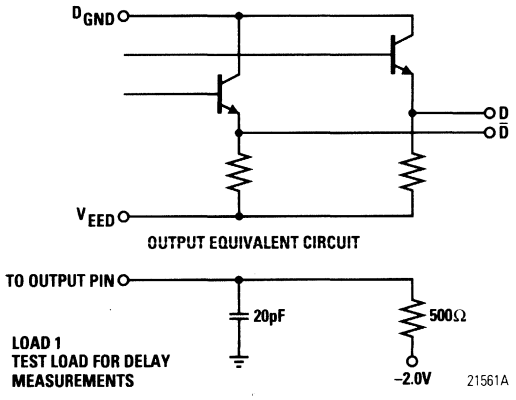


Figure 4. Equivalent Output Circuits



Output Coding

Input Voltage	$D_1 \ldots D_{10}$, MSB LSB	OVF, OVFR
>0.500V	0 0000 0000	1
+0.500V	0 0000 0000	0
+0.498V	0 0000 0001	0
+0.496V	0 0000 0010	0
•	•	
•	•	
+0.004V	1 1111 1110	0
+0.002V	1 1111 1111	0
0.000V	0 0000 0000	0
–0.002V	0 0000 0001	0
–0.004V	0 0000 0010	0
•	•	
•	•	
–0.496V	1 1111 1101	0
–0.498V	1 1111 1110	0
–0.500V	1 1111 1111	0
<–0.5V	1 1111 1111	0

Notes: 1. Input range = ±0.5 Volts.
2. Voltages measured at code centers.

Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltages

V_{CCA} (Measured to A_{GND}) ..... –0.5 to +7.0V
V_{EEA} (Measured to A_{GND}) ..... +0.5 to –7.0V
V_{EED} (Measured to D_{GND}) ..... +0.5 to –7.0V
A_{GND}, A_{RTN} (Measured to D_{GND}) ..... –0.5 to +0.5V

Input Voltages[2]

CONV, $\overline{CONV}$ (Measured to D_{GND}) ..... D_{GND} to V_{EED}
A_{IN} (Measured to A_{GND}) ..... V_{EEA} to V_{CCA}
A_{OFF}, RANGE (Measured to A_{GND}) ..... V_{EEA} to V_{CCA}

Outputs[2,3]

Digital Outputs, Applied Voltage (Measured to D_{GND}) ..... +0.5 to V_{EED}
Digital Outputs, Applied Current, Externally Forced 50mA
Short-Circuit Duration (Single Output to D_{GND}) ..... Unlimited

Temperature

Operating, Case ..... –60 to +135°C
Lead, Soldering (10 Seconds) ..... +300°C
Storage ..... –65 to +150°C

Notes: 1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.

Operating conditions

Parameter		Temperature Range: Industrial Min	Industrial Nom	Industrial Max	Military Min	Military Nom	Military Max	Units
V_{CCA}	Positive Analog Supply Voltage (Measured to A_{GND})	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{EEA}	Negative Analog Supply Voltage (Measured to A_{GND})	–4.9	–5.2	–5.5	–4.9	–5.2	–5.5	V
V_{EED}	Negative Digital Supply Voltage	–4.9	–5.2	–5.5	–4.9	–5.2	–5.5	V
A_{GND}, A_{RTN}	Analog Ground Voltage (Measured to D_{GND})	–0.1	0.0	0.1	–0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width LOW	12			12			ns
t_{PWH}	CONV Pulse Width HIGH	15			15			ns
V_{IL}	CONV, $\overline{CONV}$ Input Voltage			–1.52			–1.52	V
V_{IH}	CONV, $\overline{CONV}$ Input Voltage	–0.99			–0.99			V
V_{RANGE}	Voltage on Pin 5, No Load	1.8	2.0	2.2	1.8	2.0	2.2	V
T_C	Case Temperature	–25		85	–55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Conditions	Temperature Range				Units
			Industrial		Military		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = Max[1]		90		95	mA
$I_{EEA} + I_{EED}$	Negative Supply Current	V_{EEA}, V_{EED} = Max		–1030		–1095	mA
R_{IN}	Analog Input Resistance		980	1020	980	1020	Ohms
C_{IN}	Analog Input Capacitance			5.5		5.5	pF
I_{IL}	Input Current, Logic LOW	V_{EED} = Max, V_{IN} = –1.7V		0.7		0.9	mA
I_{IH}	Input Current, Logic HIGH	V_{EED} = Max, V_{IN} = –0.7V		0.75		0.95	mA
V_{OL}	Output Voltage, Logic LOW	OVFR and D_{1-9} Outputs[1]		–1.575		–1.575	V
		OVF Output[2]		–1.6		–1.5	V
V_{OH}	Output Voltage, Logic HIGH	OVFR and D_{1-9} Outputs[1]	–0.89		–0.89		V
		OVF Output[2]	–0.95		–1.1		V
V_{REF}	2.5V Reference Output Voltage		2.49	2.51	2.44	2.56	V
$V_{1.0V\ OUT}$	1.0V Output Voltage	T_A = 25°C	0.99	1.01	0.99	1.01	V
C_I	Digital Input Capacitance	T_A = 25°C, f = 1MHz		20		20	pF

Note: 1. Standard 10kH ECL test load: 100Ω to –2.0V
2. ECL Test load: 500Ω to –2.0V

Switching characteristics within specified operating conditions

Parameter	Conditions	Temperature Range				Units
		Industrial		Military		
		Min	Max	Min	Max	
F_S	Maximum Conversion Rate	37		37		MSPS
t_{STO}	Sampling Time Offset	–4.5	0.6	–4.5	0.6	ns
t_{DO}	Digital Output Delay[1,2]		10		10	ns
t_{DOVF}	OVF Output Delay[3]		27		27	ns
t_{HO}	Output Hold Time[1,2]	5		5		ns

Note: 1. Standard 10kH ECL test load: 100Ω to –2.0V
2. OVFR and D_{1-9} outputs
3. OVF output, standard ECL test load: 500Ω to –2.0V

System performance characteristics within specified operating conditions

Parameter		Conditions	Temperature Range						Units
			Industrial			Military			
			Min	Typ	Max	Min	Typ	Max	
E_{LI}	Linearity Error, Integral			0.075	0.15		0.075	0.15	%
E_{LD}	Linearity Error, Differential			0.06	0.1		0.06	0.1	%
t_{TR}	Transient Response	Full-Scale		50	65		50	65	ns
t_{OR}	Overload Recovery Time	100% Overange		40	55		40	55	ns
BW_{FS}	–3 dB Bandwidth	V_{IN} = Full-Scale	50	75		50	75		MHz
BW_{SS}	–3 dB Bandwidth	V_{IN} = –20dB	60	85		60	85		MHz
SNR	Signal-to-Noise Ratio,	f_{IN} = 1.0MHz	53	54		52	54		dB
		f_{IN} = 5.0MHz	52.5	53.5		51.5	53.5		dB
		f_{IN} = 10.0MHz	52	53		51	53		dB
THD	Total Harmonic Distortion	f_{IN} = 1.0MHz		–58	–51		–58	–51	dBc
		f_{IN} = 5.0MHz		–48	–46		–48	–44	dBc
		f_{IN} = 10.0MHz		–44	–41		–44	–39.5	dBc
SINAD	Signal-to-Noise and Distortion	f_{IN} = 1.0MHz	49	52		49	52		dB
		f_{IN} = 5.0MHz	45	47.5		43	47.5		dB
		f_{IN} = 10.0MHz	40.5	43		39	43		dB
E_{AP}	Aperture Error				50			50	ps
DP	Differential Phase	f_S = 14.3 MHz		0.3	0.5		0.3		°
DG	Differential Gain	f_S = 14.3 MHz		1.0	1.5		1.0		%

Typical Interface Circuit

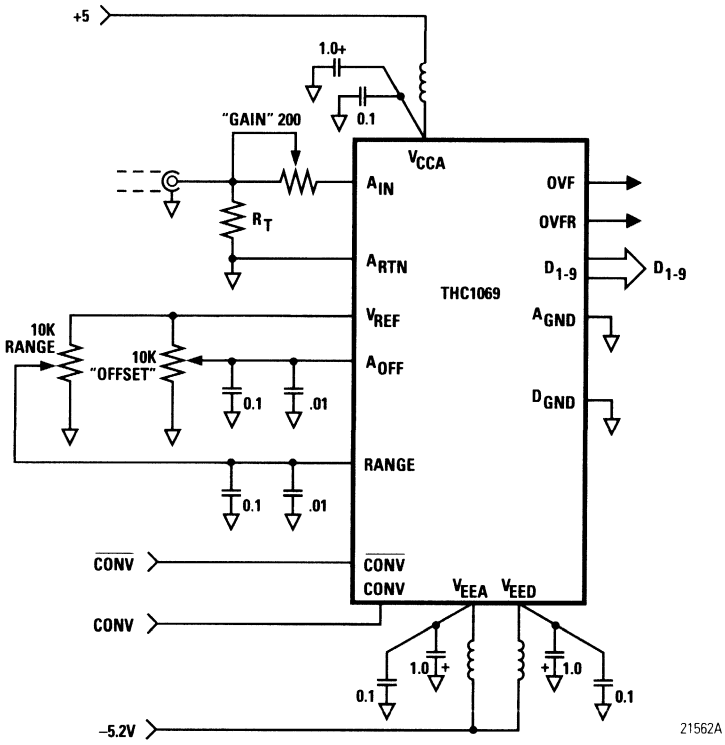
The THC1069 has a user-adjustable reference voltages. This reference voltage is laser-trimmed during the manufacturing process to optimize DC performance and may be adjusted by an external potentiometer. The external 10kΩ potentiometer, connected between V_{REF} and A_{GND} with wiper driving the RANGE pin, varies the reference voltage to the internal A/D converter. The effect is a change in the A/D converter "gain."

Should the system design require a signal gain adjustment, a 200Ω variable resistor in series with the input signal may be used. When the 200Ω potentiometer is centered, the attenuation is approximately –0.8dB and an adjustment range of ±0.8 dB is available. This corresponds to a ±10% adjustment range for gain. With R_T = 52.4Ω, the total terminating impedance varies from 49.8 to 50.2Ω as the potentiometer is varied from one end to the other. With R_T = 80.5Ω, the total terminating impedance varies from 74.5 to 75.4Ω as the potentiometer is varied from one end to the other. If an amplifier drives the THC1069 instead of a coaxial cable, no R_T is required. Both methods of gain adjustment are shown in the Typical Interface Circuit.

Offset adjustment is also illustrated in the Typical Interface circuit. Here, a 10kΩ potentiometer connected between V_{REF} and A_{GND} with wiper driving the A_{OFF} pin gives ±1 Volt of offset adjustment range.

Careful attention should be paid to power supply decoupling as shown. The use of ferrite beads to aid power supply noise rejection is optional.

Typical Interface Circuit



Evaluation Board

The THC1069E1C is a Eurocard-style printed circuit board designed to optimize the performance of, and to aid in the evaluation of, the THC1069 A/D converter. The board dimensions are 100mm x 160mm with a standard 64-pin double-row DIN male connector installed. A complementary 64-pin double-row DIN female connector is included with the board. The circuitry on the board includes the THC1069 A/D converter, a TDC1112 12-bit D/A converter, provision for an optional THC4940 Track/Hold amplifier and timing generator for generation to the Track/Hold pulse for the THC4940.

The board employs only two conducting sides. Most of the circuit interconnections are on the bottom of the board while the top is mostly solid ground plane. SMA connectors are installed on the board to facilitate analog I/O and clocks. The board is calibrated and tested at the factory and is supplied complete with THC1069, TDC1112 and timing generator components installed.

Power and Ground

Only two power supply voltages are required for the operation of the THC1069E1C when no Track/Hold is used: V_{CC} = +5, V_{EE} = –5.2 Volts. When the optional THC4940 is installed, two additional power supplies are required: V+ = +15 and V– = –15 Volts. All power inputs are decoupled to a single solid ground plane, GND. All GND pins of the board are connected to the ground plane and it is recommended that all GND pins be used.

A/D Converter Inputs

The clocks to the THC1069, CONV and $\overline{\text{CONV}}$ come from the timing generator section of the board. The input to the timing generator is normally brought onto the board through the SMA connector labeled "CONV." By installing jumper J1, differential CONV and $\overline{\text{CONV}}$ signals are routed through the edge connector on pins A2 and B2. Terminating resistors, R32 and R33 are installed on the board for terminating the single-ended CONV SMA input.

Terminating resistors, R27, R28 and R29 are installed on the board for terminating the differential CONV inputs from the edge-connector. The timing generator provides proper levels and pulse widths to both the THC1069 A/D converter and the optional THC4940 Track/Hold amplifier.

The analog signal input to the THC1069E1C is brought onto the board by way of the SMA connector labeled "A/D A_{IN}." A terminating resistor, R19, is included on the board for terminating the analog input signal cable.

The AOUT SMA location allow monitoring of the analog signal within the THC1069 just prior to the internal flash A/D converter. The gain and offset of the THC1069 can be adjusted by turning all three DIP switches to their ON position and using the GAIN and OFFSET potentiometers, R47 and R48.

A/D Converter Data Outputs and D/A Converter Data Inputs

The nine data outputs of the THC1069 are brought to edge-connector pins B3 through B11. These pins are located directly across the edge-connector from the corresponding data inputs of the TDC1112 D/A converter.

D/A Converter Inputs

The clock to the TDC1112, CLK, is normally brought onto the board through an SMA connector labeled "CLK" near pin 16 of the TDC1112. The clock input to the TDC1112 is also brought to the edge-connector pin B24. Resistors, R7 and R8, provide a Thevenin equivalent 130Ω termination for the CONV signal. R5 and R6 bias the $\overline{\text{CONV}}$ input to the TDC1112 near the ECL threshold level.

D/A converter outputs are brought to SMA connectors labeled OUT+ and OUT– as well as edge-connector pins B27 and B26. Load resistors of 51.1Ω are provided on the board to facilitate 50Ω cable connection to the board.

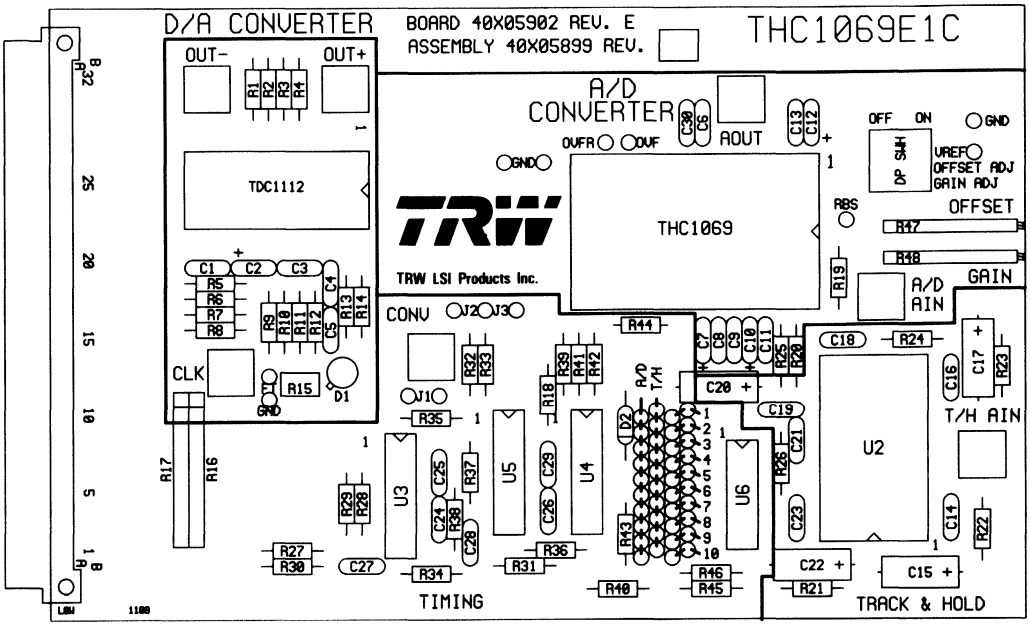
Potentiometer R11 is used to adjust the reference voltage to the TDC1112. This voltage is adjusted to –1.0V as part of the factory test and calibration procedure.

Placing a jumper in the location labeled "FT" will put the TDC1112 into feedthru (unclocked) mode. This eliminates the requirement for a D/A clock signal, but will degrade the fidelity of the TDC1112 reconstruction signal.

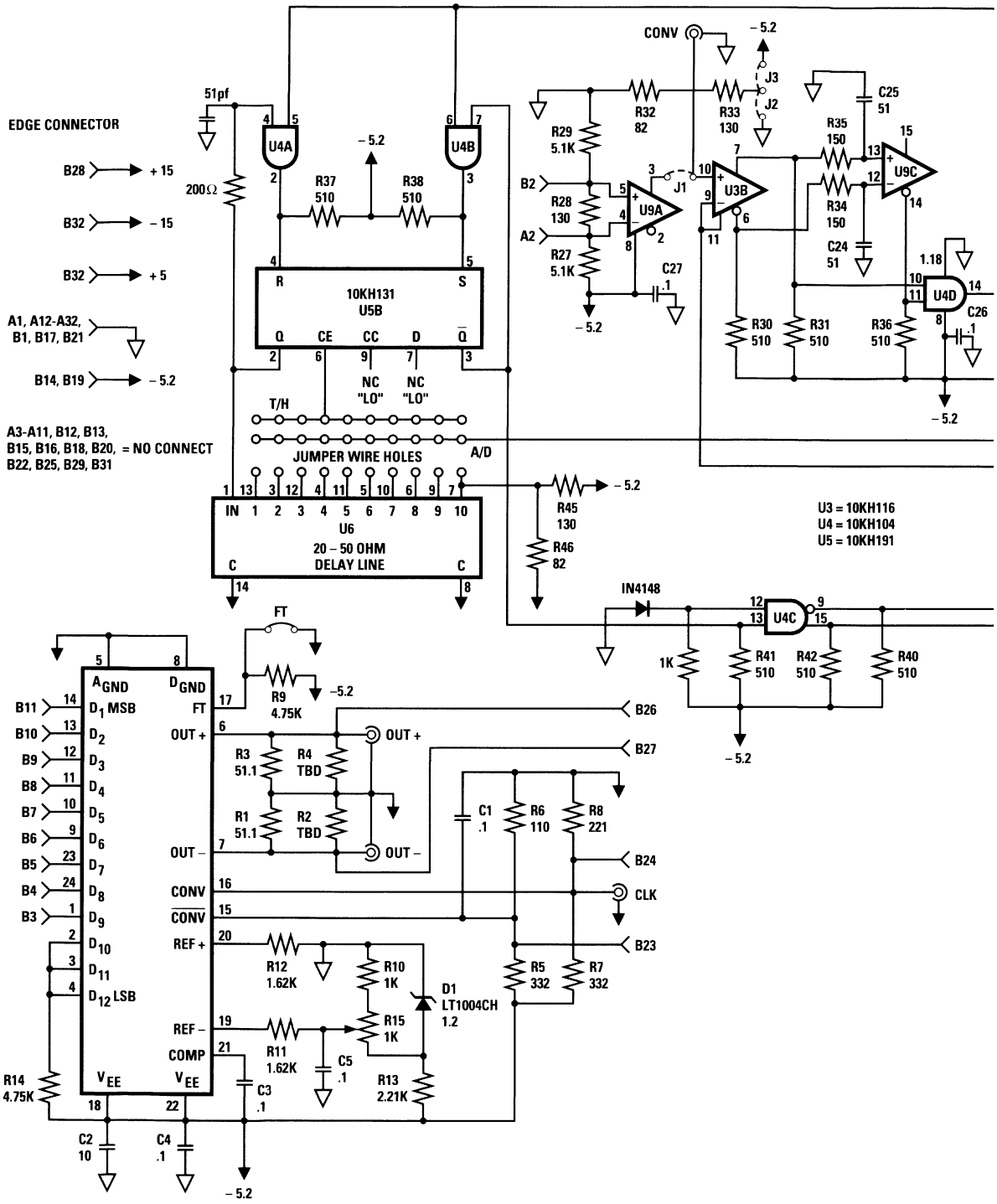
THC4940 Track/Hold Amplifier Option

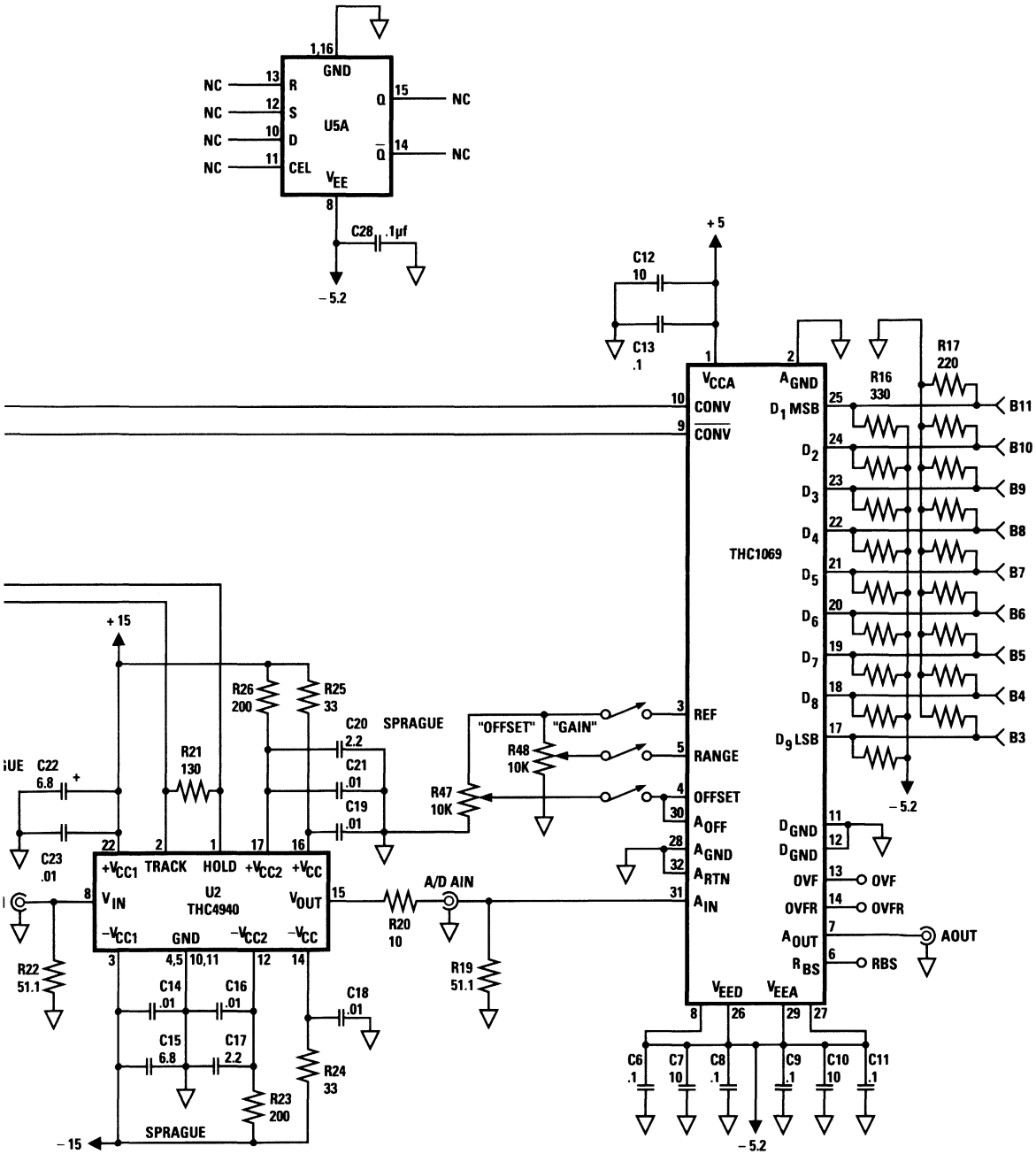
A THC4940 may be added to the THC1069E1C just prior to the THC1069 A/D converter. When the THC4940 is used, +15 and –15 Volt power supplies are required on edge-connector pins B28 and B32 respectively. The analog signal input is connected to the SMA labeled "T/H AIN" which has a terminating resistor R22. When the THC4940 is used, terminating resistor R19 should be removed.

THC1069E1C Silkscreen Layout



THC1069E1C A/D Converter Schematic Diagram




1,16
GND
NC
13
R
NC
12
S
NC
10
D
NC
11
CEL
U5A
15
Q
NC
14
Q
NC
VEE
8
C28 .1µf
-5.2
+5
C12
10
C13
.1
1
VCCA
2
AGND
10
CONV
9
CONV
R17
220
R16
330
25
D1 MSB
B11
24
D2
B10
23
D3
B9
22
D4
B8
THC1069
21
D5
B7
20
D6
B6
19
D7
B5
18
D8
B4
17
D9 LSB
B3
-5.2
+15
R26
200
R25
33
C20
2.2
SPRAGE
C21
.01
C19
.01
"OFFSET"
"GAIN"
R48
10K
R47
10K
3
REF
5
RANGE
4
OFFSET
30
AOFF
28
AGND
32
ARTN
31
AIN
11
DGND
12
DGND
13
OVF
OVF
14
OVFR
OVFR
7
AOUT
AOUT
6
RBS
RBS
R21
130
C22
6.8
C23
.01
22
2
1
17
16
+VCC1
TRACK
HOLD
+VCC2
+VCC
8
VIN
U2
THC4940
VOUT
15
-VCC1
GND
-VCC2
-VCC
3
4,5
10,11
12
14
A/D AIN
R20
10
R22
51.1
R19
51.1
C14
.01
C16
.01
C18
.01
C15
6.8
C17
2.2
R24
33
R23
200
SPRAGUE
-15
VEED
VEEA
8
26
29
27
C6
.1
C7
10
C8
.1
C9
.1
C10
10
C11
.1
-5.2

Evaluation Board Pin Assignments

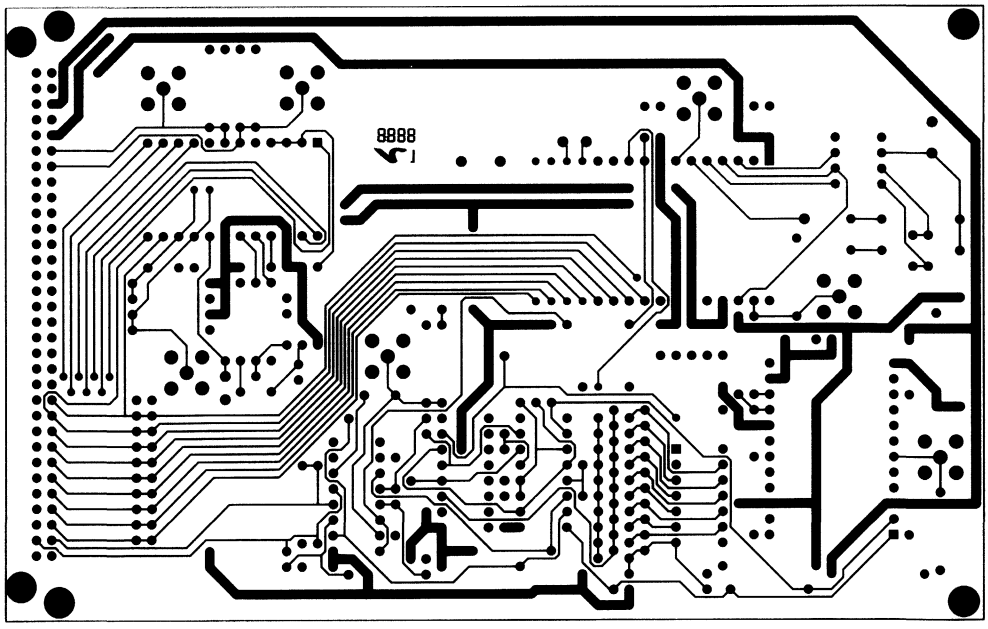
GND	A32	B32	V_{CC} (+5V)
GND	A31	B31	N/C
GND	A30	B30	V– (–15V)
GND	A29	B29	N/C
GND	A28	B28	V+ (+15V)
GND	A27	B27	D/A OUT–
GND	A26	B26	D/A OUT+
GND	A25	B25	N/C
GND	A24	B24	D/A CONV
GND	A23	B23	D/A $\overline{\text{CONV}}$
GND	A22	B22	N/C
GND	A21	B21	GND
GND	A20	B20	N/C
GND	A19	B19	V_{EE} (–5.2V)
GND	A18	B18	N/C
GND	A17	B17	GND
GND	A16	B16	N/C
GND	A15	B15	N/C
GND	A14	B14	V_{EE} (–5.2V)
GND	A13	B13	N/C
GND	A12	B12	N/C
D/A D_1 MSB	A11	B11	A/D D_1 MSB
D/A D2	A10	B10	A/D D_2
D/A D3	A9	B9	A/D D_3
D/A D4	A8	B8	A/D D_4
D/A D5	A7	B7	A/D D_5
D/A D6	A6	B6	A/D D_6
D/A D7	A5	B5	A/D D_7
D/A D8	A4	B4	A/D D_8
D/A D_8 LSB	A3	B3	A/D D_9 LSB
A/D $\overline{\text{CONV}}$	A2	B2	A/D CONV
GND	A1	B1	GND

Mating Connectors for THC1069E1C

AMP	532507-2	Wire-wrap
AMP	532507-1	Solder tail
Robinson-Nugent	RNE-64BS-W-TG30	Wire-wrap
Robinson-Nugent	RNE-64BS-S-TG30	Solder tail
Souriau	8609-264-6115-7550E1	Wire-wrap
Souriau	8609-264-6114-7550E1	Solder tail
Souriau	8609-264-6813-7550E1	Solder tail, right-angle bend

THC1069E1C component side layout

THC1069E1C circuit side layout



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
THC1069S5B	IND - T_C = –25°C to 85°C	Industrial	32 Pin Metal DIP	THC1069S5B
THC1069S5V	EXT - T_C = –55°C to 125°C	MIL-STD-883	32 Pin Metal DIP	THC1069S5V
THC1069E1C	STD - T_A = 0°C to 70°C	–	Eurocard PC Board	THC1069E1C

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THC1070

Complete High-Speed A/D Converter
10-Bit, 25 Msps

The TRW THC1070 is a complete analog-to-digital converter that combines all the circuitry required to convert high-speed analog signals into 10-bit digital data at rates up to 25 Msps (Megasamples per second). The THC1070 comprises a wideband input amplifier stage, voltage references, and 10-bit flash A/D converter, which make the THC1070 very easy to use. The THC1070 offers precision gain, linearity and offset performance.

The THC1070 is housed in a 32-pin hermetic package with guaranteed performance over the industrial (–25 to 85°C) or military (–55 to 125°C) case temperature ranges. Military THC1070s are manufactured in compliance with MIL-STD-883C in facilities certified and qualified to MIL-STD-1772.

Features:

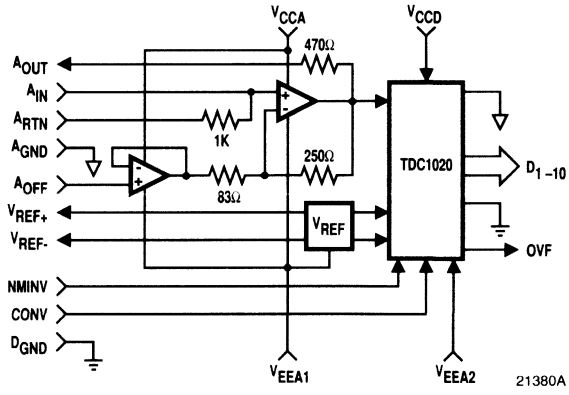
- 20 Msps Conversion Rate, Guaranteed
- Guaranteed Performance Over All Operating Conditions
- Complete Analog Front-End
- Requires Only +5 And –5.2 Volt Power Supplies
- ±0.5 Volt Input Range
- Input Capacitance Less Than 5.5pF
- Offset Externally Adjustable
- Outstanding Overload Recovery
- TTL Compatible
- Overflow Output Flag
- Industrial Or Military Temperature Range
- 32-Pin Hermetic Package

Applications

- Broadcast And Studio Video
- Medical Imaging
- Magnetic Resonance Signal Acquisition
- Radar
- Digital Oscilloscopes
- Spectrum Analysis

A

Functional Block Diagram

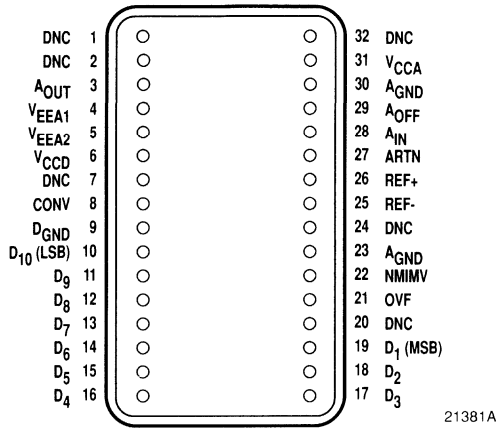


TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

40G06204 Rev. B – 8/90
Printed in the U.S.A.

Pin Assignments



32 Pin Hermetic DIP – S5 Package

Functional Description

The THC1070 is a complete 10-bit A/D converter in a hermetically sealed 32-pin package. It has three major functional sections: Wideband input amplifier stage, voltage reference generators, and a monolithic 10-bit flash A/D converter.

Conversion is initiated (i.e. the analog input signal is sampled) by the rising edge of the clock (CONV) signal. Data corresponding to that sample is available two clock cycles later. The output format is user-selectable between binary and two's-complement.

Power

The THC1070 requires +5 and –5.2 Volts for operation. VCC_D (the positive digital supply voltage) and V_{CCA} (the positive analog supply voltage) may be from the same power source but should be decoupled to ground separately as shown in the *Typical Interface Circuit*. The two negative analog supply voltages (V_{EEA1} and V_{EEA2}) may also be from the same power source but also should be separately decoupled. Decoupling capacitors of 10µF and 0.1µF should be placed as close to the power pins of the THC1070 as possible. Small value (0.01µF) decoupling capacitors are inside the THC1070 on each power supply input.

Analog and digital grounds are isolated from each other inside the THC1070 to minimize crosstalk and achieve optimum performance. It is recommended that the THC1070 be mounted on printed circuit boards with one solid ground plane used for all ground pins of the THC1070. Analog and digital grounds may be kept separate if required by the system grounding plan, however, the voltage difference between A_{GND} and D_{GND} must be kept low (within ±0.1 Volts).

Reference

A precision voltage reference is generated within the THC1070. The V_{REF+} and V_{REF-} outputs have nominal voltages of +2.0 and –2.0 Volts respectively, and can be used to drive external circuitry that may require a stable voltage reference. A potentiometer connected between these terminals with its wiper connected to the A_{OFF} pin provides a stable method of adjusting input offset voltage.

Analog Input

The input amplifier of the THC1070 has a non-inverting gain of +4 to match the ±0.5 input range to the ±2 Volt range required by the internal 10-bit flash A/D converter. An offset adjustment pin, A_{OFF}, is provided for easy adjustment of the input to accommodate any 1.0 Volt peak-to-peak input range within a –2.0 to +2.0 Volt window. A_{RTN} is the ground reference point for the analog input stage and voltage reference generator. It should be connected to a low-noise ground point. The input impedance of the THC1070 is 1kΩ from A_{IN} to ground. For impedance matching and lower noise in all applications, a termination resistor should be located as close to the A_{IN} pin as possible.

Offset Adjustment

The THC1070 is designed for, and its performance guaranteed for, the ±0.5 Volt input range. It can easily be configured to operate with any other 1.0 Volt peak-to-peak input signal in the range from +2.0 to –2.0 Volts by driving the A_{OFF} input. Both unipolar positive (0.0 to +1.0 Volts) and unipolar negative (0.0 to –1.0 Volts) input ranges are possible.

The A_{OFF} pin provides a high-impedance offset adjustment point for the THC1070. Since this offset input is wideband, the offset may be varied at high rates and even used as an alternate analog signal input. Care must be taken (by proper decoupling) in applications where this pin is used to inject a DC offset to prevent high-frequency noise from being introduced into the THC1070. The voltage present at the A_{OFF} pin is amplified with a gain of –3.

For normal ±0.5 Volt input operation, connect A_{OFF} to A_{GND}. For an analog voltage range of 0.0 to –1.0 Volts, connect A_{OFF} to –0.667 Volts; for 0.0 to +1.0V, connect A_{OFF} to +0.667V. A 10KΩ potentiometer connected between V_{REF+} and V_{REF-} with its wiper connected to A_{OFF} will provide a variable DC offset. Decoupling capacitors of 0.1 and 0.01μF should be connected from A_{OFF} to A_{RTN} to reduce noise injection into the THC1070.

Analog Output

The A_{OUT} pin allows monitoring of the ±2.0 Volt analog signal at the flash converter input and is normally left unconnected. A_{OUT} is isolated from the flash A/D converter input with a series resistor of 470Ω.

CONVert

The THC1070 requires a TTL clock signal, CONV. The analog signal is sampled at t_{STO} (Sampling Time Offset) after the rising edge of CONV. The ten binary and 1 overflow digital outputs becomes valid after the next rising edge of CONV. Data for sample N becomes valid t_D after the rising edge of the N+1 CONV edge and remains valid until t_{HO} after the rising edge of CONV N+2 as shown on the *Timing Diagram*.

Output Format

The NMINV (Not MSB INVert) control allows the inversion of the MSB to provide either binary or two's complement output formats. The THC1070 contains a 5kΩ pull-up resistor for NMINV. The NLINV input of the internal flash A/D converter is HIGH and is not available to the user. The OVF output is not affected by the NMINV state.

Overflow

The overflow flag, OVF, originates from the internal flash A/D converter of the THC1070. It is synchronous with respect to CONV. OVF goes HIGH whenever the voltage at the input of the THC1070 exceeds the most positive full-scale value.

Data Outputs

The data and overflow outputs of the THC1070 are TTL compatible and are capable of driving four low-power Schottky TTL loads. Their operation is synchronous with respect to CONV.

Do Not Connect

DNC (Do Not Connect) pins are connected to internal test points used in the factory calibration of the THC1070. These pins should be left unconnected.

Package Interconnections

Signal Type	Signal Name	Function	Value	Pin
Power	V_{EEA1}	Negative Analog Supply	–5.2V	4
	V_{EEA2}	Negative Analog Supply	–5.2V	5
	V_{CCD}	Positive Digital Supply	+5.0V	6
	V_{CCA}	Positive Analog Supply	+5.0V	31
	A_{GND}	Analog Ground	0.0V	23, 30
	D_{GND}	Digital Ground	0.0V	9
Reference	V_{REF+}	Positive Reference Output	+2.0V	26
	V_{REF-}	Negative Reference Output	–2.0V	25
Analog Input	A_{IN}	Analog Input	±0.5V	28
	A_{RTN}	Analog Input Return	0.0V	27
Offset Adjust	A_{OFF}	Input Offset Control	0.0V	29
Analog Output	A_{OUT}	Amplifier Monitor Point	±2.0V	3
Clock	CONV	Convert	TTL	8
Format Control	NMINV	Format Control	TTL	22
Overflow	OVF	Overflow Flag	TTL	21
Data Output	D_1 (MSB)	Most Significant Bit	TTL	19
	D_2		TTL	18
	D_3		TTL	17
	D_4		TTL	16
	D_5		TTL	15
	D_6		TTL	14
	D_7		TTL	13
	D_8		TTL	12
	D_9		TTL	11
	D_{10} (LSB)	Least Significant Bit	TTL	10
Not Used	DNC	Do Not Connect	Open	1,2,7,20,24,32

Figure 1. Timing Diagram

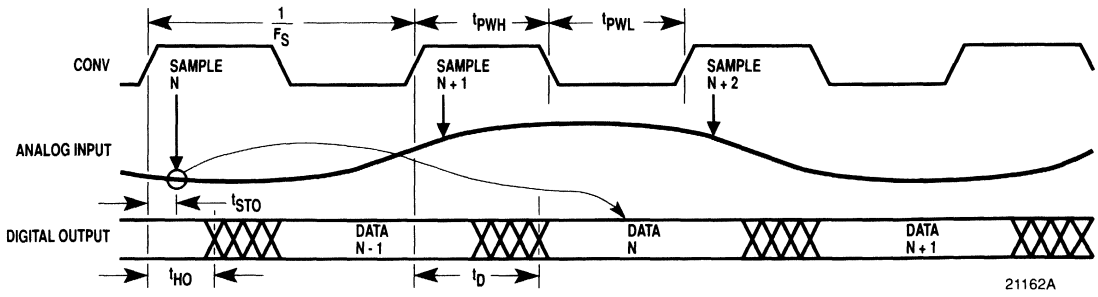


Figure 2. Equivalent Analog Input Circuit

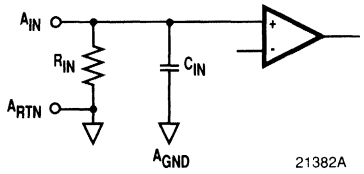


Figure 3. Equivalent Digital Input Circuit

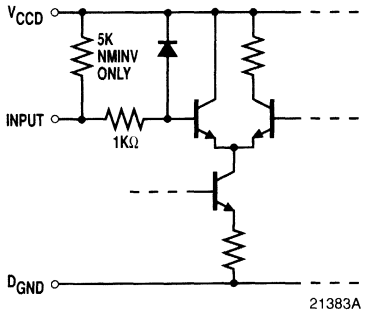
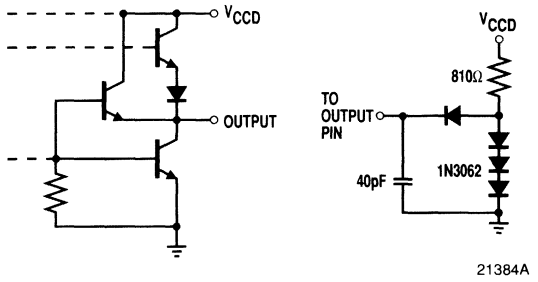


Figure 4. Equivalent Output Circuits



Output Coding Table

Input Voltage	Binary NMINV = HIGH D1 ..... D10, MSB LSB	OVF	Two's Complement NMINV = LOW D1 ..... D10, MSB LSB	OVF
>0.500V	00 0000 0000	1	10 0000 0000	1
+0.500V	00 0000 0000	0	10 0000 0000	0
+0.499V	00 0000 0001	0	10 0000 0001	0
•	•		•	
•	•		•	
•	•		•	
+0.001V	01 1111 1111	0	11 1111 1111	0
0.000V	10 0000 0000	0	00 0000 0000	0
-0.001V	10 0000 0001	0	00 0000 0001	0
•	•		•	
•	•		•	
•	•		•	
–0.499V	11 1111 1110	0	01 1111 1110	0
–0.500V	11 1111 1111	0	01 1111 1111	0
<–0.5V	11 1111 1111	0	01 1111 1111	0

Notes: 1. Input range = ±0.5 Volts.
2. Voltages measured at code centers.

Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltages

V_{CC} (Measured to D_{GND}) ..... –0.5 to +7.0V
V_{EEA1}, V_{EEA2} (Measured to A_{GND}) ..... +0.5 to –7.0V
A_{GND} (Measured to D_{GND}) ..... –0.5 to +0.5V

Input Voltages[2]

CONV, NMINV (Measured to D_{GND}) ..... V_{CC} to –0.5V
A_{IN} (Measured to A_{GND}) ..... V_{EE} to V_{CC}
A_{OFF} (Measured to A_{GND}) ..... V_{EE} to V_{CC}

Outputs[2,3]

Digital Outputs, Applied Voltage(Measured to DGN_D) ..... –0.5 to V_{CC}
Digital Outputs, Applied Current, Externally Forced 50mA
Short-Circuit Duration (Single Output to GND) ..... Unlimited

Temperature

Operating, Case ..... –60 to +135°C
Lead, Soldering (10 Seconds) ..... +300°C
Storage ..... –65 to +150°C

Notes: 1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.

Operating conditions

Parameter		Temperature Range: Industrial Min	Industrial Nom	Industrial Max	Extended Min	Extended Nom	Extended Max	Units
V_{CCA}, V_{CCD}	Positive Power Supply Voltages	4.75	5.0	5.25	4.75	5.0	5.5	V
V_{EEA}, V_{EED}	Negative Power Supply Voltage	–4.9	–5.2	–5.5	–4.9	–5.2	–5.5	V
A_{GND}, A_{RTN}	Analog Ground Voltage	–0.1	0.0	0.1	–0.1	0.0	0.1	V
V_{CCA}-V_{CCD}	Power Supply Voltage Differential	–0.1	0.0	0.1	–0.1	0.0	0.1	V
V_{EEA}-V_{EED}	Power Supply Voltage Differential	–0.1	0.0	0.1	–0.1	0.0	0.1	V
V_{EEA1}-V_{EEA2}	Power Supply Voltage Differential	–0.1	0.0	0.1	–0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	22			22			ns
t_{PWH}	CONV Pulse Width, HIGH	18			18			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.4			2.4			V
V_{IN}	Input Voltage Range		±0.5			±0.5		V
	(A_{OFF} = A_{GND})							
T_C	Case Temperature	–25		85	–55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Industrial Min	Industrial Max	Extended Min	Extended Max	Units
I_{CC}	Total Positive Supply Current	V_{CC} = Max		930		975	mA
I_{EE}	Total Negative Supply Current	V_{EE} = Max		–550		–600	mA
R_{IN}	Analog Input Resistance	A_{RTN} Grounded	980	1020	980	1020	Ω
C_{IN}	Analog Input Capacitance			5.5		5.5	pF
V_{OS}	Offset Voltage		-.01	.01	–.01	.01	V
V_{OL}	Output Voltage, Logic LOW			0.5		0.5	V
VOH	Output Voltage, Logic HIGH		2.4		2.4		V
V_{REF+}	Reference Voltage Positive		+1.8	+2.2	+1.8	+2.2	V
V_{REF-}	Reference Voltage Negative		–1.8	–2.2	–1.8	–2.2	V
CI	Digital Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
IOS	Short Circuit Output Current	V_{CC} = Max, Outputs HIGH, One Pin Shorted to Ground, One Second Duration		–40		–50	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.5V,					
		NMINV		–1.2		–1.2	mA
		CONV		200		200	µA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V,					
		NMINV		0		0	A
		CONV		50		50	µA

Switching characteristics within specified operating conditions

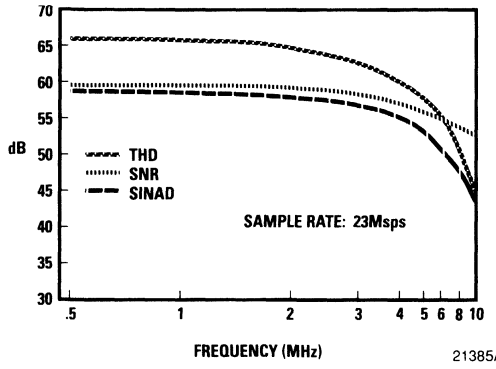
Parameter		Test Conditions	Temperature Range				Units
			Industrial		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{EE} = Min,V_{CC} = Max	25		25		Msps
t_{STO}	Sampling Time Offset	V_{EE} = Min,V_{CC} = Max	–5	10	–5	10	ns
t_D	Digital Output Delay	V_{EE} = Min,V_{CC} = Max		37		37	ns
t_{HO}	Output Hold Time	V_{EE} = Min,V_{CC} = Max	5		5		ns

System performance characteristics within specified operating conditions

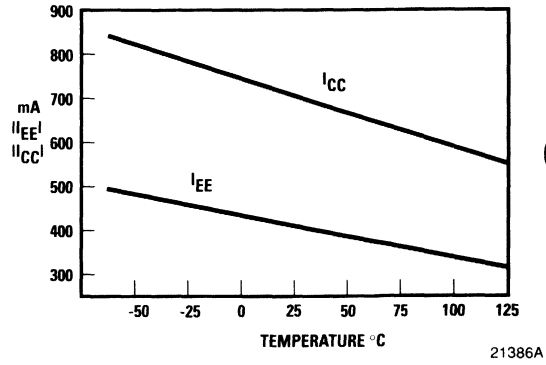
Parameter		Test Conditions	Temperature Range						Units
			Industrial			Extended			
			Min	Typ	Max	Min	Typ	Max	
E_G	Absolute Gain Error				2			2	%
E_{LI}	Linearity, Integral			0.08	0.2		0.08	0.3	%
E_{LD}	Linearity, Differential			0.05	0.1		0.05	0.1	%
t_{TR}	Transient Response	Full-Scale		50	80		50	80	ns
t_{OR}	Overload Recovery Time	100% Overange		35	60		35	60	ns
BW_{FS}	–3dB Bandwidth	Full-Scale Input	30	35		30	35		MHz
BW_{SS}	–3dB Bandwidth	–20dB F_S Input	40	45		40	45		MHz
SNR	Signal-to-Noise Ratio, F_S = 21Msps	1.0MHz	59	59.5		58	59.5		dB
		2.0MHz	57	59		57	59		dB
		5.0MHz	55	56.5		54	56.5		dB
		8.0MHz	53	55.5		52	55.5		dB
		10.0MHz	51	53		50	53		dB
THD	Total Harmonic Distortion F_S = 21Msps	1.0MHz		–65	–52		–65	–49	dBc
		2.0MHz		–63	–51		–63	–48	dBc
		5.0MHz		–57	–48		–57	–46	dBc
		8.0MHz		–51	–44		–51	–40	dBc
		10.0MHz		–46	–40		–46	–36	dBc
SINAD	SNR + Distortion F_S = 21Msps	1.0MHz	51	58		48	58		dB
		2.0MHz	50.5	57		47.5	57		dB
		5.0MHz	47	53.5		45	53.5		dB
		8.0MHz	44	49		39.5	49		dB
		10.0MHz	39.5	45		35.5	45		dB
E_{AP}	Aperture Error			50				50	ps
DP	Differential Phase	F_S = 4 x NTSC SC		0.3	0.5		0.3	0.5	°
DG	Differential Gain	F_S = 4 x NTSC SC		0.8	1.0		0.8	2.0	%

Typical Performance Curves

A. SNR, THD, and SINAD vs. Input Frequency

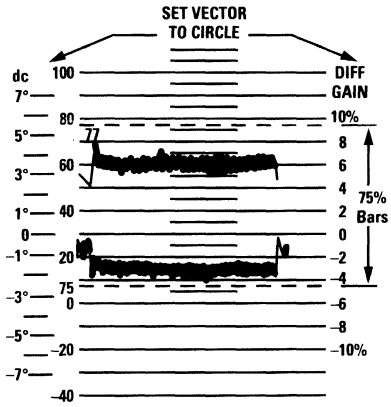


B. Power Supply Current vs. Temperature



A

C. Differential Gain and Differential Phase

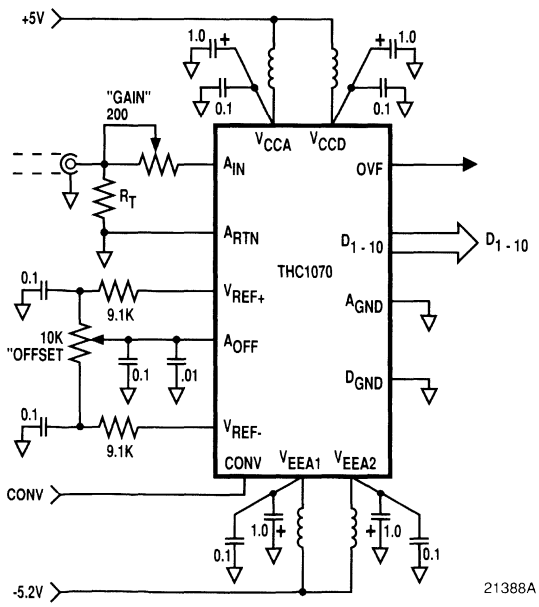


Typical Interface Circuit

The THC1070 does not have user-adjustable reference voltages. The reference voltages of the THC1070 are laser-trimmed during the manufacturing process to optimize dynamic performance. Should the system design requires a "gain" adjustment for the THC1070, this must be done in the signal path prior to the A_{IN} terminal. The *Typical Interface Circuit* uses a 200Ω variable resistor in series with the input to the THC1070. When the potentiometer is centered, the attenuation is approximately -0.8dB and an adjustment range of ±0.8dB is available. This corresponds to a ±10% adjustment range for gain. With R_T = 52.4Ω, the total terminating impedance varies from 49.8 to 50.2Ω as the potentiometer is varied from one end to the other. With R_T = 80.5Ω, the total terminating impedance varies from 74.5 to 75.4Ω as the potentiometer is varied from one end to the other. If an amplifier drives the THC1070 instead of a coaxial cable, no R_T is required.

Offset adjustment is also illustrated in the *Typical Interface Circuit*. Here, a voltage divider network comprising two fixed resistors of 9.1 kΩ and a 10kΩ potentiometer with wiper driving the A_{OFF} pin of the THC1070. This circuit provides a ±1 Volt adjustment range for offset.

Typical Interface Circuit



Careful attention should be paid to power supply decoupling as shown. The use of ferrite beads to aid power supply noise rejection is optional.

Evaluation Board

The THC1070E1C is a Eurocard-style printed circuit board designed to optimize the performance of, and to aid in the evaluation of, the THC1070 A/D converter. The board dimensions are 100 mm x 160 mm with a standard 64-pin double-row DIN male connector installed. A complementary 64-pin double-row DIN female connector is included with the board. The circuitry on the board includes the THC1070 A/D converter, a TDC1012 12-bit D/A converter, provision for an optional THC4940 Track/Hold amplifier and timing generator for generation to the Track/Hold pulse for the THC4940.

The board employs only two conducting sides. Most of the circuit interconnections are on the bottom of the board while the top is mostly solid ground plane. SMA connectors are installed on the board to facilitate analog I/O and clocks. The board is calibrated and tested at the factory and is supplied complete with THC1070, TDC1012 and timing generator components installed.

Power and Ground

Only two power supply voltages are required for the operation of the THC1070E1C when no Track/Hold is used: V_{CC} = +5, V_{EE} = –5.2 Volts. When the optional THC4940 is installed, two additional power supplies are required: V+ = +15 and V– = –15 Volts. All power inputs are decoupled to a single solid ground plane, GND. All GND pins of the board are connected to the ground plane and it is recommended that all GND pins be used.

A/D Converter Inputs

The clock to the THC1070, CONV, comes from the timing generator section of the board. The input to the timing generator is brought onto the board through the SMA connector labeled "CONV."By installing jumper J1, CONV is routed through the edge connector on pin B2. Terminating resistor, R24 (with J2) is available on the board for terminating the CONV input. The timing generator provides proper levels and pulse widths to both the THC1070 A/D converter and the optional THC4940 Track/Hold amplifier.

The analog signal input to the THC1070E1C is brought onto the board by way of the SMA connector labeled "A/D A_{IN}."A terminating resistor, R14, is included on the board for terminating the analog input signal.

The A_{OUT} SMA location allows monitoring of the analog signal within the THC1070 just prior to the internal flash A/D converter. The offset of the THC1070 can be adjusted by turning DIP switches #2, #3, and #4 ON and switch #1 OFF and using the OFFSET potentiometer, R13. DIP switch positions #5 and #6 control the OE\ and NMINV inputs to the THC1070.

A/D Converter Data Outputs and D/A Converter Data Inputs

The ten data outputs of the THC1070 are brought to edge-connector pins B11 through B21 (excluding B18). These pins are located directly across the edge-connector from the corresponding data inputs of the TDC1012 D/A converter.

D/A Converter Inputs

The clock to the TDC1012, CLK, is normally brought onto the board through an SMA connector labeled "CLK" near pin 16 of the TDC1012. The clock input to the TDC1012 is also brought to the edge-connector pin B24. Resistor R6 can be used toterminate the D/A CLK signal.

D/A converter outputs are brought to SMA connectors labeled "OUT+" and "OUT–" as well as edge-connector pins B27 and B26. Load resistors of 51.1Ω are provided on the board to facilitate 50Ω cable connection to the board.

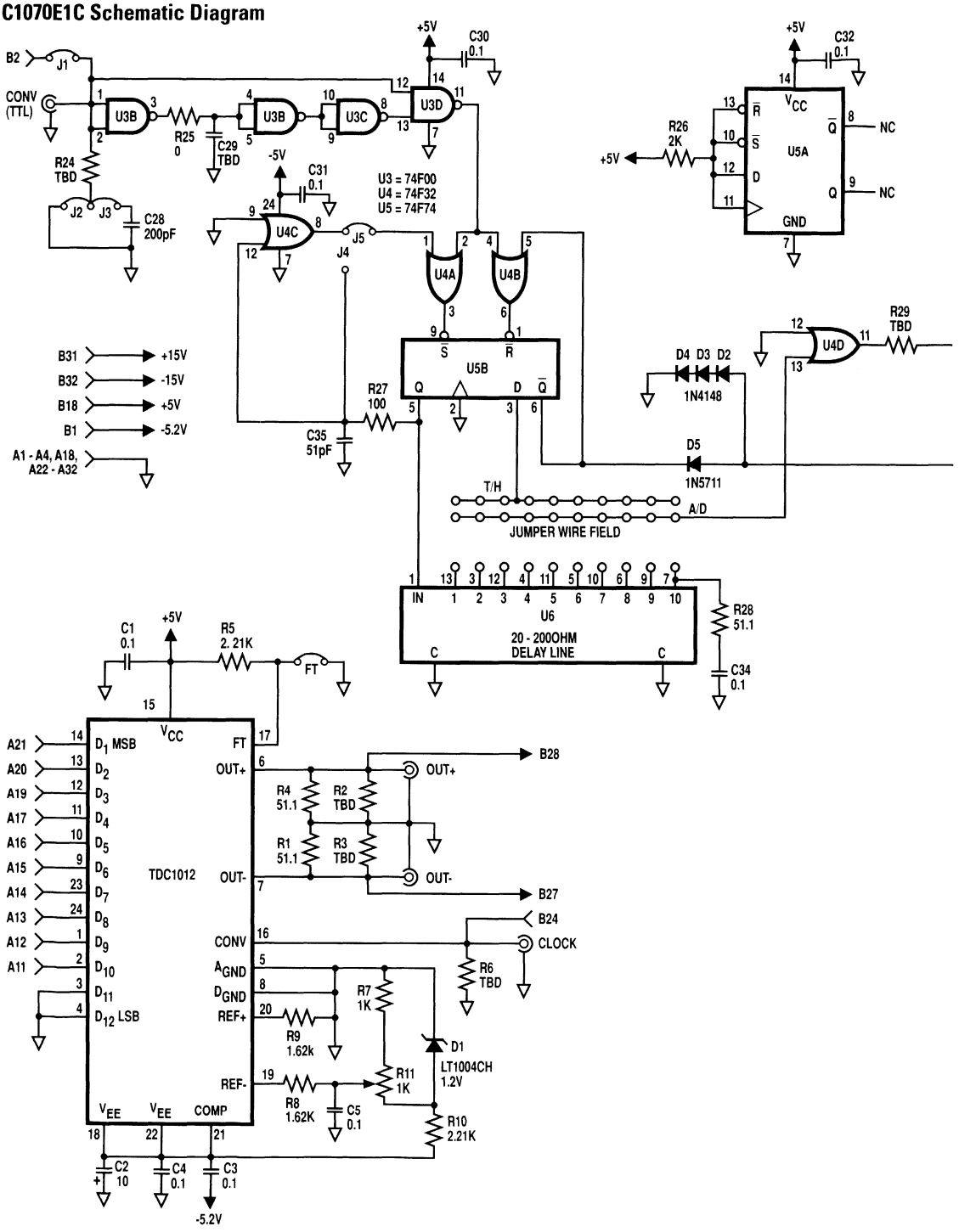
Potentiometer R11 is used to adjust the reference voltage to the TDC1012. This voltage is adjusted to –1.0V as part of the factory test and calibration procedure.

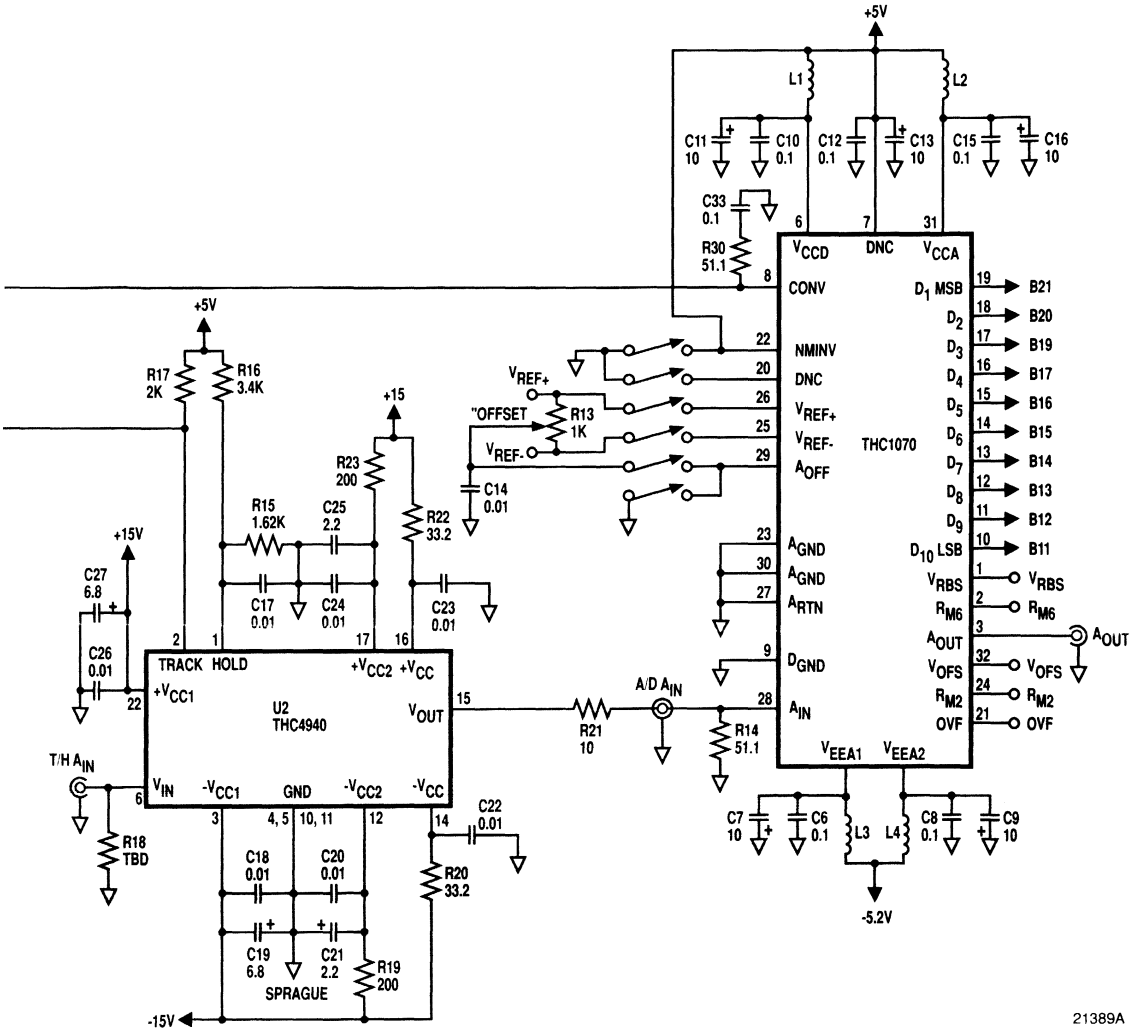
Removing the jumper in the location labeled "FT" will put the TDC1012 into feedthru (unclocked) mode. This eliminates the requirement for a D/A CLK signal, but will degrade the fidelity of the TDC1012 reconstruction signal.

THC4940 Track/Hold Amplifier Option

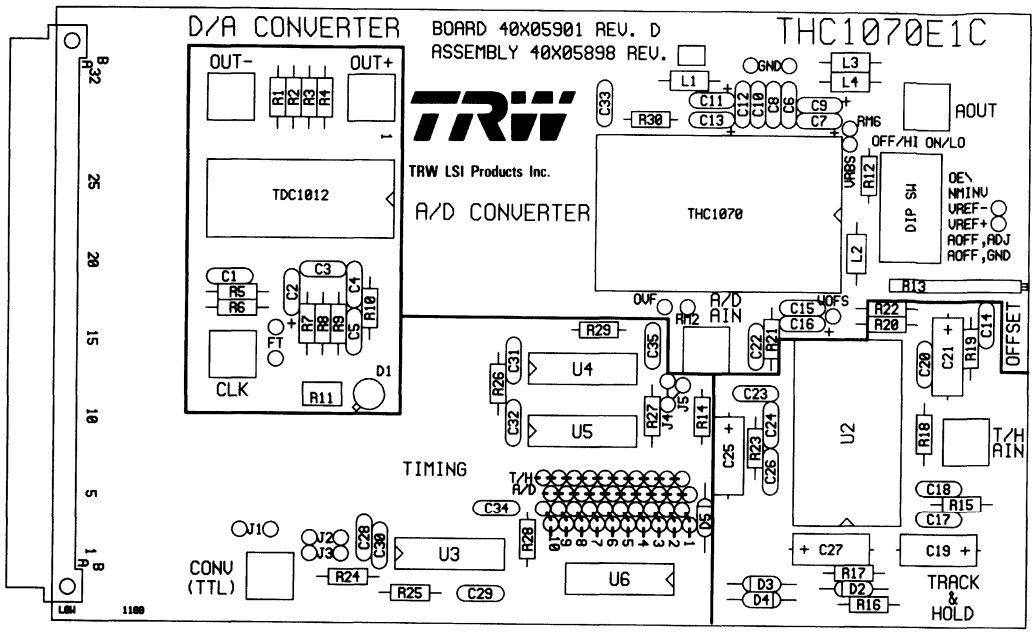
A THC4940 may be added to the THC1069E1C just prior to the THC1070 A/D converter. When the THC4940 is used, +15 and –15 Volt power supplies are required on edge-connector pins B31 and B32, respectively. The analog signal input is connected to the SMA labeled "T/H A_{IN}" which has a terminating resistor R18. When the THC4940 is used, terminating resistor R14 should be removed.

THC1070E1C Schematic Diagram

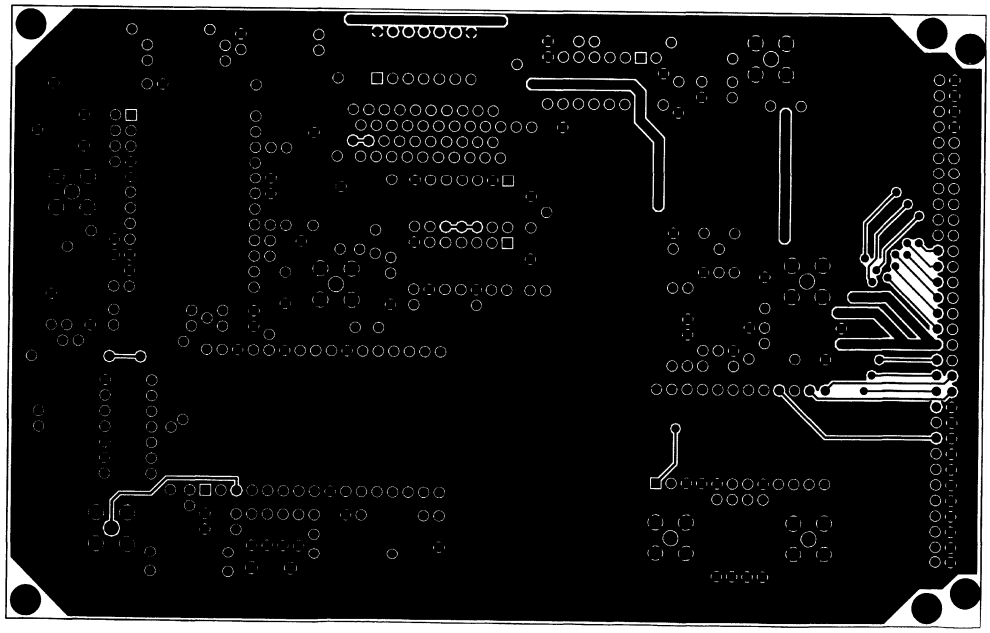



+5V
L1
L2
C11 10
C10 0.1
C12 0.1
C13 10
C15 0.1
C16 10
C33 0.1
R30 51.1
6
7
31
VCCD
DNC
VCCA
8
CONV
D1 MSB
B21
D2
B20
D3
B19
D4
B17
D5
B16
D6
B15
D7
B14
D8
B13
D9
B12
D10 LSB
B11
22
NMINV
20
DNC
26
VREF+
25
VREF-
29
AOFF
THC1070
23
AGND
30
AGND
27
ARTN
1
VRBS
2
RM6
3
AOUT
32
VOFS
24
RM2
21
OVF
9
DGND
28
AIN
VEEA1
VEEA2
+5V
R17 2K
R16 3.4K
+15
VREF+
"OFFSET
R13 1K
VREF-
C14 0.01
R23 200
R22 33.2
R15 1.62K
C25 2.2
C17 0.01
C24 0.01
C23 0.01
+15V
C27 6.8
C26 0.01
2
1
17
16
TRACK HOLD
+VCC2
+VCC
+VCC1
22
U2
THC4940
VOUT
15
A/D AIN
R21 10
R14 51.1
T/H AIN
R18 TBD
6
VIN
-VCC1
GND
-VCC2
-VCC
3
4, 5
10, 11
12
14
C22 0.01
C18 0.01
C20 0.01
R20 33.2
C19 6.8
C21 2.2
SPRAGUE
R19 200
-15V
C7 10
C6 0.1
L3
L4
C8 0.1
C9 10
-5.2V
21389A

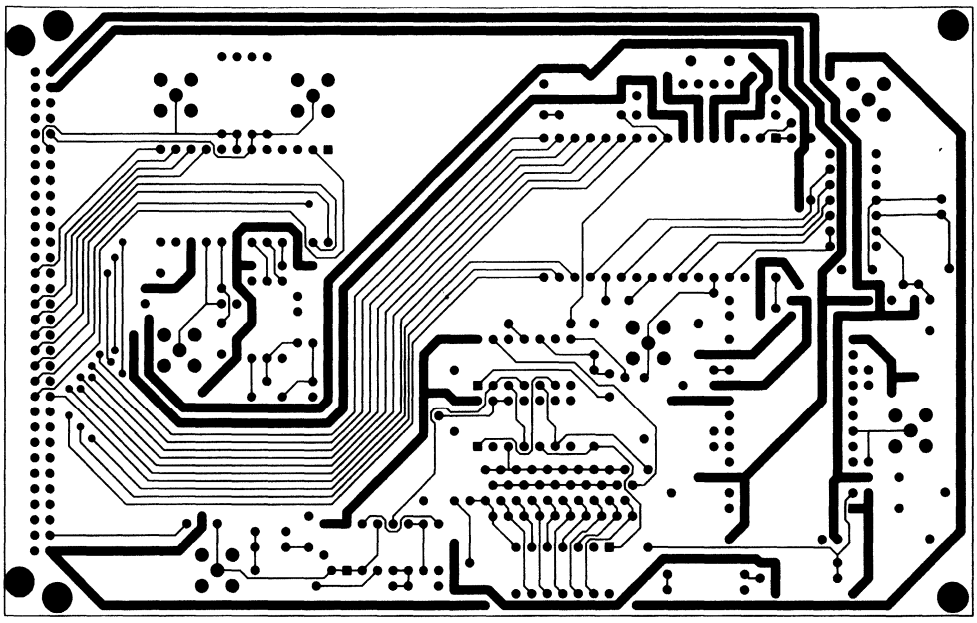
THC1070E1C Silkscreen Layout



THC1070EIC Component Side Layout



TCH1070E1C Circuit Side Layout



THC1070E1C Evaluation Board Pin Assignments

GND	A32	B32	V- (-15V)
GND	A31	B31	V+ (+15V)
GND	A30	B30	N/C
GND	A29	B29	N/C
GND	A28	B28	D/A OUT+
GND	A27	B27	D/A OUT-
GND	A26	B26	N/C
GND	A25	B25	N/C
GND	A24	B24	D/A CLK
GND	A23	B23	N/C
GND	A22	B22	N/C
D/A D1 MSB	A21	B21	A/D D1 MSB
D/A D2	A20	B20	A/D D_2
D/A D_3	A19	B19	A/D D_3
GND	A18	B18	VCC (+5V)
D/A D_4	A17	B17	A/D D_4
D/A D_5	A16	B16	A/D D_5
D/A D_6	A15	B15	A/D D_6
D/A D_7	A14	B14	A/D D_7
D/A D_8	A13	B13	A/D D_8
D/A D_9	A12	B12	A/D D_9
D/A D_{10}	A11	B11	A/D D_{10} LSB
N/C	A10	B10	N/C
N/C	A9	B9	N/C
N/C	A8	B8	N/C
N/C	A7	B7	N/C
N/C	A6	B6	N/C
N/C	A5	B5	N/C
GND	A4	B4	N/C
GND	A3	B3	N/C
GND	A2	B2	A/D CONV
GND	A1	B1	VEE (-5.2V)

Mating Connectors for THC1070E1C

AMP	532507-2	Wire-wrap
AMP	532507-1	Solder tail
Robinson-Nugent	RNE-64BS-W-TG30	Wire-wrap
Robinson-Nugent	RNE-64BS-S-TG30	Solder tail
Souriau	8609-264-6115-7550E1	Wire-wrap
Souriau	8609-264-6114-7550E1	Solder tail
Souriau	8609-264-6813-7550E1	Solder tail, Night-Angle Bend

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
THC1070S5B	IND - T_C = -25°C to 85°C	Industrial	32 Pin Metal DIP	THC1070S5B
THC1070S5V	EXT - T_C = -55°C to 125°C	MIL-STD-883	32 Pin Metal DIP	THC1070S5V
THC1070E1C	STD - T_A = 0°C to 70°C	—	Eurocard PC Board	THC1070E1C

A

Life Support Policy

TRW LSI Products Inc. components are not designed for use in life support applications, wherein a failure or malfunction of the component can reasonably be expected to result in personal injury. The user of TRW LSI Products Inc. components in life support applications assumes all risk of such use and indemnifies TRW LSI Products Inc. and TRW Inc. against all damages.

TDC1147

Monolithic Video A/D Converter
7-Bit, 15Msps

The TDC1147 is a 7-bit "flash" analog-to-digital converter which has no pipeline delay between sampling and valid data. The output data register normally found on flash A/D converters has been bypassed, allowing data to transfer directly to output drivers from the encoding logic section of the circuit. The converter requires only one clock pulse to perform the complete conversion operation. The conversion time is guaranteed to be less than 60 nanoseconds.

The TDC1147 is function and pin-compatible with TRW's TDC1047 7-bit flash A/D converter which has an output data register. The TDC1147 will operate accurately at sampling rates up to 15Msps and has an analog bandwidth of 7MHz. Linearity errors are guaranteed to be less than 0.4% over the operating temperature range.

Features

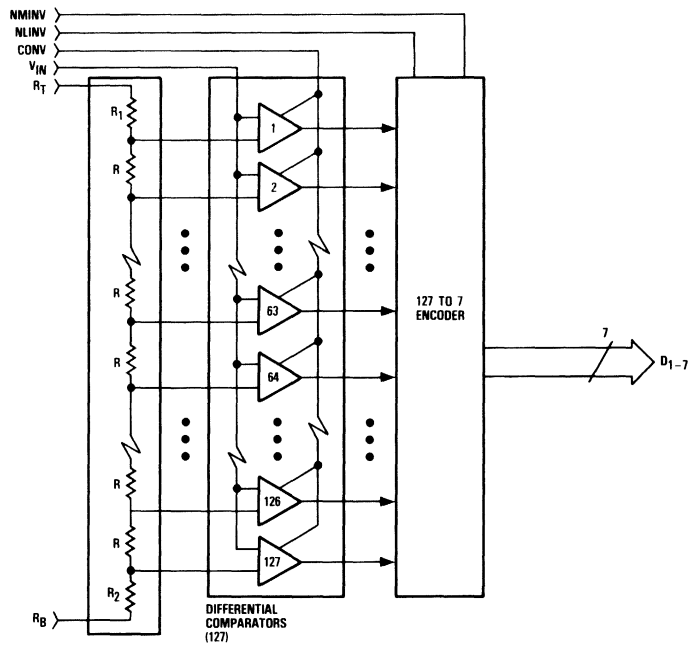
- No Digital Pipeline Delay
- 7-Bit Resolution
- 1/2 LSB Linearity
- Sample-And-Hold Circuit Not Required
- TTL Compatible
- Selectable Output Format
- Available In 24 Pin CERDIP

Applications

- Low-Cost Video Digitizing
- Medical Imaging
- Data Acquisition
- High Resolution A/D Converters
- Telecommunications Systems
- Radar Data Conversion

A

Functional Block Diagram



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La Jolla, CA 92038

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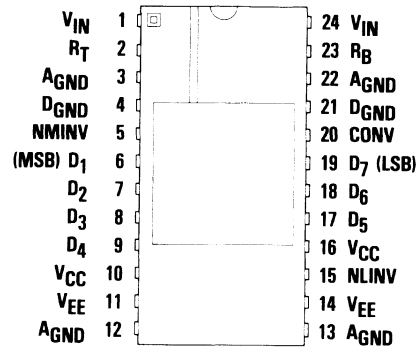
FAX: (619) 455-6314

40G01900 Rev. E–11/90
Printed in the U.S.A.

Pin Assignments



24 Pin CERDIP – B7 Package

Functional Description

General Information

The TDC1147 has two functional sections: a comparator array and encoding logic. The comparator array compares the input signal with 127 reference voltages to produce an N-of-127 code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-127 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV.

Power

The TDC1147 operates from two supply voltages, +5.0V and −5.2V. The return path for I_{CC} (the current drawn from the +5.0V supply) is D_{GND}. The return path for I_{EE} (the current drawn from the −5.2V supply) is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1147 converts analog signals in the range $V_{RB} \leqslant V_{IN} \leqslant V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and −1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 0.8V and 1.2V. The nominal voltages are V_{RT} = 0.00V and V_{RB} = −1.00V. These voltages may be varied dynamically up to 7MHz. Due to slight variations in the reference current with clock and input signals, R_T and R_B should be low-impedance points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are varied dynamically as in an Automatic Gain Control (AGC) circuit, a low-impedance reference source is recommended.

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***.

Convert

The TDC1147 uses a CONVert (CONV) input signal to initiate the A/D conversion process. Unlike other flash A/D converters which have a one-clock-cycle pipeline delay between sampling and output data, the TDC1147 requires only a single pulse to perform the entire conversion operation. The analog input is sampled (comparators are latched) within the maximum Sampling Time Offset (t_{STO}, see ***Figure 1***). Data from that sample becomes valid after a maximum Output Delay Time (t_D) while data from the previous sample is held at the outputs for a minimum Output Hold Time (t_{HO}). This allows data from the TDC1147 to be acquired by an external register or other circuitry. Note that there are minimum time requirements for the HIGH and LOW portions (t_{PWH}, t_{PWL}) of the CONV waveform and all output timing specifications are measured with respect to the rising edge of CONV.

Analog Input

The TDC1147 uses latching comparators which cause the input impedance to vary slightly with the signal level. For optimal performance, both V_{IN} pins must be used and the source impedance of the driving circuit must be less than 30 Ohms. The input signal will not damage the TDC1147 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 127 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Outputs

The outputs of the TDC1147 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. New data becomes valid after a maximum time (t_D) after the rising edge of the CONV signal. The use of 2.2 kOhm pull-up resistors is recommended.

Package Interconnections

Signal Type	Signal Name	Function	Value	B7 Package Pins
Power	V_{CC}	Positive Supply Voltage	+5.0V	10, 16
	V_{EE}	Negative Supply Voltage	−5.2V	11, 14
	D_{GND}	Digital Ground	0.0V	4, 21
	A_{GND}	Analog Ground	0.0V	3, 12, 13, 22
Reference	R_T	Reference Resistor (Top)	0.00V	2
	R_B	Reference Resistor (Bottom)	−1.00V	23
Controls	NMINV	Not Most Significant Bit INVert	TTL	5
	NLINV	Not Least Significant Bit INVert	TTL	15
Convert	CONV	Convert	TTL	20
Analog Input	V_{IN}	Analog Signal Input	0V to −1V	1, 24
Outputs	D_1	MSB Output	TTL	6
	D_2		TTL	7
	D_3		TTL	8
	D_4		TTL	9
	D_5		TTL	17
	D_6		TTL	18
	D_7	LSB Output	TTL	19

Figure 1. Timing Diagram

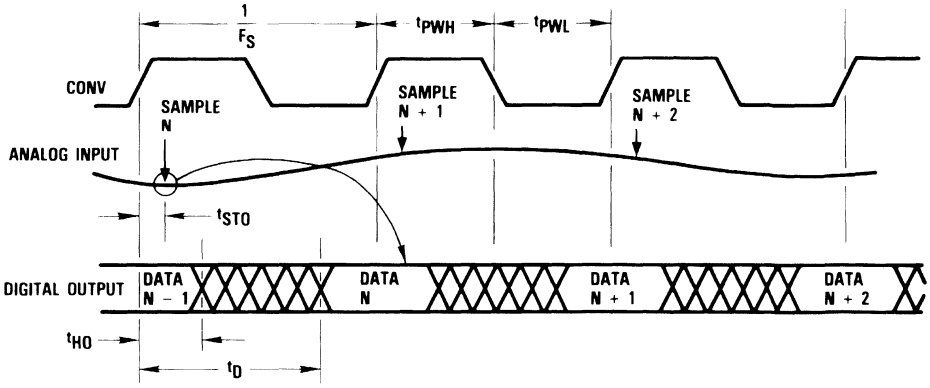


Figure 2. Simplified Analog Input Equivalent Circuit

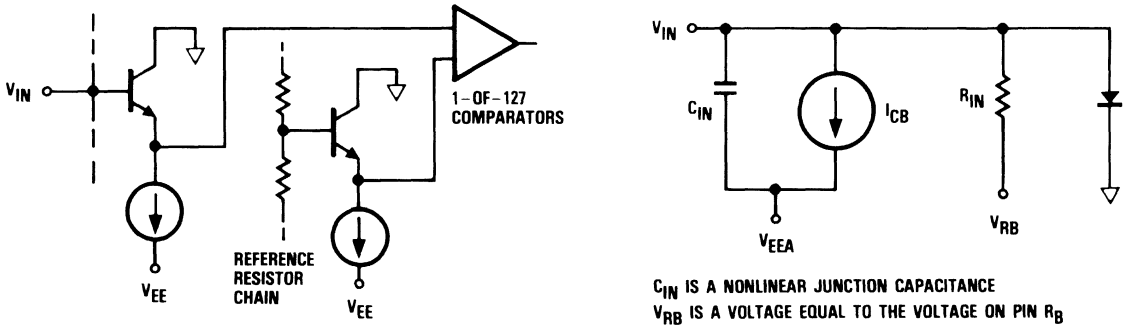


Figure 3. Digital Input Equivalent Circuit

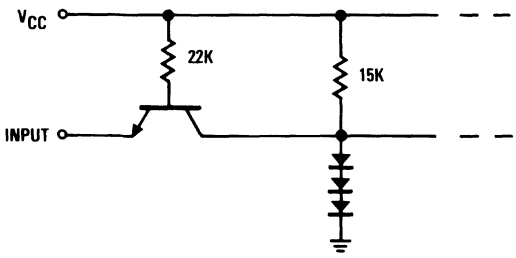
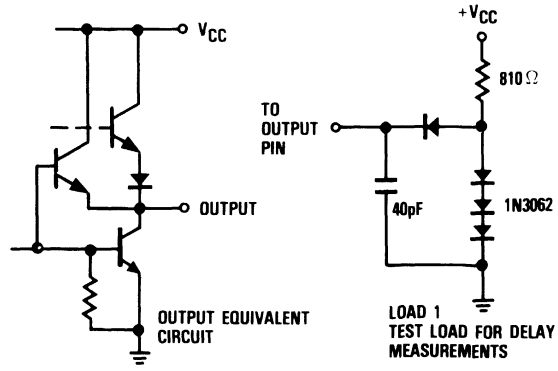


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input Voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}
V_{RT} (measured to V_{RB})	+2.2 to −2.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to 5.5V [2]
Applied current, externally forced	−1.0 to 6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, case	−55 to +125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter	Test Conditions	Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, LOW	22			22			ns
t_{PWH}	CONV Pulse Width, HIGH	18			18			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			2.0	mA
I_{OH}	Output Current, Logic HIGH			−0.4			−0.4	mA
V_{RT}	Most Positive Reference Input [1]	−0.1	0.0	0.1	−0.1	0.0	0.1	V
V_{RB}	Most Negative Reference Input [1]	−0.9	−1.0	−1.1	−0.9	−1.0	−1.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.8	1.0	1.2	0.8	1.0	1.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note: 1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Positive Supply Current	V_{CC} = Max, static [1]		25		30	mA
I_{EE}	Negative Supply Current	V_{EE} = Max, static [1]					
		T_A = 0°C to 70°C		-170			mA
		T_A = 70°C		-135			mA
		T_C = -55°C to 125°C				-220	mA
		T_C = 125°C				-130	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = Nom		35		50	mA
R_{REF}	Total Reference Resistance		34		20		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}	100		40		kOhms
C_{IN}	Input Capacitance			60		60	pF
I_{CB}	Input Constant Bias Current	V_{EE} = Max		160		300	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.5V CONV		-0.4		-0.6	mA
		$\overline{\text{NMINV, NLINV}}$		-0.6		-0.8	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = Max, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = Max, one pin to ground, one second duration.		-30		-30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{CC} = Min, V_{EE} = Min	15		15		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = Min, V_{EE} = Min		7		10	ns
t_D	Output Delay	V_{CC} = Min, V_{EE} = Min, Load 1		60		70	ns
t_{HO}	Output Hold Time	V_{CC} = Max, V_{EE} = Max, Load 1	15		15		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error, Integral Independent	V_{RT}, V_{RB} = Nom		0.4		0.4	%
E_{LD}	Linearity Error, Differential			0.4		0.4	%
CS	Code Size	V_{RT}, V_{RB} = Nom	30	170	30	170	% Nominal
V_{OT}	Offset Voltage, Top	V_{IN} = V_{RT}		+50		+50	mV
V_{OB}	Offset Voltage, Bottom	V_{IN} = V_{RB}		−30		−30	mV
T_{CO}	Temperature Coefficient			±20		±20	μV/°C
BW	Bandwidth, Full Power Input		7		7		MHz
t_{TR}	Transient Response, Full Scale			10		10	ns
SNR	Signal-to-Noise Ratio	7MHz Bandwidth,					
		20MSPS Conversion Rate					
	Peak Signal/RMS Noise	1MHz Input	45		46		dB
		7MHz Input	43		44		dB
	RMS Signal/RMS Noise	1MHz Input	36		37		dB
		7MHz Input	34		35		dB
E_{AP}	Aperture Error			50		50	ps
DP	Differential Phase Error[1]	F_S = 4 x NTSC		1.5		1.5	Degree
DG	Differential Gain Error[1]	F_S = 4 x NTSC		2.5		2.5	%

Note:

1. In excess of quantization.

Output Coding

Range	Binary		Offset Two's Complement	
	True	Inverted	True	Inverted
−1.00V FS	NMINV = 1	0	0	1
	NLINV = 1	0	1	0
0.0000V	0000000	1111111	1000000	0111111
−0.0078V	0000001	1111110	1000001	0111110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.4960V	0111111	1000000	1111111	0000000
−0.5039V	1000000	0111111	0000000	1111111
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.9921V	1111110	0000001	0111110	1000001
−1.0000V	1111111	0000000	0111111	1000000

Note:

1. Voltages are code midpoints.

Calibration

To calibrate the TDC1147, adjust V_{RT} and V_{RB} to set the 1st and 127th thresholds to the desired voltages. Assuming a 0V to −1V input range, continuously strobe the converter with −0.0039V (1/2 LSB from 0V) on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −0.996V (1/2 LSB from −1V) and adjust V_{RB} for toggling between codes 126 and 127.

The degree of required adjustment is indicated by the offset voltages, V_{OT} and V_{OB}. Offset voltages are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the integrated circuit. These parasitic resistors are shown as R_1 and R_2 in the ***Functional Block Diagram***. Calibration will cancel all offset voltages, eliminating offset and gain errors.

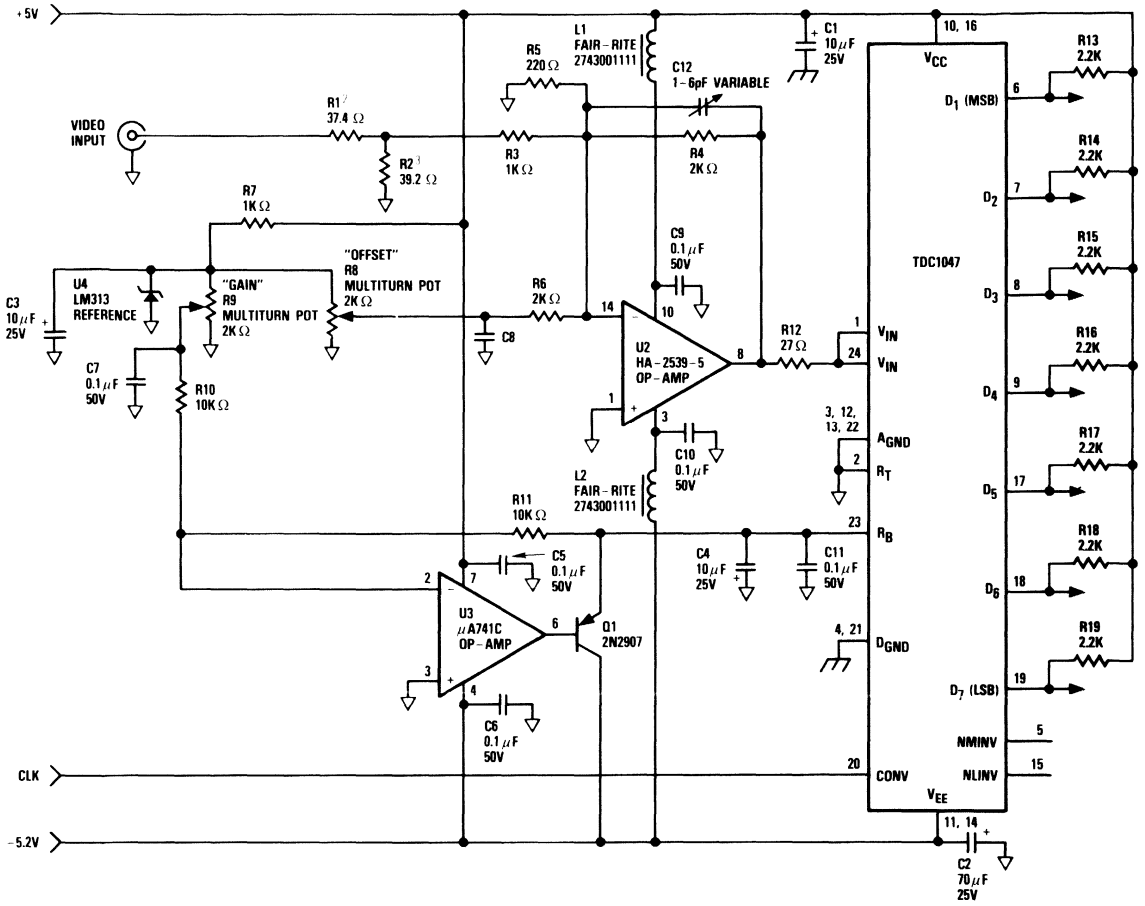
The above method for calibration requires that both ends of the resistor chain, R_T and R_B, are driven by variable voltage sources. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with an input amplifier offset control. The offset error at the bottom of the resistor chain causes a slight gain error, which can be compensated for by varying the voltage applied to R_B. The bottom reference is a convenient point for gain adjust that is not in the analog signal path.

Typical Interface Circuit

Figure 5 shows an example of a typical interface circuit for the TDC1147. The analog input amplifier is a bipolar wideband operational amplifier, which is used to directly drive the A/D converter. Bipolar inputs may be accommodated by adjusting the offset control. A zener diode provides a stable reference for both the offset and gain control. The amplifier has a gain of −1 providing the recommended 1Vp-p input for the A/D converter. Proper decoupling is recommended for all supplies, although the degree of decoupling shown may not be needed. A variable capacitor permits either step response or frequency response optimization. This may be replaced with a fixed capacitor, whose value depends upon the circuit board layout and desired optimization.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier, followed with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain. The bottom reference voltage can be adjusted to cancel the gain error introduced by the offset voltage, V_{OB}, as discussed in the ***Calibration*** section.

Figure 5. Typical Interface Circuit



Notes:

1. Unless otherwise specified, all resistors are 1/4W, 2%.
2. $R1 = Z_{IN} \left(\frac{1000\ R2}{1000 + R2} \right)$
3. $R2 = \frac{1}{\left(\frac{2V_{Range}}{V_{REF}\ Z_{IN}} \right) - 0.001}$

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1147B7C	STD – T_A = 0°C to 70°C	Commercial	24 Pin CERDIP	1147B7C
TDC1147B7V	EXT – T_C = –55°C to 125°C	MIL-STD-883	24 Pin CERDIP	1147B7V

TMC1175

Advance Information

Monolithic CMOS A/D Converter

8 Bit, 30 Msps

The TMC1175 is a two-step CMOS analog-to-digital converter with an integral track-and-hold amplifier. It converts an analog signal with full-power bandwidths of 7 MHz into an 8-bit data stream at rates up to 30 MegaSamples Per Second (Msps). This conversion rate is sufficient for sampling video signals at 8 times the NTSC, PAL, or SECAM subcarrier frequency.

The TMC1175 comprises an integrated track-and-hold amplifier, two quantizers, a reference voltage generator, and digital encoding logic. The T/H holds the input signal stable while the coarse quantizer estimates the input value. The references of the fine quantizer are then set to bound this initial estimate and the fine quantizer completes the conversion. An on-chip reference source is provided for medium-performance applications: alternatively, an external reference may be used.

The two-step architecture, implemented in TRW's Omicron-C™ 1μCMOS process, results in low 200mW power dissipation. Operation is controlled by a single CONVert signal. All digital inputs and outputs are TTL compatible.

Features

- 8-Bit Resolution
- 30 Msps Conversion Rate
- Internal Track/Hold
- 7 MHz Full Power Bandwidth
- Linearity Error Less Than ±1/2 LSB
- 0.5° Differential Phase
- 1% Differential Gain
- Single +5V Power Supply
- 200mW Power Dissipation
- Three-State TTL Outputs
- TTL/CMOS Compatible
- Low Cost

A

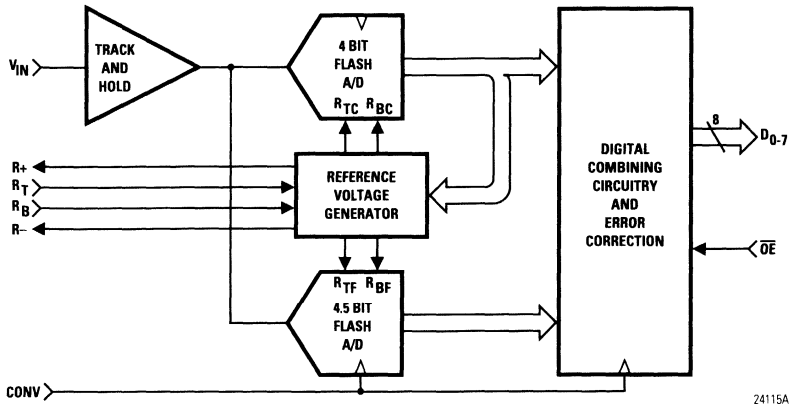
Applications

- Digital Television
- Ultrasound Systems
- High Speed Data Acquisition
- Video Frame Grabbers
- Image Scanners

Associated Products

- TDC1041 D/A Converter
- TDC4614 Reference/Amplifier
- TMC2242 Half-Band Filter

Simplified Block Diagram



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Printed in the U.S.A.

THC1200

Dual-Range High-Speed Analog-to-Digital Converter
12-Bit, 8 Msps

The THC1200 is a complete 12-bit 8 Msps (Mega-samples-per-second) analog-to- digital converter that includes all the circuitry required to digitize signals within a DC to 35MHz band. The THC1200 features two user-selectable input voltage ranges which give the A/D converter a large dynamic range. With its two-step architecture, the THC1200 achieves a very high conversion rate and superior performance. The device contains a wideband input amplifier, a precision track/hold, analog-to-digital quantizer, voltage reference, precision timing generator and registered three-state TTL output drivers.

The THC1200 offers significant advantages over previous converter boards in space efficiency, ease of use, power dissipation, DC and AC performance, reliability and flexibility.

Designed to meet demanding requirements, the THC1200 is housed in a 46-pin hermetically sealed dual-in-line package. Specified performance is guaranteed over the industrial (–25 to 85°C case) and extended (–55 to 125°C case) temperature ranges. Military-grade parts are in compliance with MIL-STD-883 and are manufactured in facilities certified and qualified to MIL-STD-1772.

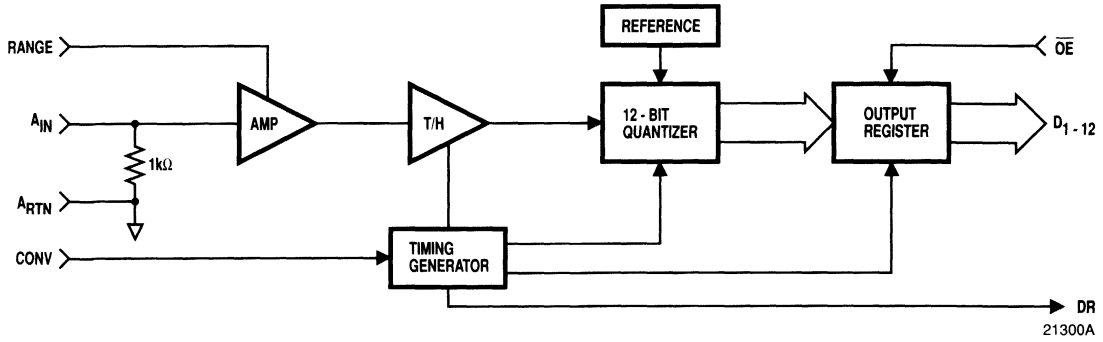
Features

- Conversion Rate DC To 8 Msps
- Two User-Selectable Input Voltage Ranges
- Analog Input Ranges: ±2.5 and ±0.167 Volts
- Input Signal Bandwidth >30MHz
- No Missing Codes, Guaranteed
- SNR = 62dB At 8 Msps With 2.5MHz Input, Guaranteed
- TTL-Compatible Input And Three-State Outputs
- 46-Pin Metal DIP
- Evaluation Board (THC1200E1C) Available

Applications

- Radar
- Data Acquisition Systems
- Digital Oscilloscopes
- Medical Imaging
- Communications
- CCD Digitization
- Transient Recorders
- Forward-Looking InfraRed Systems
- Focal Plane Arrays

Functional Block Diagram



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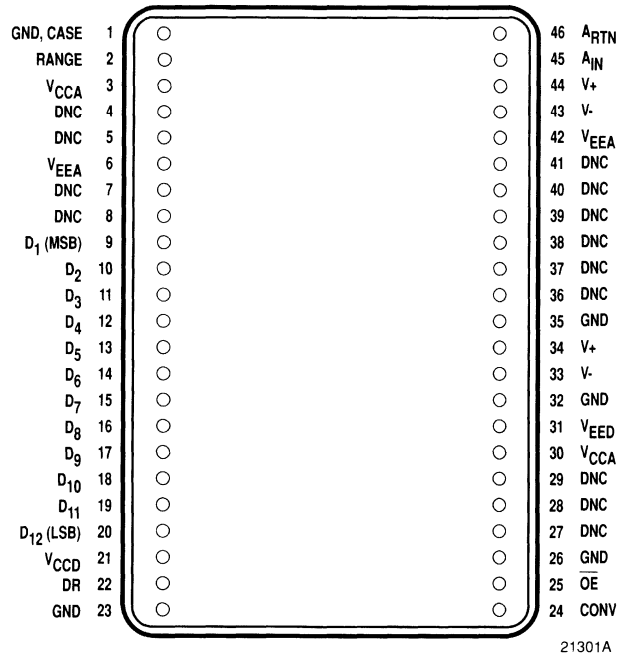
40G05735 Rev. A – 8/90
Printed in the U.S.A.

Pin Assignments



46-Pin Metal DIP, S3 Package

Functional Description

General Information

The THC1200 is a complete 12-bit 8 Msps A/D converter that features a wideband input amplifier, precision track/hold, voltage reference, timing circuitry and a three-state digital output register all housed in a 46-pin hermetic DIP. Input voltage ranges of ±2.5 and ±0.167 Volts are selectable by way of a single TTL-compatible input. The THC1200 employs a two-step analog-to-digital converter architecture and proprietary components to achieve a 8 Msps conversion rate and superior performance. The THC1200 is guaranteed to meet all specifications without additional adjustment or calibration. Additional information on applying the THC1200 is found in TRW *Application Note TP-45, "Designing with the THC1200 A/D Converter Family."*

Three-state TTL-compatible outputs permit the THC1200 to drive a shared data bus directly. Data emerges from the THC1200 synchronously with respect to CONV. The digital output corresponding to the sample of the analog input signal is valid after the rising edge CONV. The THC1200 provides a 12-bit two's-complement digital output as indicated in the *Output Coding Table*.

Power and Ground

The THC1200 requires four standard power supplies for operation: $V_{CCA} = V_{CCD} = +5V$, $V_{EEA} = V_{EED} = -5.2V$, V+ = +15V, and V– = –15V. Linear regulated power supplies are preferred over switching power supplies for optimum performance. All power supply inputs to the THC1200 should be properly decoupled.

Separate analog and digital grounds are maintained within the the THC1200, but no distinction is made at the package pins. For optimum converter performance, all ground pins should be connected to a common solid ground plane. Wire-wrap breadboarding techniques are not recommended for use with this high-speed high- precision analog-to-digital converters. TRW LSI Products Inc. *Application Note TP-45, "Designing with the THC1200 A/D Converter Family"* is recommended for additional information on using the THC1200.

Analog Input and Analog Input Return

The two input voltage ranges of the THC1200 are: –2.500 to +2.500 Volts and +0.167 to –0.167 Volts. This results in a Least Significant Bit weight of 80 microvolts in the smaller range, giving the THC1200 an overall dynamic range of nearly 96dB. A 1kΩ thin-film resistor is connected between A_{IN} and A_{RTN} and is provided for termination of analog input signals

A_{RTN} is the internal ground reference point for internal analog circuitry and voltage references within the THC1200. In normal operation A_{RTN} should be connected to signal ground where the analog input signal connection is in close proximity to the THC1200. A_{RTN} should also be connected to power supply ground.

RANGE

The RANGE input selects which of the two analog input voltage ranges the THC1200 is to use. When LOW, the input range of the THC1200 is 5.0 Volts peak- to-peak, centered around zero Volts. When RANGE is HIGH, the analog input voltage range is 0.333 Volts peak-to-peak, centered around zero Volts.

CONV

Each rising edge of the CONV signal initiates conversion (*See Timing Diagram*). The THC1200 operates independently of the duty cycle of CONV as long as t_{PWH} and t_{PWL} limitations are not exceeded.

CONV clock jitter, t_{CJ}, must be minimized in order to optimize performance. Time errors in sampling a high slew rate (large $\Delta V/\Delta T$) signal appear as voltage errors in the conversion. The high-speed and precision of the THC1200 may reveal system timing errors (jitter) that would not be apparent with lower resolution converters (see *TP-45*).

Data Outputs and Output Enable

The 12 TTL-compatible data outputs (D_1–D_{12}) provide two's-complement data as shown in the *Output Coding Table*. The output data becomes valid t_D after the rising edge of CONV, and remains valid until t_{HO} after the next rising edge of CONV. D_{12} is the least significant bit.

The output drivers become disabled (high-impedance) within t_{DIS} after the asynchronous input $\overline{OE}$ is switched HIGH. The outputs are enabled within t_{ENA} after $\overline{OE}$ is switched LOW.

Data Ready

A Data Ready output is provided which may be used to control the registering of data from the THC1200 into storage devices following in the data path. DR is generated within the THC1200 by inverting the CONV signal. As long as the user operates the THC1200 within the t_{PWH} and t_{PWL} limits on CONV, the rising edge of DR will occur when output data is valid and therefore can be used as the clock input to positive edge-triggered storage devices.

Do Not Connect

DNC pins are used in factory calibration and must remain unconnected.

Package Interconnections

Name	Function	Value	Package Pins
V_{CCA}	Positive Analog Supply	+5.0V	3, 30
V_{CCD}	Positive Digital Supply	+5.0V	21
V_{EEA}	Negative Analog Supply	–5.2V	6, 42
V_{EED}	Negative Digital Supply	–5.2V	31
V+	Positive Supply	+15V	34, 44
V–	Negative Supply	–15V	33, 43
GND	Ground	0.0V	1, 23, 26, 32, 35
CONV	Convert Input	TTL	24
A_{IN}	Analog Input	see text	45
A_{RTN}	Analog Input Return	0.0V	46
RANGE	Range Control Input	TTL	2
D_1 (MSB)	Most Significant Bit	TTL	9
D_2		TTL	10
D_3		TTL	11
D_4		TTL	12
D_5		TTL	13
D_6		TTL	14
D_7		TTL	15
D_8		TTL	16
D_9		TTL	17
D_{10}		TTL	18
D_{11}		TTL	19
D_{12} (LSB)	Least Significant Bit	TTL	20
DR	Data Ready Output	TTL	22
OE\	Output Enable Control	TTL	25
DNC	Do Not Connect	Open	4, 5, 7, 8, 27, 28, 29, 36, 37, 38, 39, 40, 41

Output Coding Table

Input Voltage (Code Midpoints) RANGE = LOW	Input Voltage (Code Midpoints) RANGE = HIGH	Digital Outputs MSB LSB
+2.5000	+0.16700	1000 0000 0000
+2.4988	+0.16692	1000 0000 0001
+2.4975	+0.16684	1000 0000 0010
•	•	• •
•	•	• •
•	•	• •
+0.0024	+0.00016	1111 1111 1110
+0.0012	+0.00008	1111 1111 1111
0.0000	0.00000	0000 0000 0000
–0.0012	–0.00008	0000 0000 0001
–0.0024	–0.00016	0000 0000 0010
•		• •
•		• •
•		• •
–2.4963	–0.16676	0111 1111 1101
–2.4975	–0.16684	0111 1111 1110
–2.4988	–0.16692	0111 1111 1111

Notes: 1. For RANGE = HIGH, 1 LSB Step size = 0.330 / 4095 = 80.6uV.

2. For RANGE = LOW, 1 LSB Step size = 5.000 / 4095 = 1.22mV.

Figure 1. Timing Diagram

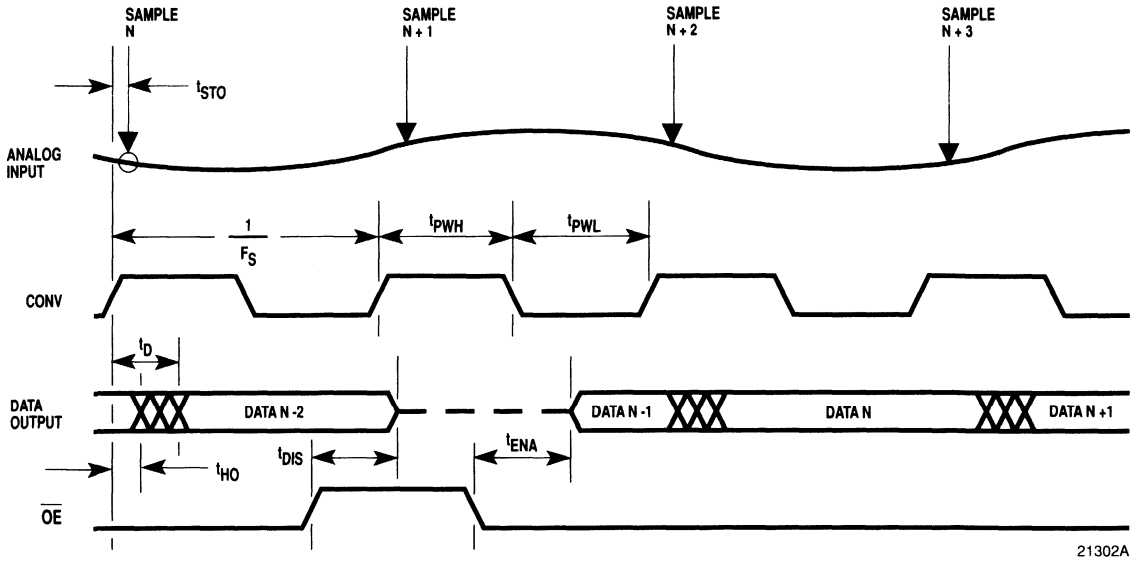


Figure 2. Simplified Analog Input Equivalent Circuit

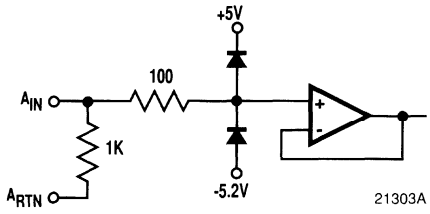
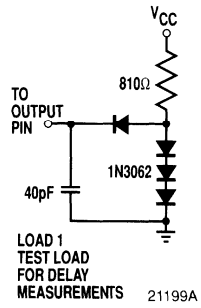


Figure 3. Standard TTL Test Load



Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltages

V_{CC}	-0.5 to +7.0V
V_{EE}	–7.0 to +0.5V
V+	–0.5 to + 18.0V
V–	–18.0 to +0.5V

Input Voltages

A_{IN}	+8.0 to –8.0
CONV, $\overline{OE}$	–0.5V to V_{CC}

Outputs

Digital Outputs, Applied Voltage[2]	–0.5V to V_{CC}
Digital Outputs, Applied Current[3]	100mA
Short-Circuit Duration (Single Output to Ground)	1 sec

Temperature

Operating, Case	–65 to +130°C
Lead, Soldering (10 seconds)	+300°C
Storage	–60 to +150°C

Notes: 1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.

2. Applied voltage must be current limited to specified range.

3. Forcing voltage must be limited to specified range.

Operating conditions

Parameter		Min	Nom	Max	Units
V_{CC}	Positive Supply Voltage	4.7	5.0	5.3	V
V_{EE}	Negative Supply Voltage	–4.89	–5.2	–5.51	V
V+	Positive Supply Voltage	14.4	15.0	15.6	V
V–	Negative Supply Voltage	–14.4	–15.0	–15.6	V
t_{PWH}	CONV Pulse Width HIGH	45			ns
t_{PWL}	CONV Pulse Width LOW	25			ns
f_S	Conversion Rate	0		8	msps
t_{CJ}	CONV Clock Jitter			10	ps_{RMS}
V_{IL}	Input Voltage, Logic LOW			0.7	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
A_{IN}	Analog Input Range, RANGE = LOW	–2.50		+2.50	V
A_{IN}	Analog Input Range, RANGE = HIGH	–0.167		+0.167	V
T_C	Case Temperature, B–grade	–25		85	°C
T_C	Case Temperature, V-grade	–55		125	°C

A

Electrical characteristics within specified operating conditions

Parameter		Conditions	Typ	Temperature Range				Units
				Industrial		Military		
				Min	Max	Min	Max	
I_{CC}	Total +5V Power Supply Current[1]		485		600		600	mA
I_{EE}	Total –5.2V Power Supply Current[1]		–315		–640		–640	mA
I+	Total V+ Power Supply Current[1]		150		400		400	mA
I–	Total V– Power Supply Current[1]		–180		–400		–400	mA
P_D	Total Power Dissipation[2]		9.45		13.7		13.7	W
I_{IH}	Input Current, Logic HIGH	V_{IH} = 2.4V			150		150	µA
I_{IL}	Input Current, Logic LOW	V_{IL} = 0.5V			–3.2		–3.2	mA
V_{OH}	Output Voltage, Logic HIGH	I_{OH} = 160µA		2.4		2.4		V
V_{OL}	Output Voltage, Logic LOW	I_{OL} = –3.2mA			0.5		0.5	V
I_{OZH}	Output Leakage Current, Logic HIGH	$\overline{OE}$ = HIGH, V_{OH} = 2.4V			±50		±50	µA
I_{OZL}	Output Leakage Current, Logic LOW	$\overline{OE}$ = HIGH, V_{OL} = 0.7V			±50		±50	µA
I_{OS}	Short Circuit Current	1 second Max., one pin shorted to ground		–30	–100	–30	–100	mA
R_{IN}	Analog Input Resistance	A_{RTN} connected to GND	1000	950	1050	950	1050	Ω
C_{IN}	Input Capacitance	All Inputs			20		20	pF
V_{FP1}	Full-Scale Positive Input	A_{IN} at 1/2 LSB above most positive transition, RANGE = LOW	2.50	2.45	2.55	2.45	2.55	V
V_{FN1}	Full-Scale Negative Input	A_{IN} at 1/2 LSB below most negative transition, RANGE = LOW	–2.50	–2.45	–2.55	–2.45	–2.55	V
V_{FP2}	Full-Scale Positive Input	A_{IN} at 1/2 LSB above most positive transition, RANGE = HIGH	0.167	0.157	0.177	0.157	0.177	V
V_{FN2}	Full-Scale Negative Input	A_{IN} at 1/2 LSB below most negative transition, RANGE = HIGH	–0.167	–0.157	–0.177	–0.157	–0.177	V

Notes: 1. Typical values are the statistical average of actual measurements taken over the Operating Temperature Range.

2. Typical value is calculated from typical power supply currents and maximum power supply voltages over the Operating Temperature Range. Maximum values are calculated from measured maximum currents and maximum voltages over the Operating Temperature Range.

Switching characteristics within specified operating conditions

Parameter		Conditions	Typ	Temperature Range				Units
				Industrial		Military		
				Min	Max	Min	Max	
f_S	Maximum Conversion Rate			8		8		Msps
t_{STO}	Sampling Time Offset	RANGE = LOW		–2.0	4.0	–2.0	4.0	ns
t_{STO}	Sampling Time Offset	RANGE = HIGH		–11.0	–17.0	–11.0	–17.0	ns
t_D	Data Output Delay Time	C_{LOAD} = 50pF Max			50		50	ns
t_{HO}	Data Output Hold Time	C_{LOAD} = 50pF Max		5		5		ns
t_{ENA}	Output Enable Time	C_{LOAD} = 50pF Max			40		40	ns
t_{DIS}	Output Disable Time	C_{LOAD} = 50pF Max			100		100	ns
t_G	Gain switch settling time				1		1	µs
t_{OR1}	Overload Recovery Time	V_{IN} = 2x Full-Scale			140		140	ns
t_{OR1}	Overload Recovery Time	V_{IN} = ±8V			4		4	µs

A

Thermal Characteristics

Parameter		Conditions	Typ	Units
delta T_{JC}	Junction-to-Case Temperature Rise	Worst-Case Power Dissipation	20	°C
$theta_{CA}$	Case-to-Ambient Thermal Resistance	in Still Air	10	°C/W
		with 500 LFPM Airflow	6	°C/W

System Performance Characteristics

Parameter		Conditions	Typ	Temperature Range				Units
				Industrial		Military		
				Min	Max	Min	Max	
E_{LI}	Integral Linearity Error	Independent based			±4.0		±4.0	LSB
E_{LD}	Differential Linearity Error	f_S = 8 Msps, f_{IN} = 2.5MHz	±0.6		±1.8		±1.8	LSB
SNR	Signal-to-Noise Ratio	f_S = 8 Msps, f_{IN} = 2.5MHz		59		59		dB
		V_{IN} is 1dB below Full-Scale RANGE = HIGH						
		f_S = 8 Msps, f_{IN} = 2.5MHz		62		62		dB
		V_{IN} is 1dB below Full-scale RANGE = LOW						
SFDR	Spurious Free Dynamic Range	f_S = 8 Msps, f_{IN} = 2.5MHz		65		65		dB
		V_{IN} is 1dB below Full-Scale RANGE = HIGH						
		f_S = 8 Msps, f_{IN} = 2.5MHz		62		62		dB
		V_{IN} is 1dB below Full-Scale RANGE = LOW						
IMD	Intermodulation Distortion	f_S = 8 Msps, f_{IN1} = 2.4MHz		62		62		dB
		f_{IN2} = 2.45 MHz, each input signal is 7dB below Full-Scale						
BW	–3dB Analog Bandwidth	V_{IN} = 0.330 Volts p-p, RANGE = HIGH		8		8		MHz
		V_{IN} = 5 Volts p-p, RANGE = LOW		25		25		MHz
E_{AP}	Aperture Jitter		±40					ps
SC	Spurious Codes				0		0	codes
MC	Missing Codes				0		0	codes
E_G	Gain Error				±1.5		±1.5	%FS
V_{OS1}	Offset Error	A_{IN} at Mid-Scale code transition, RANGE = HIGH			±5		±5	%FS
V_{OS2}	Offset Error	A_{IN} at Mid-Scale code transition, RANGE = LOW			±2.2		±2.2	%FS
PSR_1	Power Supply Rejection	V+, V–			0.05		0.05	%FS/%V
PSR_2	Power Supply Rejection	V_{CC}, V_{EE}			0.025		0.025	%FS/%V

Definitions

SNR (Signal-to-Noise Ratio)
The ratio, expressed in decibels, of the RMS level of the output signal to the RMS level of the in-band noise. This noise is measured with the signal present and excludes harmonic distortion products.

HD (Harmonic Distortion)
The ratio, expressed in decibels, of the second harmonic of the output fundamental to the RMS level of the output fundamental.

SINAD (Signal-to-Noise and Distortion)
The ratio, expressed in decibels, of the RMS level of the output signal to the RMS sum of both the in-band noise and the RMS sum of the first 10 harmonics of the output fundamental.

IMD (Intermodulation Distortion)
The ratio, expressed in decibels, of the largest output frequency spur to either of the two equal-level output fundamentals.

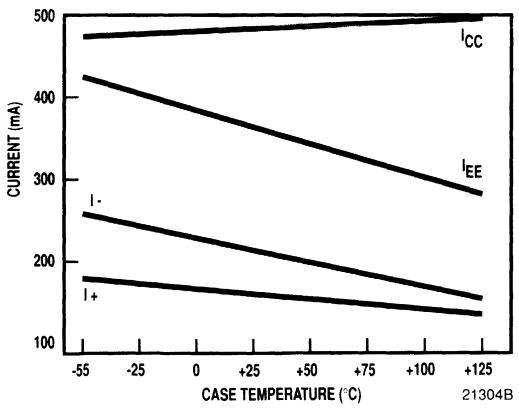
t_{TR} (Transient Response Time)
The time required to begin returning accurate data after a full scale input voltage step whose initial and final voltages are within the analog input range. t_{TR} is an analog domain parameter and excludes pipeline latency.

t_{OR} (Overload Recovery Time)
The time required to begin producing accurate data after the input voltage returns to the allowable range, following an excursion to 200% of either full-scale limit. t_{OR} is an analog domain parameter and excludes pipeline latency.

A

Typical Performance Curves

Power Supply Current vs Temperature



Dynamic Performance vs. Input Frequency

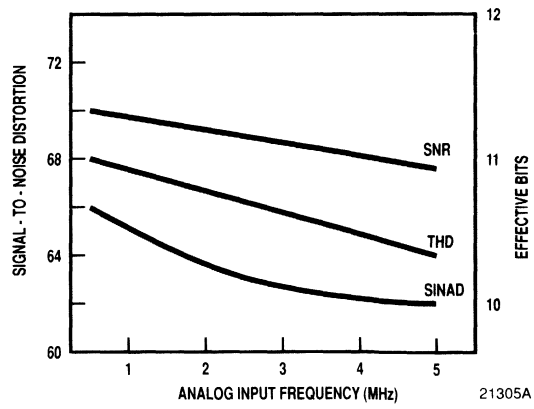
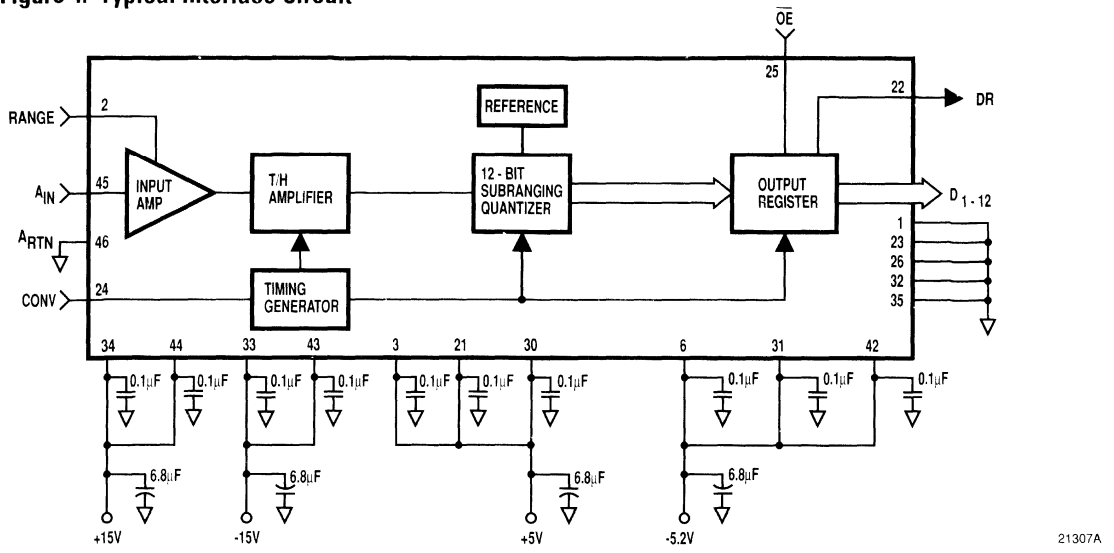


Figure 4. Typical Interface Circuit



Evaluation Board

The THC1200E1C is a Eurocard-style printed circuit board designed to aid in the evaluation of the THC1200 A/D converter. The board dimensions are 100mm x 160mm with a standard 64-pin double-row DIN male connector installed. A complementary 64-pin double-row DIN female connector is included with the board.

The board employs only two conducting sides. Most of the circuit interconnections are on the bottom of the board while the top is mostly solid ground plane. SMA connectors are installed on the board to facilitate analog I/O and clocks. The circuitry on the board includes all power supply decoupling required for the THC1200, and a TDC1012 12-bit D/A converter which may be used in evaluating certain parameters of the THC1200. Additional information on applying the THC1200 is found in TRW Application Note *TP-45, "Designing with the THC1200 A/D Converter Family"*.

The THC1200E1C board has been designed to be used, not only for the THC1200, but also for the THC1201 and THC1202 A/D converters. Therefore, the board has interconnect patterns for some circuitry that is not used by the THC1200. Jumpers J1, J6 and FT will be installed while all others are not.

The board is calibrated and tested at the factory and is supplied complete with THC1200 and TDC1012 installed.

Power and Ground

Four power supply voltages are required for the operation of the THC1200E1C: V_{CC} = +5V, V_{EE} = –5.2V, V+ = +15V and V– = –15 Volts. All power inputs are decoupled to a single solid ground plane, GND. All GND pins of the board are connected to the ground plane and it is recommended that all GND pins be used.

A/D Converter Inputs

The clock to the THC1200, CONV, is normally brought onto the board by way of an SMA connector labeled "CONV" near pin 24 of the THC1200. A location for a terminating resistor, R20 is available on the board for terminating cables. CONV may be brought onto the board through the edge-connector pin B2 by installing jumper J9. The DIP switch enables control of $\overline{OE}$ and RANGE which are both pulled HIGH when the switches are open.

The analog signal input to the THC1200, A_{IN} is normally brought onto the board by way of an SMA connector labeled "A_{IN}" near pin 45 of the THC1200. A resistor network, R13 through R16, is included on the board for terminating and attenuating the signal in user-determined impedances and losses.

A/D Converter Data Outputs and D/A Converter Data Inputs

The 12 data outputs of the THC1200 are brought to edge-connector pins B9 through B21 (excluding B18). These pins are located directly across the edge-connector from the 12 data inputs of the TDC1012 D/A converter to simplify connection of A/D outputs to D/A inputs.

D/A Converter Inputs

The clock to the TDC1012, CLK, is normally brought onto the board through an SMA connector labeled "CLK" near pin 16 of the TDC1012. A location for a terminating resistor, R6 is provided for clock cable termination. The clock input to the TDC1012 is also brought to the edge-connector pin B24.

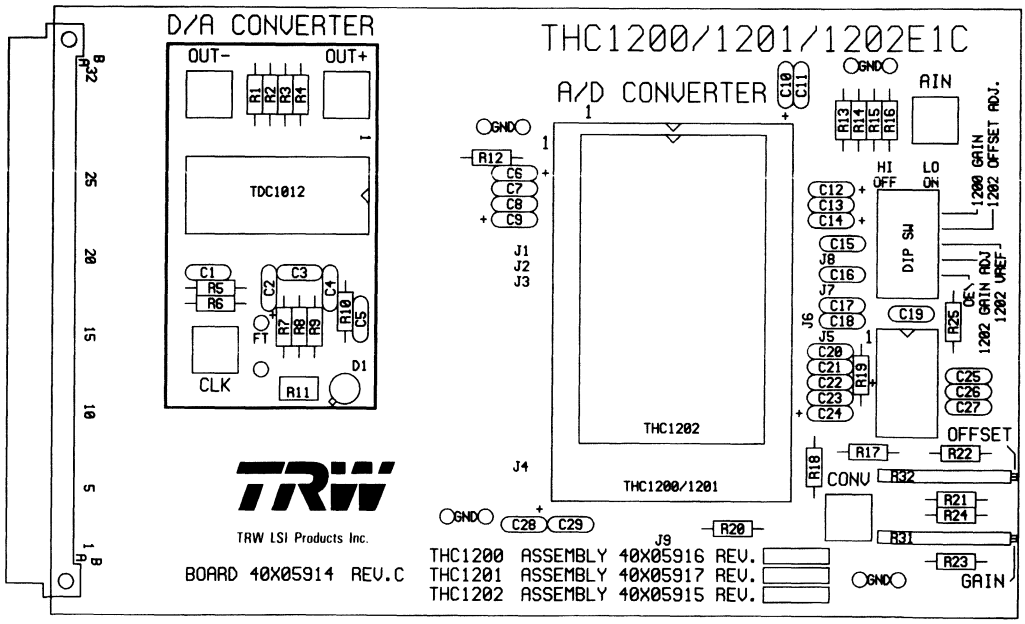
D/A converter outputs are brought to SMA connectors labeled OUT+ and OUT– as well as edge-connector pins B28 and B27. Load resistors of 51.1Ω are provided on the board to facilitate 50Ω cable connection to the board.

Potentiometer R11 is used to adjust the reference voltage to the TDC1012. This voltage is adjusted to –1.0 V as part of the factory test and calibration procedure.

Removing the jumper in the location labeled "FT" will put the TDC1012 into feedthru (unclocked) mode. This eliminates the requirement for a D/A clock signal, but will degrade the fidelity of the TDC1012 reconstruction.

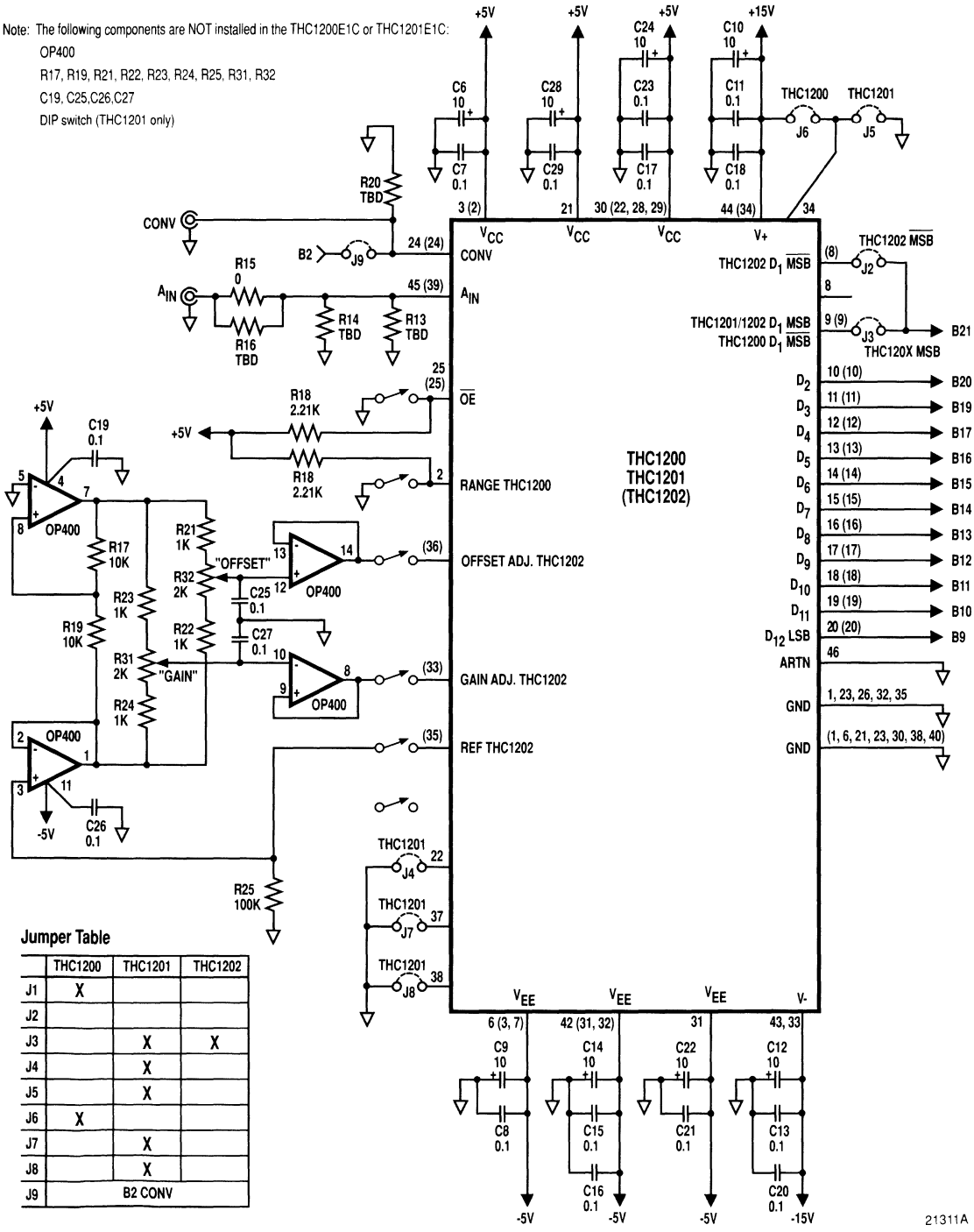
A

THC1200E1C silkscreen layout



THC1200E1C A/D Converter Schematic Diagram

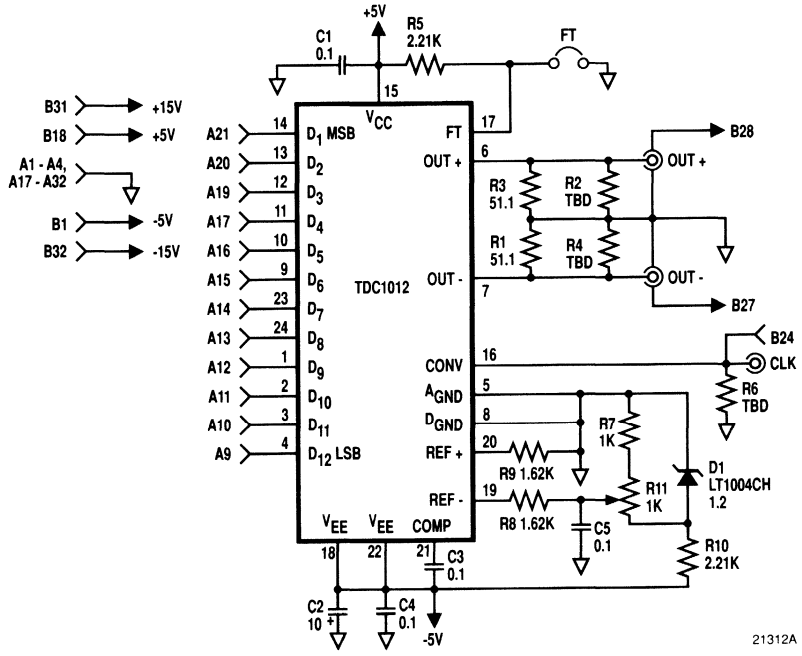
Note: The following components are NOT installed in the THC1200E1C or THC1201E1C:
OP400
R17, R19, R21, R22, R23, R24, R25, R31, R32
C19, C25,C26,C27
DIP switch (THC1201 only)



Jumper Table

	THC1200	THC1201	THC1202
J1	X		
J2			
J3		X	X
J4		X	
J5		X	
J6	X		
J7		X	
J8		X	
J9	B2 CONV		

THC1200E1C D/A Converter Schematic Diagram



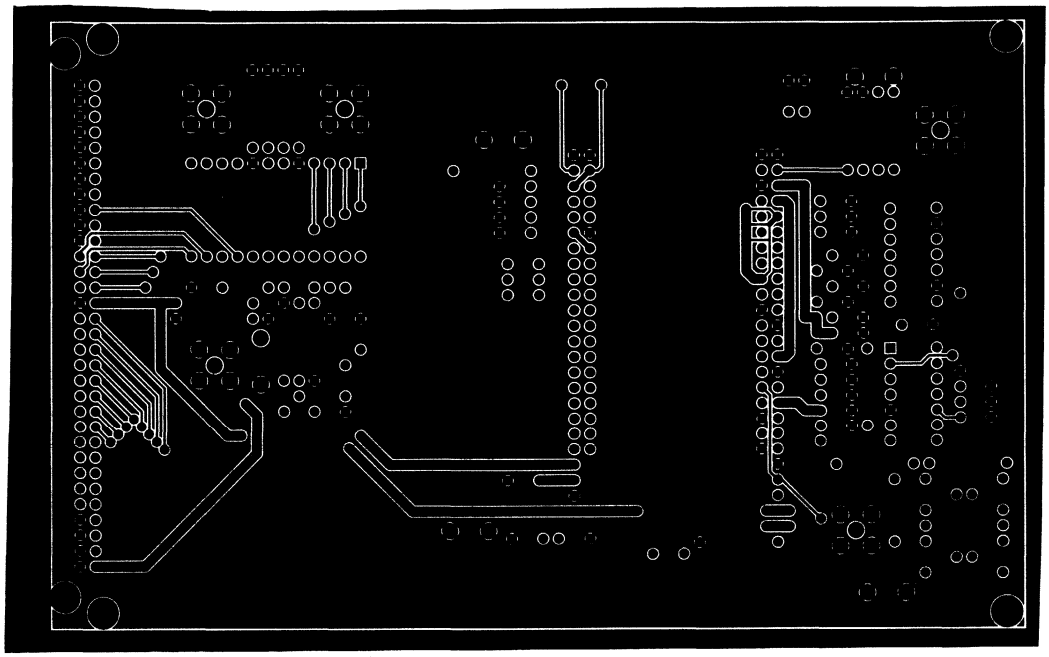
Evaluation Board Pin Assignments

GND	A32	B32	V– (–15V)
GND	A31	B31	V+ (+15V)
GND	A30	B30	N/C
GND	A29	B29	N/C
GND	A28	B28	D/A OUT+
GND	A27	B27	D/A OUT–
GND	A26	B26	N/C
GND	A25	B25	N/C
GND	A24	B24	D/A CLK
GND	A23	B23	N/C
GND	A22	B22	N/C
D/A D_1 MSB	A21	B21	A/D D_1 MSB
D/A D_2	A20	B20	A/D D_2
D/A D_3	A19	B19	A/D D_3
GND	A18	B18	V_{CC} (+5V)
D/A D_4	A17	B17	A/D D_4
D/A D_5	A16	B16	A/D D_5
D/A D_6	A15	B15	A/D D_6
D/A D_7	A14	B14	A/D D_7
D/A D_8	A13	B13	A/D D_8
D/A D_9	A12	B12	A/D D_9
D/A D_{10}	A11	B11	A/D D_{10}
D/A D_{11}	A10	B10	A/D D_{11}
D/A D_{12} LSB	A9	B9	A/D D_{12} LSB
N/C	A8	B8	N/C
N/C	A7	B7	N/C
N/C	A6	B6	N/C
N/C	A5	B5	N/C
GND	A4	B4	N/C
GND	A3	B3	N/C
GND	A2	B2	A/D CONV
GND	A1	B1	V_{EE} (–5.2V)

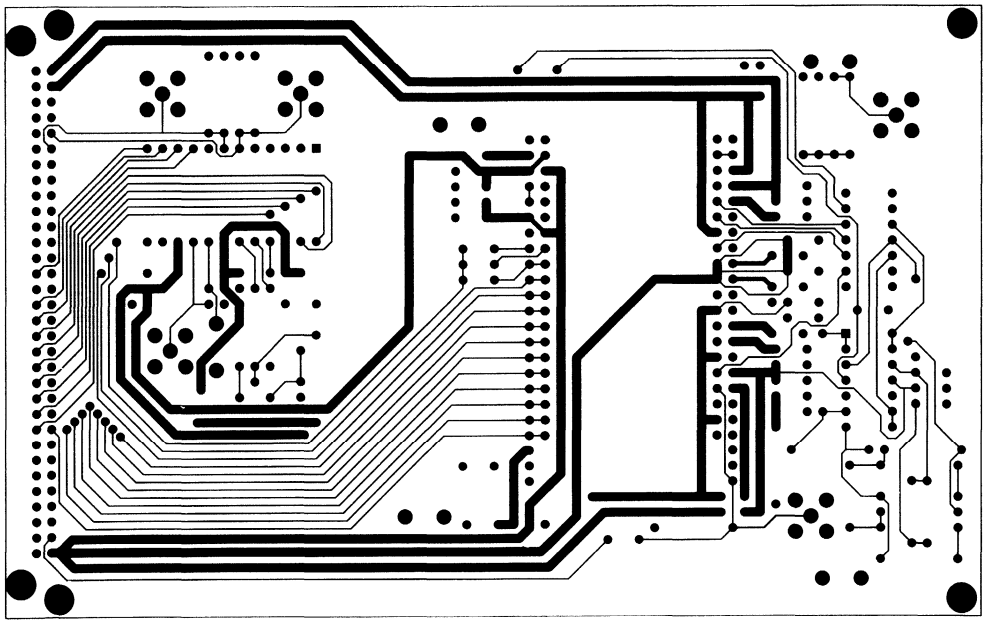
Mating Connectors for THC1200E1C

AMP	532507-2	Wire-wrap
AMP	532507-1	Solder tail
Robinson-Nugent	RNE-64BS-W-TG30	Wire-wrap
Robinson-Nugent	RNE-64BS-S-TG30	Solder tail
Souriau	8609-264-6115-7550E1	Wire-wrap
Souriau	8609-264-6114-7550E1	Solder tail
Souriau	8609-264-6813-7550E1	Solder tail, right-angle bend

THC1200E1C Component Side Layout



THC1200E1C Circuit Side Layout



Ordering Information

Product Number	Temperature Range	Screening	Package	Marking
THC1200S3B	IND, T_C = –25 to 85°C	Industrial	46 Pin Hermetic Metal DIP	THC1200S3B
THC1200S3V	EXT, T_C = –55 to 125°C	MIL-STD-883	46 Pin Hermetic Metal DIP	THC1200S3V
THC1200E1C	STD, T_A = 0 to 70°C	—	Eurocard PC Board	THC1200E1C

Life Support Policy

TRW LSI Products Inc. components are not designed for use in life support applications, wherein a failure or malfunction of the component can reasonably be expected to result in personal injury. The user of TRW LSI Products Inc. components in life support applications assumes all risk of such use and indemnifies TRW LSI Products Inc. and TRW Inc. against all damages.

THC1201

Complete High-Speed A/D Converter

12-Bit, 10Msps

The THC1201 is a complete 12-bit 10Msps (Mega-Samples Per Second) analog-to-digital converter that includes all the circuitry required to digitize signals within a DC to 70MHz band. With its two-step architecture, the THC1201 achieves a very high conversion rate and superior performance. The device contains a wideband input amplifier, a precision track/hold, analog-to-digital quantizer, voltage reference, precision timing generator and registered three-state TTL output drivers.

The THC1201 offers significant advantages over previous converter boards in space efficiency, ease of use, power dissipation, DC and AC performance, reliability and flexibility.

Designed to meet demanding requirements, the THC1201 is housed in a 46 pin hermetically sealed dual-in-line package. Specified performance is guaranteed over the industrial (−25 to 85°C case) and extended (−55 to 125°C case) temperature ranges. Military-grade parts are in compliance with MIL-STD-883C and are manufactured in facilities certified and qualified to MIL-STD-1772.

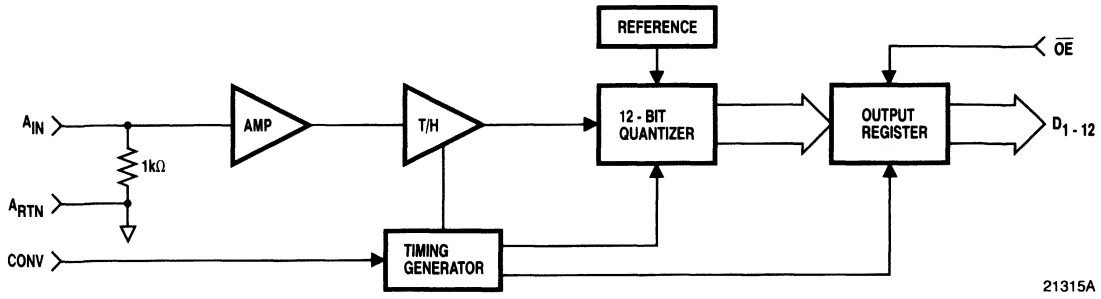
Features

- DC To 10Msps Conversion Rate
- Analog Input Range Is ±1.024V
- Large-Signal Bandwidth >70MHz
- No Missing Codes, Guaranteed
- SNR = 66dB At 10Msps With 2.3MHz Input, Guaranteed
- TTL Compatible Input And Three-State Outputs
- Available In A 46 Pin Hermetic Metal DIP
- Evaluation Board (THC1201E1C) Available

Applications

- Radar
- Data Acquisition Systems
- Digital Oscilloscopes
- Medical Imaging
- Communications
- CCD Digitization
- Transient Recorders
- Forward-Looking InfraRed Systems
- Focal Plane Arrays

Interface Diagram



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40G05736 Rev. D – 11/90
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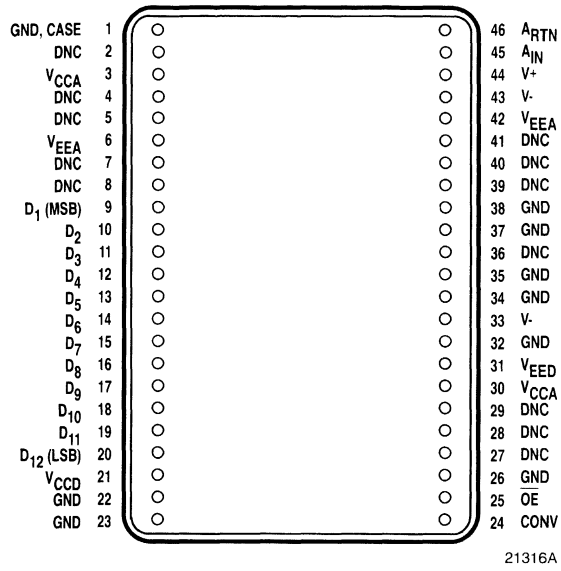
Pin Assignments



21316A

46 Pin Hermetic Metal DIP – S3 Package

Functional Description

General Information

The THC1201 is a complete 12-bit 10Msps A/D converter that features a wideband input amplifier, precision track/hold, voltage reference, timing circuitry and a three-state digital output register all housed in a 46 pin hermetic metal DIP. The device uses a two-step analog-to-digital converter architecture and proprietary components to achieve a 10Msps conversion rate and superior performance. The THC1201 is guaranteed to meet all specifications without additional adjustment or calibration. Additional information on applying the THC1201 is found in the TRW LSI Products Inc. *Application Note TP-45, "Designing with the THC1200 A/D Converter Family."*

Three-state TTL compatible outputs permit the THC1201 to drive a shared data bus directly. Data emerges from the THC1201 synchronously with respect to CONV. The digital output corresponding to the sample of the analog input signal is valid after the rising edge CONV. The THC1201 provides a 12-bit straight binary digital output as indicated in the *Output Coding Table*.

Power and Ground

The THC1201 requires four standard power supplies for operation: $V_{CCA}=V_{CCD}=+5V$, $V_{EEA}=V_{EED}=-5.2V$, $V+=+15V$, and $V-=-15V$. Linear regulated power supplies are preferred over switching power supplies for optimum performance. All power supply inputs to the THC1201 should be properly decoupled.

Separate analog and digital grounds are maintained within the the THC1201, but no distinction is made at the package pins. For optimum converter performance, all ground pins should be connected to a common solid ground plane. Wire-wrap breadboarding techniques are not recommended for use with this high-speed high-precision analog-to-digital converters. *Application Note TP-45, "Designing with the THC1200 A/D Converter Family,"* is recommended for additional information on using the THC1201.

Analog Input and Analog Input Return

The input voltage range of the THC1201 is from $-1.024V$ to $+1.024V$. This results in a least significant bit weight of 0.5mV. A 1 kOhm thin-film resistor is connected between A_{IN} and A_{RTN} and is provided for termination of analog input signals.

A_{RTN} is the internal ground reference point for internal analog circuitry and voltage references within the THC1201. In normal operation A_{RTN} should be connected to signal ground where the analog input signal connection is in close proximity to the THC1201. A_{RTN} should also be connected to power supply ground.

For applications where more dynamic range is required, the THC1200 is recommended. The THC1200 is similar to the THC1201 except that two user-selectable input voltage ranges are provided: $\pm 2.5V$ and $\pm 0.167V$.

CONV

Each rising edge of the CONV signal initiates conversion (See *Timing Diagram*). The THC1201 operates independently of the duty cycle of CONV as long as t_{PWH} and t_{PWL} limitations are not exceeded.

CONV clock jitter, t_{CJ}, must be minimized in order to optimize performance. Time errors in sampling a high slew rate (large $\Delta V/\Delta t$) signal appear as voltage errors in the conversion. The high-speed and precision of the THC1201 may reveal system timing errors (jitter) that would not be apparent with lower resolution converters (see *Application Note TP-45*).

Data Outputs and Output Enable

The 12 TTL compatible data outputs ($D_{1\text{-}12}$) provide straight binary data as shown in the ***Output Coding Table***. The output data becomes valid t_D after the rising edge of CONV, and remains valid until t_{HO} after the next rising edge of CONV. D_{12} is the least significant bit.

The output drivers become disabled (high-impedance) within t_{DIS} after the asynchronous input $\overline{OE}$ is switched HIGH. The outputs are enabled within t_{ENA} after $\overline{OE}$ is switched LOW.

Do Not Connect

DNC pins are used in factory calibration and must remain unconnected.

A

Package Interconnections

Signal Type	Function	Value	S3 Package Pins
V_{CCA}	Positive Analog Supply	+5.0V	3, 30
V_{CCD}	Positive Digital Supply	+5.0V	21
V_{EEA}	Negative Analog Supply	−5.2V	6, 42
V_{EED}	Negative Digital Supply	−5.2V	31
V+	Positive Supply	+15V	44
V−	Negative Supply	−15V	33, 43
GND	Ground	0.0V	1, 22, 23, 26, 32, 35, 37, 38
CONV	Convert Input	TTL	24
A_{IN}	Analog Input	±1.024V	45
A_{INRTN}	Analog Input Return	0.0V	46
D_1 (MSB)	Most Significant Bit	TTL	9
D_2		TTL	10
D_3		TTL	11
D_4		TTL	12
D_5		TTL	13
D_6		TTL	14
D_7		TTL	15
D_8		TTL	16
D_9		TTL	17
D_{10}		TTL	18
D_{11}		TTL	19
D_{12} (LSB)	Least Significant Bit	TTL	20
$\overline{OE}$	Output Enable Control	TTL	25
DNC	Do Not Connect	Open	2, 4, 5, 7, 8, 27, 28, 29, 36, 39, 40, 41

Output Coding Table

Input Voltage (Code Midpoint)	Digital Outputs MSB		LSB
+1.0240V	1111	1111	1111
+1.0235V	1111	1111	1110
+1.0230V	1111	1111	1101
•		•	
•		•	
•		•	
+0.0010V	1000	0000	0010
+0.0005V	1000	0000	0001
0.0000V	1000	0000	0000
−0.0005V	0111	1111	1111
−0.0010V	0111	1111	1110
•		•	
•		•	
•		•	
−1.0225V	0000	0000	0010
−1.0230V	0000	0000	0001
−1.0235V	0000	0000	0000

Note: 1. LSB Step = 2.048/4095 = 0.50mV.

Figure 1. Timing Diagram

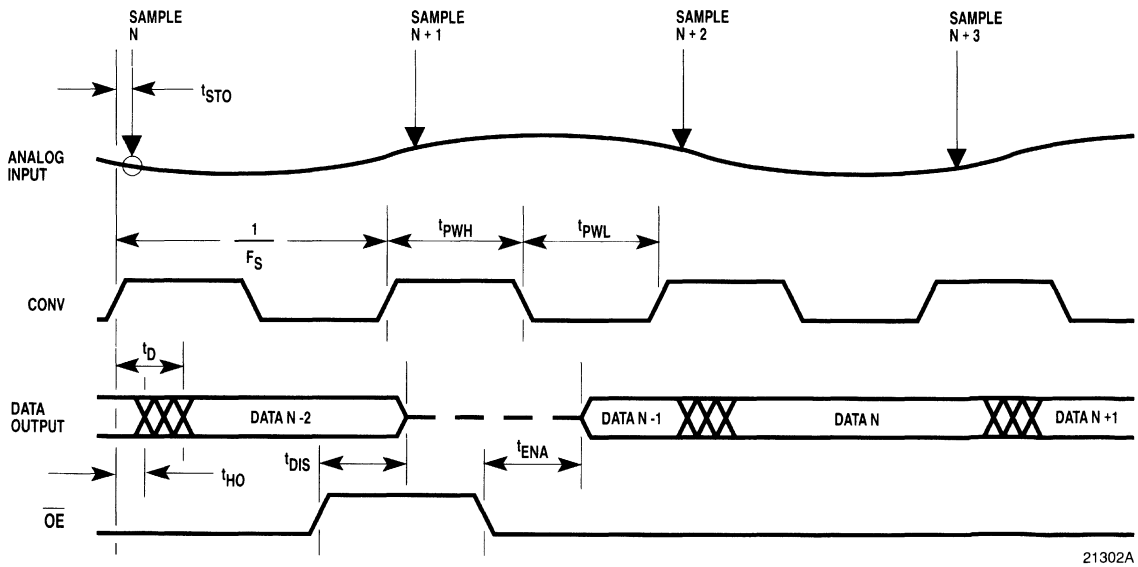


Figure 2. Simplified Analog Input Equivalent Circuit

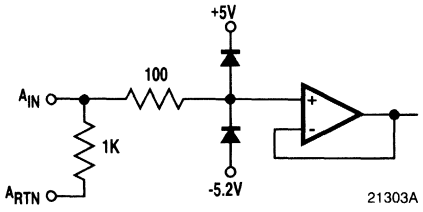
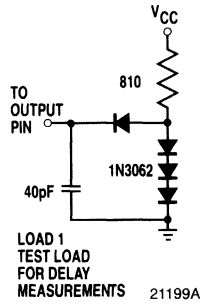


Figure 3. Standard TTL Test Load



A

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC}	−0.5 to +7.0V
V_{EE}	−7.0 to +0.5V
V+	−0.5 to +18.0V
V−	−18.0 to +0.5V

Input Voltages

A_{IN}	V_{EE} to V_{CC}
CONV, $\overline{OE}$	−0.5V to V_{CC}

Outputs

Digital outputs, applied voltage [2]	−0.5V to V_{CC}
applied current [3]	100mA
Short-circuit duration (single output to GND)	1 Second

Temperature

Operating, case	−60 to +130°C
Lead, soldering (10 seconds)	+300°C
Storage	−60 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating range. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. Applied voltage must be current limited to the specified range.
3. Forcing voltage must be limited to the specified range.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{CC}	Positive Supply Voltage	4.7	5.0	5.3	V
V_{EE}	Negative Supply Voltage	−4.9	−5.2	−5.5	V
V+	Positive Supply Voltage	11.4	12.0	16.5	V
V−	Negative Supply Voltage	−11.4	−12.0	−16.5	V
t_{PWH}	CONV Pulse Width, HIGH	30			ns
t_{PWL}	CONV Pulse Width, LOW	40			ns
F_S	Conversion Rate			10	Msps
t_{CJ}	CONV Clock Jitter			10	ps_{rms}
V_{IH}	Input Voltage, Logic HIGH	2.0			V
V_{IL}	Input Voltage, Logic LOW			0.8	V
A_{IN}	Analog Input Range	−1.024		+1.024	V
I_{OH}	Output Current, Logic HIGH			−0.4	mA
I_{OL}	Output Current, Logic LOW			4.0	mA
T_C	Case Temperature, B-Grade	−25		85	°C
T_C	Case Temperature, V-Grade	−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Ind/Mil Typ	Industrial Min	Industrial Max	Military Min	Military Max	Units
I_{CC}	Total V_{CC} Power Supply Current		525		650		650	mA
I_{EE}	Total V_{EE} Power Supply Current		−460		−600		−600	mA
I+	Total V+ Power Supply Current		15		50		50	mA
I−	Total V− Power Supply Current		−20		−50		−50	mA
I_{IL}	Input Current, Logic LOW	CONV			350		350	μA
		$\overline{OE}$			100		100	μA
I_{IH}	Input Current, Logic HIGH	CONV		−1.8		−2.8	−2.8	mA
		$\overline{OE}$		−0.5		−0.8	−0.8	mA
V_{OL}	Output Voltage, Logic LOW	I_{OL} = Max	0.2		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	I_{OH} = Max	3.4	2.4		2.4		V
I_{OZL}	Output Leakage Current, Logic LOW	$\overline{OE}$ = HIGH			±150		±150	μA
I_{OZH}	Output Leakage Current, Logic HIGH	$\overline{OE}$ = HIGH			±150		±150	μA
I_{OS}	Short-Circuit Current	Note 1	−50	−30	−100	−30	−100	mA
R_{IN}	Analog Input Resistance	A_{RTN} to GND	1000	975	1025	975	1025	Ohms
C_{IN}	Input Capacitance	All Inputs			10		10	pF
V_{OS}	Offset Voltage	Note 2			±25		±25	mV
V_{FP}	Full-Scale Positive Input	Note 3	1.024	0.973	1.075	0.973	1.075	V
V_{FN}	Full-Scale Negative Input	Note 4	−1.024	−0.973	−1.075	−0.973	−1.075	V

Notes:
1. 1 second max, one pin shorted to ground.
2. A_{IN} at mid-scale code transition.
3. A_{IN} at 1/2 LSB above most positive transition.
4. A_{IN} at 1/2 LSB below most negative transition.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range					Units
			Ind/Mil	Industrial		Military		
			Typ	Min	Max	Min	Max	
F_S	Maximum Conversion Rate			10			10	Msps
t_{STO}	Sampling Time Offset		−3.0	−6.0	0.0	−6.0	0.0	ns
t_D	Data Output Delay Time	C_{LOAD} = 50pF Max	20		50		50	ns
t_{HO}	Data Output Hold Time	C_{LOAD} = 50pF Max	19	5		5		ns
t_{ENA}	Output Enable Time	C_{LOAD} = 50pF Max	12		40		40	ns
t_{DIS}	Output Disable Time	C_{LOAD} = 50pF Max	20		40		40	ns

A

Thermal characteristics within specified operating conditions

Parameter		Max	Units
ΔT_{JC}	Junction-to-Case Temperature Rise (Worst Case Power Dissipation)	20	°C
Θ_{CA}	Case-to-Ambient Thermal Resistance		
	Still Air	10	°C/W
	500 LFPM Airflow	6	°C/W

System performance characteristics within specified operating conditions

Parameter		Test Conditions [1]	Temperature Range					Units
			Ind/Mil	Industrial		Military		
			Typ	Min	Max	Min	Max	
E_{LI}	Linearity Error, Integral	Independent Based	1.6		±3.0		±3.0	LSB
E_{LD}	Linearity Error, Differential	F_{IN} = 100kHz	0.3		±0.75		±0.75	LSB
SNR	Signal-to-Noise Ratio	F_{IN} = 540kHz	69.6	66.5		66.2		dB
		F_{IN} = 2.3MHz	69.4	66.0		66.0		dB
		F_{IN} = 5.0MHz	68.0	64.2		64.0		dB
SINAD	Signal-to-Noise-	F_{IN} = 540kHz	67.0	60.2		57.2		dB
	and-Distortion Ratio	F_{IN} = 2.3MHz	65.7	58.0		58.0		dB
	(Includes Noise and Distortion)	F_{IN} = 5.0MHz	63.2	58.0		57.1		dB
THD	Total Harmonic Distortion	F_{IN} = 540kHz	−70.6		−61.0		−57.5	dBc
		F_{IN} = 2.3MHz	−68.3		−58.3		−58.5	dBc
		F_{IN} = 5.0MHz	−64.2		−58.6		−58.0	dBc
SFDR	Spurious-Free Dynamic Range	F_{IN} = 540kHz	72.3	62.5		59.0		dB
		F_{IN} = 2.3MHz	71.0	59.2		59.2		dB
		F_{IN} = 5.0MHz	66.6	60.5		60.5		dB
BW	Analog −3dB Bandwidth	V_{IN} = 2Vp-p		70		70		MHz
		V_{IN} = 0.2Vp-p		70		70		MHz
E_{AP}	Aperture Jitter				±5		±5	ps

Note: 1. All tests conditions conducted at F_S = 10Msps, $V_{CC} = V_{EE}$ = Nom.

System performance characteristics within specified operating conditions (cont.)

Parameter		Test Conditions	Temperature Range					Units
			Ind/Mil	Industrial		Military		
			Typ	Min	Max	Min	Max	
SC	Spurious Codes				0		0	Codes
MC	Missing Codes				0		0	Codes
t_{TR}	Transient Response Time	Full-Scale Transition	20		30		30	ns
t_{OR}	Overload Recovery Time	100% Overdrive	20		100		100	ns
E_G	Gain Error		±0.5		±2		±2	%FS

Signal Definitions

SNR (Signal-to-Noise Ratio)

The ratio, expressed in decibels, of the RMS level of the output signal to the RMS level of the in-band noise. This noise is measured with the signal present and excludes harmonic distortion products.

THD (Total Harmonic Distortion)

The ratio, expressed in decibels, of the RMS sum of the first 10 harmonics of the output fundamental to the RMS level of the output fundamental.

SINAD (Signal-to-Noise and Distortion Ratio)

The ratio, expressed in decibels, of the RMS level of the output signal to the RMS sum of both the in-band noise and the RMS sum of the first 10 harmonics of the output fundamental.

SFDR (Spurious-Free Dynamic Range)

The ratio, expressed in decibels, of the RMS level of the output fundamental to the RMS level of the largest spurious signal.

IMD (Intermodulation Distortion)

The ratio, expressed in decibels, of the largest output frequency spur to either of the two equal-level output fundamentals.

t_{TR} (Transient Response Time)

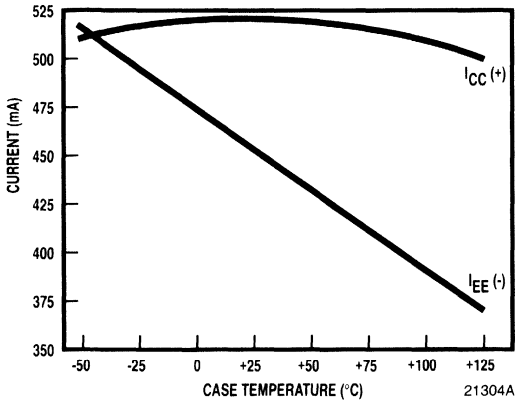
The time required to begin returning accurate data after a full-scale input voltage step whose initial and final voltages are within the analog input range. t_{TR} is an analog domain parameter and excludes pipeline latency.

t_{OR} (Overload Recovery Time)

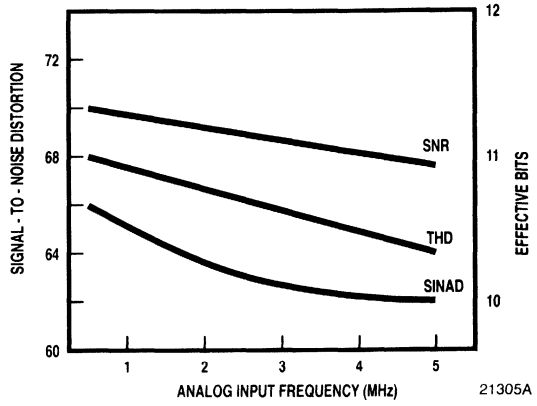
The time required to begin producing accurate data after the input voltage returns to the allowable range, following an excursion to 200% of either full-scale limit. t_{OR} is an analog domain parameter and excludes pipeline latency.

Typical Performance Curves

A. Typical Power Supply Current vs. Temperature



B. Typical SINAD, SNR and Distortion vs. Analog Input Frequency ($F_S = F_S = 10MSPS$)



C. Typical Output Spectrum

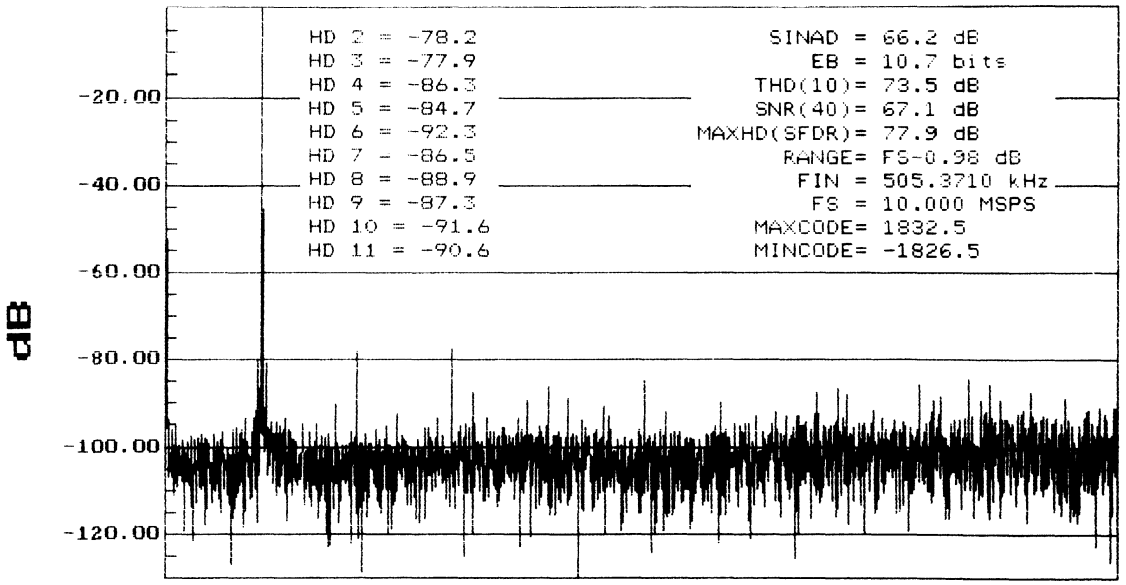
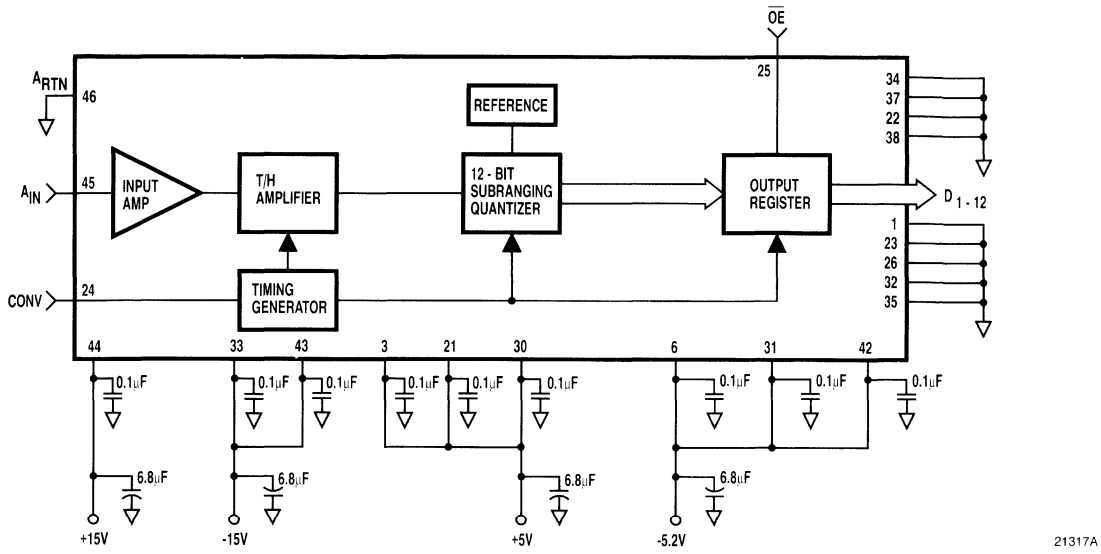


Figure 4. Typical Interface Circuit



Evaluation Board

The THC1201E1C is a Eurocard-style printed circuit board designed to aid in the evaluation of the THC1201 A/D converter. The board dimensions are 100mm x 160mm with a standard 64 pin double-row DIN male connector installed. A complementary 64 pin double-row DIN female connector is included with the board.

The board employs only two conducting sides. Most of the circuit interconnections are on the bottom of the board while the top is mostly solid ground plane. SMA connectors are installed on the board to facilitate analog I/O and clocks. The circuitry on the board includes all power supply decoupling required for the THC1201, and a TDC1012 12-bit D/A converter which may be used in evaluating certain parameters of the THC1201. Additional information on applying the THC1201 is found in *Application Note TP-45, "Designing with the THC1200 A/D Converter Family."*

The THC1201E1C board has been designed to be used, not only for the THC1201, but also for the THC1200 and THC1202 A/D converters. Therefore, the board has interconnect patterns for some circuitry that is not used by the THC1201. Jumpers J3, J4, J5, J7, J8 and FT will be installed while all others are not.

The board is calibrated and tested at the factory and is supplied complete with THC1201 and TDC1012 installed.

Power and Ground

Four power supply voltages are required for the operation of the THC1201E1C: $V_{CC} = +5V$, $V_{EE} = -5.2V$, $V+ = +15V$ and $V- = -15V$. All power inputs are decoupled to a single solid ground plane, GND. All GND pins of the board are connected to the ground plane and it is recommended that all GND pins be used.

A/D Converter Inputs

The clock to the THC1201, CONV, is normally brought onto the board by way of an SMA connector labeled "CONV" near pin 24 of the THC1201. A location for a terminating resistor, R20 is available on the board for terminating cables. CONV may be brought onto the board through the edge-connector pin B2 by installing jumper J9.

The analog signal input to the THC1201, A_{IN} is normally brought onto the board by way of an SMA connector labeled "A_{IN}" near pin 45 of the THC1201. A resistor network, R13 through R16, is included on the board for terminating and attenuating the signal in user-determined impedances and losses.

A/D Converter Data Outputs and D/A Converter Data Inputs

The 12 data outputs of the THC1201 are brought to edge-connector pins B9 through B21 (excluding B18). These pins are located directly across the edge-connector from the 12 data inputs of the TDC1012 D/A converter to simplify connection of A/D outputs to D/A inputs.

D/A Converter Inputs

The clock to the TDC1012, CLK, is normally brought onto the board through an SMA connector labeled "CLK" near pin 16 of the TDC1012. A location for a terminating resistor, R6 is provided for clock cable termination. The clock input to the TDC1012 is also brought to the edge-connector pin B24.

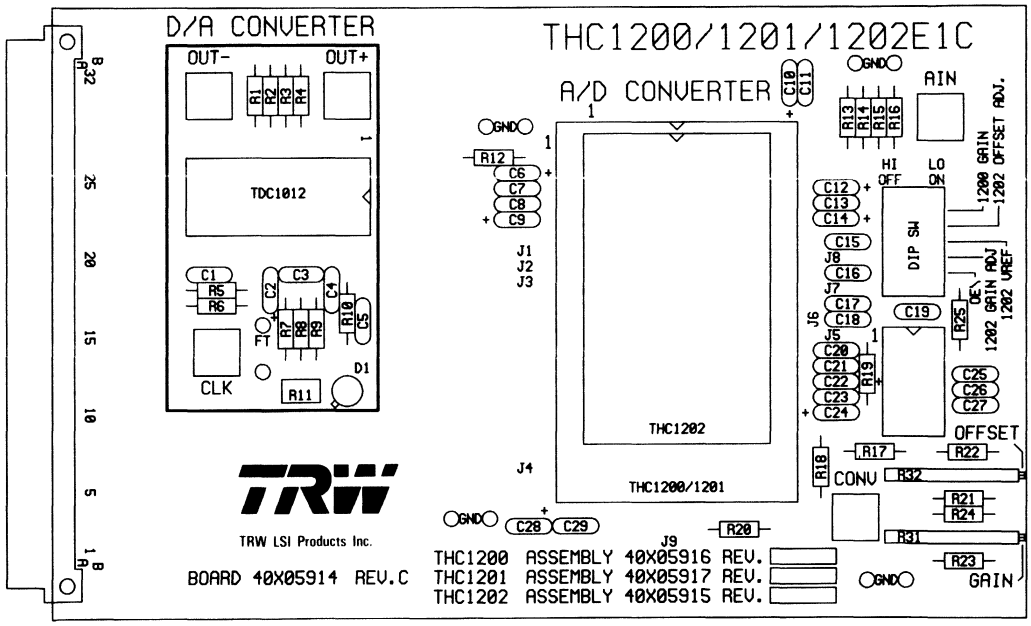
D/A converter outputs are brought to SMA connectors labeled OUT+ and OUT– as well as edge-connector pins B28 and B27. Load resistors of 51.1Ω are provided on the board to facilitate 50Ω cable connection to the board.

Potentiometer R11 is used to adjust the reference voltage to the TDC1012. This voltage is adjusted to −1.0V as part of the factory test and calibration procedure.

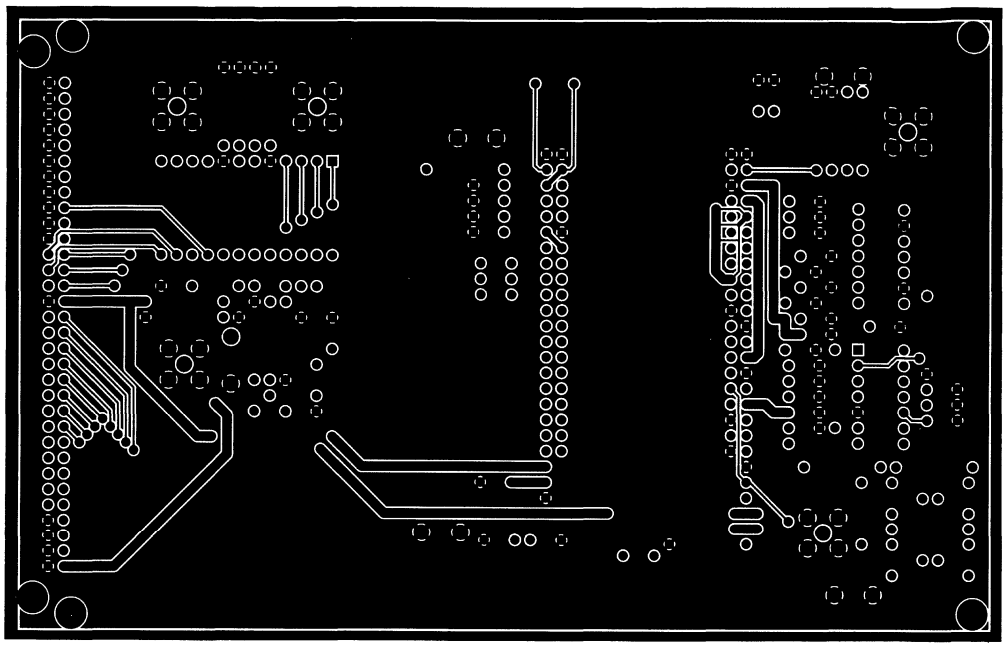
Removing the jumper in the location labeled "FT" will put the TDC1012 into feedthrough (unclocked) mode. This eliminates the requirement for a D/A clock signal but will degrade the fidelity of the TDC1012 signal reconstruction.

A

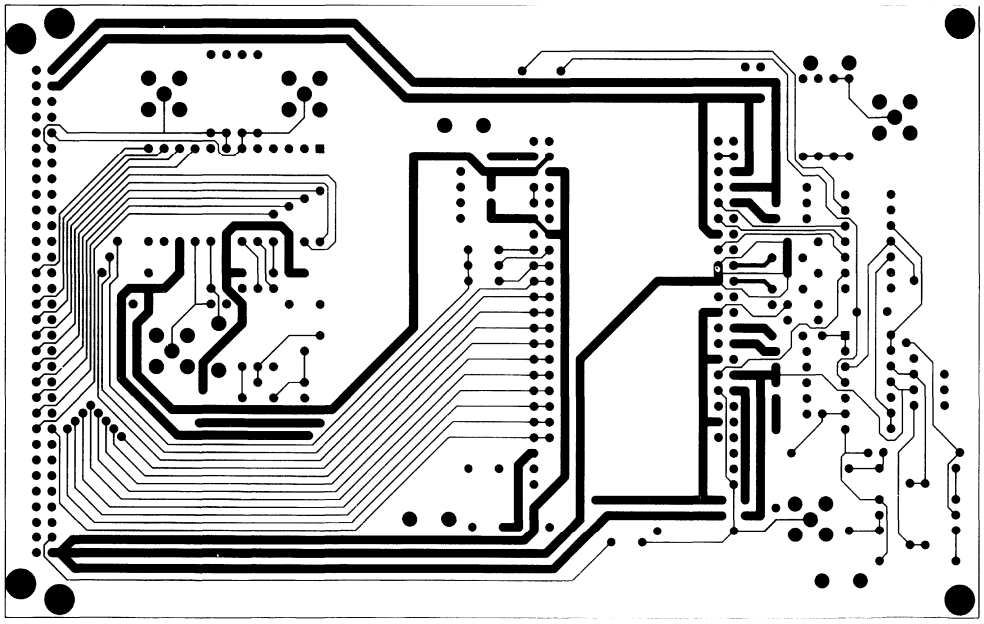
THC1201E1C Silkscreen Layout



THC1201E1C Component Side Layout



THC1201E1C Circuit Side Layout



THC1201E1C Eurocard Edgeconnector Pinout

GND	A32	B32	V– (–15V)
GND	A31	B31	V+ (+15V)
GND	A30	B30	N/C
GND	A29	B29	N/C
GND	A28	B28	D/A OUT+
GND	A27	B27	D/A OUT–
GND	A26	B26	N/C
GND	A25	B25	N/C
GND	A24	B24	D/A CLK
GND	A23	B23	N/C
GND	A22	B22	N/C
D/A D_1 MSB	A21	B21	A/D D_1 MSB
D/A D_2	A20	B20	A/D D_2
D/A D_3	A19	B19	A/D D_3
GND	A18	B18	V_{CC} (+5V)
D/A D_4	A17	B17	A/D D_4
D/A D_5	A16	B16	A/D D_5
D/A D_6	A15	B15	A/D D_6
D/A D_7	A14	B14	A/D D_7
D/A D_8	A13	B13	A/D D_8
D/A D_9	A12	B12	A/D D_9
D/A D_{10}	A11	B11	A/D D_{10}
D/A D_{11}	A10	B10	A/D D_{11}
D/A D_{12} LSB	A9	B9	A/D D_{12} LSB
N/C	A8	B8	N/C
N/C	A7	B7	N/C
N/C	A6	B6	N/C
N/C	A5	B5	N/C
GND	A4	B4	N/C
GND	A3	B3	N/C
GND	A2	B2	A/D CONV
GND	A1	B1	V_{EE} (–5.2V)

Mating Connectors for THC1201E1C

AMP	532507-2	Wire-wrap
AMP	532507-1	Solder tail
Robinson-Nugent	RNE-64BS-W-TG30	Wire-wrap
Robinson-Nugent	RNE-64BS-S-TG30	Solder tail
Souriau	8609-264-6115-7550E1	Wire-wrap
Souriau	8609-264-6114-7550E1	Solder tail
Souriau	8609-264-6813-7550E1	Solder tail, right-angle bend

A

Figure 5. THC1201E1C A/D Converter Schematic Diagram

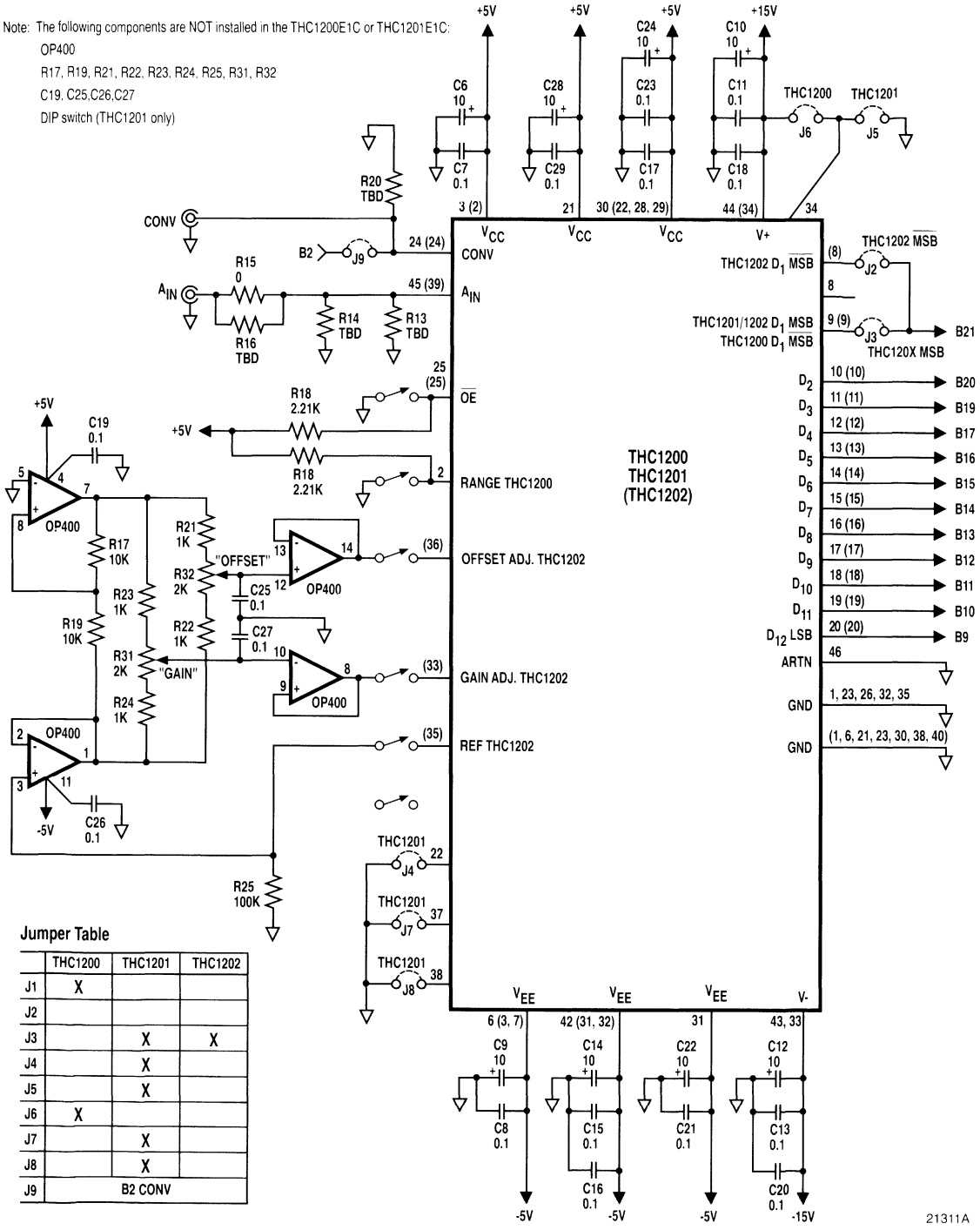
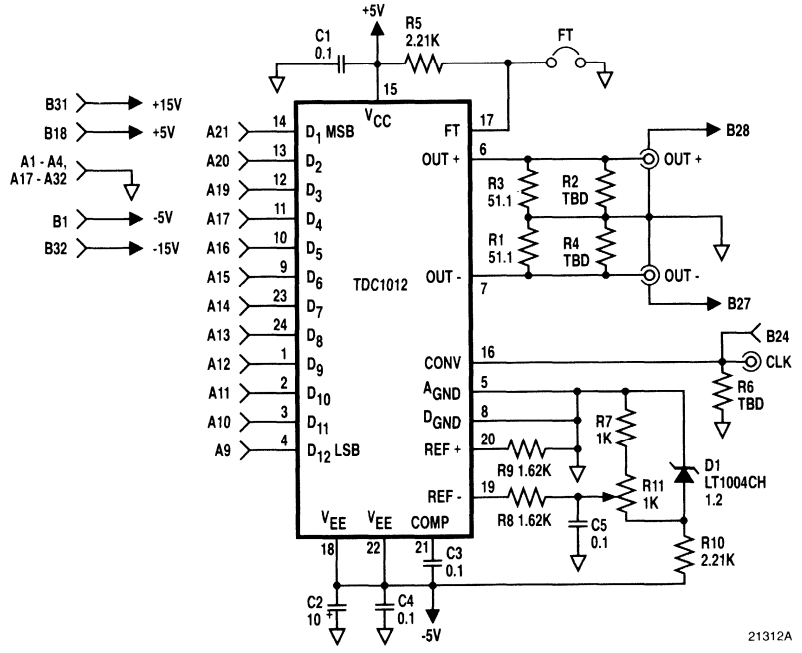


Figure 6. THC1201E1C D/A Converter Schematic Diagram



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
THC1201S3B	IND – T_C = –25°C to 85°C	Industrial	46 Pin Hermetic Metal DIP	1201S3B
THC1201S3V	EXT – T_C = –55°C to 125°C	MIL-STD-883	46 Pin Hermetic Metal DIP	1201S3V
THC1201E1C	STD – T_A = 0°C to 70°C	– –	Eurocard Format Board with Industrial Grade A/D Converter	THC1201E1C

THC1202

Complete High-Speed A/D Converter

12-Bit, 10Msps

The THC1202 is a complete 12-bit 10Msps analog-to-digital converter that includes all the circuitry required to digitize signals within a DC to 70MHz band. With its subranging two-step architecture, the THC1202 achieves a very high conversion rate and superior performance. The device contains a wideband input amplifier, a precision track-and-hold, an analog-to-digital quantizer, a voltage reference, a precision timing generator and registered three-state TTL output drivers for simplified system interface.

The THC1202 offers significant advantages over previous converter boards in space efficiency, ease of use, power dissipation, DC and AC performance, and reliability. Since the THC1202 is a complete 12-bit A/D converter, it reduces system assembly and final test costs.

Designed to meet demanding requirements, the THC1202 is housed in a hermetic 40 pin DIP. Specified performance is guaranteed over the industrial (−25 to 85°C case) and extended (−55 to 125°C case) temperature ranges. Military-grade parts comply with MIL-STD-883C and are manufactured in facilities certified and qualified to MIL-STD-1772.

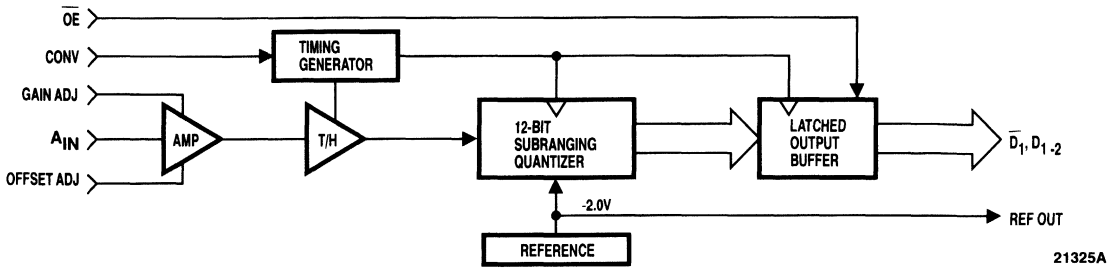
Features

- Conversion Rate DC To 10Msps
- Large-Signal Bandwidth >70MHz
- No Missing Codes, Guaranteed
- 4.5W Typical Power Dissipation
- +5V, −5.2V And +15V Power Supplies
- SNR=67dB At 10Msps With 5MHz Input
- Analog Input Range −1V To +1V Or 2Vp-p Within −2V to +2V Window
- Gain And Offset Internally Trimmed And Externally Adjustable
- TTL Compatible Input And Three-State Outputs
- 40 Pin 1.1" Wide Hermetic Ceramic DIP
- Evaluation Board (THC1202E1C) Available

Applications

- Radar
- Digital Oscilloscopes
- Medical Imaging
- Communications
- CCD Digitization
- Transient Recorders
- Forward-Looking InfraRed Systems
- Focal Plane Arrays

Functional Block Diagram



TRW LSI Products Inc.
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La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

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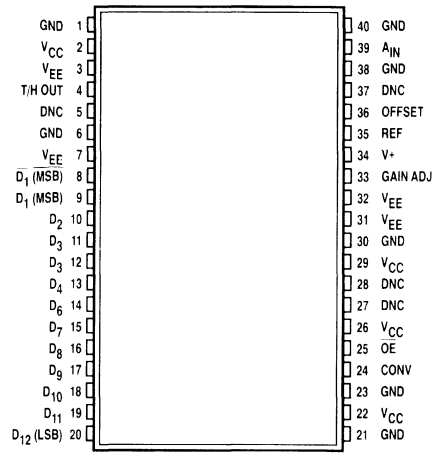
Printed in the U.S.A.

Pin Assignments



40 Pin Hermetic Ceramic DIP – S6 Package

Functional Description

General Information

The THC1202 is a complete 12-bit 10Msps A/D converter that features an input amplifier, track-and-hold (T/H), precision voltage reference, timing circuitry and a three-state digital output register in a 40 pin hermetic ceramic DIP. The device uses a sub-ranging architecture and proprietary components to achieve 10Msps Nyquist sampling.

The laser-trimmed THC1202 is guaranteed to meet data sheet specifications without additional adjustment or calibration. The GAIN ADJust pin may be used to vary the analog input range between 1.8 and 2.2Vp-p, and the OFFSET ADJ pin may be used to shift this range anywhere within a $-2V$ to $+2V$ overall limit. As indicated in the ***Output Coding Table***, the THC1202 provides 12-bit offset binary (using the non-inverted MSB output) or two's complement (using the inverted MSB output) digital outputs.

Three-state TTL compatible outputs permit the THC1202 to drive a shared data bus directly. At the output pins, the digital equivalent of the sample taken at t_{STO} after CONVert rising edge N is valid from t_D after CONVert rising edge N+2 until t_{HO} after CONVert rising edge N+3. (See the *Timing Diagram*.)

Power

The THC1202 requires $V_{CC} = +5V$, $V_{EE} = -5.2V$ and $V+ = +15V$ power supplies, preferably from linearly regulated (as opposed to switching) power supplies. All power supply lines should be properly decoupled.

Grounds

The layout of system grounding is as important as the layout of any other signal path. Separate analog and digital grounds are maintained within the THC1202 but no distinction is made at the package pins. For optimal converter performance, all ground pins should be connected to a common low-noise solid ground plane. Wire-wrap is not recommended for use with any high-speed high-precision analog circuit.

Reference Output (Pin 35)

The REFerence OUTput pin is the precision internal $-2.000V$ reference. This pin can drive a 1000Ω load (2mA) directly without affecting the THC1202's performance.

Analog Input (Pin 39)

The Analog Input pin (A_{IN}) has a minimum input resistance of $100k\Omega$ and a maximum input capacitance of 10pF (*Figure 2*). The input amplifier's $-3dB$ bandwidth of 70MHz minimizes phase distortion. The proprietary track-and-hold has a typical aperture jitter of 5ps. The input voltage range is $-1V$ to $+1V$ with no offset applied (OFFSET ADJ pin grounded) and may be offset to cover any 2Vp-p range in a $+2V$ to $-2V$ window. See the ***OFFSET*** section. Great care must be paid to circuit board layout to prevent the digital signals, which are high-amplitude fast-risetime wave-forms, from corrupting the analog signal paths.

Offset Adjustment (Pin 36)

The OFFSET ADJust pin allows the 2.0Vp-p input range to be shifted anywhere within a $-2.0V$ to $+2.0V$ window. If unused, the pin MUST be grounded, leaving the analog input range at $-1.0V$ to $+1.0V$. A $+2.0V$ or $-2.0V$ DC input will shift the input range by $\pm 1.0V$, providing a unipolar input. If OFFSET ADJ is connected to REF OUT ($-2.0V$), the input range is $-2.0V$ to 0.0V. If OFFSET ADJ is connected to $+2.0V$, as shown in *Figure 4*, the input range is 0.0V to $+2.0V$. The performance of the THC1202 is specified with OFFSET ADJ grounded. Input impedance at this pin is $500\Omega \pm 100\Omega$ to ground.

Gain Adjustment (Pin 33)

The full-scale peak-to-peak analog input range may be adjusted up to ±10% by using the GAIN ADJust pin. If unused, GAIN ADJ MUST be grounded and the full-scale analog input range will be 2.0Vp-p. (The performance of the THC1202 is specified with GAIN ADJ grounded.)

If GAIN ADJ is connected to REF OUT (−2.0V), the input range is compressed to 1.8Vp-p, and the system gain is correspondingly increased. If GAIN ADJust is connected to +2.0V, the input range is expanded to 2.2Vp-p, and the system gain is correspondingly reduced. A simple circuit that allows continuous adjustment of the input range using the THC1202's internal reference is shown in ***Figure 4***. If the maximum offset is used (giving a 0V to +2.0V or −2.0V to 0V range) and the largest peak-to-peak input range is selected, the allowable input range becomes −0.1V to 2.1V or −2.1V to +0.1V. Input impedance at this pin is 8700Ω.

Convert (Pin 24)

Each rising edge of the CONVert signal initiates conversion (***Figure 1***), which is independent of the CONVert duty cycle (within the limits allowed by minimum t_{PWH} and t_{PWL}). Failure to observe the minimum t_{PWL} specification will reduce SNR, since the T/H will not have adequate time to acquire the analog input signal to 12-bit accuracy. CONVert clock jitter, t_{CJ}, must be less than 10ps. A crystal oscillator or high performance synthesizer (e.g., HP8662) triggering a pulse generator can supply the necessary CONVert signal. High frequency performance of any A/D may suffer if the clock signal has excess jitter. Time errors in sampling a high slew rate (large $\Delta V/\Delta T$) signal appear as voltage errors in the digital datastream. The high-speed and precision of the THC1202 may show system timing errors (jitter) that were not apparent with lower resolution converters.

T/H Output (Pin 4)

The T/H OUTput pin, used by the manufacturer for calibration, is not recommended for other uses. Any noise or loading introduced here will degrade the dynamic performance of the converter.

Output Enable (Pin 25)

The output drivers become disabled (high-impedance) within t_{DIS} after the asynchronous input $\overline{OE}$ is brought HIGH, and are enabled within t_{ENA} after $\overline{OE}$ is brought LOW. $\overline{OE}$ MUST be grounded if unused.

Data (Pins 8 through 20)

The 13 data output pins ($D_{1\text{-}12}$, $\overline{D_1}$) are TTL compatible. $D_{1\text{-}12}$ provide offset binary data, whereas connecting $\overline{D_1}$ instead of D_1 yields two's complement data. Each new output becomes valid t_D after the rising edge of CONVert, and remains valid until t_{HO} after the next rising edge of CONVert.

Do Not Connect (Pins 5, 27, 28, and 37)

These pins used in factory calibration must remain unconnected (open).

Unused Functions

D_1 or $\overline{D_1}$ and REF OUT should be left open if unused. $\overline{OE}$, GAIN ADJ and OFFSET ADJ should be connected to ground if unused.

Package Interconnections

Name	Function	Value	S6 Package Pins
V_{CC}	Positive Supply Voltage	+5.0V	2, 22, 26, 29
V_{EE}	Negative Supply Voltage	−5.2V	3, 7, 31, 32
V+	Positive Supply Voltage	+15V	34
GND	Ground	0.0V	1, 6, 21, 23, 30, 38, 40
T/H OUT	Track and Hold Output	See Text	4
REF OUT	Reference Output	−2.000V	35
GAIN ADJ	Gain Adjust Input	−2V to +2V	33
OFFSET ADJ	Offset Adjust Input	−2V to +2V	36
CONV	Convert (Clock) Input	TTL	24
A_{IN}	Analog Input	2Vp-p, See Text	39
$\overline{D_1}$ (MSB)	Most Significant Bit Output	TTL	8
D_1 (MSB)	Most Significant Bit Output	TTL	9
D_2		TTL	10
D_3		TTL	11
D_4		TTL	12
D_5		TTL	13
D_6		TTL	14
D_7		TTL	15
D_8		TTL	16
D_9		TTL	17
D_{10}		TTL	18
D_{11}		TTL	19
D_{12}	Least Significant Bit Output	TTL	20
$\overline{OE}$	Output Enable Control	TTL	25
DNC	Do Not Connect	Open	5, 27, 28, 37

Output Coding Table

Input Voltage Midpoint	Offset Binary			Two's Complement		
	MSB		LSB	$\overline{MSB}$		LSB
+0.9995V	1111	1111	1111	0111	1111	1111
+0.9990V	1111	1111	1110	0111	1111	1110
•		•			•	
+0.0005V	1000	0000	0001	0000	0000	0001
0.0000V	1000	0000	0000	0000	0000	0000
−0.0005V	0111	1111	1111	1111	1111	1111
•		•			•	
−0.9990V	0000	0000	0010	1000	0000	0010
−0.9995V	0000	0000	0001	1000	0000	0001
−1.0000V	0000	0000	0000	1000	0000	0000

Notes:
1. Step size = 1 LSB = 0.488mV = 0.0244%FS.
2. Analog input range shown off-center by −0.244mV (1/2 LSB) to accommodate two's complement asymmetry (2047 positive steps, 2048 negative steps).

Output Coding vs. Input Voltage

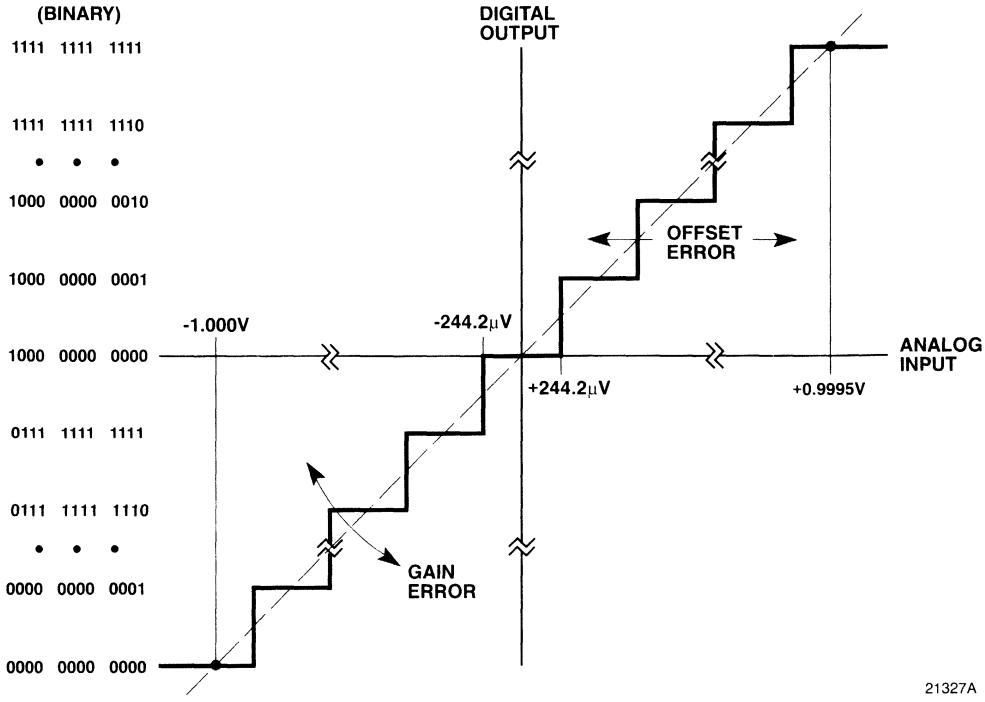


Figure 1. Timing Diagram

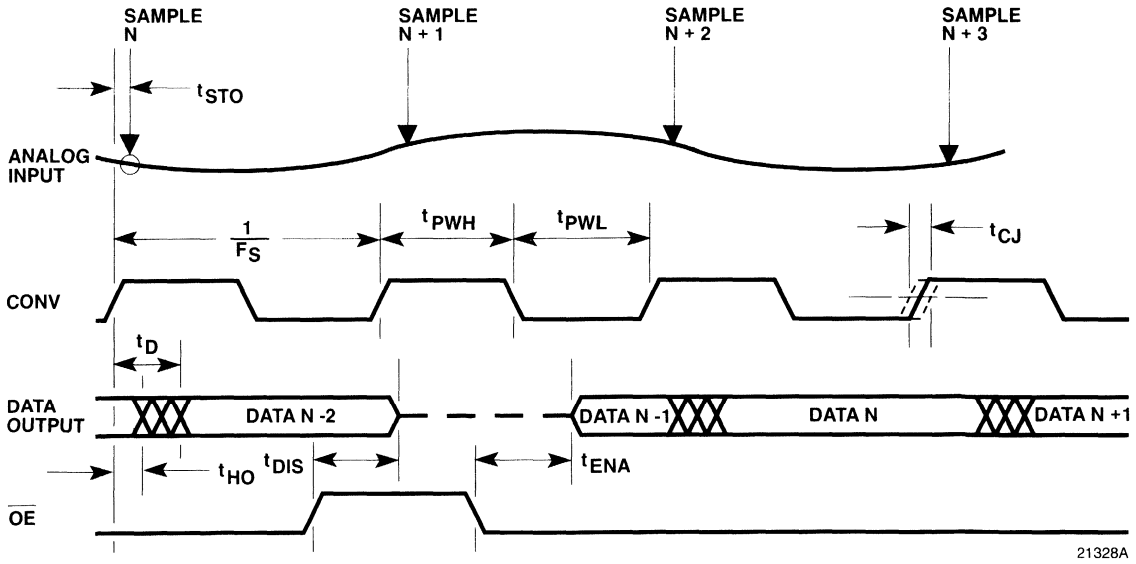


Figure 2. Simplified Analog Input Equivalent Circuit

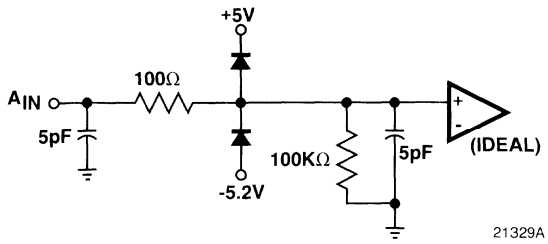


Figure 3. Standard TTL Test Load

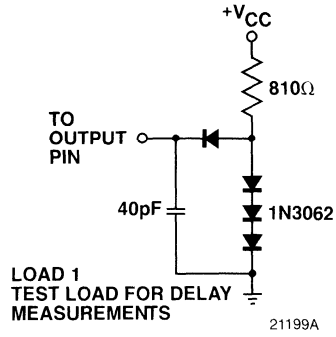
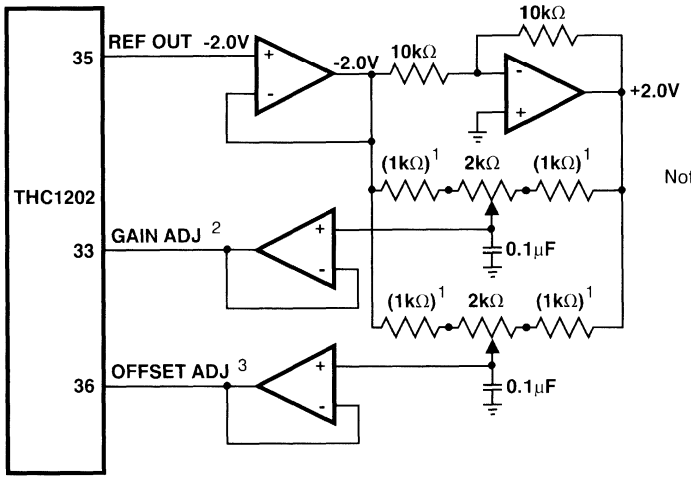


Figure 4. Optional Gain and/or Offset Adjust Circuit



Notes: 1. Select values to provide desired range of adjustment.

2. ±2V @ **GAIN ADJ** (pin 33) results in a ±10% gain change.

3. ±2V @ **OFFSET ADJ** (pin 36) results in a ±1V offset variation.

4. Op Amp is PMI OP-400 or other quad low noise, low offset device.

21330A

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{CC}	−0.5 to +7.0V
V_{EE}	−7.0 to +0.5V
V+	−0.5 to +18.0V

Input Voltages

A_{IN}	V_{EE} to V_{CC}
CONV, $\overline{OE}$	−0.5V to V_{CC}

Outputs

Digital outputs, applied voltage [2]	−0.5V to V_{CC}
Digital outputs, applied current [3]	100mA
Short-circuit duration (single output to ground)	1 Second

Temperature

Operating, case	−60 to +130°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.

Operating conditions

Parameter		Temperature Range						Units
		Industrial			Military			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V+	Positive Supply Voltage	13.5	15.0	16.5	13.5	15.0	16.5	V
t_{PWH}	CONV Pulse Width HIGH	30			30			ns
t_{PWL}	CONV Pulse Width LOW	30			30			ns
F_S	Conversion Rate	0		10	0		10	Msps
t_{CJ}	CONVert Clock Jitter			10			10	ps_{rms}
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{REF}	Reference Output Current	0		2.0	0		2.0	mA
A_{IN}	Analog Input Range	−1.0		+1.0	−1.0		+1.0	V
T_C	Case Temperature	−25		85	−55		125	°C

Electrical characteristics within specified operating conditions at nominal supply voltages

Parameter		Test Conditions	Temperature Range				Units
			Typ	Limits (Min or Max)			
T_C	Case Temperature	Industrial	+25	−25	+25	+85	°C
		Military		−55	+25	+125	°C
I_{CC}	Positive Supply Current	10Msps, No Load	500	640	600	560	mA
I_{EE}	Negative Supply Current	10Msps, No Load	440	700	630	550	mA
I+	V+ Supply Current	10Msps, No Load	21	30	30	30	mA
P_D	Power Dissipation	10Msps, No Load	4.5				W
V_{OS}	Offset Voltage Error	Note 1	3.4	30	10	12	mV
E_{GAIN}	Gain Error	Note 1	0.3	2.7	1.0	1.5	%FS
E_{REF}	Reference Voltage Error	Variation of REF OUT from 2.000V	2	10	10	10	mV
R_{IN}	Analog Input Resistance		150	50	85	85	kOhms
C_{IN}	Analog Input Capacitance		3.5	5.5	5.5	5.5	pF
I_B	Input Bias Current		10	45	25	35	μA
I_{IH}	Digital Input Current	Logic HIGH	80	350	350	350	μA
I_{IL}	Digital Input Current	Logic LOW	−1.9	−2.8	−2.8	−2.8	mA
V_{OH}	Digital Output Voltage	Logic HIGH, $I_{OH}=-1$mA	3.2	2.4	2.4	2.4	V
V_{OL}	Digital Output Voltage	Logic LOW, $I_{OL}=4$mA	0.2	0.5	0.5	0.5	V
I_{OZH}	Digital Output Leakage Current	Logic HIGH, $\overline{OE}$=HIGH	5	150	150	150	μA
I_{OZL}	Digital Output Leakage Current	Logic LOW, $\overline{OE}$=HIGH	5	150	150	150	μA
I_{OS}	Short-Circuit Output Current	Digital Outputs		−100	−100	−100	mA

Note: 1. GAIN ADJ and OFFSET ADJ pins grounded.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Typ	Limits (Min or Max)			
T_C	Case Temperature	Industrial	+25	−25	+25	+85	°C
		Military		−55	+25	+125	°C
t_{STO}	Sampling Time Offset		1.2	3.0	2.5	3.0	ns
t_D	Data Output Delay	Standard TTL Test Load, Figure 4	25	35	35	35	ns
t_{HO}	Data Output Hold Time	Standard TTL Test Load, Figure 4	15	10	10	10	ns
t_{ENA}	Output Enable Delay		16	30	30	30	ns
t_{DIS}	Output Disable Delay		45	60	60	60	ns
t_P	Pipeline Latency		2	2	2	2	Cycles

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Typ	Limits (Min or Max)			
T_C	Case Temperature	Industrial	+25	−25	+25	+85	°C
		Military		−55	+25	+125	°C
E_{LI}	Linearity Error, Integral	Note 1	1.2	4.0	4.0	4.0	LSB
E_{LD}	Linearity Error, Differential		0.35	1.0	1.0	1.0	LSB
TC_O	Offset Error, Temperature Coefficient	Note 5		300		150	μV/°C
TC_G	Gain Error, Temperature Coefficient	Note 5		.035		.010	%FS/°C
TC_{IB}	Input Bias Current, Temperature Coefficient		100	250		100	μA/°C
SNR	Signal-to-Noise Ratio	F_S = 10Msps,					
		A_{IN} = 404kHz	67.5	64.5	65	65	dB
		A_{IN} = 4.996MHz	66.6	63.5	65	65	dB
SINAD	Signal-to-Noise and Distortion	Note 2,					
		A_{IN} = 404kHz	65	59	61	61	dB
		A_{IN} = 4.996MHz	62	57	59	56.5	dB
THD	Total Harmonic Distortion	Note 2,					
		A_{IN} = 404kHz	−71.2	−60	−63	−63	dB
		A_{IN} = 4.996MHz	−64.6	−58	−60	−57	dB
IMD	Intermodulation Distortion	Note 3	−69.4				dB
SFDR	Spurious Free Dynamic Range	Note 2,					
		A_{IN} = 404kHz	74.2	60.5	64	64	dB
		A_{IN} = 4.996MHz	66.8	59	61.5	60	dB
EFB	Effective Bits	F_S = 10Msps,					
		A_{IN} = 404kHz	10.50	9.50	9.84	9.84	Bits
		A_{IN} = 4.996MHz	10.00	9.17	9.50	9.09	Bits
BW	Large Signal Bandwidth	V_{IN} = 2Vp-p	65	45	45	45	MHz
BW_{SS}	Small Signal Bandwidth	V_{IN} = 0.5Vp-p	70	50	50	50	MHz
E_{AP}	Aperture Error		4.5	7.0	6.0	6.0	ps_{rms}
SR	Slew Rate		300	250	250	230	V/μs
t_{TR}	Transient Response	Note 4	10				ns
t_{OR}	Overload Recovery	100% Overrange	26	38	38	38	ns
SPC	Spurious Codes		0	0	0	0	Codes
MC	Missing Codes		0	0	0	0	Codes

Notes:
1. F_S = 10Msps, A_{IN} = 100kHz.
2. F_S = 10Msps, 1dB below full-scale.
3. F_S = 8.006Msps, A_{IN} = 2.20 + 2.49MHz. Each fundamental 7dB below full-scale, summed signal 1dB below full-scale.
4. V_{IN} = full-scale step.
5. GAIN ADJ and OFFSET ADJ pins grounded.

Thermal characteristics

Parameter		Max	Units
ΔT_{JC}	Junction-to-Case Temperature Rise (Worst Case Power Dissipation)	20	°C
Θ_{CA}	Case-to-Ambient Thermal Resistance		
	Still Air	16	°C/W
	500 LFPM Airflow	7	°C/W

Definitions

SNR (Signal-to-Noise (S/N) Ratio)

The ratio, expressed in decibels, of the RMS level of the output signal to the RMS level of the in-band noise. This noise is measured with the signal present, and excludes harmonic distortion products.

THD (Total Harmonic Distortion)

The ratio, expressed in decibels, of the RMS sum of the first 10 harmonics of the output fundamental to the RMS level of the output fundamental.

SINAD (Signal-to-Noise and Distortion (S/[N + D]) Ratio)

The ratio, expressed in decibels, of the RMS level of the output signal to the RMS sum of both the in-band noise and the RMS sum of the first 10 harmonics of the output fundamental.

SFDR (Spurious Free Dynamic Range; also SFSR, Spurious Free Signal Range)

The ratio, expressed in decibels, of the RMS level of the output fundamental to the RMS level of the largest spurious signal.

EFB (Effective Bits)

The hypothetical number of bits possessed by a perfect A/D converter whose performance equals that of the converter under test with the signal and at the conditions specified. EFB is computed directly from SINAD with the formula:

$$EFB = (SINAD - 1.76dB)/6.02dB$$

and therefore can have any fractional value and varies with input frequency and other conditions. For a theoretically perfect 12-bit A/D converter driven to full-scale at the Nyquist frequency, SINAD = 74dB and EFB = 12.00.

IMD (Two-Tone Intermodulation Distortion)

The ratio, expressed in decibels, of the largest output frequency spur to either of the two equal-level output fundamentals.

t_{TR} (Transient Response Time)

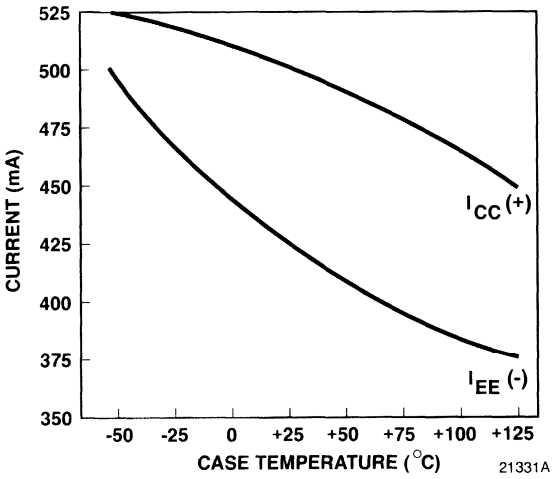
The time required to begin returning accurate data after a full-scale input voltage step whose initial and final voltages are within the analog input range. t_{TR} is an analog domain parameter and excludes pipeline latency.

t_{OR} (Overload Recovery Time)

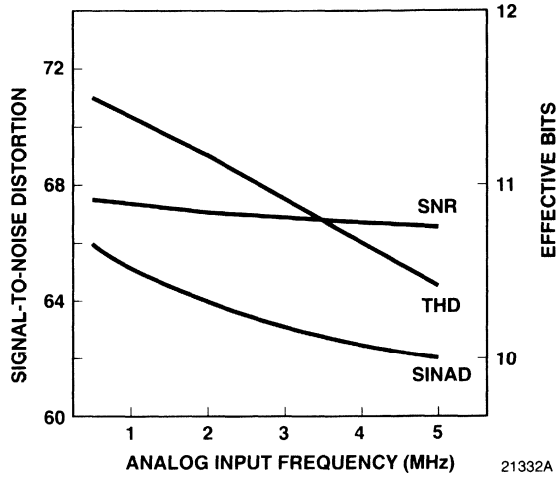
The time required to begin producing accurate data after the input voltage returns to the allowable range, following an excursion to 200% of either full-scale limit. t_{OR} is an analog domain parameter and excludes pipeline latency.

Typical Performance Curves

A. Typical Power Supply Current vs. Temperature



B. Typical SINAD, SNR and Distortion vs. Analog Input Frequency (10Msps)



C. Typical Output Spectrum

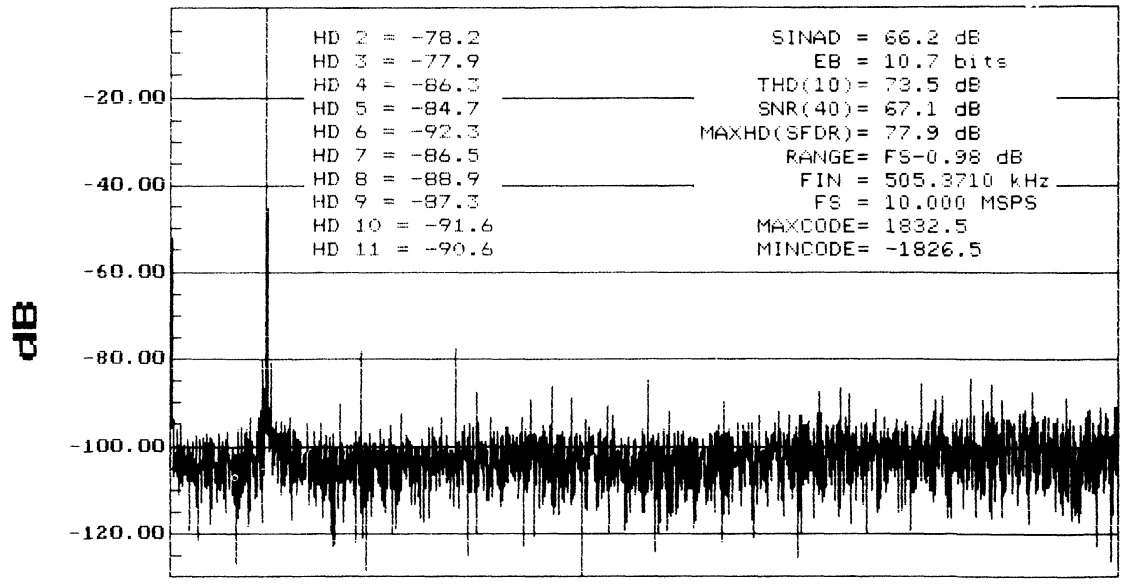
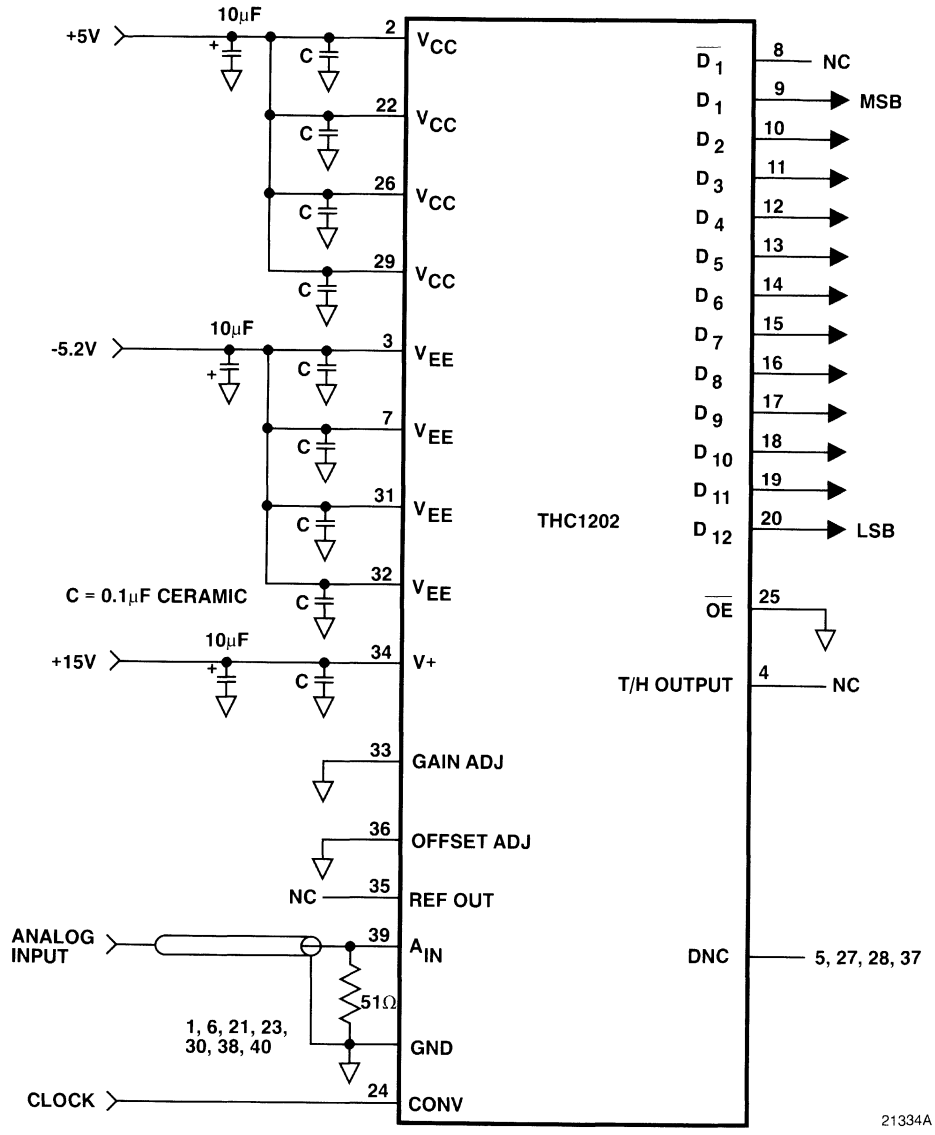


Figure 5. Typical Interface Circuit



Evaluation Board

The THC1202E1C is a Eurocard-style printed circuit board designed to aid in the evaluation of the THC1202 A/D converter. The board dimensions are 100mm x 160mm with a standard 64 pin double-row DIN male connector installed. A complementary 64 pin double-row DIN female connector is included with the board.

The board employs only two conducting sides. Most of the circuit interconnections are on the bottom of the board while the top is mostly solid ground plane. SMA connectors are installed on the board to facilitate analog I/O and clocks. The circuitry on the board includes all power supply decoupling required for the THC1202, and a TDC1012 12-bit D/A converter which may be used in evaluating certain parameters of the THC1202.

The THC1202E1C board has been designed to be used, not only for the THC1202, but also for the THC1200 and THC1201 A/D converters. Therefore, the board has interconnect patterns for some circuitry that is not used by the THC1202. Jumpers J3 and FT will be installed, while all others are not.

The board is calibrated and tested at the factory and is supplied complete with THC1202 and TDC1012 installed.

Power and Ground

Four power supply voltages are required for the operation of the THC1202E1C: $V_{CC} = +5V$, $V_{EE} = -5.2V$, $V+ = +15V$ and $V- = -15V$. All power inputs are decoupled to a single solid ground plane, GND. All GND pins of the board are connected to the ground plane and it is recommended that all GND pins be used.

A/D Converter Inputs

The clock to the THC1202, CONV, is normally brought onto the board by way of an SMA connector labeled "CONV" near pin 24 of the THC1202. A location for a terminating resistor, R20, is available on the board for terminating clock cables. CONV may be brought onto the board through the edge connector pin B2 by installing jumper J9. The DIP switch controls $\overline{OE}$ and RANGE, which are both pulled HIGH when the switches are open.

The analog signal input to the THC1202, A_{IN} is normally brought onto the board by way of an SMA connector labeled "A_{IN}" near pin 45 of the THC1202. A resistor network, R13 through R16, is included on the board for terminating and attenuating the signal in user-determined impedances and losses.

A/D Converter Data Outputs and D/A Converter Data Inputs

The 12 data outputs of the THC1202 are brought to edge connector pins B9 through B21 (excluding B18). These pins are located directly across the edge connector from the 12 data inputs of the TDC1020 D/A converter to simplify connection of A/D outputs to D/A inputs.

D/A Converter Inputs

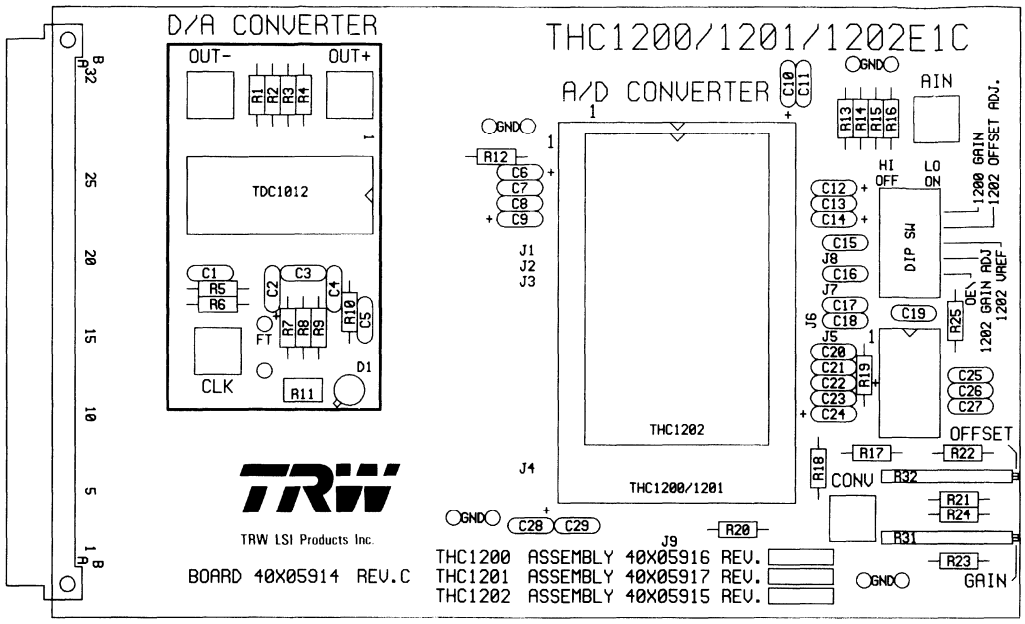
The clock to the TDC1012, CLK, is normally brought onto the board through an SMA connector labeled "CLK" near pin 16 of the TDC1012. A location for a terminating resistor, R6 is provided for clock cable termination. The clock input to the TDC1012 is also brought to the edge connector pin B24.

D/A converter outputs are brought to SMA connectors labeled OUT+ and OUT− as well as edge-connector pins B28 and B27. Load resistors of 51.1Ω are provided on the board to facilitate 50Ω cable connection to the board.

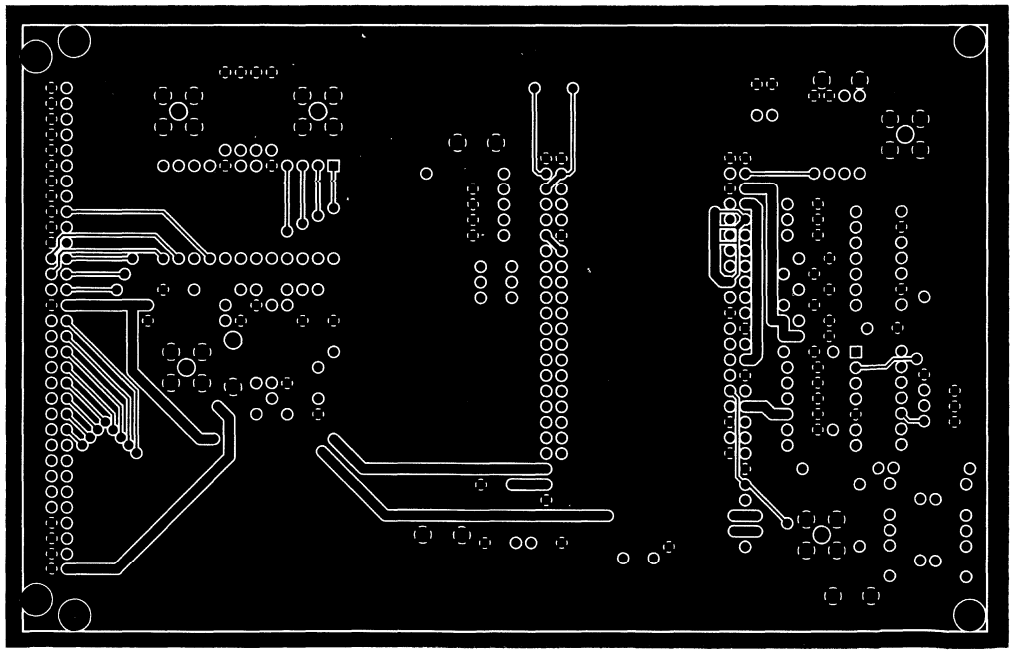
Potentiometer R11 is used to adjust the reference voltage to the TDC1012. This voltage is adjusted to −1.0V as part of the factory test and calibration procedure.

Removing the jumper in the location labeled "FT" will put the TDC1012 into feedthrough (unclocked) mode. This eliminates the requirement for a D/A clock signal, but will degrade the fidelity of the TDC1012 reconstruction.

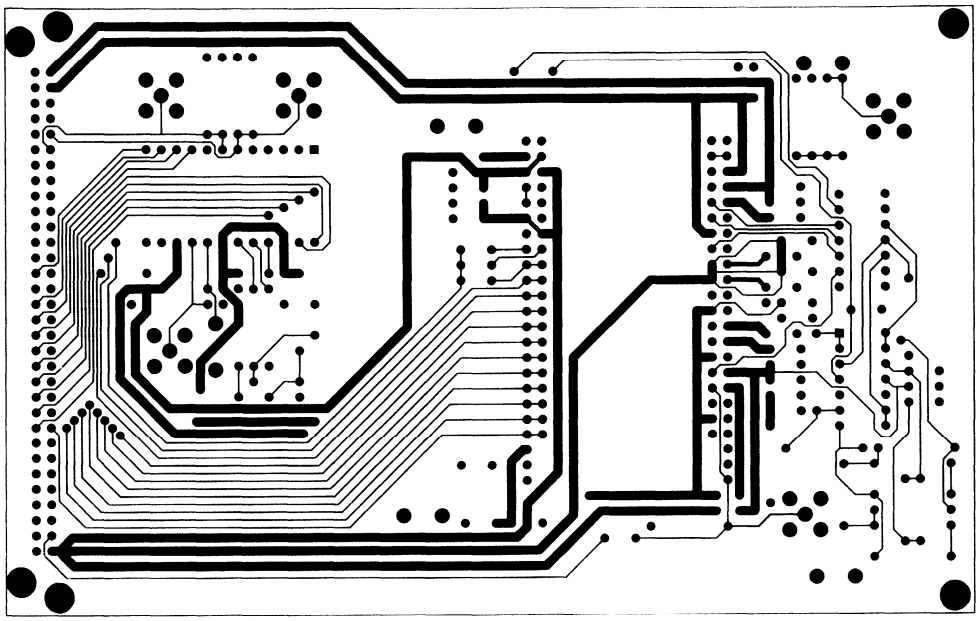
THC1202E1C Silkscreen Layout



THC1202E1C Component Side Layout



THC1202E1C Circuit Side Layout



A

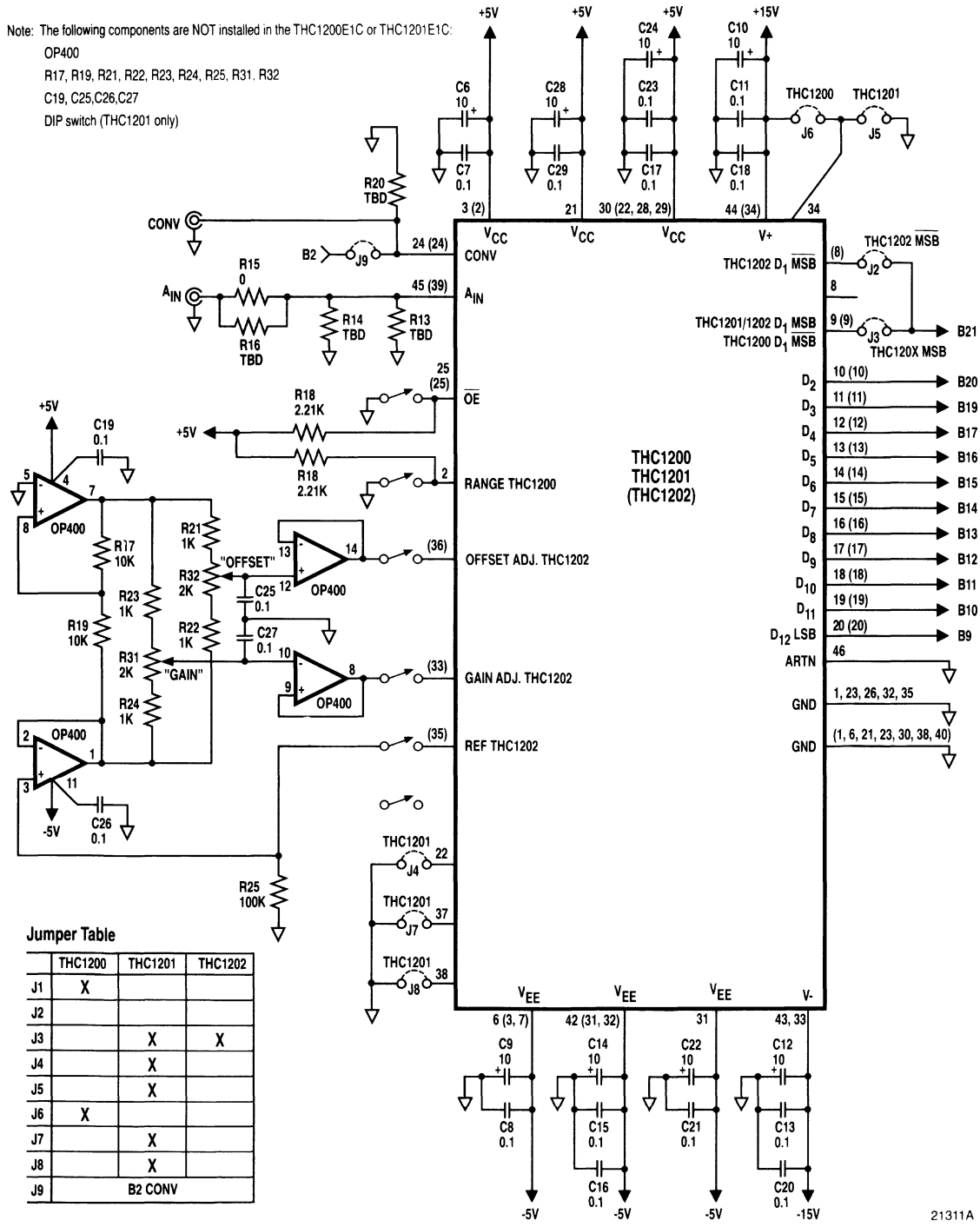
THC1202E1C Eurocard Edge Connector Pinout

GND	A32	B32	V– (–15V)
GND	A31	B31	V+ (+15V)
GND	A30	B30	NC
GND	A29	B29	NC
GND	A28	B28	D/A OUT+
GND	A27	B27	D/A OUT–
GND	A26	B26	NC
GND	A25	B25	NC
GND	A24	B24	D/A CLK
GND	A23	B23	NC
GND	A22	B22	NC
D/A D_1 MSB	A21	B21	A/D D_1 MSB
D/A D_2	A20	B20	A/D D_2
D/A D_3	A19	B19	A/D D_3
GND	A18	B18	V_{CC} (+5V)
D/A D_4	A17	B17	A/D D_4
D/A D_5	A16	B16	A/D D_5
D/A D_6	A15	B15	A/D D_6
D/A D_7	A14	B14	A/D D_7
D/A D_8	A13	B13	A/D D_8
D/A D_9	A12	B12	A/D D_9
D/A D_{10}	A11	B11	A/D D_{10}
D/A D_{11}	A10	B10	A/D D_{11}
D/A D_{12} LSB	A9	B9	A/D D_{12} LSB
NC	A8	B8	NC
NC	A7	B7	NC
NC	A6	B6	NC
NC	A5	B5	NC
GND	A4	B4	NC
GND	A3	B3	NC
GND	A2	B2	A/D CONV
GND	A1	B1	V_{EE} (–5.2V)

Mating Connectors for THC1202E1C

AMP	532507-2	Wire-wrap
AMP	532507-1	Solder tail
Robinson-Nugent	RNE-64BS-W-TG30	Wire-wrap
Robinson-Nugent	RNE-64BS-S-TG30	Solder tail
Souriau	8609-264-6115-7550E1	Wire-wrap
Souriau	8609-264-6114-7550E1	Solder tail
Souriau	8609-264-6813-7550E1	Solder tail, right-angle bend

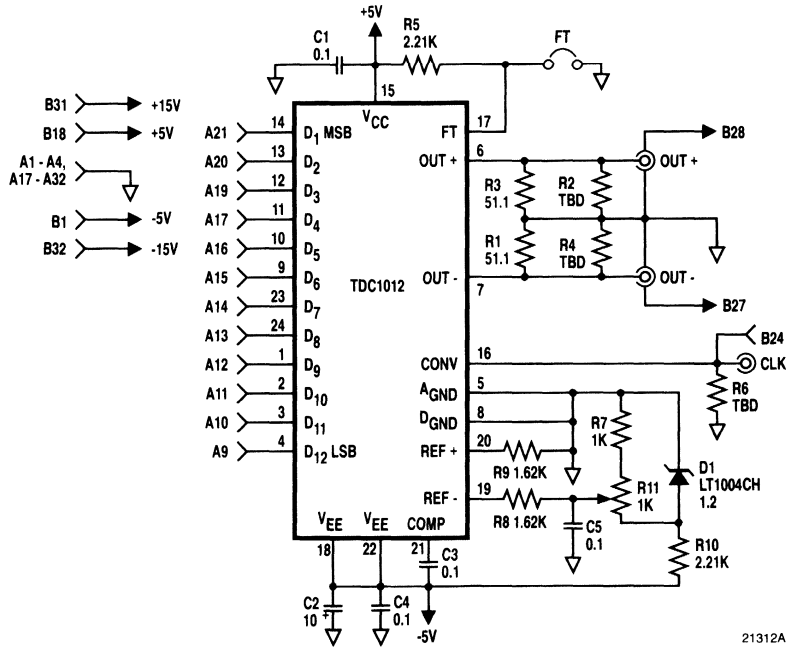
Figure 6. THC1202E1C A/D Converter Schematic Diagram



Jumper Table

	THC1200	THC1201	THC1202
J1	X		
J2			
J3		X	X
J4		X	
J5		X	
J6	X		
J7		X	
J8		X	
J9	B2 CONV		

Figure 7. THC1202E1C D/A Converter Schematic Diagram



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
THC1202S6B	IND – T_C = – 25°C to 85°C	Industrial	40 Pin Hermetic Ceramic DIP	THC1202S6B
THC1202S6V	EXT – T_C = – 55°C to 125°C	MIL-STD-883	40 Pin Hermetic Ceramic DIP	THC1202S6V
THC1202E1C	STD – T_A = 0°C to 70°C	– –	Eurocard Format Board with Industrial Grade A/D Converter	THC1202E1C

TMC1241

Self-Calibrating 12-Bit Plus Sign μP-Compatible A/D Converter with Track-and-Hold

TRW's TMC1241 is a CMOS successive approximation analog-to-digital converter with 13-bit resolution. The outstanding performance of the TMC1241 is the result of self-calibration, which reduces linearity and full-scale errors to less than ±1/2 LSB and offset error to less than ±1 LSB. The TMC1241 performs an Auto-Zero function that minimizes offset error. The Auto-Zero function can be performed as needed or prior to every A/D conversion.

The TMC1241 includes a track/hold input stage for sampling the analog input signal. Both unipolar and bipolar analog input voltage ranges (0 to +5 and ±5V) are accommodated. The TMC1241 requires only two power supplies, ±5V.

The TMC1241's two's complement output data format uses the 13th bit to indicate the polarity of the input signal. Digital inputs and outputs are compatible with TTL or CMOS logic levels and have microprocessor interface features.

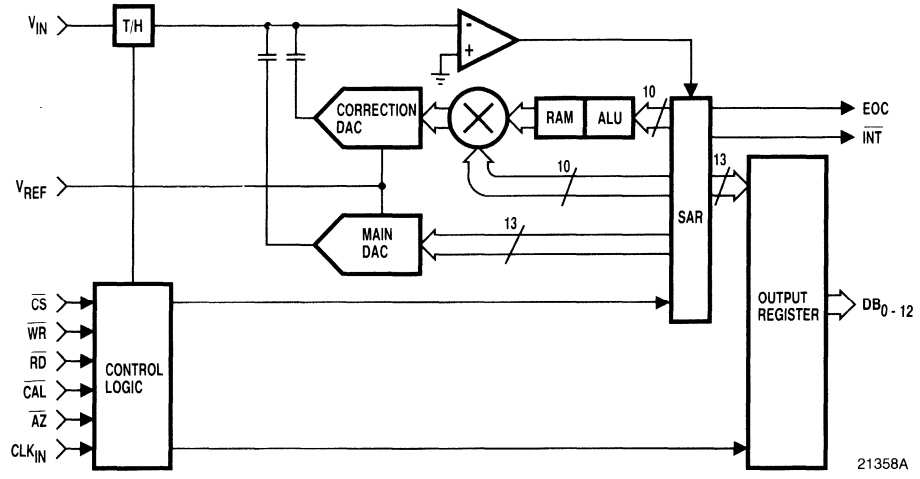
Features

- 13-Bit Resolution, 12 Bits Plus Sign
- Internal Track/Hold
- Conversion Time 13μs, Maximum
- Auto-Calibration And Auto-Zero Cycles
- Linearity Error Less Than ±1/2 LSB
- Offset Error Less Than ±1 LSB
- Full-Scale Error Less Than ±1 LSB
- Power Consumption 40mW, Maximum
- No Missing Codes, Guaranteed
- TTL/CMOS Compatible
- Standard 28 Pin DIP Package

Applications

- Process Control
- Instrumentation
- Data Acquisition Systems
- Motion Control
- Digital Signal Processing

Functional Block Diagram



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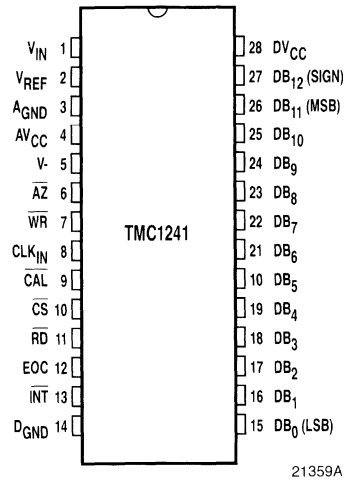
40G06671 Rev. A – 11/90
Printed in the U.S.A.

Pin Assignments



28 Pin CERDIP – B6 Package

Functional Description

General Information

The TMC1241 is a successive approximation A/D converter with 13-bit resolution (12-bit plus sign). The TMC1241 can perform Auto-Cal and Auto-Zero routines to minimize full-scale, linearity and offset errors. It comprises a D/A converter, precision comparator and a successive-approximation register (SAR) along with digital and analog circuitry for self-calibration.

The Auto-Zero cycle is an internal calibration sequence that corrects for A/D offset error caused by the input offset voltage of the comparator. The Auto-Cal cycle is a calibration sequence that not only corrects offset error but also corrects for full-scale and linearity errors caused by D/A converter gain and linearity errors. The Auto-Cal feature eliminates the need for trimming or other adjustment methods in the manufacture of the TMC1241. The Auto-Cal cycle restores the accuracy of the TMC1241 whenever it is requested. This ensures excellent long-term and temperature stability.

Power and Ground

The digital and analog power supply voltage range of the TMC1241 is +4.5V to +5.5V. To guarantee accuracy, it is required that the AV_{CC}, pin 4, and DV_{CC}, pin 28, be connected to the same power source, but with separate decoupling capacitors (10μF tantalum and a 0.1μF ceramic) between AV_{CC} and DV_{CC} and ground. V–, pin 5, has a range of –4.5V to –5.5V and and should have 10μF tantalum and 0.1μF ceramic capacitors for power supply decoupling.

Although A_{GND} and D_{GND}, pins 3 and 14 respectively, are distinguished from each other on the TMC1241, they should be connected together on the system printed circuit board to eliminate differential ground noise voltages which may degrade performance. A_{GND} and D_{GND} should be connected together as close to the TMC1241 as possible.

Analog Inputs

The voltage applied to the V_{REF} input, pin 2, defines the input voltage range of the V_{IN} input, pin 1, over which 4095 positive output codes and 4096 negative output codes are found. The A/D converter can be used in either ratiometric or absolute applications. The voltage source driving V_{REF} must have a low output impedance and low noise. The circuit in the *Typical Interface Circuit* is a good example of a very stable reference source for the TMC1241.

In a ratiometric application, the analog input voltage is proportional to the voltage used for the V_{REF}. If V_{IN} is related or proportional to AV_{CC}, V_{REF} can be connected directly to AV_{CC}. Here, V_{IN} and V_{REF} are related and track each other as the power supply voltage changes, making the output code of the TMC1241 independent of power supply voltage variations.

For absolute accuracy, where the V_{IN} varies independently of power supply voltage, V_{REF} should be driven from a time and temperature-stable voltage source like that shown in the *Typical Interface Circuit*. The magnitude of V_{REF} may require an adjustment to achieve system gain requirements.

Due to the architecture of the TMC1241, a variable current will flow into or out (depending on V_{IN} polarity) of the V_{IN} pin at the start of the analog input sampling period, t_A. The peak value of this current is proportional to the magnitude of the applied V_{IN}. A small capacitor from V_{IN} to A_{GND} can be used to reduce noise and clock feedthrough due to inductive coupling from long input leads and will not degrade the accuracy of the conversion. It is advisable, however, to keep V_{IN} and V_{REF} input lines as short as possible.

Analog Inputs (cont.)

The analog input can be modeled as shown in the *Analog Input Equivalent Circuit*. Large source resistance, R_S, will lengthen the time necessary for the voltage on C_{REF} to settle to within 1/2 LSB of the voltage on V_{IN}. With f_{CLK} of 2MHz, t_A takes seven clock periods, or 3.5μs. When R_S is less than or equal to 1kΩ, a 5.0V V_{IN} will have adequate time to settle.

Auto-Cal and Auto-Zero Cycles

When power is initially applied to the TMC1241, an Auto-Cal cycle is executed which cannot be interrupted. Since the power supply, reference, and clock are not usually stable at initial power-up, this first Auto-Cal cycle will not result in an accurate calibration of the TMC1241. An additional calibration cycle should be started after the power supplies, reference, and clock have been given adequate time to stabilize.

When $\overline{CAL}$, pin 9, is LOW, the TMC1241 is reset and an Auto-Cal cycle is initiated. During the Auto-Cal cycle, correction values are determined for the offset voltage of the comparator as well as linearity and gain errors. These values are stored in the internal RAM and used during A/D conversion cycles to reduce the TMC1241's gain, offset, and linearity errors to the specified limits. It is only necessary to go through the Auto-Cal cycle once after initial power is applied.

To correct for any change in the offset error of the A/D converter, the Auto-Zero cycle can be used. It may be necessary to execute an Auto-Zero cycle whenever the ambient temperature changes significantly (See the curve titled *"Zero Error Change vs. Ambient Temperature"* in the *Typical Performance Curves*). A change in the ambient temperature will cause the offset voltage of the comparator to change, which may cause the offset error of the A/D converter to be greater than its specified limit.

With the $\overline{AZ}$ input, pin 6, held LOW during a conversion cycle, the TMC1241 will execute an Auto-Zero cycle before the actual A/D conversion cycle is started. The total conversion time (t_C) is increased by 26 clock periods when Auto-Zero is used. An Auto-Zero cycle will reduce the offset error of the TMC1241 to less than $\pm$1 LSB.

Microprocessor Interface Controls

On initial power-up, an Auto-Cal cycle is executed by bringing $\overline{CAL}$ LOW while $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ are HIGH. To acknowledge that the Auto-Cal cycle is in progress, EOC goes LOW after the falling edge of $\overline{CAL}$ and remains LOW during the Auto-Cal cycle duration of 1,396 clock periods. During the Auto-Cal cycle, first the comparator offset error is determined and then the D/A converter gain and linearity errors are found. Correction factors for these errors are stored in the internal RAM.

An A/D conversion cycle is initiated by bringing $\overline{CS}$ and $\overline{WR}$ LOW. The $\overline{AZ}$ input should be tied HIGH or LOW during the conversion process. If $\overline{AZ}$ is LOW when A/D conversion is executed, an Auto-Zero cycle (duration equals 26 clock periods) occurs before the A/D conversion is started. If $\overline{AZ}$ is HIGH, no Auto-Zero cycle is executed. Once the A/D conversion sequence is started, V_{IN} is tracked for seven clock periods and held thereafter. EOC then goes LOW, indicating that V_{IN} is no longer being tracked and that the successive approximation conversion sequence has started.

During an A/D conversion cycle, the held V_{IN} is successively compared to the output of the corrected D/A converter (main and correction D/A converters).

First, the held voltage is compared to analog ground to determine its polarity (sign bit). The sign bit is set LOW for positive V_{IN} and HIGH for negative V_{IN}. Next, the MSB of the D/A converter is set HIGH with all other bits LOW. If the the held voltage is greater than the output of the D/A converter, then the MSB is left HIGH; otherwise, it is set LOW. The next bit is then set HIGH, making the output of the D/A converter 3/4 or 1/4 of full-scale, depending on the outcome of the previous bit. If the held voltage is greater than the new D/A converter value then the bit remains HIGH. If the held voltage is less than the new D/A converter value the bit is set LOW. This process continues until each bit has been tested. The result is then transferred to the output register of the TMC1241. EOC goes HIGH and $\overline{INT}$ goes LOW indicating the end of the conversion. The result can now be read by bringing $\overline{CS}$ and $\overline{RD}$ LOW to enable the $DB_{0\text{-}12}$ outputs.

Microprocessor Interface Controls (cont.)

The *A/D Control Input Functions (Table 1)* summarizes the effect of the digital control inputs on the TMC1241. Test Mode (where $\overline{RD}$ is HIGH and $\overline{CS}$ and $\overline{CAL}$ are LOW) is used in the manufacturing process of the TMC1241. Care should be taken to avoid this mode. In Test Mode DB_2, DB_3, DB_5, and DB_6 become active outputs, which may cause data bus contention.

The TMC1241 can be completely reset, aborting all sequences that may be in progress. The A/D converter is reset where a new conversion is started by taking $\overline{CS}$ and $\overline{WR}$ LOW. If this occurs when V_{IN} is being tracked or when EOC is LOW, the Auto-Cal correction factors in RAM may be corrupted. After reset, it is necessary to execute an Auto-Cal cycle before the next A/D conversion cycle. The Auto-Cal cycle cannot be reset once started.

Summary of Control Inputs

$\overline{CS}$ — The Chip Select control input, pin 10, is active LOW and enables the $\overline{WR}$ and $\overline{RD}$ functions.

$\overline{WR}$ — The A/D conversion is started on the rising edge of the Write control input, pin 7, when $\overline{CS}$ is LOW.

$\overline{RD}$ — The Read control input, pin 11, is active LOW and is used to enable the three-state data outputs and reset $\overline{INT}$ HIGH when $\overline{CS}$ is LOW.

$\overline{AZ}$ — With the $\overline{AZ}$ input, pin 6, held LOW during a conversion cycle, the TMC1241 will execute an Auto-Zero cycle before the actual A/D conversion cycle is started. The total conversion time (t_C) is increased by 26 clock periods when Auto-Zero is used.

$\overline{CAL}$ — When $\overline{CAL}$, pin 9, is LOW, the TMC1241 is reset and an Auto-Cal cycle is initiated.

CLK_{IN} — The clock input, pin 8, controls all sequence timing and A/D conversion time. The frequency range for CLK_{IN} is from 0.50 to 4MHz.

EOC — The End-of-Conversion control output, pin 12, is LOW during A/D conversion, Auto-Cal and Auto-Zero cycles.

$\overline{INT}$ — The interrupt control output, pin 13, goes LOW when a conversion has been completed and indicates that the conversion result is available from the output register. Reading the outputs or starting an A/D conversion, Auto-Cal or Auto-Zero cycle will reset in $\overline{INT}$ going HIGH.

$DB_{0\text{-}12}$ — The three-state outputs, pins 15 to 27, give A/D conversion results in two's complement format with DB_{12} being the sign bit, DB_{11} the MSB and DB_0 the LSB.

Table 1. A/D Control Input Functions

Control Inputs					A/D Function
$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{CAL}$	$\overline{AZ}$	
⊔	⊔	1	1	1	Start A/D conversion without Auto-Zero
⊔	1	⊔	1	1	Read A/D conversion result without Auto-Zero
⊔	⊔	1	1	0	Start A/D conversion with Auto-Zero
1	x	x	⊔	x	Start Auto-Cal cycle
0	x	1	0	x	Test Mode (DB_2, DB_3, DB_5 and DB_6 active)

Package Interconnections

Signal Type	Signal Name	Function	Value	B6 Package Pins
Power	AV_{CC}	Positive Analog Supply	+5.0V	4
	DV_{CC}	Positive Digital Supply	+5.0V	28
	V−	Negative Analog Supply	−5.0V	5
Ground	A_{GND}	Analog Ground	0.0V	3
	D_{GND}	Digital Ground	0.0V	14
Analog Inputs	V_{IN}	Analog Signal Input	±4.7V	1
	V_{REF}	Reference Input	+4.7V	2
Digital Inputs	CLK_{IN}	Clock Input	TTL	8
	$\overline{AZ}$	Auto-Zero	TTL	6
	$\overline{CAL}$	Calibrate	TTL	9
	$\overline{RD}$	Read	TTL	11
	$\overline{WR}$	Write	TTL	7
	$\overline{CS}$	Chip Select	TTL	10
Digital Outputs	EOC	End of Calibration	TTL	12
	$\overline{INT}$	Interrupt	TTL	13
	DB_{12} SGN	Sign Bit	TTL	27
	DB_{11} MSB	Most Significant Bit	TTL	26
	DB_{10}		TTL	25
	DB_9		TTL	24
	DB_8		TTL	23
	DB_7		TTL	22
	DB_6		TTL	21
	DB_5		TTL	20
	DB_4		TTL	19
	DB_3		TTL	18
	DB_2		TTL	17
	DB_1		TTL	16
	DB_0 LSB	Least Significant Bit	TTL	15

Figure 1. Timing Diagram, Auto-Cal Cycle ($\overline{CS}$ = HIGH, $\overline{WR} = \overline{RD} = \overline{AZ}$ = Don't Care)

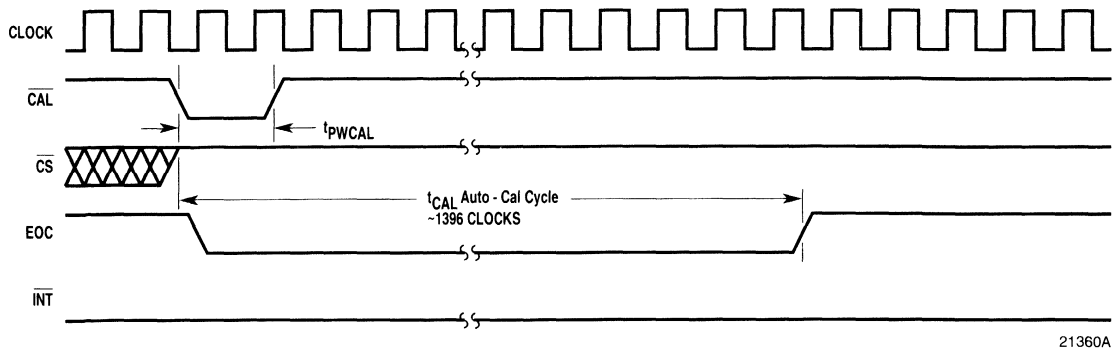


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Figure 2. Timing Diagram, A/D Conversion Cycle with Auto-Zero ($\overline{CAL}$ = HIGH, $\overline{AZ}$ = LOW)

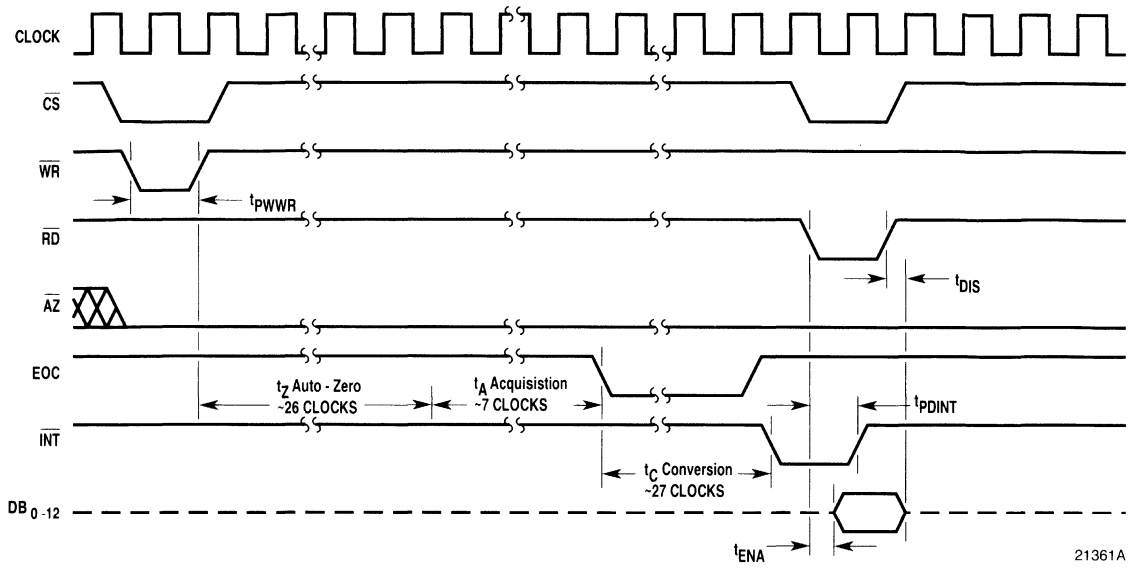


Figure 3. Timing Diagram, Normal A/D Conversion Cycle without Auto-Zero ($\overline{CAL}$ = $\overline{AZ}$ = HIGH)

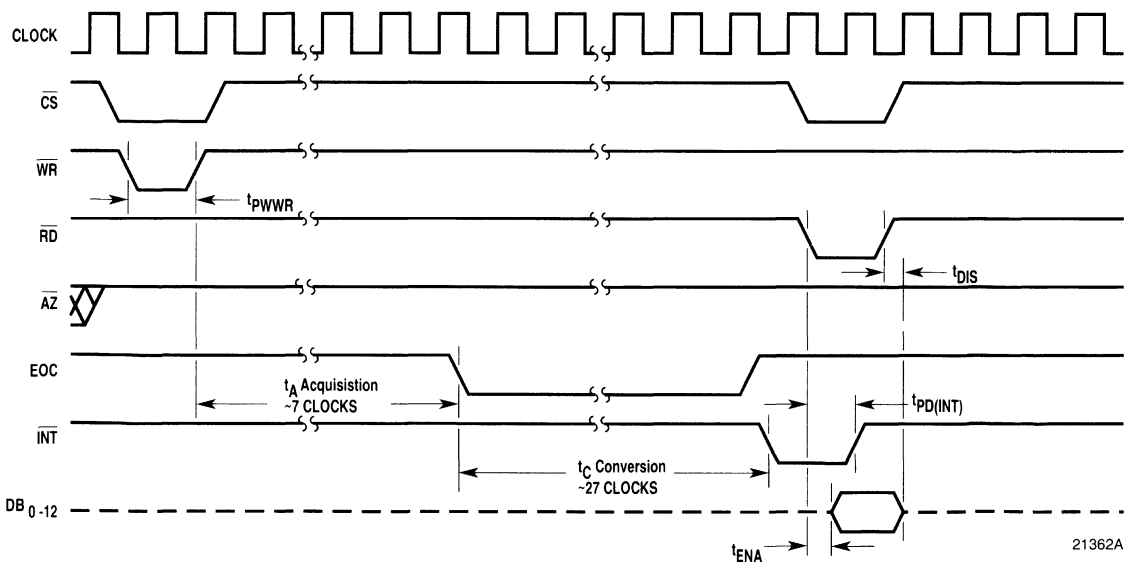


Figure 4. Simplified Error Characteristics vs. Output Code without Auto-Cal or Auto-Zero Cycles

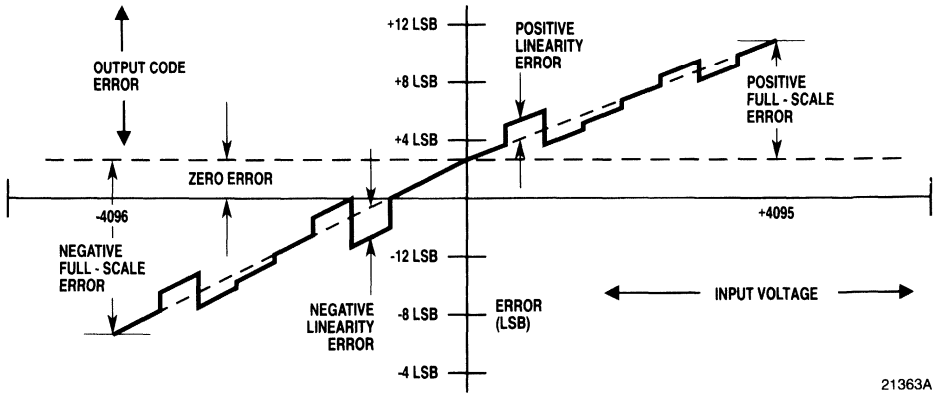


Figure 5. Simplified Error Characteristics vs. Output Code after Auto-Cal

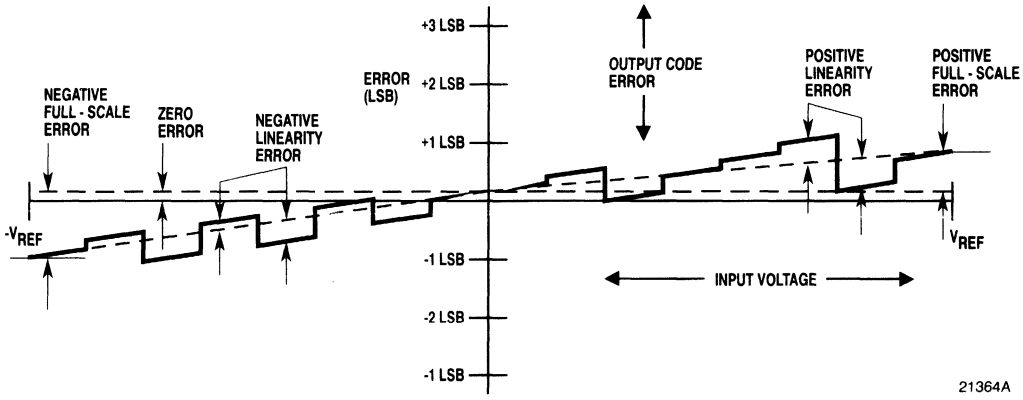


Figure 6. Transfer Characteristics

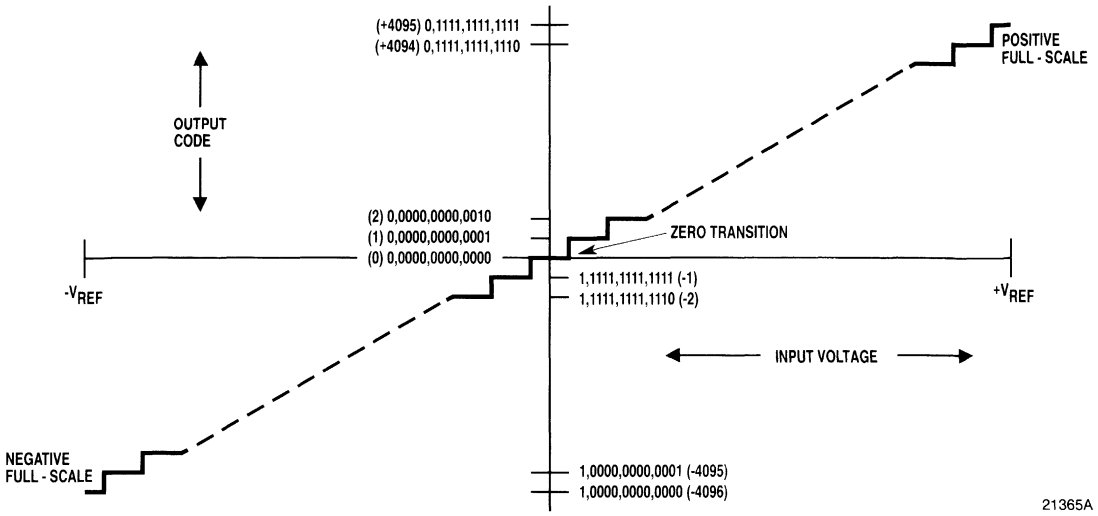


Figure 7. Analog Input Equivalent Circuit

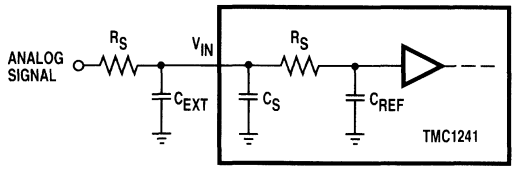
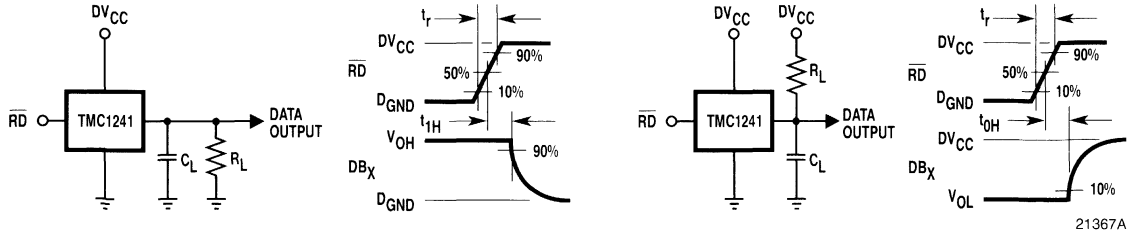


Figure 8. Output Test Loads



Output Coding Table

Input Voltage	DB_{12} Sign	DB_{11} . . . DB_0 MSB LSB
>4.096V	0	1111 1111 1111
+4.096V	0	1111 1111 1111
+4.095V	0	1111 1111 1110
+4.094V	0	1111 1111 1101
•		•
•		•
+0.002V	0	0000 0000 0010
+0.001V	0	0000 0000 0001
0.000V	0	0000 0000 0000
−0.001V	1	1111 1111 1111
−0.002V	1	1111 1111 1110
•		•
•		•
−4.094V	1	0000 0000 0010
−4.095V	1	0000 0000 0001
−4.096V	1	0000 0000 0000
≤4.096V	1	0000 0000 0000

Note: 1. The input voltage range used for this table is ±4.096V and the input voltages are measured at code centers.

Absolute maximum ratings (beyond which the device may be damaged) [1,2]

Supply Voltages

DV_{CC}	−0.5 to +6.5V
AV_{CC}	−0.5 to +6.5V
V−	+0.5 to −6.5V
$AV_{CC} - DV_{CC}$ [7]	−0.3 to +0.3V
$A_{GND} - D_{GND}$	−0.3 to +0.3V

Input Voltages

Digital Inputs	DV_{CC} +0.3) to −0.3V
Analog Inputs	(AV_{CC} +0.3) to (V− −0.3)V

Outputs

Digital Outputs, applied voltage	−0.5V to DV_{CC}
Input current, any pin, externally forced [3]	±5mA
Short-circuit duration (single output to GND)	Unlimited

Temperature

Operating, case	−60 to +135°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Package Input Current [3]	±20mA
Package Power Dissipation at 25°C [4]	875mW
ESD Susceptibility [5]	2000V

Operating conditions [1,2,16,17,18]

Parameter		Temperature Range						Units
		Industrial			Extended			
		Min	Nom	Max	Min	Nom	Max	
AV_{CC}, DV_{CC}	Positive Power Supply Voltages [6,7]	4.5	5.0	5.5	4.5	5.0	5.5	V
V−	Negative Power Supply Voltage	−4.5	−5.0	−5.5	−4.5	−5.0	−5.5	V
$AV_{CC} - DV_{CC}$	Power Supply Voltage Differential	−0.1	0.0	0.1	−0.1	0.0	0.1	V
$A_{GND} - D_{GND}$	Ground Voltage Differential	−0.1	0.0	0.1	−0.1	0.0	0.1	V
V_{IN}	Input Voltage Range	V− −.050	±4.096	AV_{CC} +.050	V− −.050	±4.096	AV_{CC} +.050	V
V_{REF}	Reference Voltage [6,7]	3.5	+4.096	AV_{CC} +.050	3.5	+4.096	AV_{CC} +.050	V
f_{CLK}	Clock Frequency	0.5	2.0	4.0	0.5	2.0	4.0	MHz
	Clock Duty Cycle	40	50	60	40	50	60	%
V_{IL}	Input Voltage, Logic LOW, all but CLK_{IN}, DV_{CC} = 4.75V		1.4	0.8		1.4	0.8	V
V_{IH}	Input Voltage, Logic HIGH, all but CLK_{IN}, DV_{CC} = 5.25V	2.0	1.4		2.0	1.4		V
I_{OL}	Output Current, Logic LOW	−6.0	−20		−6.0	−20		mA
I_{OH}	Output Current, Logic HIGH	8.0	20		8.0	20		mA
T_J	Junction Temperature, TMC1241B6B, TMC1241B6B1	−40		+85				°C
T_J	Junction Temperature, TMC1241B6F				−55		+125	°C

Electrical characteristics within specified operating conditions [1,2,6,7,8,9,16,17]

Parameter		Test Conditions	Temperature Range					Units
			Typ	Industrial		Extended		
				Min	Max	Min	Max	
DI_{CC}	DV_{CC} Supply Current	f_{CLK} = 2.0MHz, $\overline{CS}$ = HIGH	1.0		2.0		2.0	mA
AI_{CC}	AV_{CC} Supply Current	f_{CLK} = 2.0MHz, $\overline{CS}$ = HIGH	2.8		6.0		6.0	mA
I−	V− Supply Current	f_{CLK} = 2.0MHz, $\overline{CS}$ = HIGH	2.8		6.0		6.0	mA
C_{IN}	Analog Input Capacitance		65					pF
C_{REF}	Reference Input Capacitance		80					pF
I_{IL}	Input Current, Logic LOW		−0.005		−1.0		−1.0	μA
I_{IH}	Input Current, Logic HIGH		0.005		1.0		1.0	μA
V_{T+}	Positive-Going Threshold, CLK_{IN}		2.8	2.7		2.7		V
V_{T-}	Negative-Going Threshold, CLK_{IN}		2.1		2.3		2.3	V
V_H	Hysteresis, CLK_{IN}	$V_{T+} - V_{T-}$	0.7	0.4		0.4		V
V_{OL}	Output Voltage, Logic LOW	I_{OUT} = 1.6mA, V_{CC} = 4.75V			0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	I_{OUT} = −360μA, V_{CC} = 4.75V		2.4		2.4		V
		I_{OUT} = −10μA, V_{CC} = 4.75V		4.5		4.5		V
I_{OZL}	Output Leakage Current, LOW	V_{OUT} = 0.0V	−0.01		−3.0		−3.0	μA
I_{OZH}	Output Leakage Current, HIGH	V_{OUT} = 5.0V	0.01		3.0		3.0	μA

Switching characteristics within specified operating conditions [1,2,6,7,8,9,16,17,18]

Parameter		Test Conditions	Temperature Range					Units
			Typ	Industrial Min	Industrial Max	Extended Min	Extended Max	
t_C	Conversion Time				$27/f_{CLK}+0.3$		$27/f_{CLK}+0.3$	μs
		$f_{CLK}=2.0MHz$	13.5					μs
t_A	Acquisition Time [14]	$R_S=50\Omega$			$7/f_{CLK}+0.3$		$7/f_{CLK}+0.3$	μs
		$f_{CLK}=2.0MHz$	3.5					μs
t_Z	Auto-Zero Time				$26/f_{CLK}$		$26/f_{CLK}$	μs
		$f_{CLK}=2.0MHz$	13					μs
t_{CAL}	Calibration Time		$1396/f_{CLK}$					μs
		$f_{CLK}=2.0MHz$	698		706		706	μs
t_{PWCAL}	Calibration Pulse Width	Note 15	60	200		200		ns
t_{PWWR}	$\overline{WR}$ Pulse Width		60	200		200		ns
t_{PDINT}	$\overline{RD}$ or $\overline{WR}$ to Reset of $\overline{INT}$		100		175		175	ns
t_{ENA}	Output Enable Time	$C_L=100pF$	50		85		85	ns
t_{DIS}	Data Disable Time	$C_L=100pF$, $R_L=1k\Omega$	30		90		90	ns

System performance characteristics within specified operating conditions [1,2,6,7,8,9,16,17]

Parameter		Test Conditions	Temperature Range					Units
			Typ	Industrial Min	Industrial Max	Extended Min	Extended Max	
E_{LIP}	Positive Integral Linearity Error	After Auto-Cal [10,11]						
		TMC1241B6B1			±0.5			LSB
		TMC1241B6F, TMC1241B6B			±1.0		±1.0	LSB
E_{LIN}	Negative Integral Linearity Error	After Auto-Cal [10,11]						
		TMC1241B6B1			±0.5			LSB
		TMC1241B6F, TMC1241B6B			±1.0		±1.0	LSB
E_{LD}	Differential Linearity Error	After Auto-Cal [10,11]		12		12		Bits
E_{FSP}	Positive Full-Scale Error	After Auto-Cal [11]	±0.5		±1.0		±1.0	LSB
E_{FSN}	Negative Full-Scale Error	After Auto-Cal [11]	±1.0		±2.0		±2.0	LSB
E_Z	Zero Error [11,12]	After Auto-Cal or Auto-Zero			±1.0,		±1.0	LSB
PSS_Z	Power Supply Sensitivity, Zero Error [13]	$AV_{CC}=DV_{CC}=+5.0\pm5\%$ $V-=-5.0\pm5\%$, $V_{REF}=+4.75V$	±0.125					LSB
PSS_F	Power Supply Sensitivity, Full-Scale Error	$AV_{CC}=DV_{CC}=+5.0\pm5\%$ $V-=-5.0\pm5\%$, $V_{REF}=+4.75V$	±0.125					LSB
PSS_L	Power Supply Sensitivity, Linearity Error	$AV_{CC}=DV_{CC}=+5.0\pm5\%$ $V-=-5.0\pm5\%$, $V_{REF}=+4.75V$	±0.125					LSB

Notes for Specification Tables

1. Absolute Maximum Ratings are limits beyond which the device may be damaged. Operating Conditions are limits under which the device is guaranteed to be functional, but those limits do not guarantee specific performance. Guaranteed specifications and test conditions are shown in the *Electrical, Switching and System Performance Characteristics Tables*. The guaranteed specifications apply only for the test conditions listed in the *Electrical, Switching and System Performance Characteristics Tables*. Some performance characteristics may degrade when the device is operated outside the listed test conditions.

2. All voltages are measured with respect to A_{GND} and D_{GND}, unless otherwise specified.

3. When the voltage at any pin exceeds the power supply voltages ($<V-$ or $>AV_{CC}$ or $>DV_{CC}$), the current at that pin must be limited to 5mA. The 20mA maximum package input current rating allows the voltage any any four pins, with a current limit of 5mA, to simultaneously exceed the power supply voltages.

4. The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum allowable junction temperature), θ_{JA} (junction-to-ambient thermal resistance of the package). and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is given by:

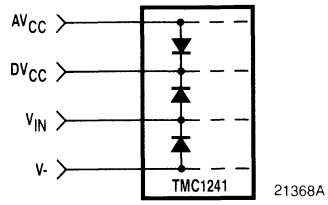
$$P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$$

   or the number given in the *Absolute Maximum Ratings Table*, whichever is lower. For the TMC1241, T_{Jmax} is 125°C and the typical thermal resistance (θ_{JA}) of the TMC1241 with B6F, B6B1, and B6B suffixes when board mounted is 47°C/W.

5. Human body model, 100pF discharged through a 1.5kΩ resistor.

6. Two on-chip diodes are tied to the analog input as shown in the following figure, *Parasitic Diode Structure*. A/D conversion errors can occur if these diodes are forward-biased more than 50mV.

Parasitic Diode Structure



7. To guarantee accuracy, it is required that AV_{CC} and DV_{CC} be connected to the same power source but with separate decoupling capacitors at each pin.

8. Accuracy is guaranteed with f_{CKL} equal to 2.0MHz. Accuracy may degrade at higher clock frequencies.

9. Typical specifications are at $T_J = 25°C$ and represent the most likely parametric norm (statistical "mode").

10. Positive linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative linearity error the straight line passes through negative full-scale and zero. (See *Simplified Error Characteristic Curves*.)

11. The TMC1214's self-calibration technique ensures linearity, full-scale and offset errors as specified. Noise inherent to the self-calibration process will result in a repeatability uncertainty of ±0.20 LSB.

12. When T_A changes, an Auto-Zero or Auto-Cal cycle will be required for specified performance. (See *Typical Performance Curves*.)

13. After Auto-Zero or Auto-Cal cycle execution at the specified power supply extremes.

14. If the CLK_{IN} is asynchronous with respect to the falling edge of $\overline{WR}$ an uncertainty of one clock period exists in the t_A interval. Therefore, the minimum t_A is six clock periods and the maximum t_A is 7 clock periods. If the falling edge of CLK_{IN} is synchronous with respect to the rising edge of $\overline{WR}$ then t_A will be exactly 6.5 clock periods.

15. The $\overline{CAL}$ input must go HIGH before an A/D conversion is started.

Notes for Specification Tables (cont.)

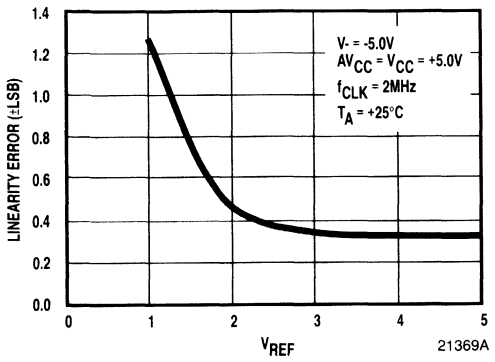
16. Guaranteed specifications apply for $AV_{CC} = DV_{CC} = +5.0V$, $V- = -5.0V$, $V_{REF} = \sim 5.0V$ and $f_{CLK} = 2.0MHz$ unless otherwise specified.

17. Typical performance specifications are for $T_J = +25°C$.

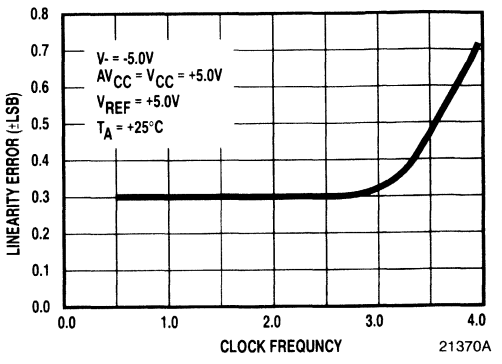
18. Rise and fall times for digital inputs = 20ns, unless otherwise specified.

Typical Performance Curves

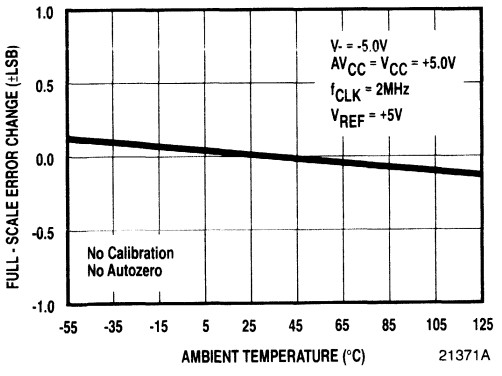
A. Linearity Error vs. V_{REF}



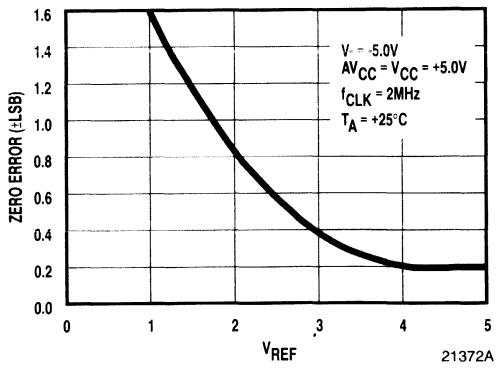
B. Linearity Error vs. Clock Frequency



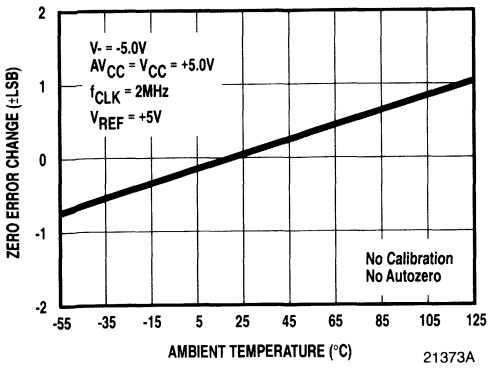
C. Full-Scale Error Change vs. Ambient Temperature



D. Zero Error vs. V_{REF}



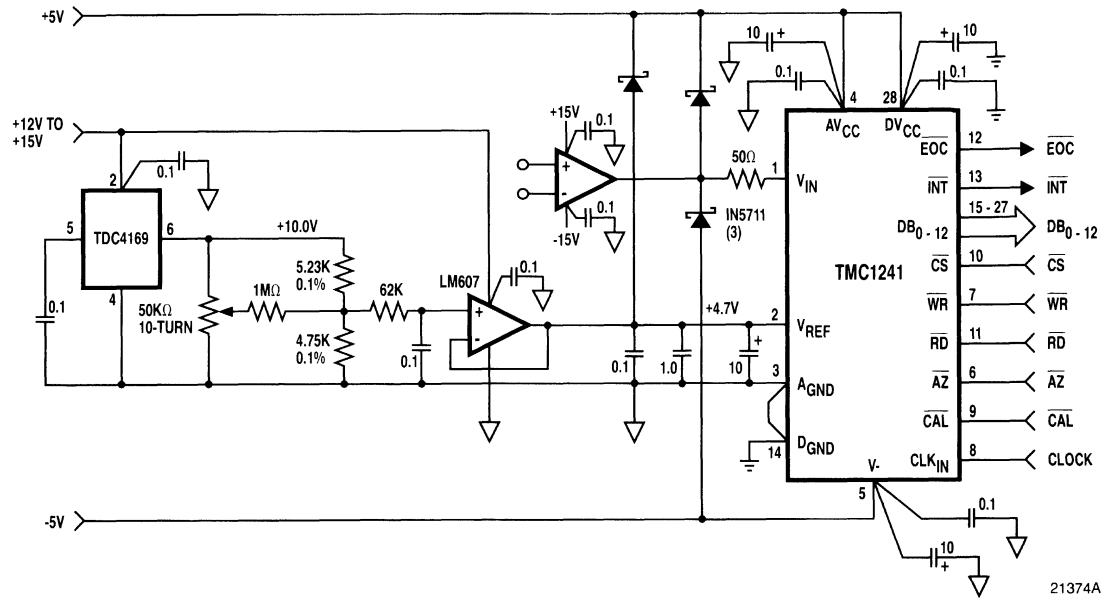
E. Zero Error Change vs. Ambient Temperature



The Typical Interface Circuit

Noise on AV_{CC}, DV_{CC} or V– power supply inputs can cause A/D conversion errors should the TMC1241 comparator be influenced by that noise. The TMC1241 is especially sensitive during the Auto-Zero or Auto-Cal cycles to power supply noise. Low inductance 10μF tantalum capacitors in parallel with 0.1μF ceramic capacitors are recommended for power supply decoupling. Separate decoupling capacitors should be placed close to the DV_{CC}, AV_{CC} and V– pins.

Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC1241B6F	EXT–T_A = –55°C to 125°C	Commercial	28 Pin CERDIP	1241B6F
TMC1241B6B	STD–T_A = –40°C to 85°C	Commercial	28 Pin CERDIP	1241B6B
TMC1241B6B1	STD–T_A = –40°C to 85°C	Commercial	28 Pin CERDIP	1241B6B1
TMC1241E1C	STD–T_A = 0°C to 70°C	– –	Eurocard PC Board	1241E1C

TMC1251

Self-Calibrating 12-Bit Plus Sign, 7.7 µs, µP-Compatible A/D Converter with Track-and-Hold

TRW's TMC1251 is a CMOS successive approximation analog-to-digital converter with 13-bit resolution. The outstanding performance of the TMC1251 is the result of self-calibration, which reduces linearity and full-scale errors to less than ±1/2 LSB and offset error to less than ±1 LSB. The TMC1251 performs an Auto-Zero function that minimizes offset error. The Auto-Zero function can be performed as needed or prior to every A/D conversion.

The TMC1251 includes an internal track/hold stage which is directly controlled with a separate $\overline{T}$/H input. Both unipolar and bipolar analog input voltage ranges (0 to + 5 and ±5 Volts) are accommodated. The TMC1251 requires only two power supplies, ±5 Volts.

The TMC1251's two's-complement output data format uses the 13th bit to indicate the polarity of the input signal. The 13-bit conversion result from the TMC1251 is read from its 8 outputs in two successive bytes. Digital inputs and outputs are compatible with TTL or CMOS logic levels and have microprocessor interface features.

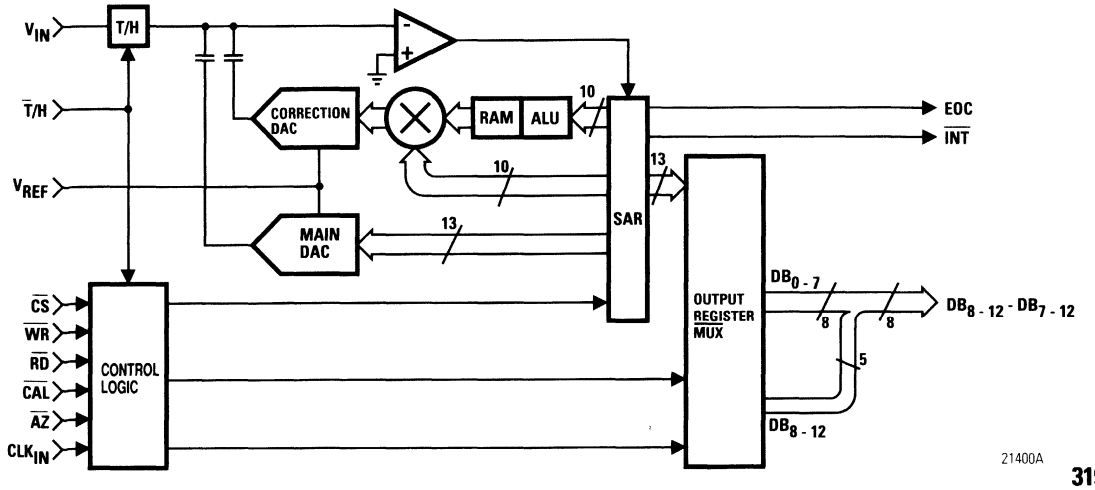
Features

- 13-Bit Resolution, 12 Bits Plus Sign
- Internal Track/Hold
- Conversion Time 7.7 µs, Maximum
- Auto-Calibration And Auto-Zero Cycles
- Linearity Error Less Than ±1/2 LSB
- Offset Error Less Than ±1 LSB
- Full-Scale Error Less Than ±1.5 LSB
- Power Consumption 113mW, Maximum
- Eight-Bit Microprocessor Interface
- TTL/CMOS Compatible
- Standard 24-lead DIP Package

Applications

- Process Control
- Instrumentation
- Data Acquisition Systems
- Motion Control
- Digital Signal Processing

Functional Block Diagram



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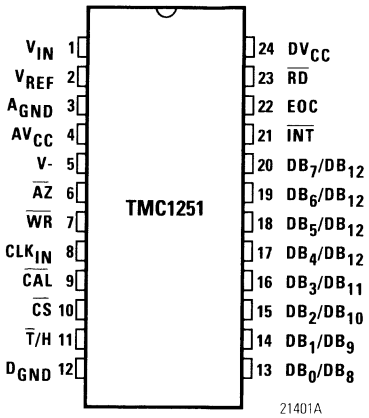
40G06674 Rev. A – 7/90
Printed in the U.S.A.

Pin Assignments



24-pin DIP package

Functional Description

General Information

The TMC1251 is a successive approximation A/D converter with 13-bit resolution (12-bit plus sign). The TMC1251 can perform Auto-Cal and Auto-Zero routines to minimize full-scale, linearity and offset errors. It comprises a D/A converter, precision comparator and a successive approximation register (SAR) along with digital and analog circuitry for self-calibration.

The Auto-Zero cycle is an internal calibration sequence that corrects for A/D offset error caused by the input offset voltage of the comparator. The Auto-Cal cycle is a calibration sequence that not only corrects offset error but also corrects for full-scale and linearity errors caused by D/A converter gain and linearity errors. The Auto-Cal feature eliminates the need for trimming or other adjustment methods in the manufacture of the TMC1251. The Auto-Cal cycle restores the accuracy of the TMC1251 whenever it is requested. This ensures excellent long-term and temperature stability.

The internal track/hold input stage can be controlled by the TMC1251 inherent conversion sequencing circuitry or externally by the use of the $\overline{T}/H$ control input. This control allows the timing and duration of the analog signal acquisition period just prior to initiating an A/D conversion cycle. The 13-bit result is made available in two successive bytes from the eight-bit wide output port.

Power and Ground

The digital and analog power supply voltage range of the TMC1251 is + 4.5V to + 5.5V. To guarantee accuracy, it is required that the AV_{CC}, pin 4, and DV_{CC}, pin 24, be connected to the same power source, but with separate decoupling capacitors (10µF tantalum and a 0.1µF ceramic) between AV_{CC} and DV_{CC} and ground. V-, pin 5, has a range of –4.5V to –5.5V and and should have 10µF tantalum and 0.1µF ceramic capacitors for power supply decoupling.

Although A_{GND} and D_{GND}, pins 3 and 24 respectively, are distinguished from each other on the TMC1251, they should be connected together on the system printed circuit board to eliminate differential ground noise voltages which may degrade performance. A_{GND} and D_{GND} should be connected together as close to the TMC1251 as possible.

Analog Inputs

The voltage applied to the V_{REF} input, pin 2, defines the input voltage range of the V_{IN} input, pin 1, over which 4095 positive output codes and 4096 negative output codes are found. The A/D converter can be used in either ratiometric or absolute applications. The voltage source driving V_{REF} must have a low output impedance and low noise. The circuit in the *Typical Interface Circuit* is a good example of a very stable reference source for the TMC1251.

In a ratiometric application, the analog input voltage is proportional to the voltage used for the V_{REF}. If V_{IN} is related or proportional to AV_{CC}, V_{REF} can be connected directly to AV_{CC}. Here, V_{IN} and V_{REF} are related and track each other as the power supply voltage changes, making the output code of the TMC1251 independent of power supply voltage variations.

For absolute accuracy, where the V_{IN} varies independently of power supply voltage, V_{REF} should be driven from a time- and temperature-stable voltage source like that shown in the *Typical Interface Circuit*. The magnitude of V_{REF} may require an adjustment to achieve system gain requirements.

Due to the architecture of the TMC1251, a variable current will flow into or out of (depending on V_{IN} polarity) the V_{IN} pin at the start of the analog input sampling period, t_A. The

Analog Inputs (cont.)

peak value of this current is proportional to the magnitude of the applied V_{IN}. A small capacitor from V_{IN} to A_{GND} can be used to reduce noise and clock feedthrough due to inductive coupling from long input leads and will not degrade the accuracy of the conversion. It is advisable, however, to keep V_{IN} and V_{REF} input lines as short as possible.

The analog input can be modeled as shown in the *Analog Input Equivalent Circuit*. Large source resistance, R_S, will lengthen the time necessary for the voltage on C_{REF} to settle to within 1/2 LSB of the voltage on V_{IN}. With f_{CLK} of 2MHz, t_A takes seven clock periods, or 3.5µs. When R_S is less than or equal to 1kΩ, a 5.0 Volt V_{IN} will have adequate time to settle.

Auto-Cal and Auto-Zero Cycles

When power is initially applied to the TMC1251, an Auto-Cal cycle is executed which cannot be interrupted. Since the power supply, reference, and clock are not usually stable at initial power-up, this first Auto-Cal cycle will not result in an accurate calibration of the TMC1251. An additional calibration cycle should be started after the power supplies, reference, and clock have been given adequate time to stabilize.

When $\overline{CAL}$, pin 9, is LOW, the TMC1251 is reset and an Auto-Cal cycle is initiated. During the Auto-Cal cycle, correction values are determined for the offset voltage of the comparator as well as linearity and gain errors. These values are stored in the internal RAM and used during A/D conversion cycles to reduce the TMC1251's gain, offset, and linearity errors to the specified limits. It is only necessary to go through the Auto-Cal cycle once after initial power is applied.

To correct for any change in the offset error of the A/D converter, the Auto-Zero cycle can be used. It may be necessary to execute an Auto-Zero cycle whenever the ambient temperature changes significantly (See the curve titled *"Zero Error Change vs Ambient Temperature"* in the *Typical Performance Characteristics*). A change in the ambient temperature will cause the offset voltage of the comparator to change, which may cause the offset error of the A/D converter to be greater than its specified limit. Since Auto-Zero cannot be activated when $\overline{T}/H$ is used to start the A/D conversion cycle, it may be necessary to do an Auto-Cal cycle (which includes Auto-Zero) periodically.

With the $\overline{AZ}$ input, pin 6, held LOW during a conversion cycle, the TMC1251 will execute an Auto-Zero cycle before the actual A/D conversion cycle is started. The total conversion time (t_C) is increased by 26 clock periods when Auto-Zero is used. An Auto-Zero cycle will reduce the offset error of the TMC1251 to less than ±1 LSB.

Microprocessor Interface Controls

On initial power-up, an Auto-Cal cycle is executed by bringing $\overline{CAL}$ LOW while $\overline{CS}$ and $\overline{T}/H$ are HIGH. To acknowledge that the Auto-Cal cycle is in progress, EOC goes LOW after the falling edge of $\overline{CAL}$ and remains LOW during the Auto-Cal cycle duration of 1,399 clock periods. During the Auto-Cal cycle, first the comparator offset error is determined and then the D/A converter gain and linearity errors are found. Correction factors for these errors are stored in the internal RAM.

An A/D conversion cycle is initiated by bringing $\overline{CS}$ and $\overline{WR}$ LOW. The $\overline{AZ}$ input should be tied HIGH or LOW during the conversion process. If $\overline{AZ}$ is LOW when A/D conversion is executed, an Auto-Zero cycle (duration equals 26 clock periods) occurs before the A/D conversion is started. $\overline{AZ}$ must be LOW during the entire A/D conversion. After Auto-Zero is complete, the analog signal acquisition time period begins and continues for 7 clock periods. If $\overline{AZ}$ is HIGH, no Auto-Zero cycle is executed. At the end of the acquisition period EOC goes LOW, indicating that V_{IN} is being held and that the successive approximation conversion sequence has started.

$\overline{CS}$ and $\overline{T}/H$ may be used to initiate a conversion cycle. Bringing both of these signals LOW begins the acquisition period; the rising edge of $\overline{T}/H$ puts the track/hold into the hold mode and begins the successive approximation conversion. DSP applications require that the time that the analog input signal is sampled (the end of the acquisition period) be well controlled. Using $\overline{T}/H$ in this way ensures control over the sampling of the analog input signal.

During an A/D conversion cycle, the held V_{IN} is successively compared to the output of the corrected D/A converter (main and correction D/A converters). First, the held voltage is compared to analog ground to determine its polarity (sign bit). The sign bit is set LOW for positive V_{IN} and HIGH for negative V_{IN}. Next, the MSB of the D/A converter is set HIGH with all other bits LOW. If the the held voltage is greater than the output of the D/A converter, then the MSB is left HIGH; otherwise it is set LOW. The next bit is then set HIGH, making the output of

Microprocessor Interface Controls (cont.)

the D/A converter 3/4 or 1/4 of full scale, depending on the outcome of the previous bit. If the held voltage is greater than the new D/A converter value then the bit remains HIGH. If the held voltage is less than the new D/A converter value the bit is set LOW. This process continues until each bit has been tested. The result is then transferred to the output register of the TMC1251. EOC goes HIGH and $\overline{INT}$ goes LOW indicating the end of the conversion. The result can now be read when $\overline{CS}$ is LOW by bringing $\overline{RD}$ LOW twice in succession to enable first, the MSBs (DB_8 thru DB_{12}) and second, the LSBs (DB_0 thru DB_7) of the result through the TMC1251's eight-bit wide output port.

The *A/D Control Input Functions (Table 1)* summarizes the effect of the digital control inputs on the TMC1251. Test Mode (where $\overline{RD}$ is HIGH and $\overline{CS}$ and $\overline{CAL}$ are LOW) is used in the manufacturing process of the TMC1251. Care should be taken to avoid this mode. In Test Mode DB_2, DB_3, DB_5, and DB_6 become active outputs, which may cause data bus contention.

The TMC1251 can be completely reset, aborting all sequences that may be in progress. The A/D converter is reset where a new conversion is started by taking $\overline{CS}$ and $\overline{WR}$ or $\overline{CS}$ and $\overline{T}$/H LOW. If this occurs when V_{IN} is being tracked or when EOC is LOW, the Auto-Cal correction factors in RAM may be corrupted. After reset, it is then necessary to execute an Auto-Cal cycle before the next A/D conversion cycle. The Auto-Cal cycle cannot be reset once started.

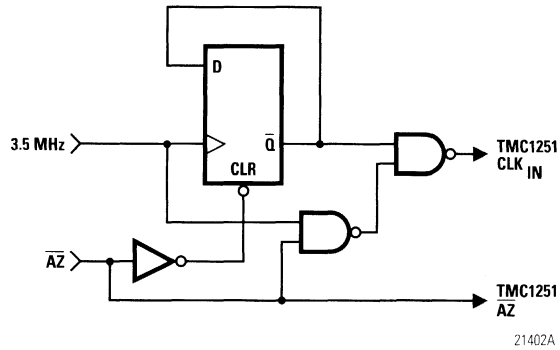
When using $\overline{WR}$ or $\overline{T}$/H without $\overline{AZ}$ to start a conversion, a new conversion may be restarted only after EOC has gone HIGH after the end of the current conversion. When using $\overline{WR}$ and $\overline{AZ}$, a new conversion may be restarted during the first 26 clock cycles after the rising edge of $\overline{WR}$ or after EOC has gone HIGH without corrupting the Auto-Cal correction factors.

Acquisition Time and Dynamic Performance

Each of the three methods of initiating a conversion affects the analog signal acquisition period. $\overline{WR}$ or $\overline{T}$/H can start a conversion when $\overline{AZ}$ is HIGH. In either of these cases, the rising edge of EOC indicates that the track/hold is in its track mode and the analog input signal is being acquired. It is advisable, however, to consider the beginning of the actual acquisition time to be AFTER the second $\overline{RD}$ pulse of the previous conversion cycle. In this way, the noise that normally accompanies the reading of data from the TMC1251's outputs will not affect the signal being acquired and therefore, the results of the following conversion.

When $\overline{WR}$ is used to start a conversion with $\overline{AZ}$ LOW, an Auto-Zero cycle is inserted prior to the acquisition period. Here, the acquisition timing and duration are controlled by the TMC1251. Since the acquisition time must always be at least 3.5µs, the maximum CLK_{IN} frequency in this mode is limited to 2.0MHz (7 cycles at 500ns). A simple circuit is shown which is useful when $\overline{WR}$ initiates conversions with and without Auto-Zero. In this circuit, when $\overline{AZ}$ is HIGH, the TMC1251 CLK_{IN} frequency is 3.5MHz. When $\overline{AZ}$ is LOW, the TMC1251 CLK_{IN} frequency is divided by two and is 1.75MHz.

Figure 1. CLK_{IN} Frequency Control Circuit



The performance of the TMC1251 with AC input signals can be better described with the use of parameters such as Signal-to-Noise Ratio (SNR), Signal-to-Noise-and-Distortion Ratio (SINAD), Total Harmonic Distortion (THD), Spurious-Free Dynamic Range (SFDR), Effective Bits, bandwidth, aperture time and aperture jitter. These parameters are a measure of the ability of the TMC1251 to digitize AC input signals without significant spectral errors such as elevated frequency spurs or noise.

An A/D converter's AC performance is evaluated using Fast Fourier Transform (FFT) methods. A sinusoidal input is applied to the A/D converter and n FFT is performed on data read from the A/D converter. SNR, SINAD, THD, SFDR and Effective Bit results are obtained in this way along with spectral plots. Typical values for unipolar and bipolar

SINAD are shown in the *System Performance Tables* along with spectral plots in the *Typical Performance Curves* section. Dynamic performance levels change with frequency, signal amplitude and conversion rate.

The performance of the internal track/hold of the TMC1251 is shown by aperture time and aperture jitter parameters. When $\overline{T}$/H is used to initiate conversions, aperture time is the delay between the rising edge of $\overline{T}$/H and the internal time when the analog input signal is actually held. Aperture jitter is the change in this time period from cycle-to-cycle.

For applications where A/D converter dynamic performance is important to determining overall system performance, TRW recommends the use of the TMC12441 or TMC12451. These A/D converters are identical to the TMC1241 and TMC1251, respectively, except that they are dynamically tested and have guaranteed SNR, THD, Effective Bits and bandwidth specifications.

Summary of Control Inputs

$\overline{CS}$ — The Chip Select control input, pin 10, is active LOW and enables the $\overline{WR}$, $\overline{RD}$, and $\overline{T}$/H functions.

$\overline{WR}$ — The A/D conversion is started on the rising edge of the Write control input, pin 7, when $\overline{CS}$ is LOW. When this control is used to start a conversion the analog signal acquisition period is controlled by the TMC1251.

$\overline{RD}$ — The Read control input, pin 23, is active LOW and is used to enable the three-state data outputs and reset $\overline{INT}$ HIGH when $\overline{CS}$ is LOW.

$\overline{T}$/H — The track/hold control input, pin 11, can be used to start a conversion. With $\overline{CS}$ LOW, the falling edge of $\overline{T}$/H begins the analog signal acquisition period. The rising edge of $\overline{T}$/H then puts the track/hold into hold mode and starts the A/D conversion.

$\overline{AZ}$ — With the $\overline{AZ}$ input, pin 6, held LOW during a conversion cycle, the TMC1251 will execute an Auto-Zero cycle before the actual A/D conversion cycle is started. The total conversion time (t_C) is increased by 26 clock periods when Auto-Zero is used.

$\overline{CAL}$ — When $\overline{CAL}$, pin 9, is LOW, the TMC1251 is reset and an Auto-Cal cycle is initiated.

CLK_{IN} — The clock input, pin 8, controls all sequence timing and A/D conversion time. The frequency range for CLK_{IN} is from 0.50 to 6MHz.

EOC — The End-of-Conversion control output, pin 22, is LOW during A/D conversion, Auto-Cal, and Auto-Zero cycles.

$\overline{INT}$ — The interrupt control output, pin 21, goes LOW when a conversion has been completed and indicates that the conversion result is available from the output register. Reading the outputs or starting an A/D conversion, Auto-Cal or Auto-Zero cycle will reset in $\overline{INT}$ going HIGH.

DB_0/DB_{12} — The three-state outputs, pins 13 to 20, give 13-bit conversion results with two successive $\overline{RD}$ pulses. The first $\overline{RD}$ pulse outputs the MSBs of the result (DB_8 thru DB_{12}) and the second $\overline{RD}$ pulse outputs the LSBs (DB_0 thru DB_7). The format is two's complement sign bit extended with DB_{12} being the sign bit, DB_{11} the MSB and DB_0 the LSB.

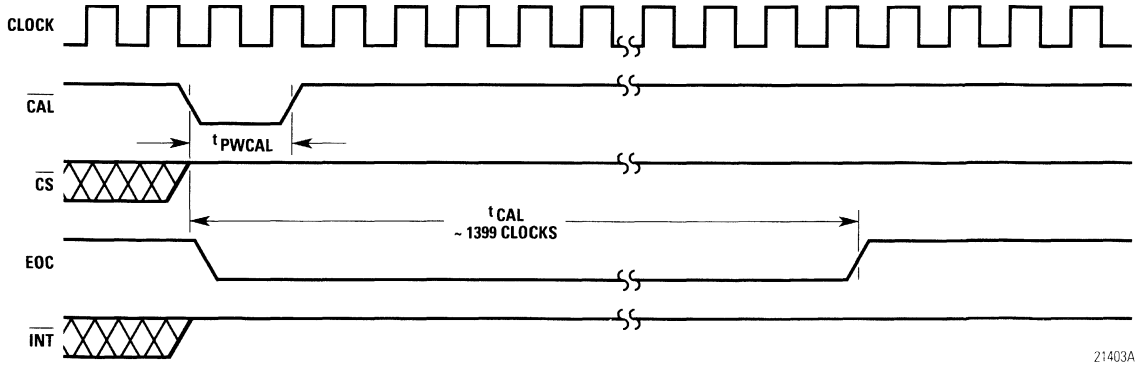
Table 1. A/D Control Input Functions

Control Inputs						A/D Function
$\overline{CS}$	$\overline{WR}$	$\overline{T}$/H	$\overline{RD}$	$\overline{CAL}$	$\overline{AZ}$	
↓	↓	1	1	1	1	Start A/D conversion without Auto-Zero
↓	1	↓	1	1	1	Start A/D conversion without Auto-Zero, synchronous with rising edge of $\overline{T}$/H.
↓	1	1	↓	1	1	Read data without Auto-Zero
↓	↓	1	1	1	0	Start A/D conversion with Auto-Zero
↓	1	1	↓	1	0	Read data with Auto-Zero
1	x	1	x	↓	x	Start Auto-Cal cycle
0	x	1	1	0	x	Test Mode (DB_2, DB_3, DB_5 and DB_6 active)

Package Interconnections

Signal Type	Signal Name	Function	Value	B7 Package Pin
Power	AV_{CC}	Positive Analog Supply	+5.0V	4
	DV_{CC}	Positive Digital Supply	+5.0V	24
	V–	Negative Analog Supply	–5.0V	5
Ground	A_{GND}	Analog Ground	0.0V	3
	D_{GND}	Digital Ground	0.0V	12
Analog Inputs	V_{IN}	Analog Signal Input	±4.7V	1
	V_{REF}	Reference Input	+4.7V	2
Digital Inputs	CLK_{IN}	Clock Input	TTL	8
	$\overline{AZ}$	Auto-Zero	TTL	6
	$\overline{CAL}$	Calibrate	TTL	9
	$\overline{RD}$	Read	TTL	23
	$\overline{WR}$	Write	TTL	7
	$\overline{CS}$	Chip Select	TTL	10
	$\overline{T}$/H	Sample-Hold	TTL	11
Digital Outputs	EOC	End of Calibration	TTL	22
	$\overline{INT}$	Interrupt	TTL	21
	DB7/DB12		TTL	20
	DB6/DB12		TTL	19
	DB5/DB12		TTL	18
	DB4/DB12		TTL	17
	DB3/DB11		TTL	16
	DB2/DB10		TTL	15
	DB1/DB9		TTL	14
	DB0/DB8		TTL	13

Figure 2. Timing Diagram, Auto-Cal Cycle ($\overline{CS}$ = HIGH, $\overline{WR}$ = $\overline{T}$/H = $\overline{RD}$ = $\overline{AZ}$ = don't care)



$\overline{CS}$ = 1
$\overline{WR}$ = X
$\overline{RD}$ = X
$\overline{AZ}$ = X
$\overline{T}$/H = 1
X = DON'T CARE

Figure 3. Timing Diagram, Using $\overline{WR}$ to Start Conversions with Auto-Zero ($\overline{CAL}$ = HIGH, $\overline{AZ}$ = LOW)

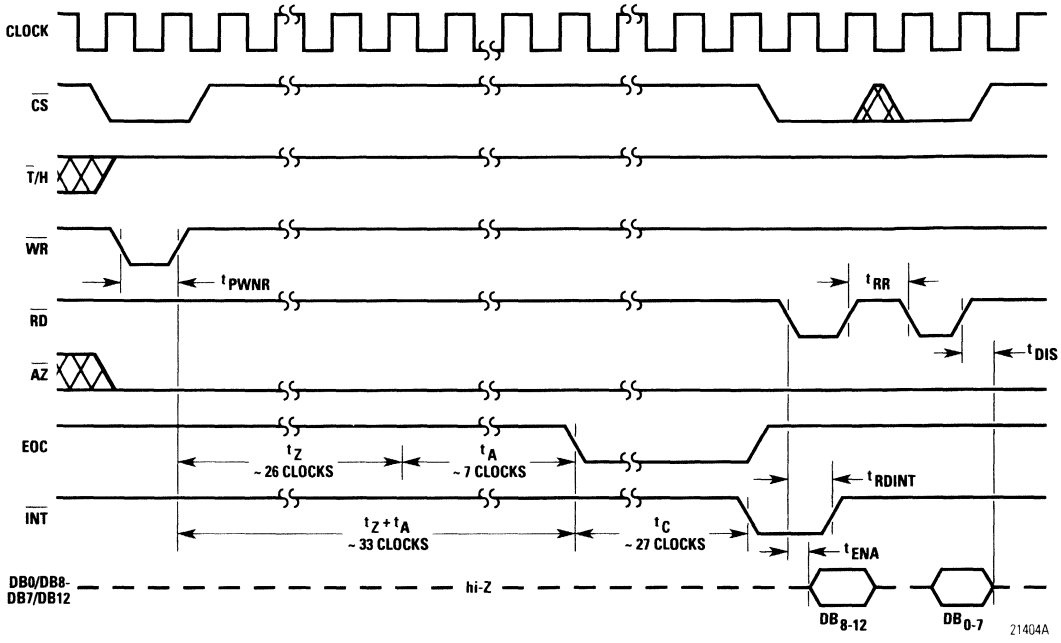


Figure 4. Timing Diagram, Using $\overline{WR}$ to Start Conversions without Auto-Zero ($\overline{CAL}$ = $\overline{AZ}$ = HIGH)

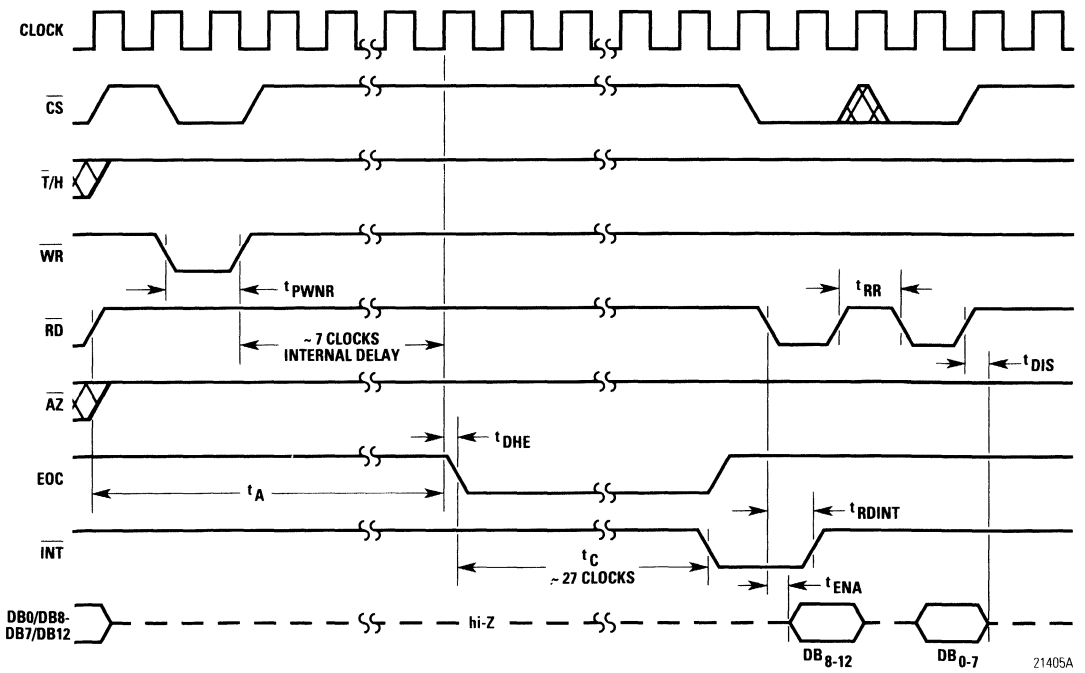


Figure 5. Timing Diagram, Using $\overline{T}$/H to Start Conversions without Auto-Zero ($\overline{CAL}$ = $\overline{AZ}$ = HIGH)

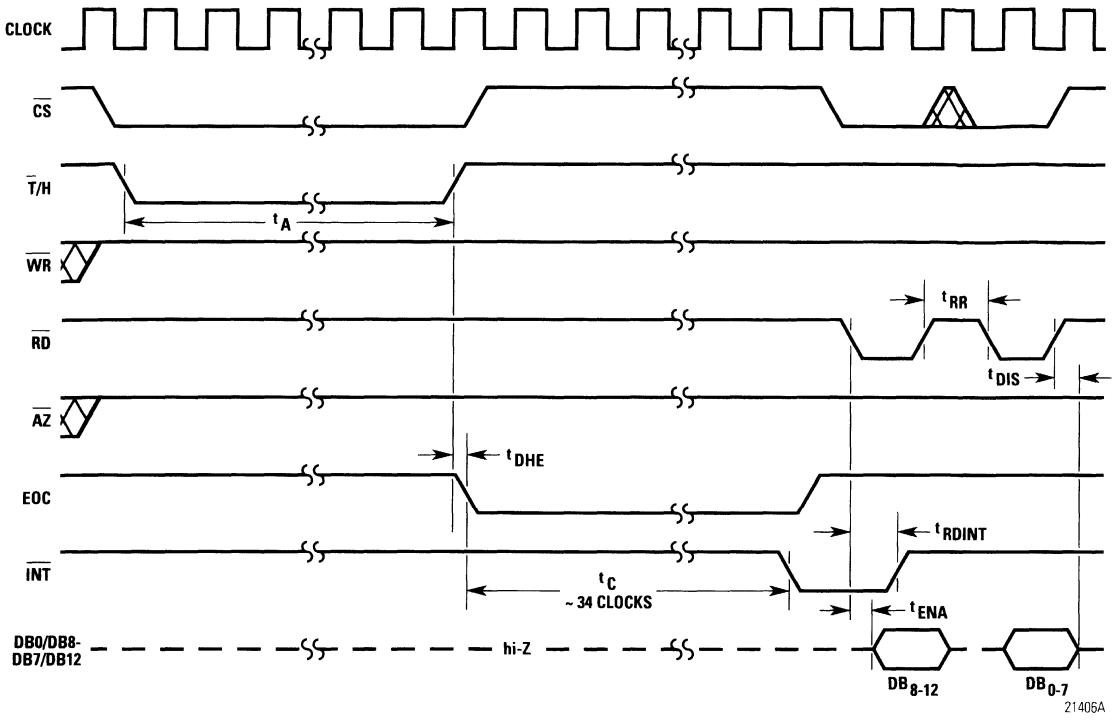


Figure 6. Transfer Characteristics

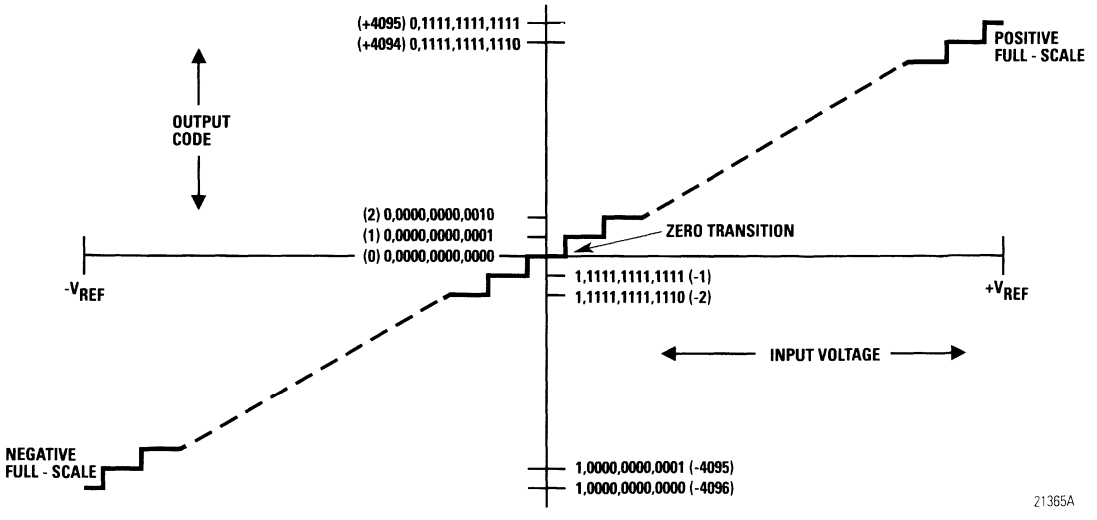


Figure 7. Simplified Error Characteristics vs. output code without Auto-Cal or Auto-Zero cycles

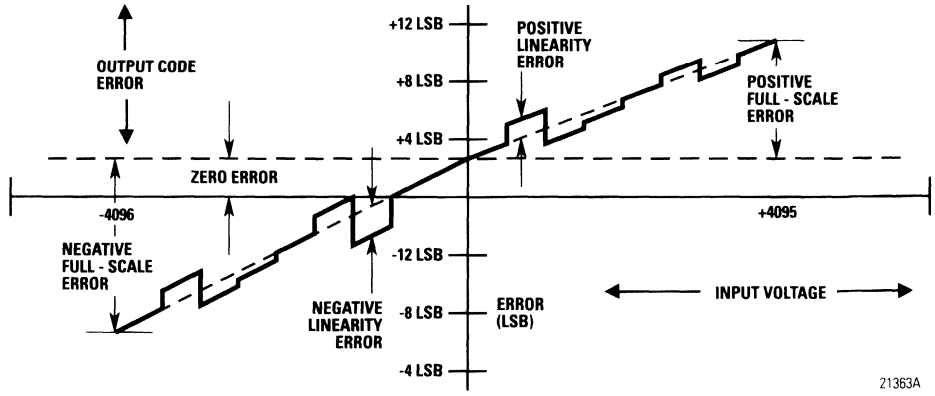


Figure 8. Simplified Error Characteristics vs. output code after Auto-Cal

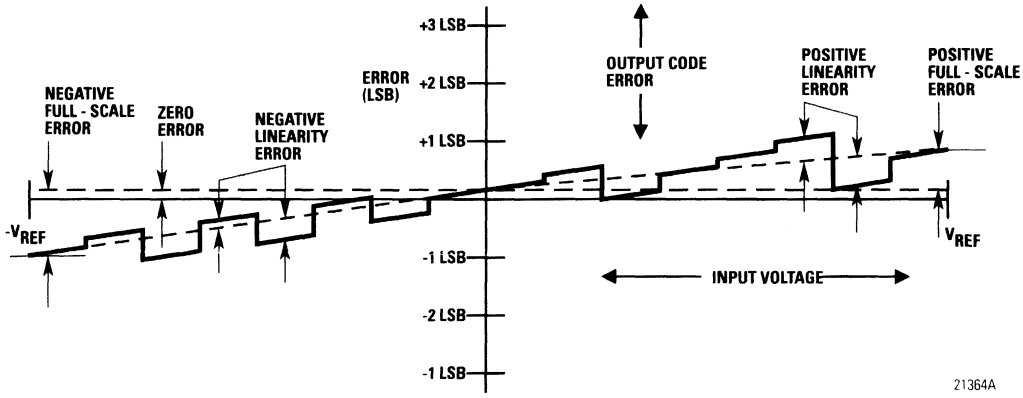


Figure 9. Output Test Loads

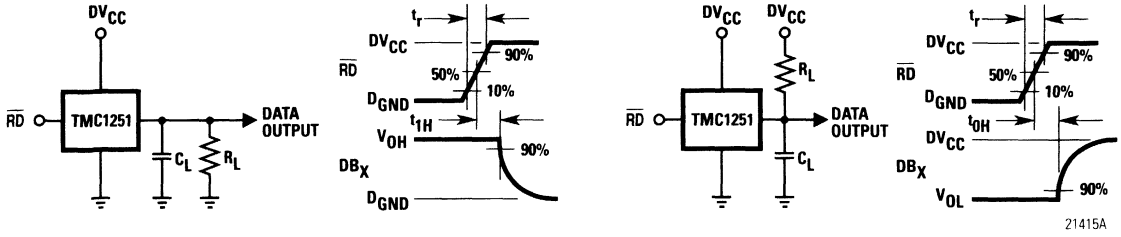
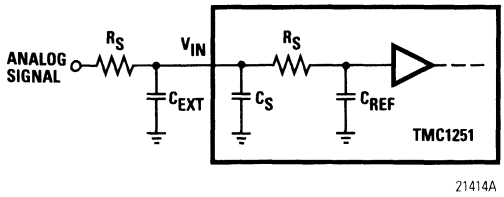


Figure 10. Analog Input Equivalent Circuit



Output Coding

Input Voltage	DB_{12} Sign	DB_{11} ..... DB_0 MSB LSB
>4.096V	0	1111 1111 1111
+4.096V	0	1111 1111 1111
+4.095V	0	1111 1111 1110
+4.094V	0	1111 1111 1101
•		•
•		•
+0.002V	0	0000 0000 0010
+0.001V	0	0000 0000 0001
0.000V	0	0000 0000 0000
-0.001V	1	1111 1111 1111
-0.002V	1	1111 1111 1110
•		•
•		•
-4.094V	1	0000 0000 0010
-4.095V	1	0000 0000 0001
-4.096V	1	0000 0000 0000
<-4.096V	1	0000 0000 0000

Note: The input voltage range used for this table is ±4.096 Volts and the input voltages are measured at code centers.

Absolute maximum ratings (beyond which the device may be damaged)[1,2]

Supply Voltages

DV_{CC}	–0.5 to +6.5V
AV_{CC}	–0.5 to +6.5V
V–	+0.5 to –6.5V
$AV_{CC} - DV_{CC}$[7]	–0.3 to +0.3V
$A_{GND} - D_{GND}$	–0.3 to +0.3V

Input Voltages

Digital Inputs	–0.3 to (DV_{CC} +0.3)V
Analog Inputs	(AV_{CC} + 0.3) to (V– – 0.3)V

Outputs

Digital Outputs, applied voltage	–0.5 to DV_{CC}
Input current, any pin, externally forced [3]	+5mA
Short-circuit duration (single output to GND)	unlimited

Temperature

Operating, case	–60 to +135°C
Lead, soldering (10 seconds)	+300°C
Storage	–65 to +150°C

Package input current [3]	+20mA
Package power dissipation at 25°C [4]	875mW
ESD Susceptibility [5]	2000V

Operating Conditions [1,2,9,16,17]

Parameter		Temperature Range: Industrial Min	Industrial Nom	Industrial Max	Extended Min	Extended Nom	Extended Max	Units
AV_{CC}, DV_{CC}	Positive Power Supply Voltages [6,7]	4.5	5.0	5.5	4.5	5.0	5.5	V
V–	Negative Power Supply Voltage	–4.5	-5.0	-5.5	–4.5	–5.0	–5.5	V
AV_{CC}-DV_{CC}	Power Supply Voltage Differential	–0.1	0.0	0.1	–0.1	0.0	0.1	V
A_{GND}-D_{GND}	Ground Voltage Differential	–0.1	0.0	0.1	–0.1	0.0	0.1	V
V_{IN}	Input Voltage Range	V– –.050	±4.096	AV_{CC}+.050	V– –.050	±4.096	AV_{CC}+.050	V
V_{REF}	Reference Voltage [6,7]	3.5	+4.096	AV_{CC}+.050	3.5	+4.096	AV_{CC}+.050	V
f_{CLK}	Clock Frequency	0.5	3.5	6.0	0.5	3.5	6.0	MHz
	Clock Duty Cycle	40	50	60	40	50	60	%
V_{IL}	Input Voltage, Logic LOW, all but CLK_{IN}, DV_{CC} = 4.75V		1.4	0.8		1.4	0.8	V
V_{IH}	Input Voltage, Logic HIGH, all but CLK_{IN}, DV_{CC} = 5.25V	2.0	1.4		2.0	1.4		V
I_{OL}	Output Current, Logic LOW	–6.0	–20		–6.0	–20		mA
I_{OH}	Output Current, Logic HIGH	8.0	20		8.0	20		mA
T_J	Junction Temperature, TMC1251B7B, TMC1251B7B1	–40		+85				°C
T_J	Junction Temperature, TMC1251B7F				–55		±125	°C

Electrical Characteristics [1,2,6,7,8,9,16]

Parameter		Test Conditions	Typ	Temperature Range: Industrial Min	Industrial Max	Extended Min	Extended Max	Units
DI_{CC}	DV_{CC} Supply Current	f_{CLK} = 2.0MHz, $\overline{CS}$ = HIGH	1.0		2.5		2.5	mA
AI_{CC}	AV_{CC} Supply Current	f_{CLK} = 2.0MHz, $\overline{CS}$ = HIGH	4.0		10.0		10.0	mA
I–	V- Supply Current	f_{CLK} = 2.0MHz, $\overline{CS}$ = HIGH	2.8		10.0		10.0	mA
C_{IN}	Analog Input Capacitance		65					pF
C_{REF}	Reference Input Capacitance		80					pF
I_{IL}	Input Current, Logic LOW	V_I = 0.0V	–0.005		–1.0		–1.0	µA
I_{IH}	Input Current, Logic HIGH	V_I = ±5.0V	0.005		1.0		1.0	µA
$V_{T\pm}$	Positive-going threshold, CLK_{IN}		2.8	2.7		2.7		V
V_{T-}	Negative-going threshold, CLK_{IN}		2.1		2.3		2.3	V
V_H	Hysteresis, CLK_{IN}	$V_{T\pm}$ - V_{T-}	0.7	0.4		0.4		V
V_{OL}	Output Voltage, Logic LOW	I_{OUT} = 1.6mA, V_{CC} = 4.75V			0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	I_{OUT} = –360µA, V_{CC} = 4.75V		2.4		2.4		V
		I_{OUT} = –10µA, V_{CC} = 4.75V		4.5		4.5		V
I_{OZL}	Output leakage current, LOW	V_{OUT} = 0.0V	–0.01		–3.0		–3.0	µA
I_{OZH}	Output leakage current, HIGH	V_{OUT} = 5.0V	0.01		3.0		3.0	µA

Switching characteristics [1,2,6,7,8,9,16,17]

Parameter		Test Conditions	Typ	Temperature Range				Units
				Industrial		Extended		
				Min	Max	Min	Max	
t_C	Conversion Time		$27/f_{CLK}$		$27/f_{CLK}+.25$		$27/f_{CLK}+.25$	µs
		f_{CLK} = 3.5MHz, $\overline{AZ}$ = HIGH	7.7		7.95		7.95	µs
		f_{CLK} = 1.75MHz, $\overline{AZ}$ = LOW	15.4		15.65		15.65	µs
		$\overline{T}$/H starts conversion,	$34/f_{CLK}$		$34/f_{CLK}+.25$		$34/f_{CLK}+.25$	µs
		f_{CLK} = 3.5MHz, $\overline{AZ}$ = HIGH	9.7		9.98		9.95	µs
t_A	Acquisition Time [14]	using $\overline{WR}$ only			$7/f_{CLK}+0.25$		$7/f_{CLK}+0.25$	µs
		R_S = 50Ω	3.5		3.5		3.5	µs
t_Z	Auto-Zero Time Plus		$33/f_{CLK}$		$33/f_{CLK}+.25$		$33/f_{CLK}+.25$	µs
	Acquisition Time	f_{CLK} = 1.75MHz	18.8		19.05		19.05	µs
t_{CAL}	Calibration Time		$1399/f_{CLK}$		$1399/f_{CLK}$		$1399/f_{CLK}$	µs
		f_{CLK} = 3.5MHz	399		400		400	µs
t_{PWCAL}	Calibration Pulse Width	Note 15	60	200		200		ns
t_{PWWR}	$\overline{WR}$ Pulse Width		60	200		200		ns
t_{DHE}	Hold-to-EOC Delay	using $\overline{WR}$ input	200		350		350	ns
		using $\overline{T}$/H input	100		150		150	ns
t_{RDINT}	$\overline{RD}$ or $\overline{WR}$ to Reset of $\overline{INT}$		100		175		175	ns
t_{ENA}	Output Enable Time	C_L = 100pF	50		95		95	ns
t_{RR}	$\overline{RD}$ to $\overline{RD}$ Pulse Width		30		60		60	ns
t_{DIS}	Data Disable Time	C_L = 100pF, R_L = 1kΩ	30		70		70	ns

System performance characteristics 1,2,6,7,8,9,16

Parameter		Test Conditions	Typ.	Temperature Range				Units
				Industrial		Extended		
				Min	Max	Min	Max	
E_{LIP}	Positive Integral Linearity Error	After Auto-Cal, 10,11						
		TMC1251B7B1			±0.5			LSB
		TMC1251B7F, TMC1251B7B			±1.0		±1.0	LSB
E_{LIN}	Negative Integral Linearity Error	After Auto-Cal, 10,11						
		TMC1251B7B1			±0.5			LSB
		TMC1251B7F, TMC1251B7B			±1.0		±1.0	LSB
E_{LD}	Differential Linearity Error	After Auto-Cal, 10,11		12		12		Bits
E_{FSP}	Positive full-scale error	After Auto-Cal, 11			±2.0		±2.0	LSB
		$\overline{AZ}$ = LOW, f_{CLK} = 1.75MHz			±1.5		±1.5	LSB
E_{FSN}	Negative full-scale error	After Auto-Cal, 11			±2.0		±2.0	LSB
		$\overline{AZ}$ = LOW, f_{CLK} = 1.75MHz			±1.5		±1.5	LSB
E_Z	Zero Error 11,12	After Auto-Cal or Auto-Zero,			±2.5		±2.5	LSB
		$\overline{AZ}$ = LOW, f_{CLK} = 1.75MHz			±1.0		±1.0	LSB
PSS_Z	Power Supply Sensitivity, Zero Error 13	AV_{CC} = DV_{CC} = ±5.0 ±5%	±0.125					LSB
		V– = –5.0 ±5%, V_{REF} = ±4.75V						
PSS_F	Power Supply Sensitivity, Full-scale error	AV_{CC} = DV_{CC} = ±5.0 ±5%	±0.125					LSB
		V– = –5.0 ±5%, V_{REF} = ±4.75V						
PSS_L	Power Supply Sensitivity, Linearity error	AV_{CC} = DV_{CC} = ±5.0 ±5%	±0.125					LSB
		V– = –5.0 ±5%, V_{REF} = ±4.75V						
$SINAD_U$ 18	Unipolar Signal-to-Noise and Distortion Ratio	f_{IN} = 1kHz, V_{IN} = 4.85V p-p	72					dB
		f_{IN} = 20kHz, V_{IN} = 4.85V p-p	72					dB
$SINAD_B$ 18	Unipolar Signal-to-Noise and Distortion Ratio	f_{IN} = 1kHz, V_{IN} = ±4.85V	76					dB
		f_{IN} = 20kHz, V_{IN} = ±4.85V	76					dB
BW_U 18	Unipolar -3dB bandwidth	V_{IN} = 4.85V p-p	32					kHz
BW_B 18	Bipolar -3dB bandwidth	V_{IN} = ±4.85V	25					kHz
	Aperture time		100					ns
	Aperture uncertainty		100					ps_{RMS}

A

Notes for specification tables

1. Absolute Maximum Ratings are limits beyond which the device may be damaged. Operating Conditions are limits under which the device is guaranteed to be functional, but those limits do not guarantee specific performance. Guaranteed specifications and test conditions are shown in the *Electrical, Switching and System Performance Characteristics Tables*. The guaranteed specifications apply only for the test conditions listed in the *Electrical, Switching and System Performance Characteristics Tables*. Some performance characteristics may degrade when the device is operated outside the listed test conditions.

2. All voltages are measured with respect to A_{GND} and D_{GND}, unless otherwise specified.

3. When the voltage at any pin exceeds the power supply voltages (< V– or >AV_{CC} or >DV_{CC}), the current at that pin must be limited to 5mA. The 20mA maximum package input current rating allows the voltage any any four pins, with a current limit of 5mA, to simultaneously exceed the power supply voltages.

4. The power dissipation of this device under normal operation should not exceed 191mW (quiescent power plus one TTL load on each of the ten digital outputs). Care must be taken to ensure that Absolute Maximum Ratings are not violated when any inputs

Notes for specification tables (cont.)

or outputs are driven to voltages greater than power supply voltages. The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum allowable junction temperature), θ_{JA} (junction-to-ambient thermal resistance of the package). and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is given by:

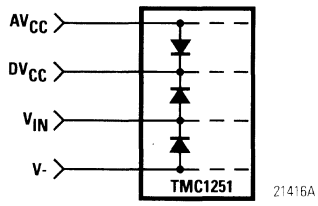
$$P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$$

or the number given in the ***Absolute Maximum Ratings Table***, whichever is lower. For the TMC1251, T_{Jmax} is 125°C and the typical thermal resistance (θ_{JA}) of the TMC1251 with B7F, B7B1, and B7B suffixes when board mounted is 51°C/W.

5. Human body model, 100pF discharged through a 1.5kΩ resistor.

6. Two on-chip diodes are tied to the analog input as shown in the following Figure, ***Parasitic Diode Structure***. A/D conversion errors can occur if these diodes are forward-biased more than 50mV. Therefore, if AV_{CC} and DV_{CC} are +4.75 Volts and V- is –4.75 Volts, the analog input range must be no greater than ±4.80 Volts.

Parasitic Diode Structure



7. To guarantee accuracy, it is required that AV_{CC} and DV_{CC} be connected to the same power source but with separate decoupling capacitors at each pin. This prevents the parasitic diode between AV_{CC} and DV_{CC} from being forward biased.

8. Accuracy is guaranteed with f_{CLK} equal to 2.0MHz. Accuracy may degrade at higher clock frequencies.

9. Typical specifications are at T_J = 25°C and represent the most likely parametric norm (statistical "mode").

10. Positive linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative linearity error the straight line passes through negative full-scale and zero. (See ***Simplified Error Characteristic Curves***)

11. The TMC1251's self-calibration technique ensures linearity, full-scale and offset errors as specified. Noise inherent to the self-calibration process will result in a repeatability uncertainty of +0.20 LSB.

12. When t_A changes, an Auto-Zero or Auto-Cal cycle will be required for specified performance. (see ***Typical Performance Curves***)

13. After Auto-Zero or Auto-Cal cycle execution at the specified power supply extremes.

14. When using $\overline{WR}$ to start an A/D conversion, if the CLK_{IN} is asynchronous with respect to the rising edge of $\overline{WR}$ an uncertainty of one clock period exists in the t_A interval. Therefore, the minimum t_A is six clock periods and the maximum t_A is 7 clock periods. If the falling edge of CLK_{IN} is synchronous with respect to the rising edge of $\overline{WR}$ then t_A will be exactly 6.5 clock periods. This does not occur when $\overline{T}/H$ is used.

15. The $\overline{CAL}$ input must go HIGH before an A/D conversion is started.

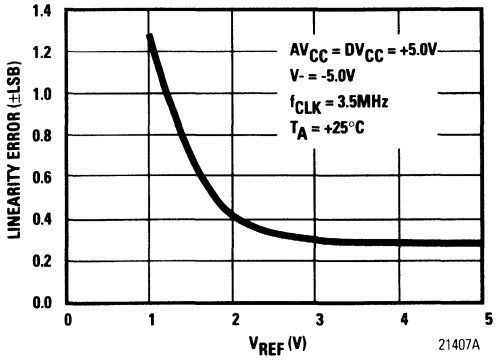
16. Guaranteed specifications apply for $AV_{CC} = DV_{CC} = \pm 5.0V$, $V- = -5.0V$, $V_{REF} = 5.0V$ and f_{CLK} = 2.0MHz unless otherwise specified.

17. Rise and fall times for digital inputs = 20ns, unless otherwise specified.

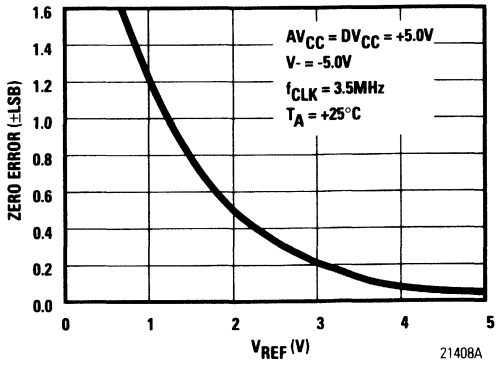
18. Dynamic performance parameters are valid only after an Auto-Cal cycle has been completed. For guaranteed dynamic performance parameters, use TMC12441 or TMC12451 A/D converters.

Typical Performance Curves

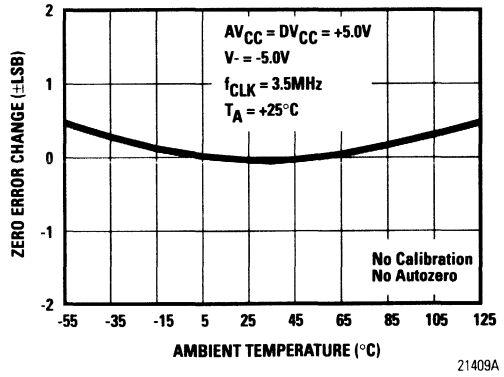
A. Linearity Error vs. V_{REF}



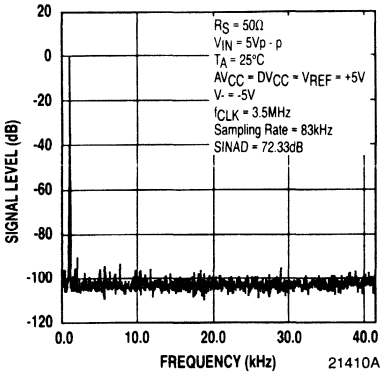
B. Zero Error vs. V_{REF}



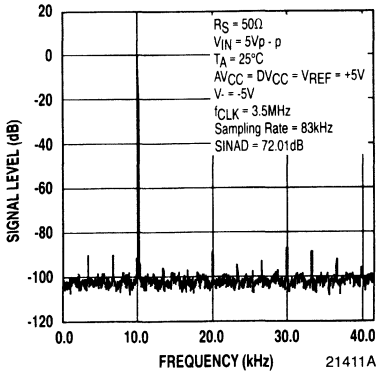
C. Zero Error Change vs. Ambient Temperature



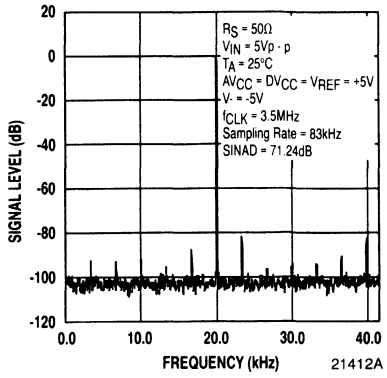
D. Unipolar Spectral Response with 1kHz Sinewave Input



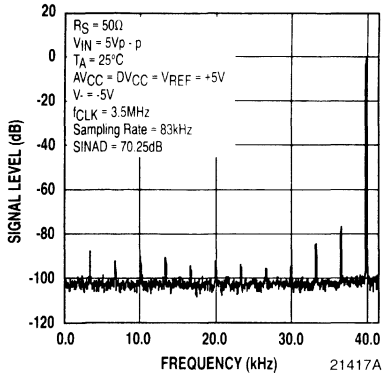
E. Unipolar Spectral Response with 10kHz Sinewave Input



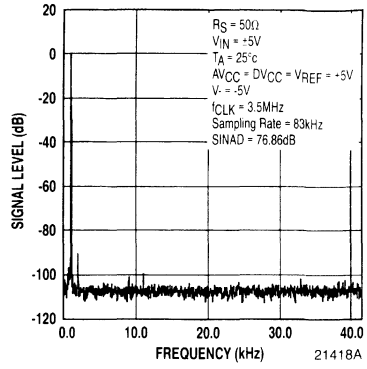
F. Unipolar Spectral Response with 20kHz Sinewave Input



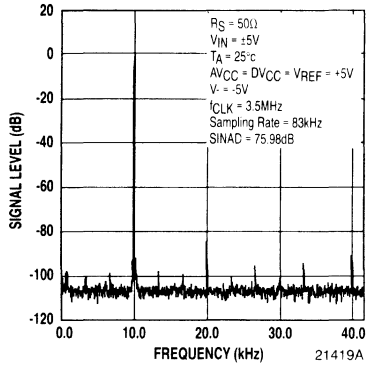
G. Unipolar Spectral Response 40kHz Sinewave Input



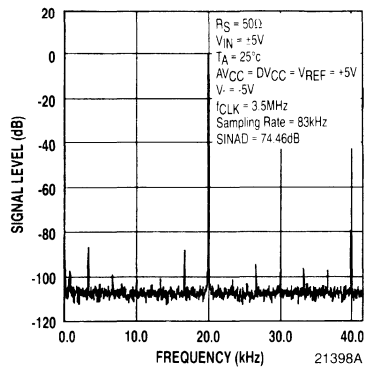
H. Bipolar Spectral Response with 1kHz Sinewave Input



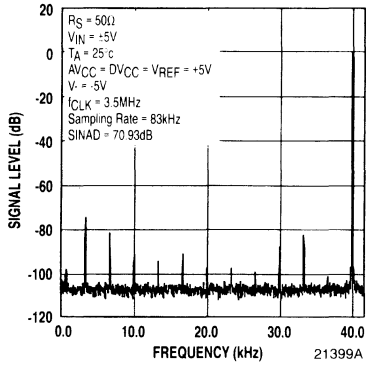
I. Bipolar Spectral Response with 10kHz Sinewave Input



J. Bipolar Spectral Response with 20kHz Sinewave Input



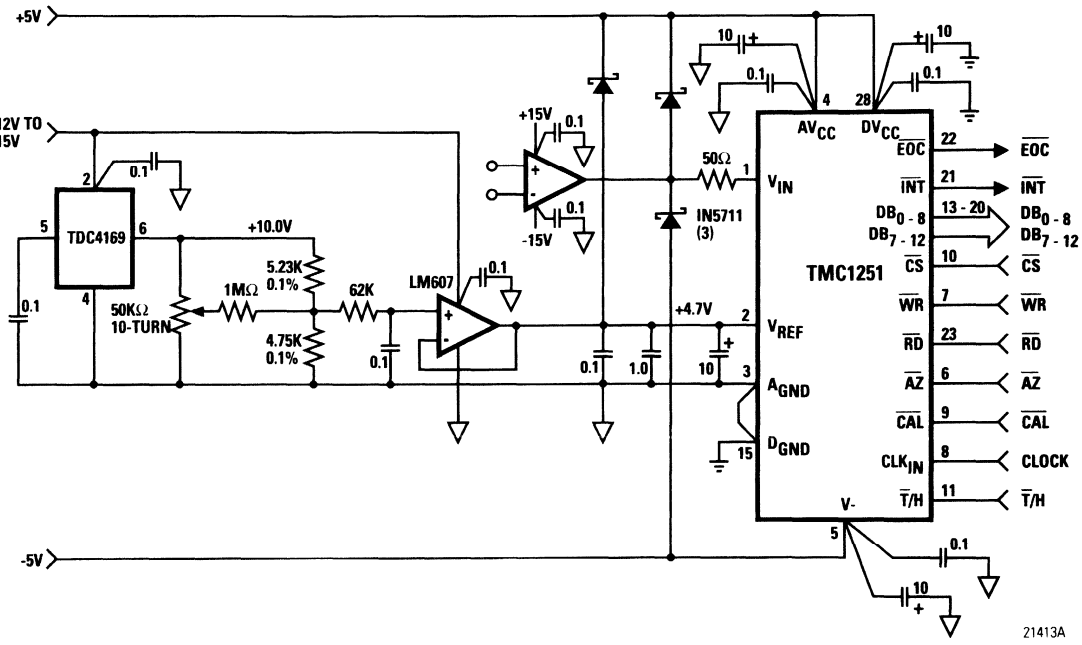
K. Bipolar Spectral Response with 40kHz Sinewave Input



The Typical Interface Circuit

Noise on AV_{CC}, DV_{CC} or V- power supply inputs can cause A/D conversion errors should the TMC1251 comparator be influenced by that noise. The TMC1251 is especially sensitive during the Auto-Zero or Auto-Cal cycles to power supply noise. Low inductance 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors are recommended for power supply decoupling. Separate decoupling capacitors should be placed close to the DV_{CC}, AV_{CC} and V- pins.

Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC1251B7F	EXT, T_A = –55°C to 125°C	Commercial	28-pin CERDIP	1251B7F
TMC1251B7B	STD, T_A = –40°C to 85°C	Commercial	28-pin CERDIP	1251B7B
TMC1251B7B1	STD, T_A = –40°C to 85°C	Commercial	28-pin CERDIP	1251B7B1
TMC1251E1C	STD, T_A = 0°C to 70°C	-	Eurocard PC Board	1251E1C

TMC12441

Self-Calibrating 12-Bit Plus Sign, 13μs, μP-Compatible Sampling A/D Converter
Tested and Specified for DSP Applications

A

TRW's TMC12441 is a CMOS successive approximation analog-to-digital converter with 13-bit resolution. Physically identical to the TMC1241, the TMC12441 is dynamically tested and guaranteed to meet Signal-to-Noise Ratio, Total Harmonic Distortion, Two-tone Intermodulation Distortion, Effective Bits, and Bandwidth specifications.

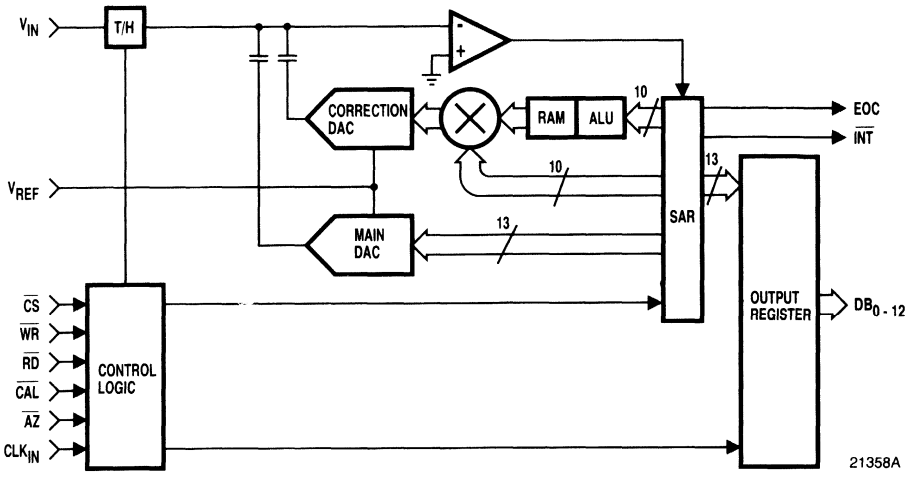
The outstanding performance of the TMC12441 is the result of self-calibration, which reduces linearity and full-scale errors while optimizing dynamic performance. The TMC12441 performs an Auto-Zero function that minimizes offset error. The Auto-Zero function can be performed as needed or prior to every A/D conversion.

The TMC12441 includes a track/hold input stage for sampling the analog input signal. Both unipolar and bipolar analog input voltage ranges (0 to +5 and ±5V) are accommodated. The TMC12441 requires only two power supplies, ±5V. Its two's complement output data format uses the 13th bit to indicate the polarity of the input signal. Digital inputs and outputs are compatible with TTL or CMOS logic levels and have microprocessor interface features.

Features

- Guaranteed SNR, THD, IMD, EFB, And Bandwidth
- 13-Bit Resolution, 12 Bits Plus Sign
- Internal Track/Hold
- Conversion Time 13μs, Maximum
- Auto-Calibration And Auto-Zero Cycles
- Linearity Error Less Than ±1/2 LSB
- Offset Error Less Than ±1 LSB
- Full-Scale Error Less Than ±1 LSB
- Power Consumption 70mW, Maximum
- No Missing Codes, Guaranteed
- TTL/CMOS Compatible
- Standard 28 Pin DIP Package

Functional Block Diagram



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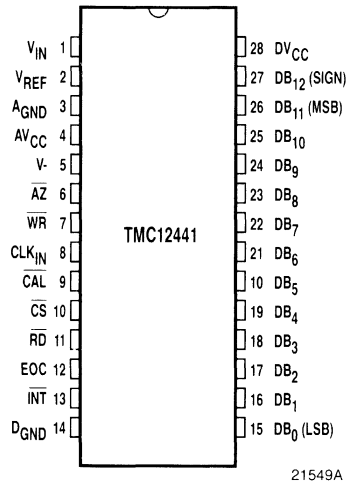
Applications

- Ultrasound Systems
- Vibration Analysis
- Audio/Speech Processing
- Sonar
- Motion Control
- Digital Signal Processing

Pin Assignments



28 Pin CERDIP – B6 Package

Functional Description

General Information

The TMC12441 is a successive approximation A/D converter with 13-bit resolution (12-bit plus sign). The TMC12441 can perform Auto-Cal and Auto-Zero routines to minimize full-scale, linearity and offset errors while optimizing dynamic performance. It comprises a D/A converter, precision comparator and a Successive Approximation Register (SAR) along with digital and analog circuitry for self-calibration. The TMC12441 is identical with TRW's TMC1241 except that it is fully tested and specified under dynamic conditions. Signal-to-Noise Ratio, Total Harmonic Distortion, Two-tone Intermodulation Distortion, Effective Bits and Bandwidth are tested and guaranteed under both bipolar and unipolar signal conditions.

The Auto-Zero cycle is an internal calibration sequence that corrects for A/D offset error caused by the input offset voltage of the comparator. The Auto-Cal cycle is a calibration sequence that not only corrects offset error but also corrects for full-scale and linearity errors caused by D/A converter gain and linearity errors. The Auto-Cal feature eliminates the need for trimming or other adjustment methods in the manufacture of the TMC12441. The Auto-Cal cycle restores the accuracy of the TMC12441 whenever it is requested. This ensures excellent long-term and temperature stability.

Power and Ground

The digital and analog power supply voltage range of the TMC12441 is +4.5V to +5.5V. To guarantee accuracy, it is required that the AV_{CC}, pin 4, and DV_{CC}, pin 28, be connected to the same power source, but with separate decoupling capacitors (10μF tantalum and a 0.1μF ceramic) between AV_{CC} and DV_{CC} and ground. V–, pin 5, has a range of –4.5V to –5.5V and and should have 10μF tantalum and 0.1μF ceramic capacitors for power supply decoupling.

Although A_{GND} and D_{GND}, pins 3 and 14 respectively, are distinguished from each other on the TMC12441, they should be connected together on the system printed circuit board to eliminate differential ground noise voltages which may degrade performance. A_{GND} and D_{GND} should be connected together as close to the TMC12441 as possible.

Analog Inputs

The voltage applied to the V_{REF} input, pin 2, defines the input voltage range of the V_{IN} input, pin 1, over which 4095 positive output codes and 4096 negative output codes are found. The A/D converter can be used in either ratiometric or absolute applications. The voltage source driving V_{REF} must have a low output impedance and low noise. The circuit in the *Typical Interface Circuit* is a good example of a very stable reference source for the TMC12441.

In a ratiometric application, the analog input voltage is proportional to the voltage used for the V_{REF}. If V_{IN} is related or proportional to AV_{CC}, V_{REF} can be connected directly to AV_{CC}. Here, V_{IN} and V_{REF} are related and track each other as the power supply voltage changes, making the output code of the TMC12441 independent of power supply voltage variations.

Analog Inputs (cont.)

For absolute accuracy, where the V_{IN} varies independently of power supply voltage, V_{REF} should be driven from a time and temperature-stable voltage source like that shown in the *Typical Interface Circuit*. The magnitude of V_{REF} may require an adjustment to achieve system gain requirements.

Due to the architecture of the TMC12441, a variable current will flow into or out (depending on V_{IN} polarity) of the V_{IN} pin at the start of the analog input sampling period, t_A. The peak value of this current is proportional to the magnitude of the applied V_{IN}. A small capacitor from V_{IN} to A_{GND} can be used to reduce noise and clock feedthrough due to inductive coupling from long input leads and will not degrade the accuracy of the conversion. It is advisable, however, to keep V_{IN} and V_{REF} input lines as short as possible.

The analog input can be modeled as shown in the *Analog Input Equivalent Circuit*. Large source resistance, R_S, will lengthen the time necessary for the voltage on C_{REF} to settle to within 1/2 LSB of the voltage on V_{IN}. With f_{CLK} of 2MHz, t_A takes seven clock periods, or 3.5μs. When R_S is less than or equal to 1kΩ, a 5.0V V_{IN} will have adequate time to settle.

Dynamic Performance

For Digital Signal Processing applications, it is not sufficient to evaluate and qualify an A/D converter only on the basis of its integral or differential linearity characteristics. In DSP applications, the A/D converter is usually digitizing dynamic signals (as opposed to static) and new concerns about noise, distortion, and frequency response become important.

The TMC12441 is intended for use in DSP applications and carries with it specifications that are not normally associated with similar A/D converters intended for application in process control, industrial control, data acquisition, and instrumentation.

Signal-to-Noise Ratio, Total Harmonic Distortion, and Two-tone Intermodulation Distortion are tested and guaranteed parameters of the TMC12441. These parameters are tested by having the A/D converter digitize a sinewave at a specified frequency and amplitude. Data is transferred from the A/D converter to a computer where Fast Fourier Transform (FFT) analysis converts the time-domain data into the frequency-domain where SNR, THD and IMD are extracted. The Effective Bits parameter of the TMC12441 is calculated from Signal-to-Noise Ratio by:

$$EFB = (SNR - 1.8)/6.02$$

A

Auto-Cal and Auto-Zero Cycles

When power is initially applied to the TMC12441, an Auto-Cal cycle is executed which cannot be interrupted. Since the power supply, reference, and clock are not usually stable at initial power-up, this first Auto-Cal cycle will not result in an accurate calibration of the TMC12441. An additional calibration cycle should be started after the power supplies, reference, and clock have been given adequate time to stabilize.

When $\overline{CAL}$, pin 9, is LOW, the TMC12441 is reset and an Auto-Cal cycle is initiated. During the Auto-Cal cycle, correction values are determined for the offset voltage of the comparator as well as linearity and gain errors. These values are stored in the internal RAM and used during A/D conversion cycles to reduce the TMC12441's gain, offset, and linearity errors to the specified limits. It is only necessary to go through the Auto-Cal cycle once after initial power is applied.

To correct for any change in the offset error of the A/D converter, the Auto-Zero cycle can be used. It may be necessary to execute an Auto-Zero cycle whenever the ambient temperature changes significantly (See the curve titled *"Zero Error Change vs. Ambient Temperature"* in the *Typical Performance Curves*). A change in the ambient temperature will cause the offset voltage of the comparator to change, which may cause the offset error of the A/D converter to be greater than its specified limit.

With the $\overline{AZ}$ input, pin 6, held LOW during a conversion cycle, the TMC12441 will execute an Auto-Zero cycle before the actual A/D conversion cycle is started. The total conversion time (t_C) is increased by 26 clock periods when Auto-Zero is used. An Auto-Zero cycle will reduce the offset error of the TMC12441 to less than $\pm$1 LSB.

Microprocessor Interface Controls

On initial power-up, an Auto-Cal cycle is executed by bringing $\overline{CAL}$ LOW while $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ are HIGH. To acknowledge that the Auto-Cal cycle is in progress, EOC goes LOW after the falling edge of $\overline{CAL}$ and remains LOW during the Auto-Cal cycle duration of 1,396 clock periods. During the Auto-Cal cycle, first the comparator offset error is determined and then the D/A converter gain and linearity errors are found. Correction factors for these errors are stored in the internal RAM.

An A/D conversion cycle is initiated by bringing $\overline{CS}$ and $\overline{WR}$ LOW. The $\overline{AZ}$ input should be tied HIGH or LOW during the conversion process. If $\overline{AZ}$ is LOW when A/D conversion is executed, an Auto-Zero cycle (duration equals 26 clock periods) occurs before the A/D conversion is started. If $\overline{AZ}$ is HIGH, no Auto-Zero cycle is executed. Once the A/D conversion sequence is started, V_{IN} is tracked for seven clock periods and held thereafter. EOC then goes LOW, indicating that V_{IN} is no longer being tracked and that the successive approximation conversion sequence has started.

During an A/D conversion cycle, the held V_{IN} is successively compared to the output of the corrected D/A converter (main and correction D/A converters).

First, the held voltage is compared to analog ground to determine its polarity (sign bit). The sign bit is set LOW for positive V_{IN} and HIGH for negative V_{IN}. Next, the MSB of the D/A converter is set HIGH with all other bits LOW. If the the held voltage is greater than the output of the D/A converter, then the MSB is left HIGH; otherwise, it is set LOW. The next bit is then set HIGH, making the output of the D/A converter 3/4 or 1/4 of full-scale, depending on the outcome of the previous bit. If the held voltage is greater than the new D/A converter value then the bit remains HIGH. If the held voltage is less than the new D/A converter value the bit is set LOW. This process continues until each bit has been tested. The result is then transferred to the output register of the TMC12441. EOC goes HIGH and $\overline{INT}$ goes LOW indicating the end of the conversion. The result can now be read by bringing $\overline{CS}$ and $\overline{RD}$ LOW to enable the $DB_{0\text{-}12}$ outputs.

The ***A/D Control Input Functions (Table 1)*** summarizes the effect of the digital control inputs on the TMC12441. Test Mode (where $\overline{RD}$ is HIGH and $\overline{CS}$ and $\overline{CAL}$ are LOW) is used in the manufacturing process of the TMC12441. Care should be taken to avoid this mode. In Test Mode DB_2, DB_3, DB_5, and DB_6 become active outputs, which may cause data bus contention.

The TMC12441 can be completely reset, aborting all sequences that may be in progress. The A/D converter is reset where a new conversion is started by taking $\overline{CS}$ and $\overline{WR}$ LOW. If this occurs when V_{IN} is being tracked or when EOC is LOW, the Auto-Cal correction factors in RAM may be corrupted. After reset, it is necessary to execute an Auto-Cal cycle before the next A/D conversion cycle. The Auto-Cal cycle cannot be reset once started.

Summary of Control Inputs

$\overline{CS}$ — The Chip Select control input, pin 10, is active LOW and enables the $\overline{WR}$ and $\overline{RD}$ functions.

$\overline{WR}$ — The A/D conversion is started on the rising edge of the Write control input, pin 7, when $\overline{CS}$ is LOW.

$\overline{RD}$ — The Read control input, pin 11, is active LOW and is used to enable the three-state data outputs and reset $\overline{INT}$ HIGH when $\overline{CS}$ is LOW.

$\overline{AZ}$ — With the $\overline{AZ}$ input, pin 6, held LOW during a conversion cycle, the TMC12441 will execute an Auto-Zero cycle before the actual A/D conversion cycle is started. The total conversion time (t_C) is increased by 26 clock periods when Auto-Zero is used.

$\overline{CAL}$ — When $\overline{CAL}$, pin 9, is LOW, the TMC12441 is reset and an Auto-Cal cycle is initiated.

CLK_{IN} — The clock input, pin 8, controls all sequence timing and A/D conversion time. The frequency range for CLK_{IN} is from 0.50 to 4MHz.

EOC — The End-of-Conversion control output, pin 12, is LOW during A/D conversion, Auto-Cal and Auto-Zero cycles.

$\overline{INT}$ — The interrupt control output, pin 13, goes LOW when a conversion has been completed and indicates that the conversion result is available from the output register.

Summary of Control Inputs (cont.)

$\overline{INT}$ (cont.) Reading the outputs or starting an A/D conversion, Auto-Cal or Auto-Zero cycle will reset in $\overline{INT}$ going HIGH.

$DB_{0\text{-}12}$ The three-state outputs, pins 15 to 27, give A/D conversion results in two's complement format with DB_{12} being the sign bit, DB_{11} the MSB and DB_0 the LSB.

Table 1. A/D Control Input Functions

Control Inputs					A/D Function
$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{CAL}$	$\overline{AZ}$	
⊔	⊔	1	1	1	Start A/D conversion without Auto-Zero
⊔	1	⊔	1	1	Read A/D conversion result without Auto-Zero
⊔	⊔	1	1	0	Start A/D conversion with Auto-Zero
1	x	x	⊔	x	Start Auto-Cal cycle
0	x	1	0	x	Test Mode (DB_2, DB_3, DB_5 and DB_6 active)

Package Interconnections

Signal Type	Signal Name	Function	Value	B6 Package Pins
Power	AV_{CC}	Positive Analog Supply	+5.0V	4
	DV_{CC}	Positive Digital Supply	+5.0V	28
	V–	Negative Analog Supply	–5.0V	5
Ground	A_{GND}	Analog Ground	0.0V	3
	D_{GND}	Digital Ground	0.0V	14
Analog Inputs	V_{IN}	Analog Signal Input	±4.7V	1
	V_{REF}	Reference Input	+4.7V	2
Digital Inputs	CLK_{IN}	Clock Input	TTL	8
	$\overline{AZ}$	Auto-Zero	TTL	6
	$\overline{CAL}$	Calibrate	TTL	9
	$\overline{RD}$	Read	TTL	11
	$\overline{WR}$	Write	TTL	7
	$\overline{CS}$	Chip Select	TTL	10
Digital Outputs	EOC	End of Calibration	TTL	12
	$\overline{INT}$	Interrupt	TTL	13
	DB_{12} SGN	Sign Bit	TTL	27
	DB_{11} MSB	Most Significant Bit	TTL	26
	DB_{10}		TTL	25
	DB_9		TTL	24
	DB_8		TTL	23
	DB_7		TTL	22
	DB_6		TTL	21
	DB_5		TTL	20
	DB_4		TTL	19
	DB_3		TTL	18
	DB_2		TTL	17
	DB_1		TTL	16
	DB_0 LSB	Least Significant Bit	TTL	15

Figure 1. Timing Diagram, Auto-Cal Cycle ($\overline{CS}$ = HIGH, $\overline{WR}$ = $\overline{RD}$ = $\overline{AZ}$ = Don't Care)

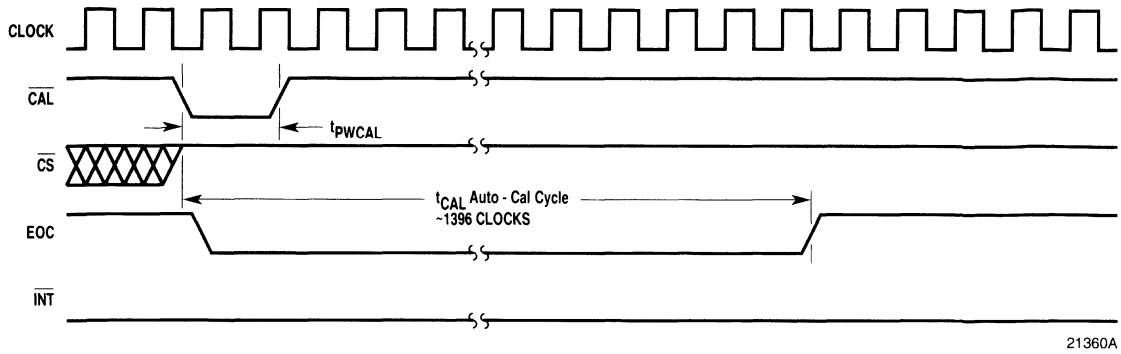


Figure 2. Timing Diagram, A/D Conversion Cycle with Auto-Zero ($\overline{CAL}$ = HIGH, $\overline{AZ}$ = LOW)

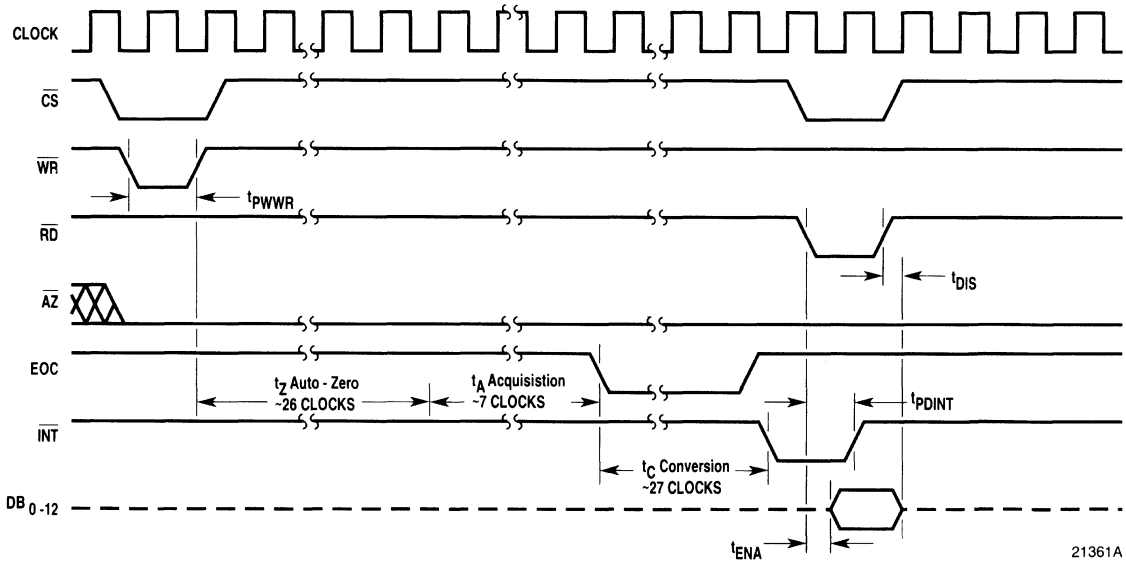


Figure 3. Timing Diagram, Normal A/D Conversion Cycle without Auto-Zero ($\overline{CAL} = \overline{AZ} = HIGH$)

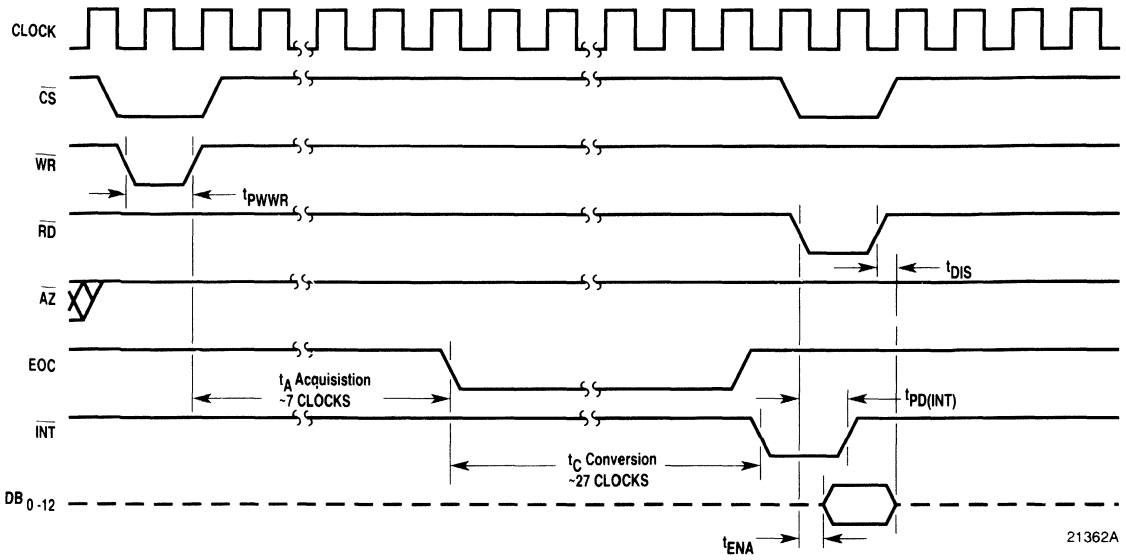


Figure 4. Simplified Error Characteristics vs. Output Code without Auto-Cal or Auto-Zero Cycles

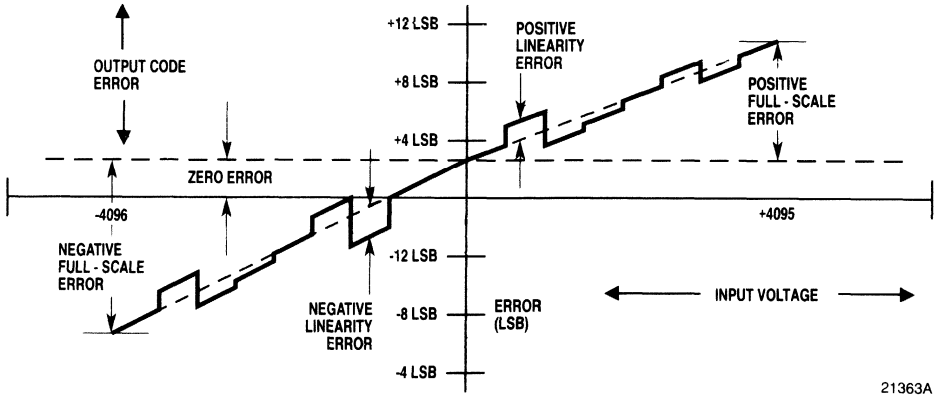


Figure 5. Simplified Error Characteristics vs. Output Code after Auto-Cal

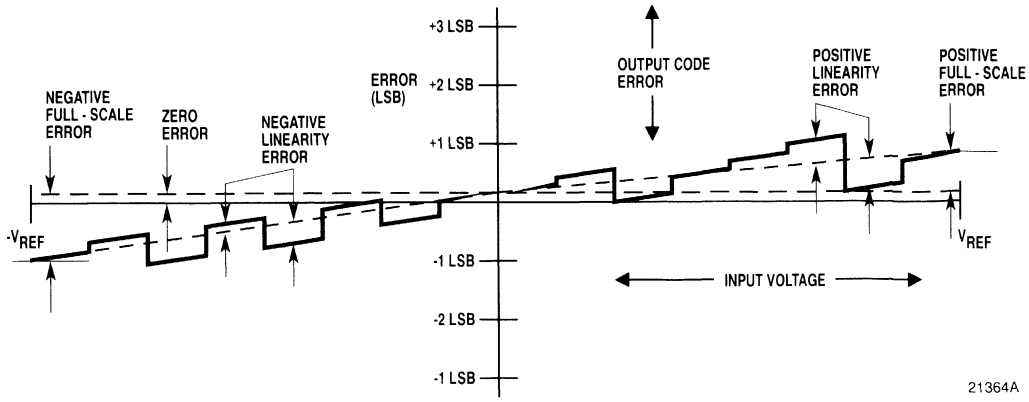


Figure 6. Transfer Characteristics

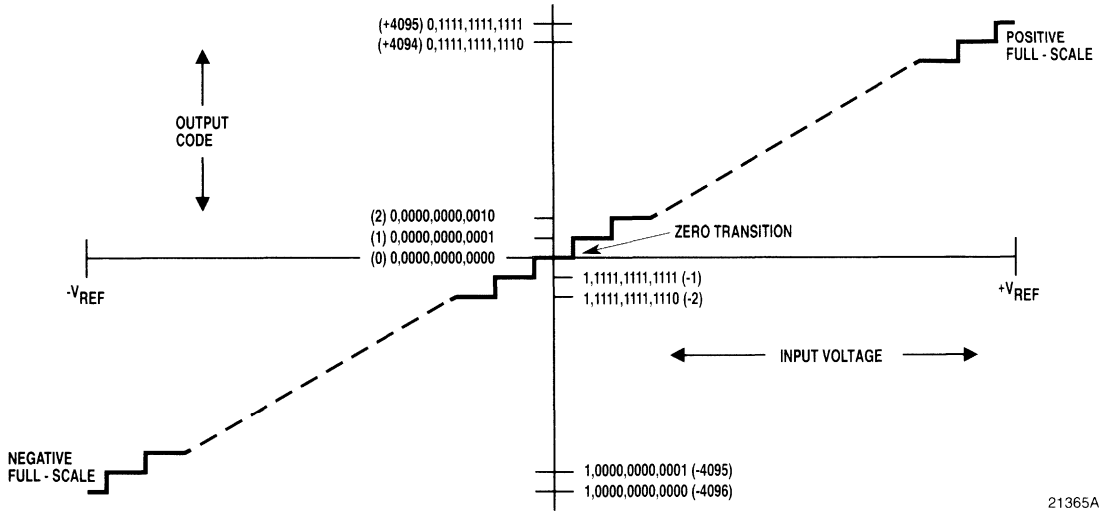


Figure 7. Analog Input Equivalent Circuit

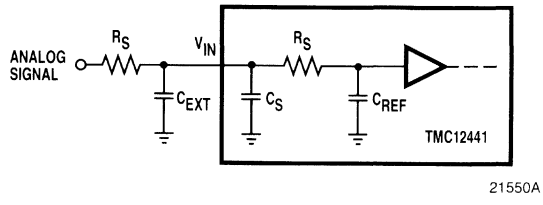
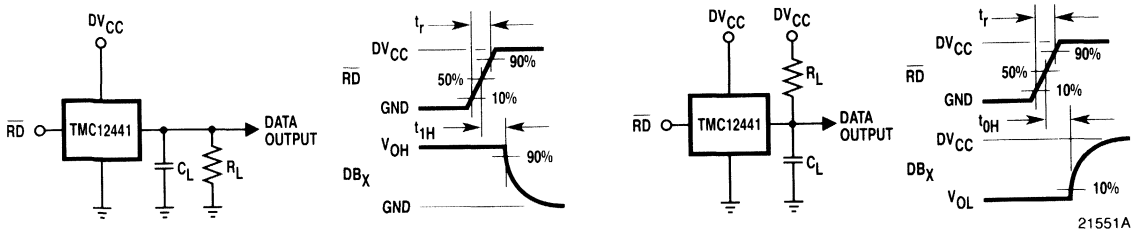


Figure 8. Output Test Loads



Output Coding Table

Input Voltage	DB_{12} Sign	DB_{11} MSB	. . .	DB_0 LSB
>4.096V	0	1111	1111	1111
+4.096V	0	1111	1111	1111
+4.095V	0	1111	1111	1110
+4.094V	0	1111	1111	1101
•			•	
•			•	
+0.002V	0	0000	0000	0010
+0.001V	0	0000	0000	0001
0.000V	0	0000	0000	0000
−0.001V	1	1111	1111	1111
−0.002V	1	1111	1111	1110
•			•	
•			•	
−4.094V	1	0000	0000	0010
−4.095V	1	0000	0000	0001
−4.096V	1	0000	0000	0000
≤4.096V	1	0000	0000	0000

Note: 1. The input voltage range used for this table is ±4.096V and the input voltages are measured at code centers.

Absolute maximum ratings (beyond which the device may be damaged) [1,2]

Supply Voltages

DV_{CC}	−0.5 to +6.5V
AV_{CC}	−0.5 to +6.5V
V−	+0.5 to −6.5V
$AV_{CC} - DV_{CC}$ [7]	−0.3 to +0.3V
$A_{GND} - D_{GND}$	−0.3 to +0.3V

Input Voltages

Digital Inputs	DV_{CC} + 0.3) to −0.3V
Analog Inputs	(AV_{CC} + 0.3) to (V− − 0.3)V

Outputs

Digital Outputs, applied voltage	−0.5V to DV_{CC}
Input current, any pin, externally forced [3]	±5mA
Short-circuit duration (single output to GND)	Unlimited

Temperature

Operating, case	−60 to +135°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Package Input Current [3]	±20mA
Package Power Dissipation at 25°C [4]	875mW
ESD Susceptibility [5]	2000V

Operating conditions [1,2,16,18]

Parameter		Temperature Range						Units
		Industrial			Extended			
		Min	Nom	Max	Min	Nom	Max	
AV_{CC}, DV_{CC}	Positive Power Supply Voltages [6,7]	4.5	5.0	5.5	4.5	5.0	5.5	V
V–	Negative Power Supply Voltage	–4.5	–5.0	–5.5	–4.5	–5.0	–5.5	V
$AV_{CC} - DV_{CC}$	Power Supply Voltage Differential	–0.1	0.0	0.1	–0.1	0.0	0.1	V
$A_{GND} - D_{GND}$	Ground Voltage Differential	–0.1	0.0	0.1	–0.1	0.0	0.1	V
V_{IN}	Input Voltage Range	V– –.050	±4.096	AV_{CC} +.050	V– –.050	±4.096	AV_{CC} +.050	V
V_{REF}	Reference Voltage [6,7]	3.5	+4.096	AV_{CC} +.050	3.5	+4.096	AV_{CC} +.050	V
f_{CLK}	Clock Frequency	0.5	2.0	4.0	0.5	2.0	4.0	MHz
	Clock Duty Cycle	40	50	60	40	50	60	%
V_{IL}	Input Voltage, Logic LOW, all but CLK_{IN}, DV_{CC}=4.75V		1.4	0.8		1.4	0.8	V
V_{IH}	Input Voltage, Logic HIGH, all but CLK_{IN}, DV_{CC}=5.25V	2.0	1.4		2.0	1.4		V
I_{OL}	Output Current, Logic LOW	–6.0	–20		–6.0	–20		mA
I_{OH}	Output Current, Logic HIGH	8.0	20		8.0	20		mA
T_J	Junction Temperature, TMC12441B6B, TMC12441B6B1	–40		+85				°C
T_J	Junction Temperature, TMC12441B6F				–55		+125	°C

Electrical characteristics within specified operating conditions [1,2,6,7,8,9,16]

Parameter		Test Conditions	Temperature Range					Units
			Typ	Industrial		Extended		
				Min	Max	Min	Max	
DI_{CC}	DV_{CC} Supply Current	f_{CLK}=2.0MHz, $\overline{CS}$=HIGH	1.0		2.0		2.0	mA
AI_{CC}	AV_{CC} Supply Current	f_{CLK}=2.0MHz, $\overline{CS}$=HIGH	2.8		6.0		6.0	mA
I–	V– Supply Current	f_{CLK}=2.0MHz, $\overline{CS}$=HIGH	2.8		6.0		6.0	mA
C_{IN}	Analog Input Capacitance		65					pF
C_{REF}	Reference Input Capacitance		80					pF
I_{IL}	Input Current, Logic LOW		–0.005		–1.0		–1.0	μA
I_{IH}	Input Current, Logic HIGH		0.005		1.0		1.0	μA
V_{T+}	Positive-Going Threshold, CLK_{IN}		2.8	2.7		2.7		V
V_{T-}	Negative-Going Threshold, CLK_{IN}		2.1		2.3		2.3	V
V_H	Hysteresis, CLK_{IN}	$V_{T+} - V_{T-}$	0.7	0.4		0.4		V
V_{OL}	Output Voltage, Logic LOW	I_{OUT}=1.6mA, V_{CC}=4.75V			0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	I_{OUT}=–360μA, V_{CC}=4.75V		2.4		2.4		V
		I_{OUT}=–10μA, V_{CC}=4.75V		4.5		4.5		V
I_{OZL}	Output Leakage Current, LOW	V_{OUT}=0.0V	–0.01		–3.0		–3.0	μA
I_{OZH}	Output Leakage Current, HIGH	V_{OUT}=5.0V	0.01		3.0		3.0	μA

Switching characteristics within specified operating conditions [1,2,6,7,8,9,16,18]

Parameter		Test Conditions	Temperature Range					Units
			Typ	Industrial Min	Industrial Max	Extended Min	Extended Max	
t_C	Conversion Time				$27/f_{CLK}+0.3$		$27/f_{CLK}+0.3$	μs
		$f_{CLK}=2.0MHz$	13.5					μs
t_A	Acquisition Time [14]	$R_S=50\Omega$			$7/f_{CLK}+0.3$		$7/f_{CLK}+0.3$	μs
		$f_{CLK}=2.0MHz$	3.5					μs
t_Z	Auto-Zero Time				$26/f_{CLK}$		$26/f_{CLK}$	μs
		$f_{CLK}=2.0MHz$	13					μs
t_{CAL}	Calibration Time		$1396/f_{CLK}$					μs
		$f_{CLK}=2.0MHz$	698		706		706	μs
t_{PWCAL}	Calibration Pulse Width	Note 15	60	200		200		ns
t_{PWWR}	$\overline{WR}$ Pulse Width		60	200		200		ns
t_{PDINT}	$\overline{RD}$ or $\overline{WR}$ to Reset of $\overline{INT}$		100		175		175	ns
t_{ENA}	Output Enable Time	$C_L=100pF$	50		85		85	ns
t_{DIS}	Data Disable Time	$C_L=100pF$, $R_L=1k\Omega$	30		90		90	ns

System performance characteristics within specified operating conditions [1,2,6,7,8,9,16]

Parameter		Test Conditions	Temperature Range					Units
			Typ	Industrial Min	Industrial Max	Extended Min	Extended Max	
E_{LIP}	Positive Integral Linearity Error	After Auto-Cal [10,11]	±0.5					LSB
E_{LIN}	Negative Integral Linearity Error	After Auto-Cal [10,11]	±0.5					LSB
E_{LD}	Differential Linearity Error	After Auto-Cal [10,11]	12					Bits
E_{FSP}	Positive Full-Scale Error	After Auto-Cal [11]	±0.5		±1.0		±1.0	LSB
E_{FSN}	Negative Full-Scale Error	After Auto-Cal [11]	±1.0		±2.0		±2.0	LSB
E_Z	Zero Error [11,12]	After Auto-Cal or Auto-Zero			±1.0		±1.0	LSB
PSS_Z	Power Supply Sensitivity, Zero Error [13]	$AV_{CC}=DV_{CC}=+5.0\pm5\%$ $V_{--}=-5.0\pm5\%$, $V_{REF}=+4.75V$	±0.125					LSB
PSS_F	Power Supply Sensitivity, Full-Scale Error	$AV_{CC}=DV_{CC}=+5.0\pm5\%$ $V_{--}=-5.0\pm5\%$, $V_{REF}=+4.75V$	±0.125					LSB
PSS_L	Power Supply Sensitivity, Linearity Error	$AV_{CC}=DV_{CC}=+5.0\pm5\%$ $V_{--}=-5.0\pm5\%$, $V_{REF}=+4.75V$	±0.125					LSB

Dynamic performance characteristics within specified operating conditions [1,2,6,7,8,9,16,17]

Parameter		Test Conditions	Temperature Range					Units
			Typ	Industrial Min	Industrial Max	Extended Min	Extended Max	
SNR_B	Signal-to-Noise Ratio, Bipolar Input	f_{IN} = 1kHz, V_{IN} = ±4.85Vp-p	78					dB
		f_{IN} = 10kHz, V_{IN} = ±4.85Vp-p	78					dB
		f_{IN} = 20kHz, V_{IN} = ±4.85Vp-p	78	76.5		76.5		dB
SNR_U	Signal-to-Noise Ratio, Unipolar Input	f_{IN} = 1kHz, V_{IN} = 4.85Vp-p	73					dB
		f_{IN} = 10kHz, V_{IN} = 4.85Vp-p	73					dB
		f_{IN} = 20kHz, V_{IN} = 4.85Vp-p	73	71.5		71.5		dB
$SFDR_B$	Spurious Free Dynamic Range, Bipolar Input	f_{IN} = 1kHz, V_{IN} = ±4.85Vp-p	−88					dB
		f_{IN} = 10kHz, V_{IN} = ±4.85Vp-p	−84					dB
		f_{IN} = 20kHz, V_{IN} = ±4.85Vp-p	−80					dB
$SFDR_U$	Spurious Free Dynamic Range, Unipolar Input	f_{IN} = 1kHz, V_{IN} = 4.85Vp-p	−90					dB
		f_{IN} = 10kHz, V_{IN} = 4.85Vp-p	−86					dB
		f_{IN} = 20kHz, V_{IN} = 4.85Vp-p	−82					dB
THD_B	Total Harmonic Distortion, Bipolar Input	f_{IN} = 1kHz, V_{IN} = ±4.85Vp-p	−82					dB
		f_{IN} = 19.688kHz, V_{IN} = ±4.85Vp-p	−80		−75		−75	dB
THD_U	Total Harmonic Distortion, Unipolar Input	f_{IN} = 1kHz, V_{IN} = ±4.85Vp-p	−82					dB
		f_{IN} = 19.688kHz, V_{IN} = ±4.85Vp-p	−80		−75		−75	dB
IMD_B	Two-Tone Intermodulation Distortion, Bipolar Input	V_{IN} = ±4.85Vp-p, f_{IN1} = 19.375kHz, f_{IN2} = 20.625kHz	−78		−74		−74	dB
IMD_U	Two-Tone Intermodulation Distortion, Unipolar Input	V_{IN} = 4.85Vp-p, f_{IN1} = 19.375kHz, f_{IN2} = 20.625kHz	−78		−73		−73	dB
EFB_B	Effective Bits, Bipolar Input	f_{IN} = 1kHz, V_{IN} = ±4.85Vp-p	12.6					Bits
		f_{IN} = 20kHz, V_{IN} = ±4.85Vp-p	12.6	12.4		12.4		Bits
EFB_U	Effective Bits, Unipolar Input	f_{IN} = 1kHz, V_{IN} = 4.85Vp-p	11.8					Bits
		f_{IN} = 20kHz, V_{IN} = 4.85Vp-p	11.8	11.6		11.6		Bits
BW_B	Bandwidth, Bipolar Input	V_{IN} = ±4.85Vp-p	25	20		20		kHz
BW_U	Bandwidth, Unipolar Input	V_{IN} = 4.85Vp-p	30	20		20		kHz
t_{AP}	Aperture Time		100					ns
t_{APJ}	Aperture Jitter		100					ps_{rms}

Notes for Specification Tables

1. Absolute Maximum Ratings are limits beyond which the device may be damaged. Operating Conditions are limits under which the device is guaranteed to be functional, but those limits do not guarantee specific performance. Guaranteed specifications and test conditions are shown in the *Electrical, Switching and System Performance Characteristics Tables*. The guaranteed specifications apply only for the test conditions listed in the *Electrical, Switching and System Performance Characteristics Tables*. Some performance characteristics may degrade when the device is operated outside the listed test conditions.

2. All voltages are measured with respect to A_{GND} and D_{GND}, unless otherwise specified.

3. When the voltage at any pin exceeds the power supply voltages ($< V-$ or $> AV_{CC}$ or $> DV_{CC}$), the current at that pin must be limited to 5mA. The 20mA maximum package input current rating allows the voltage any any four pins, with a current limit of 5mA, to simultaneously exceed the power supply voltages.

Notes for Specification Tables (cont.)

4. The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum allowable junction temperature), θ_{JA} (junction-to-ambient thermal resistance of the package). and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is given by:

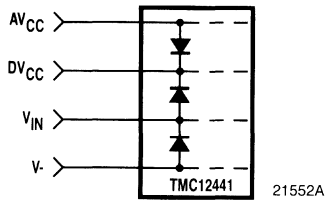
$$P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$$

or the number given in the ***Absolute Maximum Ratings Table***, whichever is lower. For the TMC12441, T_{Jmax} is 125°C and the typical thermal resistance (θ_{JA}) of the TMC12441 with B6F, B6B1, and B6B suffixes when board mounted is 47°C/W.

5. Human body model, 100pF discharged through a 1.5kΩ resistor.

6. Two on-chip diodes are tied to the analog input as shown in the following figure, ***Parasitic Diode Structure***. A/D conversion errors can occur if these diodes are forward-biased more than 50mV.

Parasitic Diode Structure



7. To guarantee accuracy, it is required that AV_{CC} and DV_{CC} be connected to the same power source but with separate decoupling capacitors at each pin.

8. Accuracy is guaranteed with f_{CKL} equal to 2.0MHz. Accuracy may degrade at higher clock frequencies.

9. Typical specifications are at $T_J = 25°C$ and represent the most likely parametric norm (statistical "mode").

10. Positive linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative linearity error the straight line passes through negative full-scale and zero. (See ***Simplified Error Characteristic Curves***.)

11. The TMC12441's self-calibration technique ensures linearity, full-scale and offset errors as specified. Noise inherent to the self-calibration process will result in a repeatability uncertainty of ±0.20 LSB.

12. When T_A changes, an Auto-Zero or Auto-Cal cycle will be required for specified performance. (See ***Typical Performance Curves***.)

13. After Auto-Zero or Auto-Cal cycle execution at the specified power supply extremes.

14. If the CLK_{IN} is asynchronous with respect to the falling edge of WR an uncertainty of one clock period exists in the t_A interval. Therefore, the minimum t_A is six clock periods and the maximum t_A is 7 clock periods. If the falling edge of CLK_{IN} is synchronous with respect to the rising edge of WR then t_A will be exactly 6.5 clock periods.

15. The CAL input must go HIGH before an A/D conversion is started.

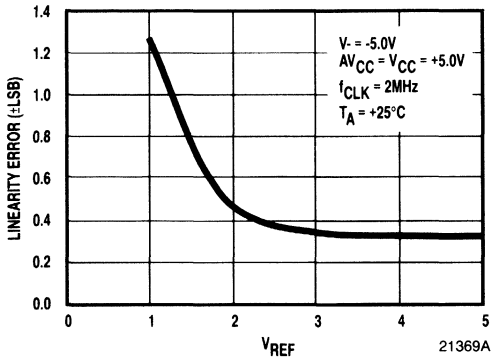
16. Guaranteed specifications apply for $AV_{CC} = DV_{CC} = +5.0V$, $V- = -5.0V$, $V_{REF} = \sim 5.0V$ and $f_{CLK} = 2.0MHz$ unless otherwise specified.

17. Specifications guaranteed after Auto-Cal cycle is completed.

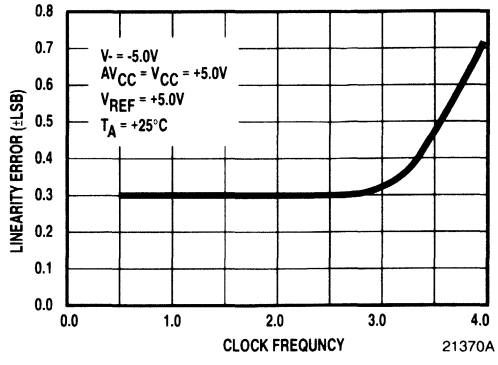
18. Rise and fall times for digital inputs = 20ns, unless otherwise specified.

Typical Performance Curves

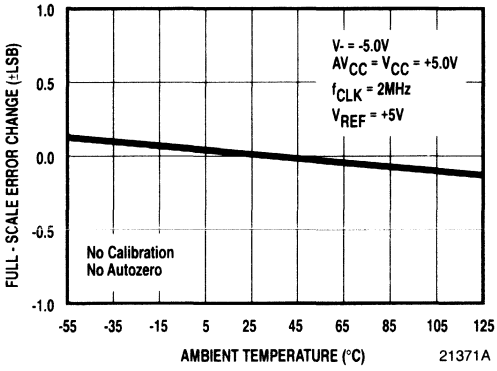
A. Linearity Error vs. V_{REF}



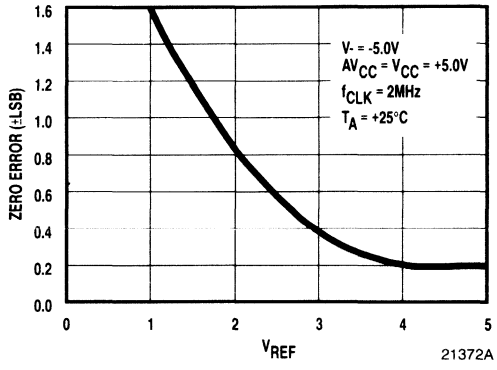
B. Linearity Error vs. Clock Frequency



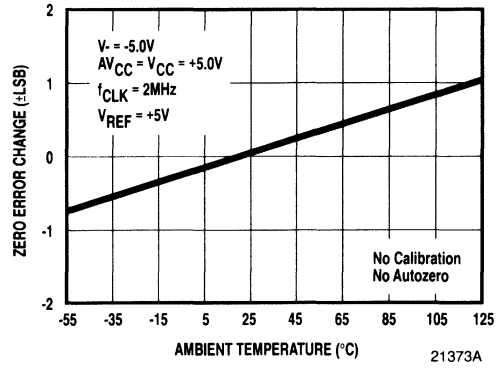
C. Full-Scale Error Change vs. Ambient Temperature



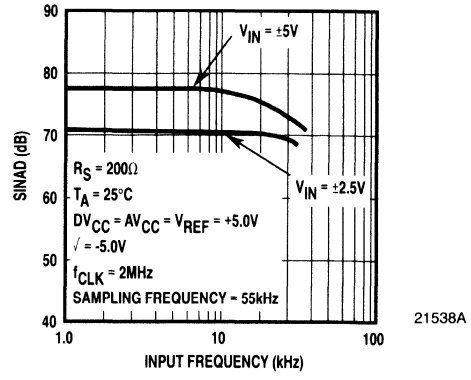
D. Zero Error vs. V_{REF}



E. Zero Error Change vs. Ambient Temperature

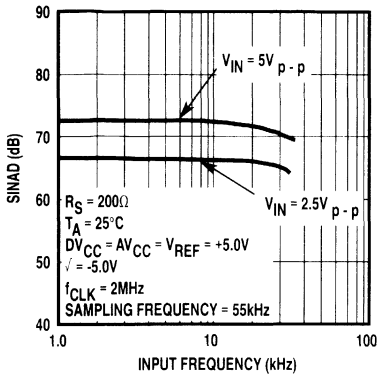


F. Bipolar SINAD vs. Input Frequency



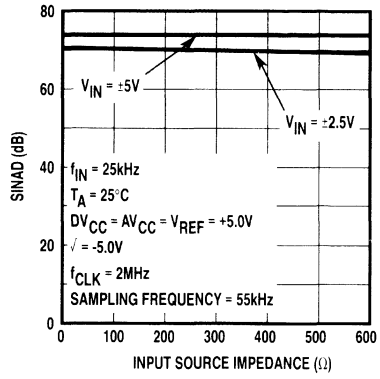
Typical Performance Curves (cont.)

G. Unipolar SINAD vs. Input Frequency



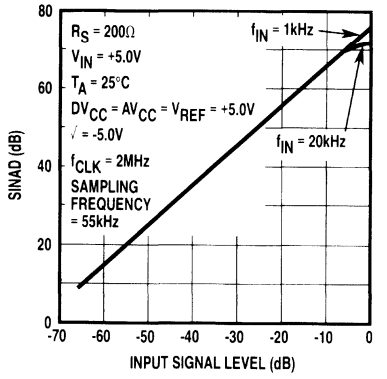
21539A

H. Bipolar SINAD vs. Input Source Impedance



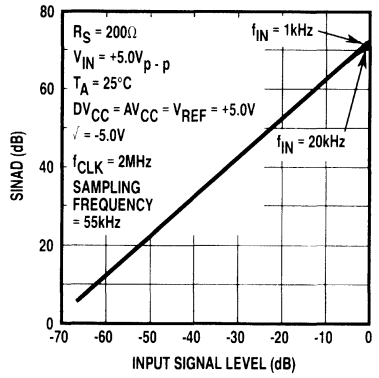
21540A

I. Bipolar SINAD vs. Input Signal Level



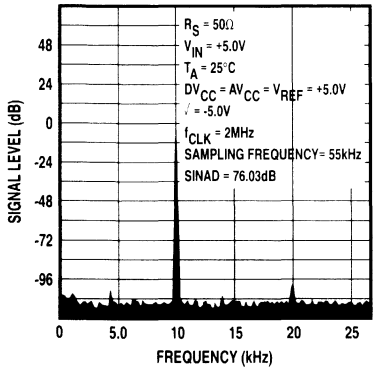
21541A

J. Unipolar SINAD vs. Input Signal Level



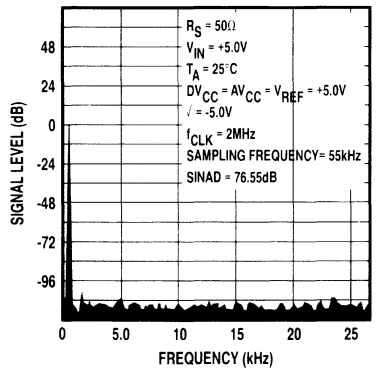
21542A

K. Bipolar Spectral Response with 10kHz Sine Wave Input



21543A

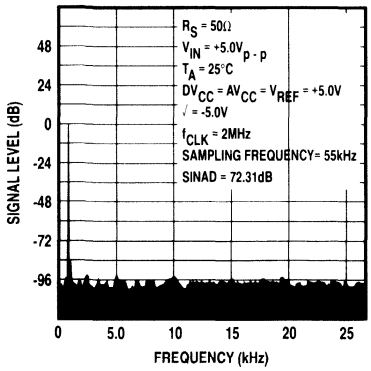
L. Bipolar Spectral Response with 1kHz Sine Wave Input



21544A

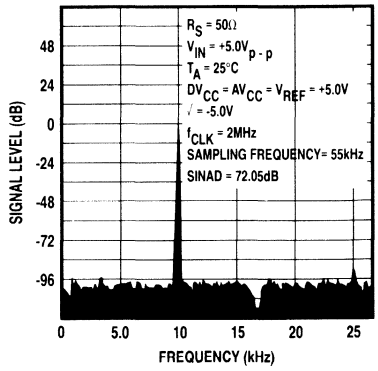
Typical Performance Curves (cont.)

M. Unipolar Spectral Response with 1kHz Sine Wave Input



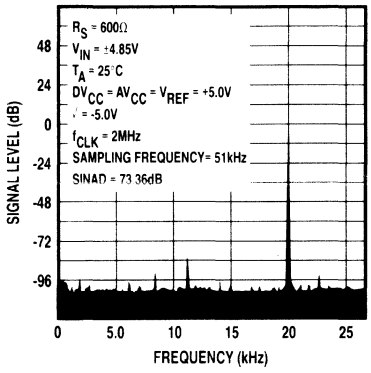
21545A

N. Unipolar Spectral Response with 10kHz Sine Wave Input



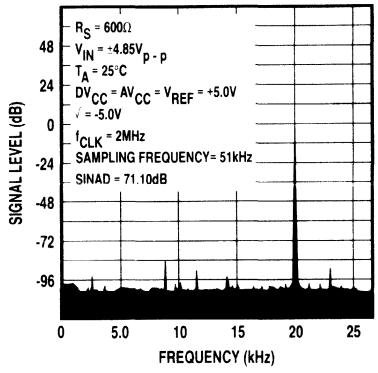
21546A

O. Bipolar Spectral Response with 20kHz Sine Wave Input



21547A

P. Unipolar Spectral Response with 20kHz Sine Wave Input

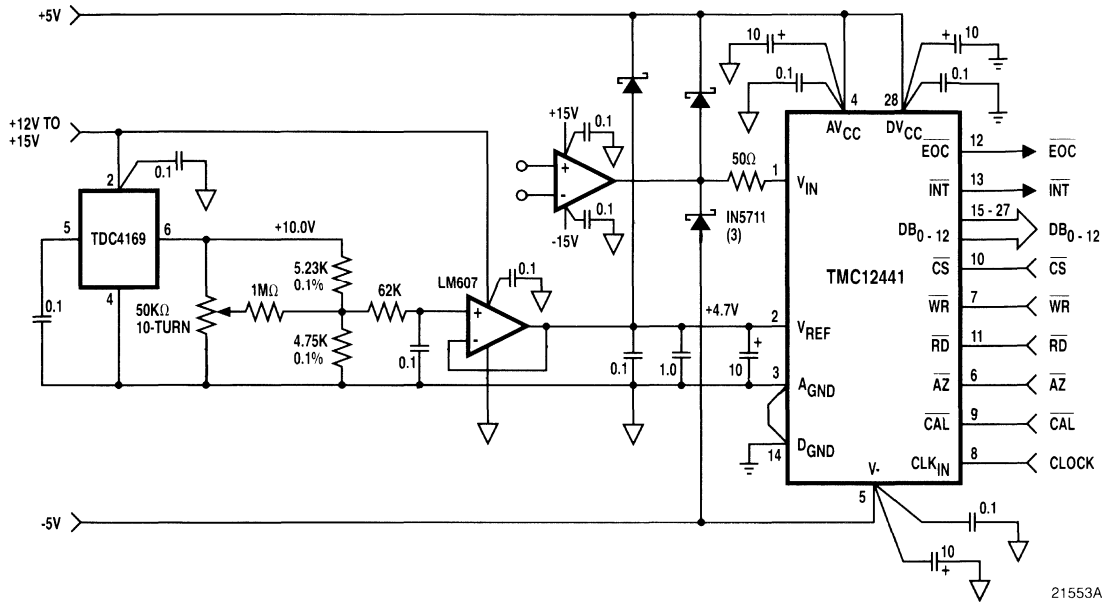


21548A

The Typical Interface Circuit

Noise on AV_{CC}, DV_{CC} or V– power supply inputs can cause A/D conversion errors should the TMC12441 comparator be influenced by that noise. The TMC12441 is especially sensitive during the Auto-Zero or Auto-Cal cycles to power supply noise. Low inductance 10μF tantalum capacitors in parallel with 0.1μF ceramic capacitors are recommended for power supply decoupling. Separate decoupling capacitors should be placed close to the DV_{CC}, AV_{CC} and V– pins.

Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC12441B6F	EXT–T_A = –55°C to 125°C	Commercial	28 Pin CERDIP	12441B6F
TMC12441B6B	STD–T_A = –40°C to 85°C	Commercial	28 Pin CERDIP	12441B6B
TMC1241E1C	STD–T_A = 0°C to 70°C	– –	Eurocard Format Board with A/D Converter	1241E1C

TMC12451

Self-Calibrating 12-Bit Plus Sign, 7.7 μs, μP-Compatible Sampling A/D Converter Tested and Specified for DSP Applications

TRW's TMC12451 is a CMOS successive-approximation analog-to-digital converter with 13-bit resolution. Physically identical to the TMC1251, the TMC12451 is dynamically tested and guaranteed to meet Signal-to-Noise Ratio, Total Harmonic Distortion, Two-tone Intermodulation Distortion, Effective Bits, and Bandwidth specifications.

The outstanding performance of the TMC12451 is the result of self-calibration, which reduces linearity and full-scale errors while optimizing dynamic performance. The TMC12451 performs an Auto-Zero function that minimizes offset error. The Auto-Zero function can be performed as needed or prior to every A/D conversion.

The TMC12451 includes a track/hold input stage for sampling the analog input signal. Both unipolar and bipolar analog input voltage ranges (0 to +5 and ±5 Volts) are accommodated. The TMC12451 requires only two power supplies, ±5 Volts. Its two's-complement output data format uses the 13th bit to indicate the polarity of the input signal. The 13-bit conversion result from the TMC12451 is read from its 8 outputs in two successive bytes. Digital inputs and outputs are compatible with TTL or CMOS logic levels and have microprocessor interface features.

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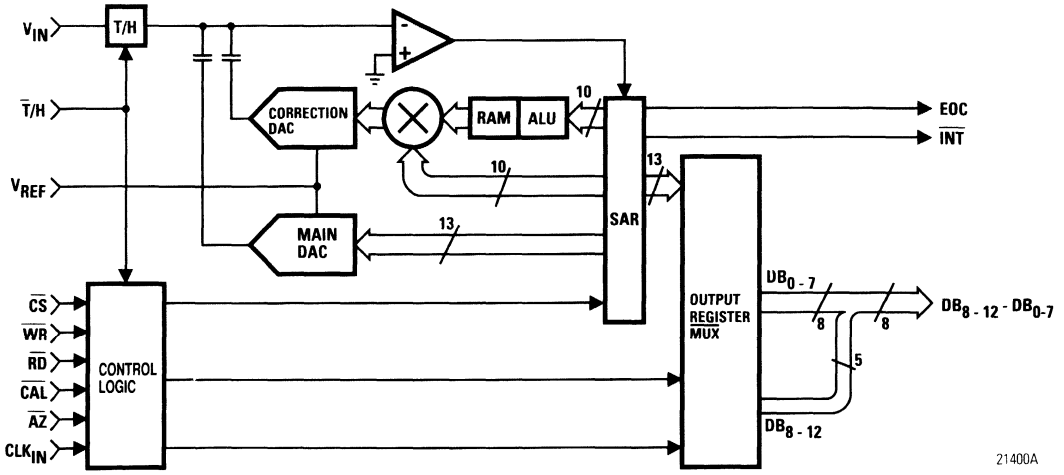
Features

- Guaranteed SNR, THD, IMD, EFB, and Bandwidth
- 13-Bit Resolution, 12 Bits Plus Sign
- Internal Track/Hold
- Conversion Time 7.7μs, Maximum
- Auto-Calibration And Auto-Zero Cycles
- Linearity Error Less Than ±1/2 LSB
- Offset Error Less Than ±1 LSB
- Full-Scale Error Less Than ±1.5 LSB
- Power Consumption 113 mW, Maximum
- Eight-Bit Microprocessor Interface
- TTL/CMOS Compatible
- Standard 24-lead DIP Package

Functional Block Diagram



TRW LSI Products Inc.
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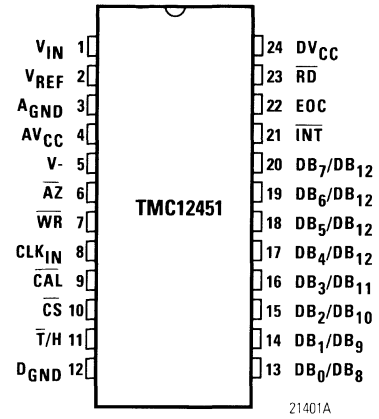
40G06716 Rev. A – 8/90
Printed in the U.S.A.

Pin Assignments



24-pin DIP package

Applications

- Ultrasound Systems
- Vibration Analysis
- Audio/Speech Processing
- Sonar
- Motion Control
- Digital Signal Processing

Functional Description

General Information

The TMC12451 is a successive approximation A/D converter with 13-bit resolution (12-bit plus sign). The TMC12451 can perform Auto-Cal and Auto-Zero routines to minimize full-scale, linearity and offset errors while optimizing dynamic performance. It comprises a D/A converter, precision comparator and a successive-approximation register (SAR) along with digital and analog circuitry for self-calibration. The TMC12451 is identical with TRW's TMC1251 except that it is fully tested and specified under dynamic conditions. Signal-to-Noise Ratio, Total Harmonic Distortion, Two-tone Intermodulation Distortion, Effective Bits and Bandwidth are tested and guaranteed under both bipolar and unipolar signal conditions.

The Auto-Zero cycle is an internal calibration sequence that corrects for A/D offset error caused by the input offset voltage of the comparator. The Auto-Cal cycle is a calibration sequence that not only corrects offset error but also corrects for full-scale and linearity errors caused by D/A converter gain and linearity errors. The Auto-Cal feature eliminates the need for trimming or other adjustment methods in the manufacture of the TMC1251. The Auto-Cal cycle restores the accuracy of the TMC1251 whenever it is requested. This ensures excellent long-term and temperature stability.

The internal track/hold input stage can be controlled by the TMC1251 inherent conversion sequencing circuitry or externally by the use of the $\overline{T}/H$ control input. This control allows the timing and duration of the analog signal acquisition period just prior to initiating an A/D conversion cycle. The 13-bit result is made available in two successive bytes from the eight-bit wide output port.

Power and Ground

The digital and analog power supply voltage range of the TMC1251 is + 4.5V to + 5.5V. To guarantee accuracy, it is required that the AV_{CC}, pin 4, and DV_{CC}, pin 24, be connected to the same power source, but with separate decoupling capacitors (10µF tantalum and a 0.1µF ceramic) between AV_{CC} and DV_{CC} and ground. V-, pin 5, has a range of –4.5V to –5.5V and and should have 10µF tantalum and 0.1µF ceramic capacitors for power supply decoupling.

Although A_{GND} and D_{GND}, pins 3 and 24 respectively, are distinguished from each other on the TMC1251, they should be connected together on the system printed circuit board to eliminate differential ground noise voltages which may degrade performance. A_{GND} and D_{GND} should be connected together as close to the TMC1251 as possible.

Analog Inputs

The voltage applied to the V_{REF} input, pin 2, defines the input voltage range of the V_{IN} input, pin 1, over which 4095 positive output codes and 4096 negative output codes are found. The A/D converter can be used in either ratiometric or absolute applications. The voltage source driving V_{REF} must have a low output impedance and low noise. The circuit in the *Typical Interface Circuit* is a good example of a very stable reference source for the TMC1251.

In a ratiometric application, the analog input voltage is proportional to the voltage used for the V_{REF}. If V_{IN} is related or proportional to AV_{CC}, V_{REF} can be connected directly to AV_{CC}. Here, V_{IN} and V_{REF} are related and track each other as the power supply voltage changes, making the output code of the TMC1251 independent of power supply voltage variations.

For absolute accuracy, where the V_{IN} varies independently of power supply voltage, V_{REF} should be driven from a

time- and temperature-stable voltage source like that shown in the *Typical Interface Circuit*. The magnitude of V_{REF} may require an adjustment to achieve system gain requirements.

Due to the architecture of the TMC1251, a variable current will flow into or out of (depending on V_{IN} polarity) the V_{IN} pin at the start of the analog input sampling period, t_A. The peak value of this current is proportional to the magnitude of the applied V_{IN}. A small capacitor from V_{IN} to A_{GND} can be used to reduce noise and clock feedthrough due to inductive coupling from long input leads and will not degrade the accuracy of the conversion. It is advisable, however, to keep V_{IN} and V_{REF} input lines as short as possible.

The analog input can be modeled as shown in the *Analog Input Equivalent Circuit*. Large source resistance, R_S, will lengthen the time necessary for the voltage on C_{REF} to settle to within 1/2 LSB of the voltage on V_{IN}. With f_{CLK} of 2MHz, t_A takes seven clock periods, or 3.5µs. When R_S is less than or equal to 1kΩ, a 5.0 Volt V_{IN} will have adequate time to settle.

Auto-Cal and Auto-Zero Cycles

When power is initially applied to the TMC1251, an Auto-Cal cycle is executed which cannot be interrupted. Since the power supply, reference, and clock are not usually stable at initial power-up, this first Auto-Cal cycle will not result in an accurate calibration of the TMC1251. An additional calibration cycle should be started after the power supplies, reference, and clock have been given adequate time to stabilize.

When $\overline{CAL}$, pin 9, is LOW, the TMC1251 is reset and an Auto-Cal cycle is initiated. During the Auto-Cal cycle, correction values are determined for the offset voltage of the comparator as well as linearity and gain errors. These values are stored in the internal RAM and used during A/D conversion cycles to reduce the TMC1251's gain, offset, and linearity errors to the specified limits. It is only necessary to go through the Auto-Cal cycle once after initial power is applied.

To correct for any change in the offset error of the A/D converter, the Auto-Zero cycle can be used. It may be necessary to execute an Auto-Zero cycle whenever the ambient temperature changes significantly (See the curve titled *"Zero Error Change vs Ambient Temperature"* in the *Typical Performance Characteristics*). A change in the ambient temperature will cause the offset voltage of the comparator to change, which may cause the offset error of the A/D converter to be greater than its specified limit. Since Auto-Zero cannot be activated when $\overline{T}/H$ is used to start the A/D conversion cycle, it may be necessary to do an Auto-Cal cycle (which includes Auto-Zero) periodically.

With the $\overline{AZ}$ input, pin 6, held LOW during a conversion cycle, the TMC1251 will execute an Auto-Zero cycle before the actual A/D conversion cycle is started. The total conversion time (t_C) is increased by 26 clock periods when Auto-Zero is used. An Auto-Zero cycle will reduce the offset error of the TMC1251 to less than ±1 LSB.

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Microprocessor Interface Controls

On initial power-up, an Auto-Cal cycle is executed by bringing $\overline{CAL}$ LOW while $\overline{CS}$ and $\overline{T}/H$ are HIGH. To acknowledge that the Auto-Cal cycle is in progress, EOC goes LOW after the falling edge of $\overline{CAL}$ and remains LOW during the Auto-Cal cycle duration of 1,399 clock periods. During the Auto-Cal cycle, first the comparator offset error is determined and then the D/A converter gain and linearity errors are found. Correction factors for these errors are stored in the internal RAM.

An A/D conversion cycle is initiated by bringing $\overline{CS}$ and $\overline{WR}$ LOW. The $\overline{AZ}$ input should be tied HIGH or LOW during the conversion process. If $\overline{AZ}$ is LOW when A/D conversion is executed, an Auto-Zero cycle (duration equals 26 clock periods) occurs before the A/D conversion is started. $\overline{AZ}$ must be LOW during the entire A/D conversion. After Auto-Zero is complete, the analog signal acquisition time period begins and continues for 7 clock periods. If $\overline{AZ}$ is HIGH, no Auto-Zero cycle is executed. At the end of the acquisition period EOC goes LOW, indicating that V_{IN} is being held and that the successive approximation conversion sequence has started.

$\overline{CS}$ and $\overline{T}/H$ may be used to initiate a conversion cycle. Bringing both of these signals LOW begins the acquisition period; the rising edge of $\overline{T}/H$ puts the track/hold into the hold mode and begins the successive approximation conversion. DSP applications require that the time that the analog input signal is sampled (the end of the acquisition period) be well controlled. Using $\overline{T}/H$ in this way ensures control over the sampling of the analog input signal.

During an A/D conversion cycle, the held V_{IN} is successively compared to the output of the corrected D/A converter (main and correction D/A converters). First, the held voltage is compared to analog ground to determine its

Microprocessor Interface Controls (cont.)

polarity (sign bit). The sign bit is set LOW for positive V_{IN} and HIGH for negative V_{IN}. Next, the MSB of the D/A converter is set HIGH with all other bits LOW. If the the held voltage is greater than the output of the D/A converter, then the MSB is left HIGH; otherwise it is set LOW. The next bit is then set HIGH, making the output ofthe D/A converter 3/4 or 1/4 of full scale, depending on the outcome of the previous bit. If the held voltage is greater than the new D/A converter value then the bit remains HIGH. If the held voltage is less than the new D/A converter value the bit is set LOW. This process continues until each bit has been tested. The result is then transferred to the output register of the TMC1251. EOC goes HIGH and $\overline{INT}$ goes LOW indicating the end of the conversion. The result can now be read when $\overline{CS}$ is LOW by bringing $\overline{RD}$ LOW twice in succession to enable first, the MSBs (DB_8 thru DB_{12}) and second, the LSBs (DB_0 thru DB_7) of the result through the TMC1251's eight-bit wide output port.

The *A/D Control Input Functions (Table 1)* summarizes the effect of the digital control inputs on the TMC1251. Test Mode (where $\overline{RD}$ is HIGH and $\overline{CS}$ and $\overline{CAL}$ are LOW) is used in the manufacturing process of the TMC1251. Care should be taken to avoid this mode. In Test Mode DB_2, DB_3, DB_5, and DB_6 become active outputs, which may cause data bus contention.

The TMC1251 can be completely reset, aborting all sequences that may be in progress. The A/D converter is reset where a new conversion is started by taking $\overline{CS}$ and $\overline{WR}$ or $\overline{CS}$ and $\overline{T}$/H LOW. If this occurs when V_{IN} is being tracked or when EOC is LOW, the Auto-Cal correction factors in RAM may be corrupted. After reset, it is then necessary to execute an Auto-Cal cycle before the next A/D conversion cycle. The Auto-Cal cycle cannot be reset once started.

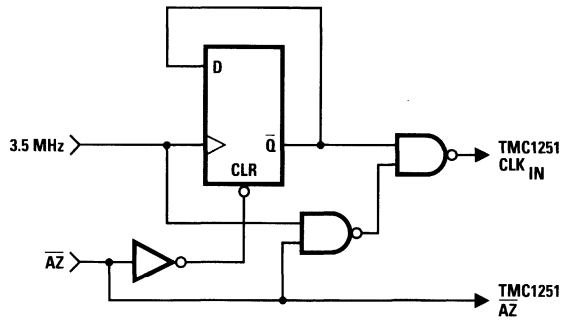
When using $\overline{WR}$ or $\overline{T}$/H without $\overline{AZ}$ to start a conversion, a new conversion may be restarted only after EOC has gone HIGH after the end of the current conversion. When using $\overline{WR}$ and $\overline{AZ}$, a new conversion may be restarted during the first 26 clock cycles after the rising edge of $\overline{WR}$ or after EOC has gone HIGH without corrupting the Auto-Cal correction factors.

Acquisition Time

Each of the three methods of initiating a conversion affects the analog signal acquisition period. $\overline{WR}$ or $\overline{T}$/H can start a conversion when $\overline{AZ}$ is HIGH. In either of these cases, the rising edge of EOC indicates that the track/hold is in its track mode and the analog input signal is being acquired. It is advisable, however, to consider the beginning of the actual acquisition time to be AFTER the second $\overline{RD}$ pulse of the previous conversion cycle. In this way, the noise that normally accompanies the reading of data from the TMC1251's outputs will not affect the signal being acquired and therefore, the results of the following conversion.

When $\overline{WR}$ is used to start a conversion with $\overline{AZ}$ LOW, an Auto-Zero cycle is inserted prior to the acquisition period. Here, the acquisition timing and duration are controlled by the TMC1251. Since the acquisition time must always be at least 3.5µs, the maximum CLK_{IN} frequency in this mode is limited to 2.0MHz (7 cycles at 500ns). A simple circuit is shown which is useful when $\overline{WR}$ initiates conversions with and without Auto-Zero. In this circuit, when $\overline{AZ}$ is HIGH, the TMC1251 CLK_{IN} frequency is 3.5MHz. When $\overline{AZ}$ is LOW, the TMC1251 CLK_{IN} frequency is divided by two and is 1.75MHz.

Figure 1. CLK_{IN} Frequency Control Circuit



Dynamic Performance

For Digital Signal Processing Applications, it is not sufficient to evaluate and qualify an A/D converter only on the basis of its integral or differential linearity characteristics. In DSP applications, the A/D converter is usually digitizing dynamic signals (as opposed to static) and new concerns about noise, distortion, and frequency response become important.

The TMC12451 is intended for use in DSP applications and carries with it specifications that are not normally associated with similar A/D converters intended for application in process control, industrial control, data acquisition, and instrumentation.

Signal-to-Noise Ratio, Total Harmonic Distortion, and Two-tone Intermodulation Distortion are tested and guaranteed parameters of the TMC12451. These parameters are tested by having the A/D converter digitize a sinewave at a specified frequency and amplitude. Data is transferred from the A/D converter to a computer where Fast Fourier Transform (FFT) analysis converts the time- domain data into the frequency domain where SNR, THD and IMD are extracted. The Effective Bits parameter of the TMC12451 is calculated from Signal-to-Noise Ratio by:

$$EFB = (SNR - 1.8) / 6.02$$

The performance of the internal track/hold of the TMC12451 is shown by aperture time and aperture jitter parameters. When $\overline{T}/H$ is used to initiate conversions, aperture time is the delay between the rising edge of $\overline{T}/H$ and the internal time when the analog input signal is actually held. Aperture jitter is the change in this time period from cycle-to-cycle.

Summary of Control Inputs

$\overline{CS}$ The Chip Select control input, pin 10, is active LOW and enables the $\overline{WR}$, $\overline{RD}$, and $\overline{T}/H$ functions.

$\overline{WR}$ The A/D conversion is started on the rising edge of the Write control input, pin 7, when $\overline{CS}$ is LOW. When this control is used to start a conversion the analog signal acquisition period is controlled by the TMC1251.

$\overline{RD}$ The Read control input, pin 23, is active LOW and is used to enable the three-state data outputs and reset $\overline{INT}$ HIGH when $\overline{CS}$ is LOW.

$\overline{T}/H$ The track/hold control input, pin 11, can be used to start a conversion. With $\overline{CS}$ LOW, the falling edge of $\overline{T}/H$ begins the analog signal acquisition period. The rising edge of $\overline{T}/H$ then puts the track/hold into hold mode and starts the A/D conversion.

$\overline{AZ}$ With the $\overline{AZ}$ input, pin 6, held LOW during a conversion cycle, the TMC1251 will execute an Auto-Zero cycle before the actual A/D conversion cycle is started. The total conversion time (t_C) is increased by 26 clock periods when Auto-Zero is used.

$\overline{CAL}$ When $\overline{CAL}$, pin 9, is LOW, the TMC1251 is reset and an Auto-Cal cycle is initiated.

CLK_{IN} The clock input, pin 8, controls all sequence timing and A/D conversion time. The frequency range for CLK_{IN} is from 0.50 to 6MHz.

EOC The End-of-Conversion control output, pin 22, is LOW during A/D conversion, Auto-Cal, and Auto-Zero cycles.

$\overline{INT}$ The interrupt control output, pin 21, goes LOW when a conversion has been completed and indicates that the conversion result is available from the output register. Reading the outputs or starting an A/D conversion, Auto-Cal or Auto-Zero cycle will reset in $\overline{INT}$ going HIGH.

DB_0/DB_{12} The three-state outputs, pins 13 to 20, give 13-bit conversion results with two successive $\overline{RD}$ pulses. The first $\overline{RD}$ pulse outputs the MSBs of the result (DB_8 thru DB_{12}) and the second $\overline{RD}$ pulse outputs the LSBs (DB_0 thru DB_7). The format is two's complement sign bit extended with DB_{12} being the sign bit, DB_{11} the MSB and DB_0 the LSB.

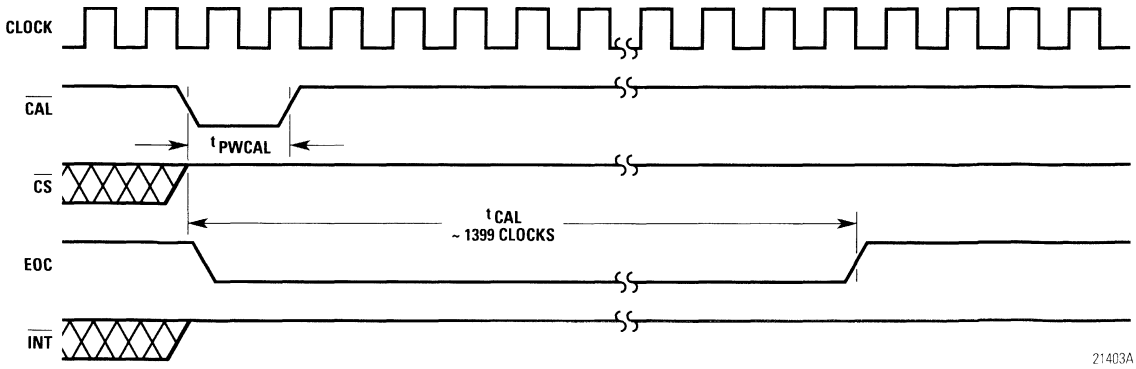
Table 1. A/D Control Input Functions

Control Inputs						A/D Function
$\overline{CS}$	$\overline{WR}$	$\overline{T}/H$	$\overline{RD}$	$\overline{CAL}$	$\overline{AZ}$	
↓	↓	1	1	1	1	Start A/D conversion without Auto-Zero
↓	1	↓	1	1	1	Start A/D conversion without Auto-Zero, synchronous with rising edge of $\overline{T}/H$.
↓	1	1	↓	1	1	Read data without Auto-Zero
↓	↓	1	1	1	0	Start A/D conversion with Auto-Zero
↓	1	1	↓	1	0	Read data with Auto-Zero
1	x	1	x	↓	x	Start Auto-Cal cycle
0	x	1	1	0	x	Test Mode (DB_2, DB_3, DB_5 and DB_6 active)

Package Interconnections

Signal Type	Signal Name	Function	Value	B7 Package Pin
Power	AV_{CC}	Positive Analog Supply	+5.0V	4
	DV_{CC}	Positive Digital Supply	+5.0V	24
	V–	Negative Analog Supply	–5.0V	5
Ground	A_{GND}	Analog Ground	0.0V	3
	D_{GND}	Digital Ground	0.0V	12
Analog Inputs	V_{IN}	Analog Signal Input	±4.7V	1
	V_{REF}	Reference Input	+4.7V	2
Digital Inputs	CLK_{IN}	Clock Input	TTL	8
	$\overline{AZ}$	Auto-Zero	TTL	6
	$\overline{CAL}$	Calibrate	TTL	9
	$\overline{RD}$	Read	TTL	23
	$\overline{WR}$	Write	TTL	7
	$\overline{CS}$	Chip Select	TTL	10
	$\overline{T}$/H	Sample-Hold	TTL	11
Digital Outputs	EOC	End of Calibration	TTL	22
	$\overline{INT}$	Interrupt	TTL	21
	DB7/DB12		TTL	20
	DB6/DB12		TTL	19
	DB5/DB12		TTL	18
	DB4/DB12		TTL	17
	DB3/DB11		TTL	16
	DB2/DB10		TTL	15
	DB1/DB9		TTL	14
	DB0/DB8		TTL	13

Figure 2. Timing Diagram, Auto-Cal Cycle ($\overline{CS}$ = HIGH, $\overline{WR}$ = $\overline{T}$/H = $\overline{RD}$ = $\overline{AZ}$ = don't care)



$\overline{CS}$ = 1
$\overline{WR}$ = X
$\overline{RD}$ = X
$\overline{AZ}$ = X
$\overline{T}$/H = 1
X = DON'T CARE

Figure 3. Timing Diagram, Using $\overline{WR}$ to Start Conversions with Auto-Zero ($\overline{CAL}$ = HIGH, $\overline{AZ}$ = LOW)

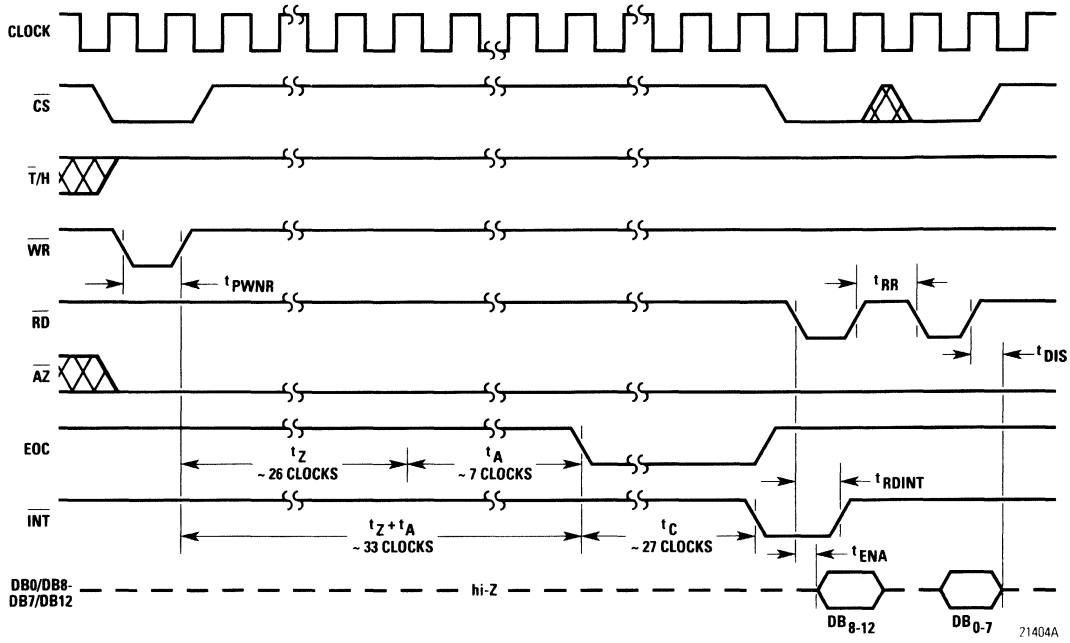


Figure 4. Timing Diagram, Using $\overline{WR}$ to Start Conversions without Auto-Zero ($\overline{CAL}$ = $\overline{AZ}$ = HIGH)

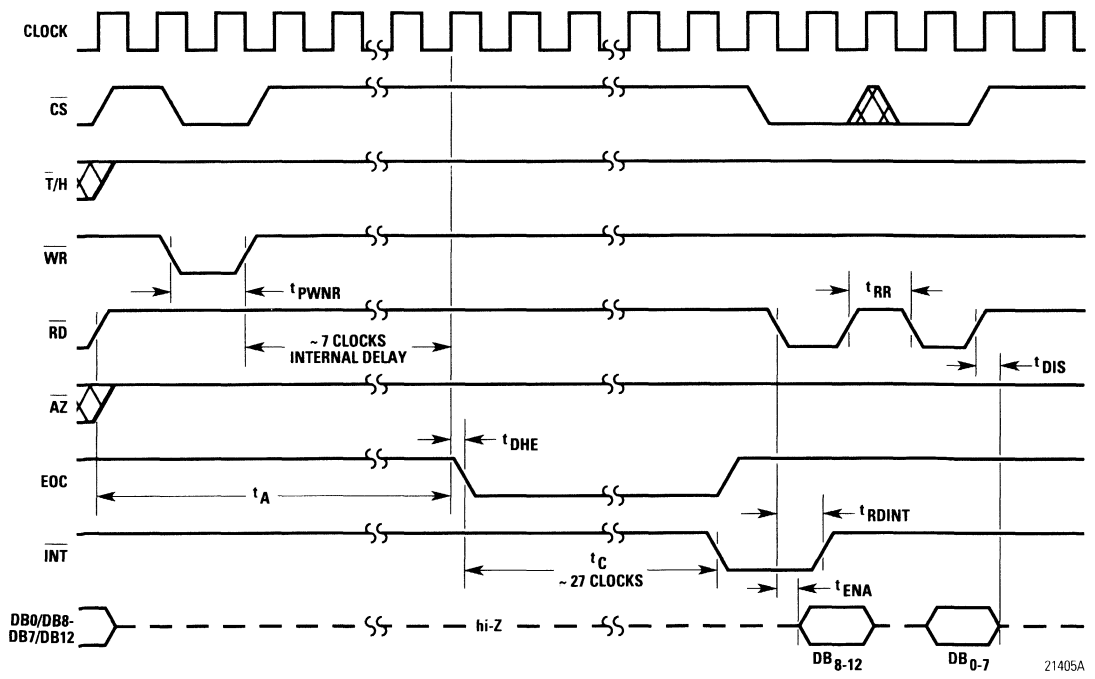


Figure 5. Timing Diagram, Using $\overline{T}$/H to Start Conversions without Auto-Zero ($\overline{CAL}$ = $\overline{AZ}$ = HIGH)

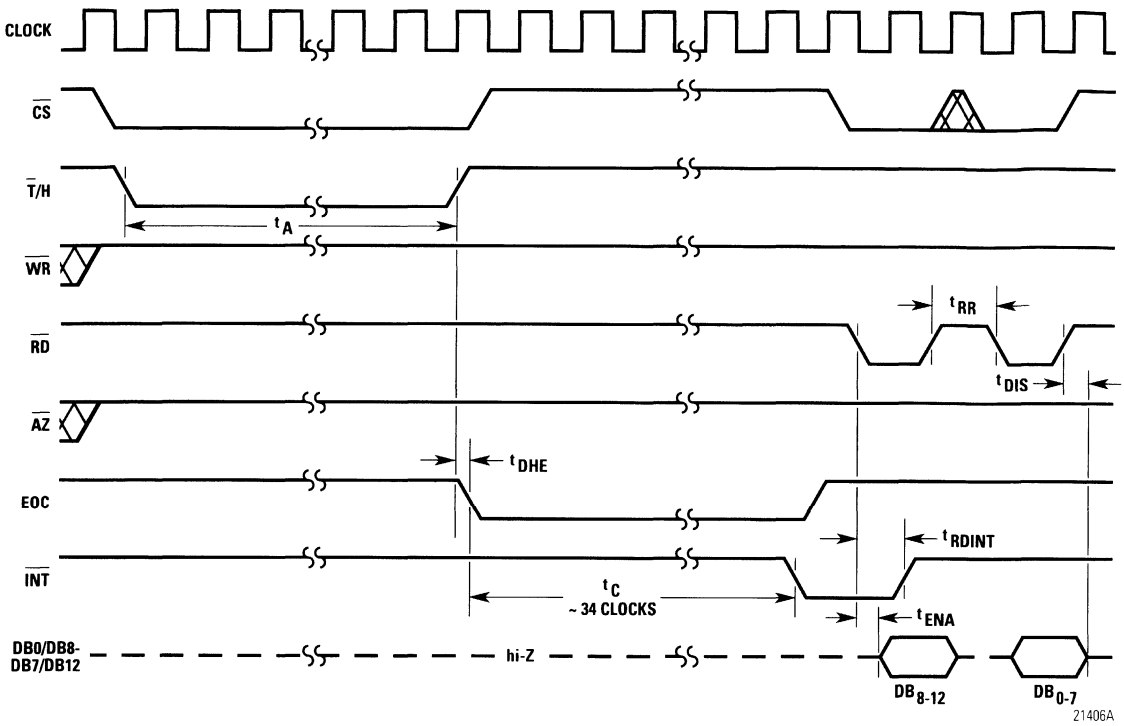


Figure 6. Transfer Characteristics

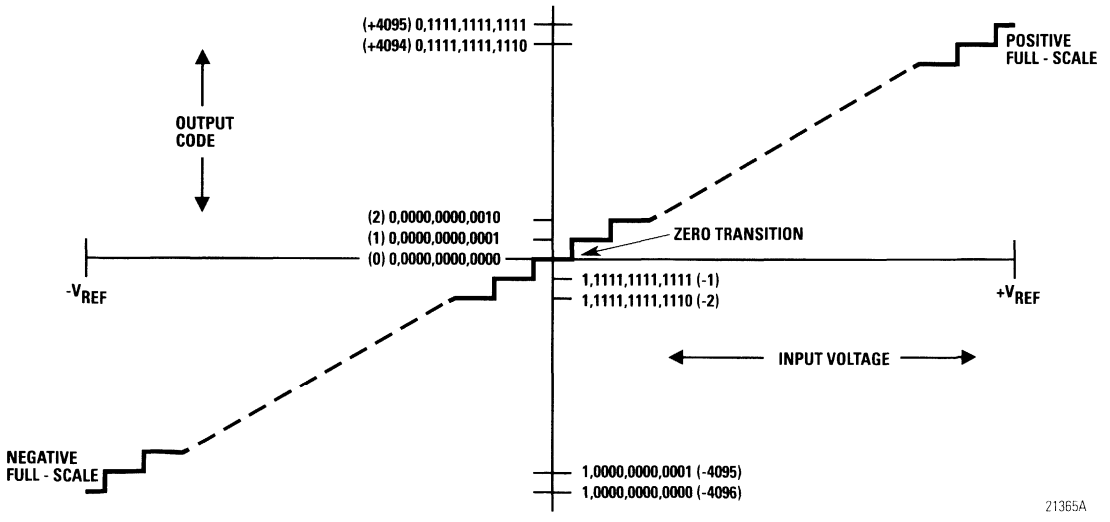


Figure 7. Simplified Error Characteristics vs. output code without Auto-Cal or Auto-Zero cycles

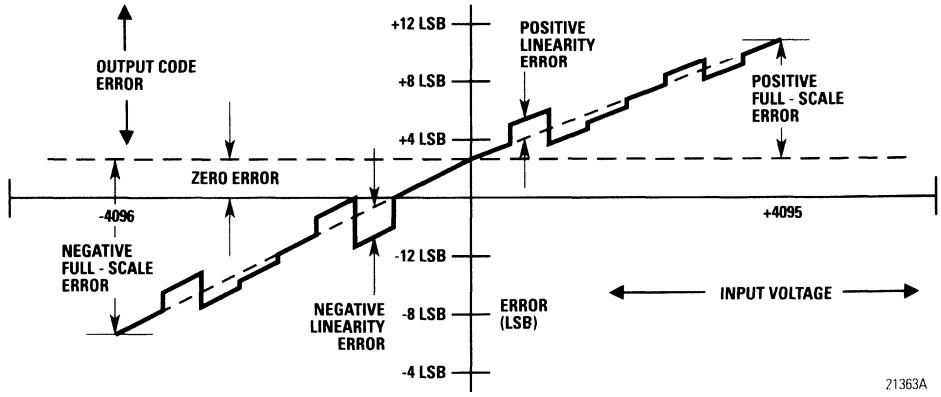


Figure 8. Simplified Error Characteristics vs. output code after Auto-Cal

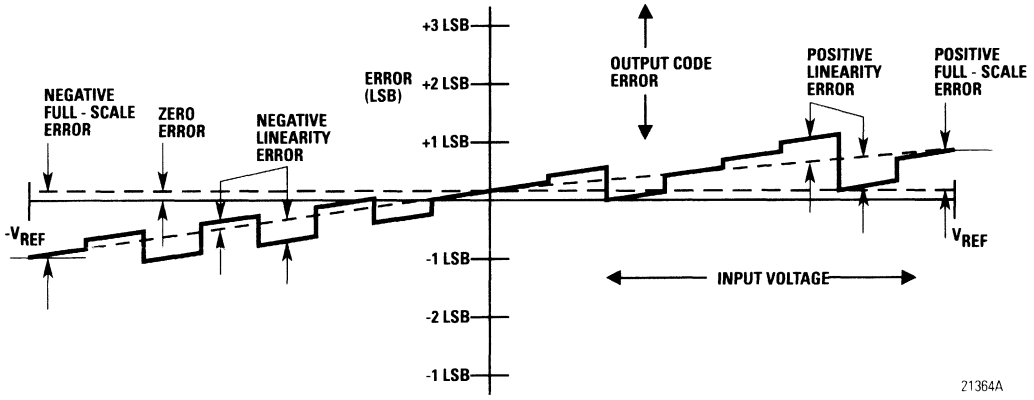


Figure 9. Output Test Loads

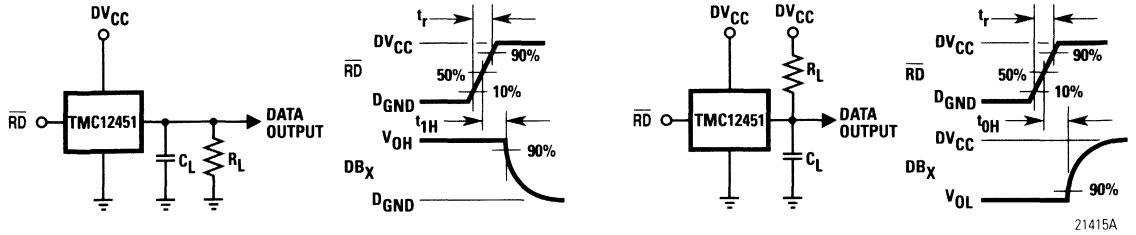
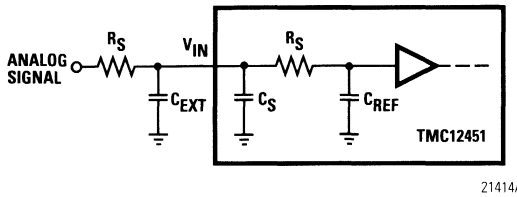


Figure 10. Analog Input Equivalent Circuit



Output Coding

Input Voltage	DB_{12} Sign	DB_{11} ..... DB_0 MSB LSB
>4.096V	0	1111 1111 1111
+4.096V	0	1111 1111 1111
+4.095V	0	1111 1111 1110
+4.094V	0	1111 1111 1101
•		•
•		•
+0.002V	0	0000 0000 0010
+0.001V	0	0000 0000 0001
0.000V	0	0000 0000 0000
-0.001V	1	1111 1111 1111
-0.002V	1	1111 1111 1110
•		•
•		•
-4.094V	1	0000 0000 0010
-4.095V	1	0000 0000 0001
-4.096V	1	0000 0000 0000
<-4.096V	1	0000 0000 0000

Note: The input voltage range used for this table is ±4.096 Volts and the input voltages are measured at code centers.

Absolute maximum ratings (beyond which the device may be damaged)[1,2]

Supply Voltages

DV_{CC}	–0.5 to +6.5V
AV_{CC}	–0.5 to +6.5V
V–	+0.5 to –6.5V
$AV_{CC} - DV_{CC}$[7]	–0.3 to +0.3V
$A_{GND} - D_{GND}$	–0.3 to +0.3V

Input Voltages

Digital Inputs	–0.3 to (DV_{CC} +0.3)V
Analog Inputs	(AV_{CC} + 0.3) to (V– – 0.3)V

Outputs

Digital Outputs, applied voltage	–0.5 to DV_{CC}
Input current, any pin, externally forced [3]	+5mA
Short-circuit duration (single output to GND)	unlimited

Temperature

Operating, case	–60 to +135°C
Lead, soldering (10 seconds)	+300°C
Storage	–65 to +150°C

Package input current [3] ..... +20mA

Package power dissipation at 25°C [4] 875mW

ESD Susceptibility [5] 2000V

Operating Conditions [1,2,9,16,17]

Parameter		Temperature Range: Industrial Min	Industrial Nom	Industrial Max	Extended Min	Extended Nom	Extended Max	Units
AV_{CC}, DV_{CC}	Positive Power Supply Voltages [6,7]	4.5	5.0	5.5	4.5	5.0	5.5	V
V–	Negative Power Supply Voltage	–4.5	-5.0	-5.5	–4.5	–5.0	–5.5	V
AV_{CC}-DV_{CC}	Power Supply Voltage Differential	–0.1	0.0	0.1	–0.1	0.0	0.1	V
A_{GND}-D_{GND}	Ground Voltage Differential	–0.1	0.0	0.1	–0.1	0.0	0.1	V
V_{IN}	Input Voltage Range	V– –.050	±4.096	AV_{CC}+.050	V– – .050	±4.096	AV_{CC}+.050	V
V_{REF}	Reference Voltage [6,7]	3.5	+4.096	AV_{CC}+.050	3.5	+4.096	AV_{CC}+.050	V
f_{CLK}	Clock Frequency	0.5	3.5	6.0	0.5	3.5	6.0	MHz
	Clock Duty Cycle	40	50	60	40	50	60	%
V_{IL}	Input Voltage, Logic LOW, all but CLK_{IN}, DV_{CC} = 4.75V		1.4	0.8		1.4	0.8	V
V_{IH}	Input Voltage, Logic HIGH, all but CLK_{IN}, DV_{CC} = 5.25V	2.0	1.4		2.0	1.4		V
I_{OL}	Output Current, Logic LOW	–6.0	–20		–6.0	–20		mA
I_{OH}	Output Current, Logic HIGH	8.0	20		8.0	20		mA
T_J	Junction Temperature, TMC1251B7B, TMC1251B7B1	–40		+85				°C
T_J	Junction Temperature, TMC1251B7F				–55		±125	°C

Electrical Characteristics [1,2,6,7,8,9,16]

Parameter		Test Conditions	Typ	Temperature Range: Industrial Min	Industrial Max	Extended Min	Extended Max	Units
DI_{CC}	DV_{CC} Supply Current	f_{CLK} = 2.0MHz, $\overline{CS}$ = HIGH	1.0		2.5		2.5	mA
AI_{CC}	AV_{CC} Supply Current	f_{CLK} = 2.0MHz, $\overline{CS}$ = HIGH	4.0		10.0		10.0	mA
I–	V- Supply Current	f_{CLK} = 2.0MHz, $\overline{CS}$ = HIGH	2.8		10.0		10.0	mA
C_{IN}	Analog Input Capacitance		65					pF
C_{REF}	Reference Input Capacitance		80					pF
I_{IL}	Input Current, Logic LOW	V_I = 0.0V	–0.005		–1.0		–1.0	µA
I_{IH}	Input Current, Logic HIGH	V_I = ±5.0V	0.005		1.0		1.0	µA
$V_{T\pm}$	Positive-going threshold, CLK_{IN}		2.8	2.7		2.7		V
V_{T-}	Negative-going threshold, CLK_{IN}		2.1		2.3		2.3	V
V_H	Hysteresis, CLK_{IN}	$V_{T\pm}$ - V_{T-}	0.7	0.4		0.4		V
V_{OL}	Output Voltage, Logic LOW	I_{OUT} = 1.6mA, V_{CC} = 4.75V			0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	I_{OUT} = –360µA, V_{CC} = 4.75V		2.4		2.4		V
		I_{OUT} = –10µA, V_{CC} = 4.75V		4.5		4.5		V
I_{OZL}	Output leakage current, LOW	V_{OUT} = 0.0V	–0.01		–3.0		–3.0	µA
I_{OZH}	Output leakage current, HIGH	V_{OUT} = 5.0V	0.01		3.0		3.0	µA

Switching characteristics [1,2,6,7,8,9,16,17]

Parameter		Test Conditions	Typ	Temperature Range				Units
				Industrial		Extended		
				Min	Max	Min	Max	
t_C	Conversion Time		$27/f_{CLK}$		$27/f_{CLK}+.25$		$27/f_{CLK}+.25$	µs
		f_{CLK} = 3.5MHz, $\overline{AZ}$ = HIGH	7.7		7.95		7.95	µs
		f_{CLK} = 1.75MHz, $\overline{AZ}$ = LOW	15.4		15.65		15.65	µs
		$\overline{T}$/H starts conversion,	$34/f_{CLK}$		$34/f_{CLK}+.25$		$34/f_{CLK}+.25$	µs
		f_{CLK} = 3.5MHz, $\overline{AZ}$ = HIGH	9.7		9.98		9.95	µs
t_A	Acquisition Time [14]	using $\overline{WR}$ only			$7/f_{CLK}+0.25$		$7/f_{CLK}+0.25$	µs
		R_S = 50Ω	3.5		3.5		3.5	µs
t_Z	Auto-Zero Time Plus		$33/f_{CLK}$		$33/f_{CLK}+.25$		$33/f_{CLK}+.25$	µs
	Acquisition Time	f_{CLK} = 1.75MHz	18.8		19.05		19.05	µs
t_{CAL}	Calibration Time		$1399/f_{CLK}$		$1399/f_{CLK}$		$1399/f_{CLK}$	µs
		f_{CLK} = 3.5MHz	399		400		400	µs
t_{PWCAL}	Calibration Pulse Width	Note 15	60	200		200		ns
t_{PWWR}	$\overline{WR}$ Pulse Width		60	200		200		ns
t_{DHE}	Hold-to-EOC Delay	using $\overline{WR}$ input	200		350		350	ns
		using $\overline{T}$/H input	100		150		150	ns
t_{RDINT}	$\overline{RD}$ or $\overline{WR}$ to Reset of $\overline{INT}$		100		175		175	ns
t_{ENA}	Output Enable Time	C_L = 100pF	50		95		95	ns
t_{RR}	$\overline{RD}$ to $\overline{RD}$ Pulse Width		30		60		60	ns
t_{DIS}	Data Disable Time	C_L = 100pF, R_L = 1kΩ	30		70		70	ns

System performance characteristics [1,2,6,7,8,9,16]

Parameter		Test Conditions	Typ.	Temperature Range				Units
				Industrial		Extended		
				Min	Max	Min	Max	
E_{LIP}	Positive Integral Linearity Error	After Auto-Cal, [10,11]	±0.5					LSB
E_{LIN}	Negative Integral Linearity Error	After Auto-Cal, [10,11]	±0.5					LSB
E_{LD}	Differential Linearity Error	After Auto-Cal, [10,11]	12					Bits
E_{FSP}	Positive full-scale error	After Auto-Cal, [11]			±2.0		±2.0	LSB
		$\overline{AZ}$ = LOW, f_{CLK} = 1.75MHz	±1.0		±1.5		±1.5	LSB
E_{FSN}	Negative full-scale error	After Auto-Cal, [11]			±2.0		±2.0	LSB
		$\overline{AZ}$ = LOW, f_{CLK} = 1.75MHz	±1.0		±1.5		±1.5	LSB
E_Z	Zero Error [11,12]	After Auto-Cal or Auto-Zero,			±2.5		±2.5	LSB
		$\overline{AZ}$ = LOW, f_{CLK} = 1.75MHz	±1.0		±1.0		±1.0	LSB
PSS_Z	Power Supply Sensitivity, Zero Error [13]	$AV_{CC} = DV_{CC}$ = ±5.0 ±5% V– = –5.0 ±5%, V_{REF} = ±4.75V	±0.125					LSB
PSS_F	Power Supply Sensitivity, Full-scale error	$AV_{CC} = DV_{CC}$ = ±5.0 ±5% V– = –5.0 ±5%, V_{REF} = ±4.75V	±0.125					LSB
PSS_L	Power Supply Sensitivity, Linearity error	$AV_{CC} = DV_{CC}$ = ±5.0 ±5% V– = –5.0 ±5%, V_{REF} = ±4.75V	±0.125					LSB

Dynamic performance characteristics [1,2,6,7,8,9,16,17,18]

Parameter		Test Conditions	Typ.	Temperature Range				Units
				Industrial		Extended		
				Min	Max	Min	Max	
SNR_B	Signal-to-Noise Ratio, Bipolar Input	f_{IN} = 1kHz, V_{IN} = ±4.85V p-p	78					dB
		f_{IN} = 10kHz, V_{IN} = ±4.85V p-p	78					dB
		f_{IN} = 20.67kHz,V_{IN} = ±4.85V p-p	78	73.5		73.5		dB
SNR_U	Signal-to-Noise Ratio, Unipolar Input	f_{IN} = 1kHz, V_{IN} = 4.85V p-p	73					dB
		f_{IN} = 10kHz, V_{IN} = 4.85V p-p	73					dB
		f_{IN} = 20.67kHz,V_{IN} = 4.85V p-p	73	68.7		68.7		dB
$SFDR_B$	Spurious Free Dynamic Range, Bipolar Input	f_{IN} = 1kHz, V_{IN} = ±4.85V p-p	–88					dB
		f_{IN} = 10kHz, V_{IN} = ±4.85V p-p	–84					dB
		f_{IN} = 20kHz, V_{IN} = ±4.85V p-p	–80					dB
$SFDR_U$	Spurious Free Dynamic Range, Unipolar Input	f_{IN} = 1kHz, V_{IN} = 4.85V p-p	–90					dB
		f_{IN} = 10kHz, V_{IN} = 4.85V p-p	–86					dB
		f_{IN} = 20kHz, V_{IN} = 4.85V p-p	–82					dB
THD_B	Total Harmonic Distortion, Bipolar Input	f_{IN} = 1kHz, V_{IN} = ±4.85V p-p	–82					dB
		f_{IN}= 20.67kHz,V_{IN} = ±4.85V p-p	–80		–78		–78	dB
THD_U	Total Harmonic Distortion, Unipolar Input	f_{IN} = 1kHz, V_{IN} = ±4.85V p-p	–82					dB
		f_{IN}= 20.67kHz,V_{IN} = ±4.85V p-p	–80		–73.1		–73.1	dB
IMD_B	Two-Tone Intermodulation Distortion, Bipolar Input	V_{IN} = ±4.85V p-p, f_{IN1} = 19.375kHz, f_{IN2} = 20.625 kHz	–78					dB
IMD_U	Two-Tone Intermodulation Distortion, Unipolar Input	V_{IN} = 4.85V p-p, f_{IN1} = 19.375kHz, f_{IN2} = 20.625 kHz	–78					dB
EFB_B	Effective Bits, Bipolar Input	f_{IN} = 1kHz, V_{IN} = ±4.85 V p-p	12.6					Bits
		f_{IN} = 20.67kHz,V_{IN} = ±4.85V p-p	12.6	11.9		11.9		Bits
EFB_U	Effective Bits, Unipolar Input	f_{IN} = 1kHz, V_{IN} = 4.85 V p-p	11.8					Bits
		f_{IN} = 20.67kHz,V_{IN} = 4.85V p-p	11.8	11.1		11.1		Bits
BW_U	Bandwidth, Bipolar Input	V_{IN} = ±4.85V p-p	25	20.67		20.67		kHz
BW_B	Bandwidth, Unipolar Input	V_{IN} = 4.85V p-p	30	20.67		20.67		kHz
t_{AP}	Aperture Time		100					ns
t_{APJ}	Aperture Jitter		100					ps_{rms}

Notes for specification tables

1. Absolute Maximum Ratings are limits beyond which the device may be damaged. Operating Conditions are limits under which the device is guaranteed to be functional, but those limits do not guarantee specific performance. Guaranteed specifications and test conditions are shown in the *Electrical, Switching and System Performance Characteristics Tables*. The guaranteed specifications apply only for the test conditions listed in the *Electrical, Switching and System Performance Characteristics Tables*. Some performance characteristics may degrade when the device is operated outside the listed test conditions.
2. All voltages are measured with respect to A_{GND} and D_{GND}, unless otherwise specified.
3. When the voltage at any pin exceeds the power supply voltages (< V– or >AV_{CC} or >DV_{CC}), the current at that pin must be limited to 5mA. The 20mA maximum package input current rating allows the voltage any any four pins, with a current limit of 5mA, to simultaneously exceed the power supply voltages.

Notes for specification tables (cont.)

4. The power dissipation of this device under normal operation should not exceed 191mW (quiescent power plus one TTL load on each of the ten digital outputs). Care must be taken to ensure that Absolute Maximum Ratings are not violated when any inputs

   or outputs are driven to voltages greater than power supply voltages. The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum allowable junction temperature), θ_{JA} (junction-to-ambient thermal resistance of the package). and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is given by:

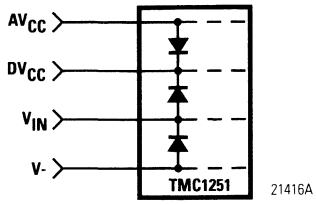
   $$P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$$

   or the number given in the ***Absolute Maximum Ratings Table***, whichever is lower. For the TMC1251, T_{Jmax} is 125°C and the typical thermal resistance (θ_{JA}) of the TMC1251 with B7F, B7B1, and B7B suffixes when board mounted is 51°C/W.

5. Human body model, 100pF discharged through a 1.5kΩ resistor.

6. Two on-chip diodes are tied to the analog input as shown in the following Figure, ***Parasitic Diode Structure***. A/D conversion errors can occur if these diodes are forward-biased more than 50mV. Therefore, if AV_{CC} and DV_{CC} are +4.75 Volts and V- is –4.75 Volts, the analog input range must be no greater than ±4.80 Volts.

Parasitic Diode Structure



7. To guarantee accuracy, it is required that AV_{CC} and DV_{CC} be connected to the same power source but with separate decoupling capacitors at each pin. This prevents the parasitic diode between AV_{CC} and DV_{CC} from being forward biased.

8. Accuracy is guaranteed with f_{CLK} equal to 2.0MHz. Accuracy may degrade at higher clock frequencies.

9. Typical specifications are at $T_J = 25^0C$ and represent the most likely parametric norm (statistical "mode").

10. Positive linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative linearity error the straight line passes through negative full-scale and zero. (See ***Simplified Error Characteristic Curves***)

11. The TMC1251's self-calibration technique ensures linearity, full-scale and offset errors as specified. Noise inherent to the self-calibration process will result in a repeatability uncertainty of +0.20 LSB.

12. When t_A changes, an Auto-Zero or Auto-Cal cycle will be required for specified performance. (see ***Typical Performance Curves***)

13. After Auto-Zero or Auto-Cal cycle execution at the specified power supply extremes.

14. When using $\overline{WR}$ to start an A/D conversion, if the CLK_{IN} is asynchronous with respect to the rising edge of $\overline{WR}$ an uncertainty of one clock period exists in the t_A interval. Therefore, the minimum t_A is six clock periods and the maximum t_A is 7 clock periods. If the falling edge of CLK_{IN} is synchronous with respect to the rising edge of $\overline{WR}$ then t_A will be exactly 6.5 clock periods. This does not occur when $\overline{T}/H$ is used.

15. The $\overline{CAL}$ input must go HIGH before an A/D conversion is started.

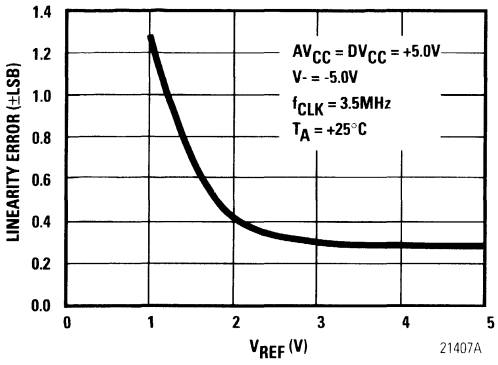
16. Guaranteed specifications apply for $AV_{CC} = DV_{CC} = \pm 5.0V$, $V- = -5.0V$, $V_{REF} = -5.0V$ and $f_{CLK} = 2.0MHz$ unless otherwise specified.

17. Rise and fall times for digital inputs = 20ns, unless otherwise specified.

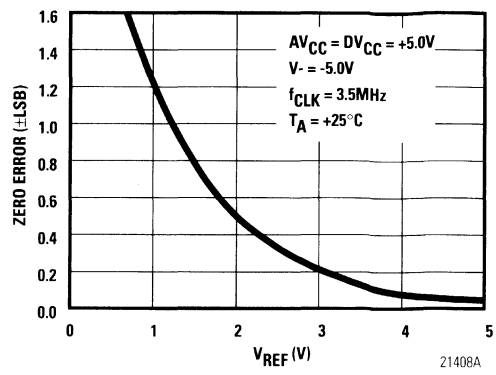
18. Dynamic performance parameters are valid only after an Auto-Cal cycle has been completed.

Typical Performance Curves

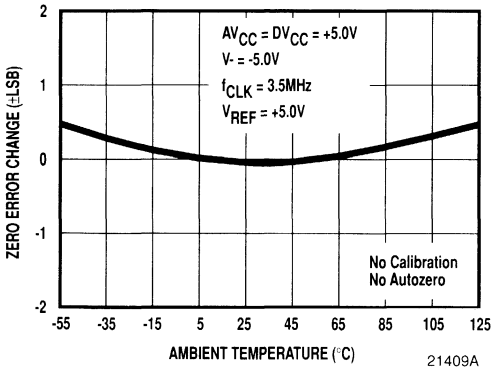
A. Linearity Error vs. V_{REF}



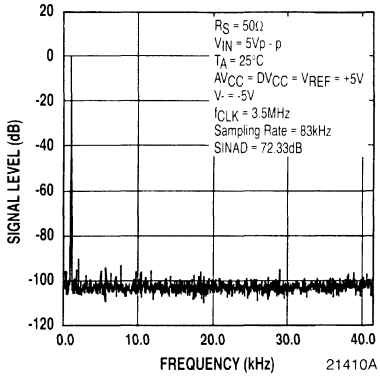
B. Zero Error vs. V_{REF}



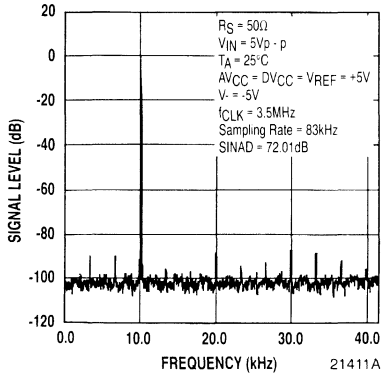
C. Zero Error Change vs. Ambient Temperature



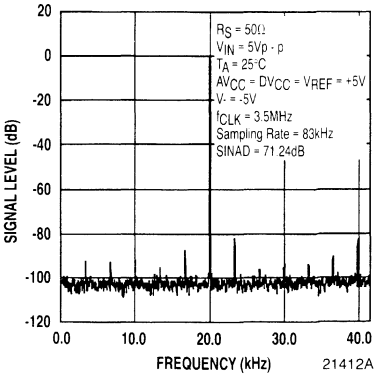
D. Unipolar Spectral Response with 1kHz Sinewave Input



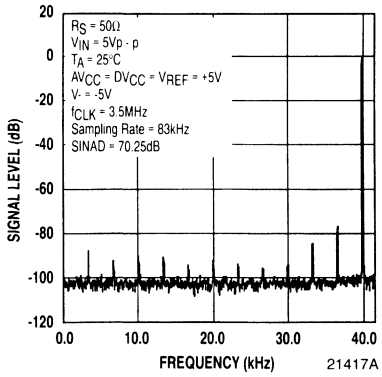
E. Unipolar Spectral Response with 10kHz Sinewave Input



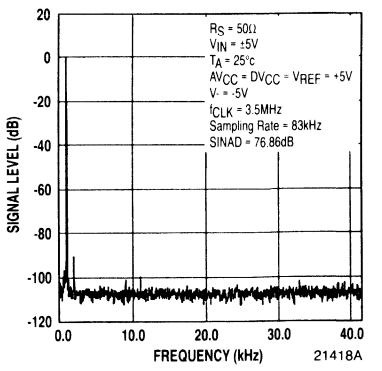
F. Unipolar Spectral Response with 20kHz Sinewave Input



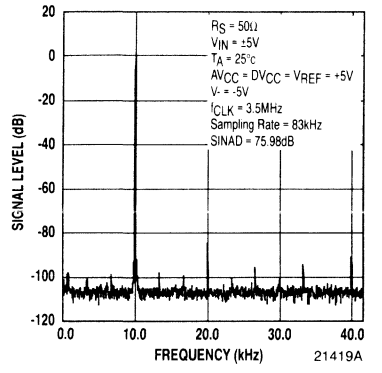
G. Unipolar Spectral Response 40kHz Sinewave Input



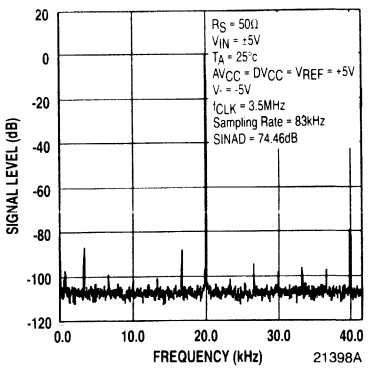
H. Bipolar Spectral Response with 1kHz Sinewave Input



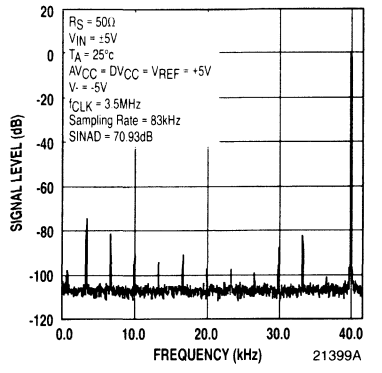
I. Bipolar Spectral Response with 10kHz Sinewave Input



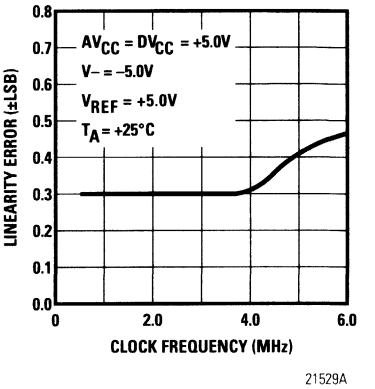
J. Bipolar Spectral Response with 20kHz Sinewave Input



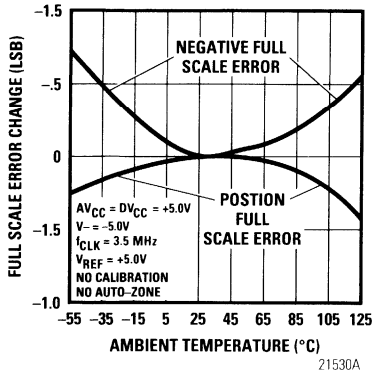
K. Bipolar Spectral Response with 40kHz Sinewave Input



L. Linearity Error vs Clock Frequency

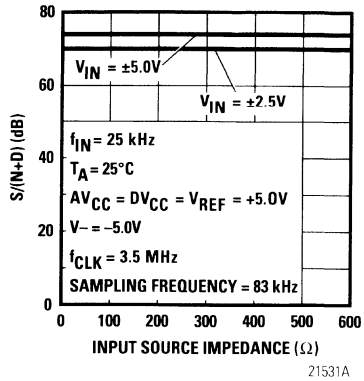


M. Full Scale Error Change vs Ambient Temperature



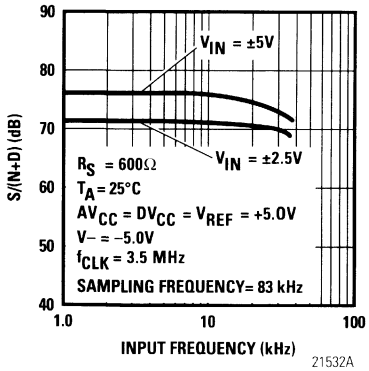
21530A

N. Bipolar SINAD vs Input Source Impedance



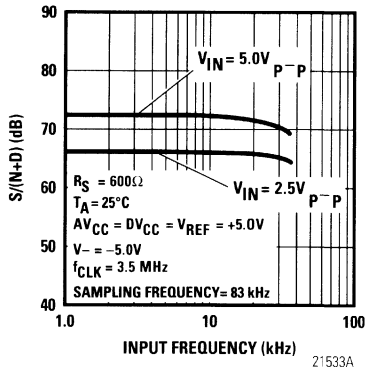
21531A

O. Biploar SINAD vs Input Frequency



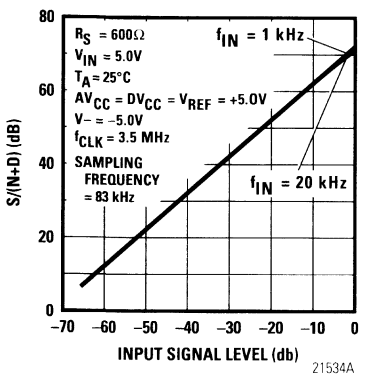
21532A

P. Unipolar SINAD vs Input Frequency



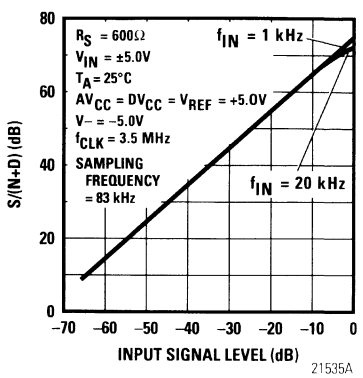
21533A

Q. Unipolar SINAD vs Input Signal Level



21534A

R. Bipolar SINAD vs Input Signal Level

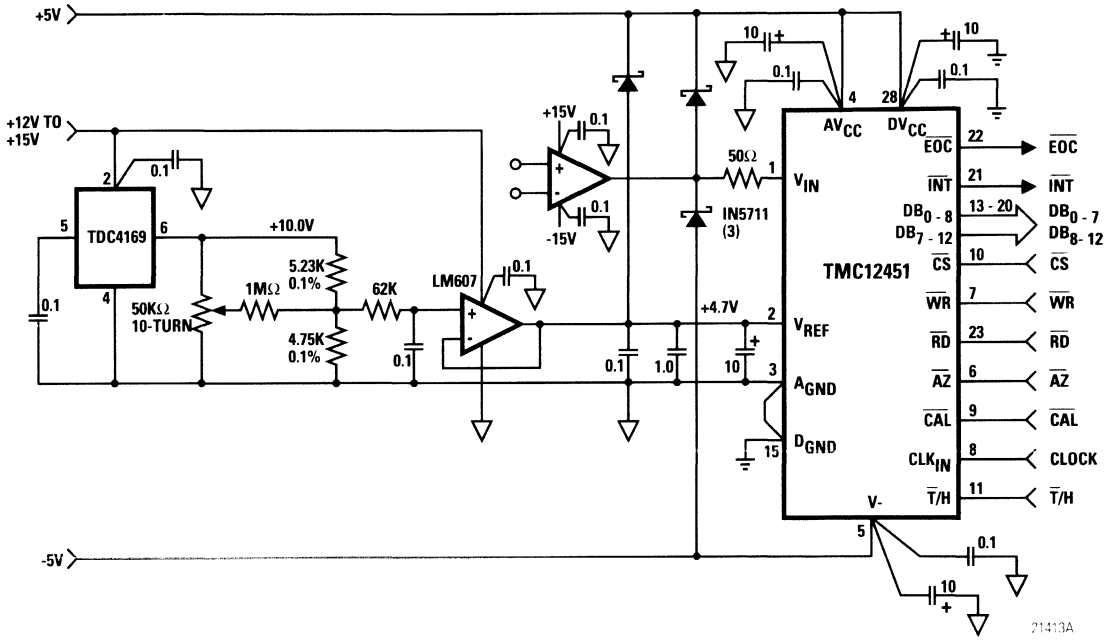


21535A

The Typical Interface Circuit

Noise on AV_{CC}, DV_{CC} or V- power supply inputs can cause A/D conversion errors should the TMC1251 comparator be influenced by that noise. The TMC1251 is especially sensitive during the Auto-Zero or Auto-Cal cycles to power supply noise. Low inductance 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors are recommended for power supply decoupling. Separate decoupling capacitors should be placed close to the DV_{CC}, AV_{CC} and V- pins.

Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC12451B7F	EXT, T_A = -55°C to 125°C	Commercial	28 Pin CERDIP	12451B7F
TMC12451B7B	IND, T_A = -40°C to 85°C	Commercial	28 Pin CERDIP	12451B7B
TMC1251E1C	STD, T_A = 0°C to 70°C		Eurocard PC Board	1251E1C

D/A Converters

TRW's D/A converters address video, signal synthesis, and graphics applications.

To the industry-standard TDC1016 10-bit video D/A (75Ω voltage output) we have recently added the smaller, less expensive, and lower-power TDC1041 (TTL) and TDC1141 (ECL) DACs. The new devices are available in 28 lead PLCCs as well as DIPs, and have been optimized to produce quality video signals.

The TDC1012 (20Msps) and TDC1112 (50Msps) have become the standard of comparison for signal synthesis applications. The 12-bit D/As have a Spurious-Free Dynamic Range (SFDR) of more than 70dBc. They can directly drive a double-terminated 50Ω line (25Ω) to 1Vp-p without an output amplifer, simplifying interfacing and reducing overall system distortion.

TRW's line of high-speed graphics DACs addresses the needs of today's high-resolution display systems. Palette DACs with 6 or 8-bit resolution meet industry-standard pinouts and exceed competitors' performance. The single and triple 4 and 8-bit 200Msps D/As are ideal for systems not requiring a palette function.

Product	Resolution Bits	Differential Linearity Error [1] (± %)	Conv Rate [1] (Msps)	Rise Time [1] (ns)	Package		Grade [2]	Notes	Page
TDC1034	4	0.80	200	2	B8	18 Pin DIP	C	Low Cost ECL. Graphics-Ready.	B63
TDC1334	4 (Triple)	0.80	200	2	B6	24 Pin DIP	C	Low Cost ECL. Graphics-Ready.	B131
TMC0171-4	6	0.78	40	8	R2	44 Lead PLCC	C	RAMDAC. 256 x 18 Lookup Table.	B3
					N6	28 Pin DIP	C	IMS171 Compatible.	
	6	0.78	35	8	N6	28 Pin DIP	C		
TMC0176-8	6	0.78	80	8	N6	28 Pin DIP	C	RAMDAC. 256 x 18 Lookup Table.	B3
-6	6	0.78	66	8	N6	28 Pin DIP	C	IMS176 Compatible.	
-5	6	0.78	50	8	N6	28 Pin DIP	C		
-4	6	0.78	40	8	R2	44 Lead PLCC	C		
					N6	28 Pin DIP	C		
TDC1018-1	8	0.20	200	1.7	B7	24 Pin DIP	C	Low Cost ECL. Graphics-Ready.	B51
					C3	28 Contact CC	C		
	8	0.20	125	1.7	B7	24 Pin DIP	C		
					C3	28 Contact CC	C		
TDC1318	8 (Triple)	0.20	200	2	B5	40 Pin DIP	C	Low Cost ECL. Graphics-Ready.	B119
TMC0458	8 (Triple)	0.20	200		H7	89 Pin Plastic PGA	C	RAMDAC. 256 x 24 Lookup Table.	B21
					R0	84 Lead PLCC	C		
TDC1016-10	10	0.05	20	4	N7	24 Pin DIP	C	Industry-Standard Video DAC.	B41
					N5	40 Pin DIP	C	Operates with TTL or ECL Logic.	
-9	10	0.10	20	4	B7, N7	24 Pin DIP	C, A		
					B5, N5	40 Pin DIP	C, A		
-8	10	0.20	20	4	B7, N7	24 Pin DIP	C, A		
					B5, N5	40 Pin DIP	C, A		
TDC1041-1	10	0.048	20	4	R3	28 Lead PLCC	C	Low Cost 10-Bit Video D/A	B75
	10	0.096	20	4	R3	28 Lead PLCC	C	TTL Interface.	
TDC1141-1	10	0.048	50	4	R3	28 Lead PLCC	C	Low Cost 10-Bit Video D/A	B105
	10	0.096	50	4	R3	28 Lead PLCC	C	ECL Interface.	
TDC1012-3	12	0.012	20	4	J7, N7	24 Pin DIP	C	Signal Synthesis D/A.	B23
					R3	28 Lead PLCC	C	70dBc SFDR. Very Low Glitch.	
-2	12	0.024	20	4	J7, N7	24 Pin DIP	C, V, SMD	Drives 25Ω Directly.	
					R3	28 Lead PLCC	C	TTL Interface.	
-1	12	0.048	20	4	J7, N7	24 Pin DIP	C, V, SMD		
					R3	28 Lead PLCC	C		
	12	0.048	20	4	J7, N7	24 Pin DIP	C, V, SMD		
					R3	28 Lead PLCC	C		
TDC1112-3	12	0.012	50	4	J7, N7	24 Pin DIP	C	Signal Synthesis D/A.	B87
					R3	28 Lead PLCC	C	70dBc SFDR. Very Low Glitch.	
-2	12	0.024	50	4	J7, N7	24 Pin DIP	C, V	Drives 25Ω Directly.	
					R3	28 Lead PLCC	C	ECL Interface.	
-1	12	0.048	50	4	J7, N7	24 Pin DIP	C, V		
					R3	28 Lead PLCC	C		
	12	0.048	50	4	J7, N7	24 Pin DIP	C, V		
					R3	28 Lead PLCC	C		

Notes: 1. Guaranteed. See product specifications for test conditions.

2. A = High Reliability, $T_C = -55°C$ to $125°C$.
C = Commercial, $T_A = 0°C$ to $70°C$.
V = MIL-STD-883 Compliant, $T_C = -55°C$ to $125°C$
SMD = Available per Standardized Military Drawing, $T_C = -55°C$ to $125°C$.

TMC0171, TMC0176

Color Palette with Triple 6-Bit DAC

The TMC0171 and TMC0176 are triple 6-bit video DACs with 256 x 18 RAM look-up tables and microprocessor interfaces. The devices were designed specifically for high resolution color graphics, supporting 256 simultaneous colors out of a palette of over a quarter million, at update rates fast enough to generate all common PC display resolutions.

The TTL microprocessor interface allows easy integration into personal computer systems. The three outputs are compatible with RS-170, allowing for a system design using a minimum of external components.

A pixel word mask facilitates such special effects as animation, overlays, and paged graphics without rewriting image RAM or the color look-up table.

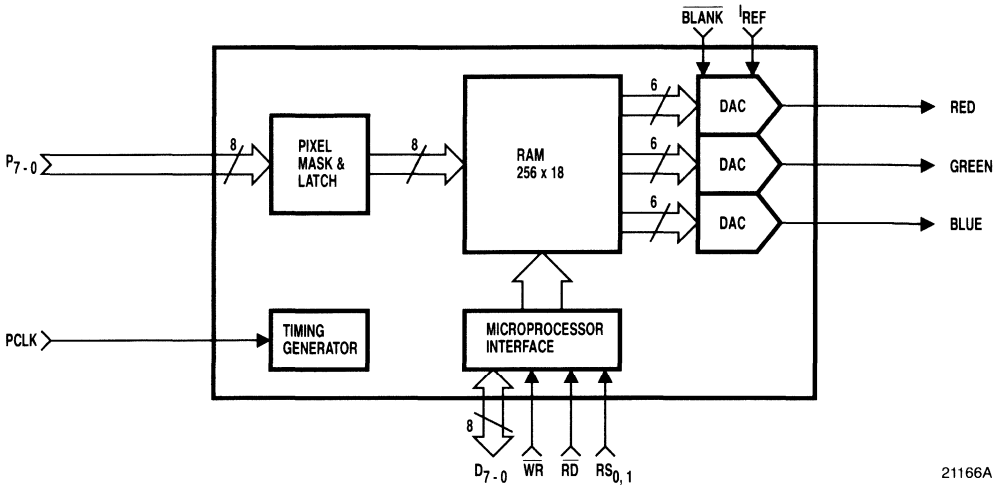
The TMC0171 is pin and function compatible with the industry standard IMS G171 high performance CMOS color look-up table DAC manufactured by Inmos, and the TMC0176 is pin and function compatible with the IMS G176.

Features

- Pixel Rates Of 0 to 80MHz
- 256 x 18 Bit Color Palette
- Color Palette Read-Back
- 75Ω RGB Analog Video Outputs
- Composite Blank
- Single +5V Power Supply
- Low Power Consumption
- TTL Compatible Inputs
- Asynchronous μP Interface
- Available In A 28 Pin Plastic DIP Or 44 Leaded PLCC

B

Interface Diagram



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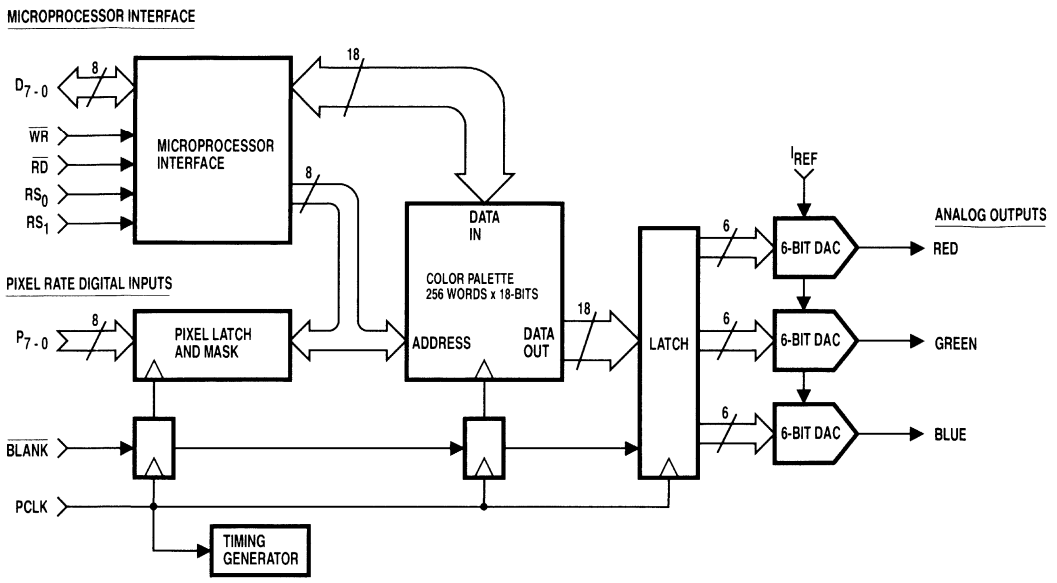
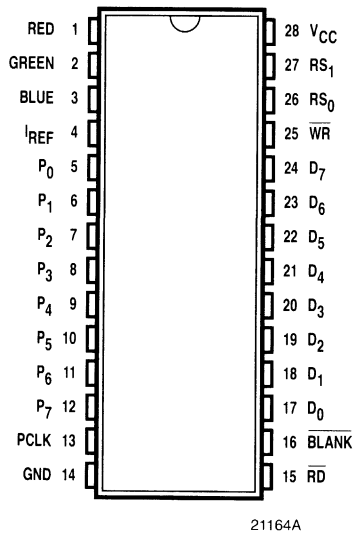
40G06616 Rev. B–11/90
Printed in the U.S.A.

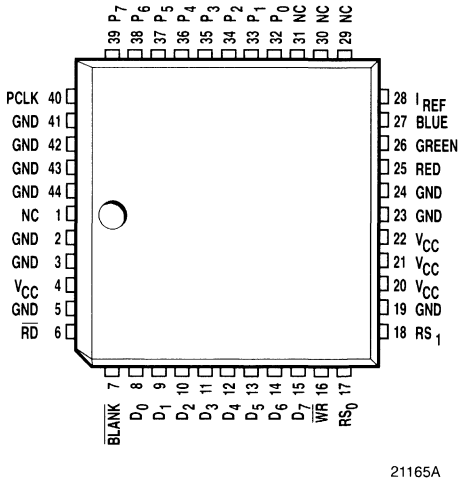
Functional Block Diagram



Pin Assignments



28 Pin Plastic DIP – N6 Package



44 Lead Plastic J-Leaded Chip Carrier – R2 Package

Functional Description

General Information

The TMC0171 and TMC0176 contain a Color Palette with 256 memory locations that are 18 bits wide. The color palette's output is connected to three high-speed current output 6-bit video DACs. The devices on-board registers easily interface with microprocessors.

Microprocessor Interface

The Microprocessor interface consists of three internal registers: Pixel Address Register, Color Value Register and Pixel Mask Register. These are individually accessed by register select signals, RS_0 and RS_1. The following table defines which register is selected by the logic states of RS_0 and RS_1:

RS_0	RS_1	Register
0	0	Pixel Address ($\overline{WRITE}$ Mode)
1	1	Pixel Address ($\overline{READ}$ Mode)
1	0	Color Value
0	1	Pixel Mask

The contents of the color palette can be accessed through the Color Value and Pixel Address registers.

All operations on the microprocessor interface can take place asynchronously to the pixel information being processed by the Color Palette.

The Pixel Address register is a byte-wide latch that receives and latches address information applied to pins P_{7-0}. It can be used in $\overline{READ}$ or $\overline{WRITE}$ mode, depending on the logic state of RS_0 and RS_1. With $RS_0 = RS_1 = 0$ (register select = 0, 0), the Pixel Address register is in the $\overline{WRITE}$ mode. To update one of the color palette's entries, the user writes the address into the Pixel Address register, then its red, green, and blue color definitions into the Color Value register. Refer to *Figures 10* and *11*.

When $RS_0 = RS_1 = 1$ (register select = 1, 1), the Pixel Address register is in the $\overline{READ}$ mode. To read one of the color palette's entries, the user writes its address into the Pixel Address register and then reads the three color definition components. The color definition data input/output sequence is always RED, GREEN, BLUE. Refer to *Figures 9, 12,* and *13*.

The 18-bit Color Value register, used as a buffer between the microprocessor interface and the color palette, is accessed by setting $RS_0 = 1$ and $RS_1 = 0$. A color definition can be read from or written to this register by a sequence of three byte-wide transfers to this register address. When a byte is written to this register, only the least significant six bits (D_{5-0}) are used. When a byte is read from this register address, only the six least significant bits contain information – the most significant two bits are set to zero. Refer to *Figures 9-13*.

After the $\overline{WRITE}$ sequence is completed, the Color Value register's contents are written to the specified color palette address stored in the Pixel Address register. Finally, the Pixel Address register is automatically incremented.

The color definitions can be read from the color palette. After setting RS_0 and RS_1 to 1, the user stores the desired color palette address in the Pixel Address register. The color definition (18 bits) in that color palette location is then transferred to the Color Value register and the Pixel Address is auto-incremented. With successive $\overline{READ}$ cycles, the color definitions pointed to by the incremented address are transferred to the Color Value register. Refer to *Figure 12*.

Attempting to update the color palette when $\overline{BLANK}$ is not asserted results in the data from the Color Value register taking precedence over the bit mapping operation. The output of the three 6-bit DACs will be based on the color definition from the memory location specified by the Pixel Address register and not the address found on P_{7-0}. This conflict causes the DACs to generate unexpected output levels for up to two PCLK periods.

The Pixel Mask register is a byte-wide latch, accessed by the microprocessor interface, D_{7-0}, when $RS_0 = 0$ and $RS_1 = 1$. This register is used to mask selected bits of the Pixel Address values applied to inputs P_{7-0}. A "1" in any location in the Pixel Mask register sets the corresponding bit to zero. The operation of the Pixel Mask register does not affect the address of the color definition when the microprocessor accesses the color palette. The masking operation makes it possible to alter the displayed colors without altering the contents of external video memory or the internal color palette.

B

Writing to the Color Palette

A new color definition can be stored in the color palette by first specifying the initial address under $\overline{\text{WRITE}}$ mode. This address is stored in the Pixel Address register ($RS_0 = RS_1 = 0$). The initial address is followed by RED, GREEN and BLUE color definition data ($RS_0 = 1$, $RS_1 = 0$). These six-bit inputs are collected together in the Color Value register. This new color definition is then transferred to the location pointed to by the information in the Pixel Address register. As soon as this transfer is completed, the Pixel Address register is auto-incremented. This allows consecutive color palette locations to be updated without the microprocessor specifying each address. The host needs only to continue supplying the RED, GREEN and BLUE data for each consecutive address. Refer to *Figures 10* and *11*.

Reading from the Color Palette

To read a location in the color palette, an address is sent on the Data I/O lines (D_{7-0}) under $\overline{\text{READ}}$ mode and stored in the Pixel Address register ($RS_0 = RS_1 = 1$). The color definition contained in the specified location is then transferred to the Color Value register. Again, the Pixel Address register is auto-incremented. The color definition can now be retrieved with three sequential $\overline{\text{READ}}$ operations ($RS_0 = 1$, $RS_1 = 0$). The first byte placed on the Data I/O lines contains the RED value; the next is GREEN and the final is BLUE. The two most significant bits are set to zero in each case. In a manner similar to the $\overline{\text{WRITE}}$ mode, consecutive color palette locations can be read by simply specifying the beginning address and reading the color palette one or more times. Refer to *Figures 9, 12* and *13*.

If the Pixel address register is updated during a $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ operation, the current data sequence is terminated and a new $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ operation is initialized.

Video Path

The Video path consists of the Pixel Latch and Mask (inputs P_{7-0}), color palette (256 18-bit wide RAM), 18-bit wide bus, and an 18-bit wide latch on the inputs of the three 6-bit high-speed video DACs. The video path uses a three clock cycle (PCLK) pipeline for the Pixel Address and $\overline{\text{BLANK}}$ inputs. These signals are latched on the rising edge of PCLK.

Analog Outputs

The analog outputs are designed to drive singly-terminated 75Ω loads to a peak-white amplitude of 0.7V.

The reference current (I_{REF}) for this output is set to 4.44mA. The analog outputs can also drive doubly-terminated 75Ω loads with I_{REF} set to 8.88mA.

The active LOW $\overline{\text{BLANK}}$ input forces the analog outputs to ground, ignoring the color definition selected by the Pixel Address. Each of the 63 current sources used in each of the 6-bit DACs produces 1/30 I_{REF}. Therefore, the magnitude of peak white voltage is a function of the output loading and is determined by:

$$V_{PEAK\ WHITE} = 2.1 \bullet I_{REF} \bullet R_L$$
$$V_{BLACK\ LEVEL} = 0V.$$

Signal Descriptions

Signal Name	Package Pin Number N6	Package Pin Number R2	Signal Type	Signal Description
Red Green Blue	1 2 3	25 26 27	O O O	These analog outputs of the 6-bit DACs are the currents used for each of the guns in an RGB (Red, Green, Blue) video display.
I_{REF}	4	28	I	The current forced out of this Reference Current Input pin to ground determines the current sourced by each of the 63 current source in each of the three 6-bit DACs. Each current source produces $I_{REF}/30$ when activated by the 6-bit digital input code.
P_{7-0}	12-5	39-32	I	The byte-wide information on these Pixel Address lines is latched and masked by the Pixel Mask Register. The resulting value addresses a location in the Color Palette RAM. P_0=LSB.
PCLK	13	40	I	The rising edges of the Pixel Clock signal control the latching of the Pixel Address and Blanking Inputs. They also control the progress of these values through the three stage pipeline of the Color Palette the DACs to the outputs.
GND	14	2, 3, 5, 19, 23, 24, 41-44		This is the power supply ground connection.
V_{CC}	28	4, 20, 21, 22		This positive power supply pin is normally connected to +5V DC and bypassed with a 10μF tantalum capacitor.
$\overline{RD}$	15	6	I	When this $\overline{READ}$ bus control signal is LOW, information present on the internal data bus is available on the Data I/O lines (D_{7-0}).
$\overline{BLANK}$	16	7	I	This active LOW signal forces the DACs' outputs to zero. When $\overline{BLANK}$ is asserted, a video monitor's screen becomes blank and the DACs ignore any output values from the Color Palette. However, the Color Palette can still be updated through D_{7-0}.
D_{7-0}	24-17	15-8	I/O	These bidirectional Data I/O lines are used by the host microprocessor to $\overline{WRITE}$ information (using the active LOW $\overline{WR}$) into and $\overline{READ}$ information (using the active LOW $\overline{RD}$) from the TMC0171's Pixel Address, Color Value and Pixel Mask registers. During the $\overline{WRITE}$ cycle, the rising edge of $\overline{WR}$ latches the data into the selected register. The rising edge of $\overline{RD}$ determines the end of the $\overline{READ}$ cycle. With $\overline{RD}$ and $\overline{WR}$ both HIGH, the Data I/O lines go into a high-impedance state.
$\overline{WR}$	25	16	I	This active LOW $\overline{WRITE}$ signal controls the timing of the $\overline{WRITE}$ operations on the microprocessor interface inputs, D_{7-0}.
RS_0, RS_1	26, 27	17, 18	I	These Register Select lines select one of the three internal registers and are sampled during the falling edges of the enable signals ($\overline{RD}$ or $\overline{WR}$). See the *Functional Description* section for more information regarding the internal registers.
NC		1, 29-31		Not connected internally.

Timing Characteristics

Figure 1. System Timing Diagram

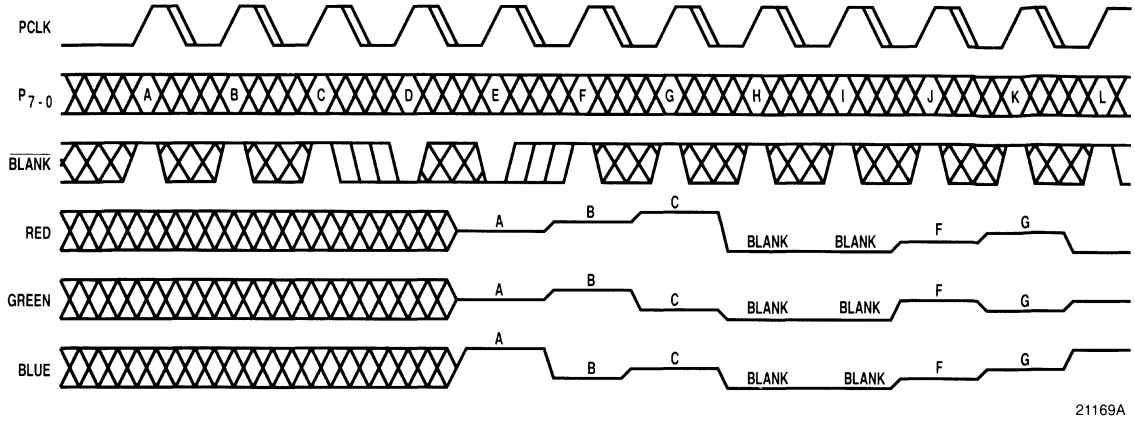


Figure 2. Timing Diagram Detailing Timing Specifications

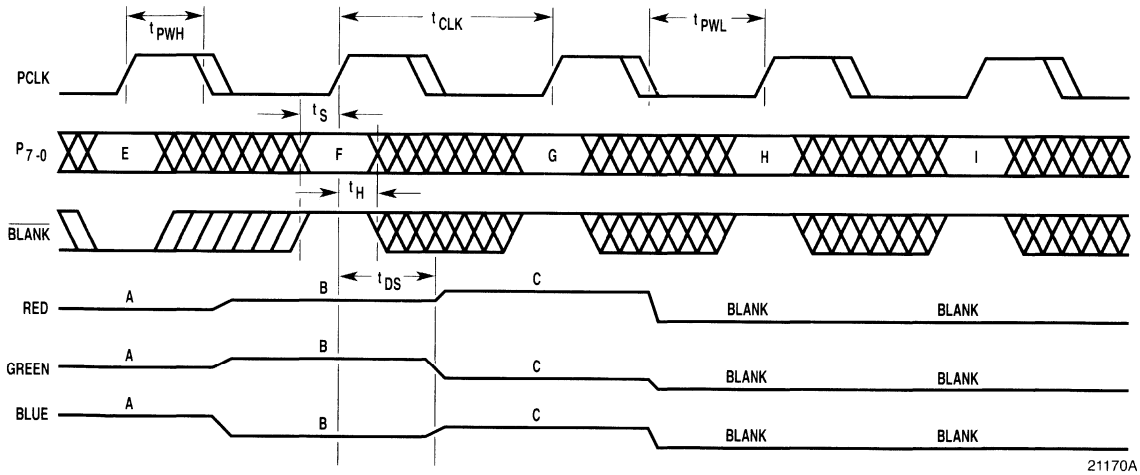


Figure 3. Basic WRITE Cycle Timing Diagram

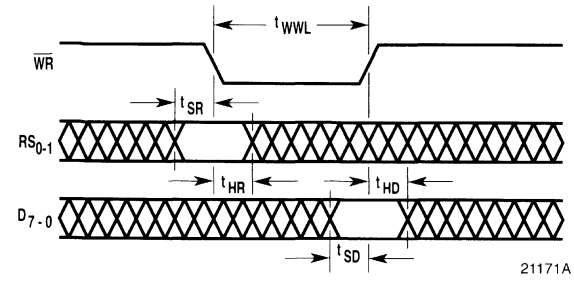


Figure 4. Basic READ Cycle Timing Diagram

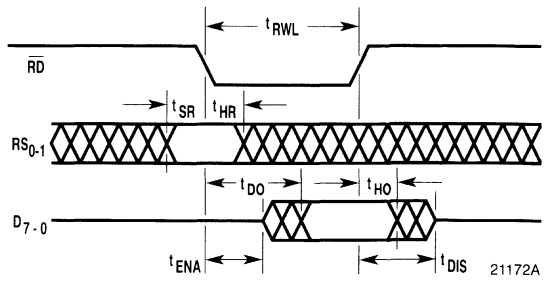


Figure 5. $\overline{\text{WRITE}}$ to Pixel Mask Register Followed by $\overline{\text{WRITE}}$ and $\overline{\text{READ}}$

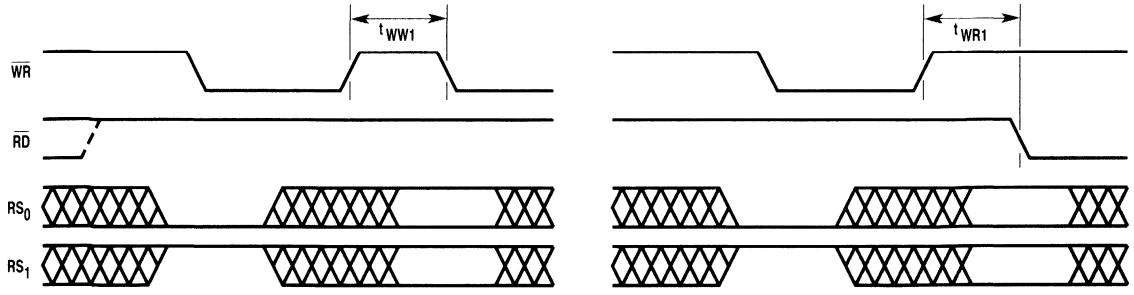


Figure 6a. $\overline{\text{READ}}$ from Pixel Mask or Pixel Address Register ($\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ Mode) Followed by $\overline{\text{READ}}$

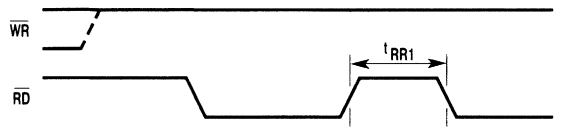


Figure 6b. $\overline{\text{READ}}$ from Pixel Mask or Pixel Address Register ($\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ Mode) Followed by $\overline{\text{WRITE}}$

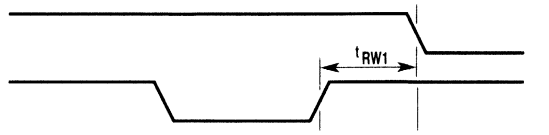


Figure 7. $\overline{\text{WRITE}}$ and $\overline{\text{READ}}$ Back Pixel Address Register ($\overline{\text{READ}}$ Mode)

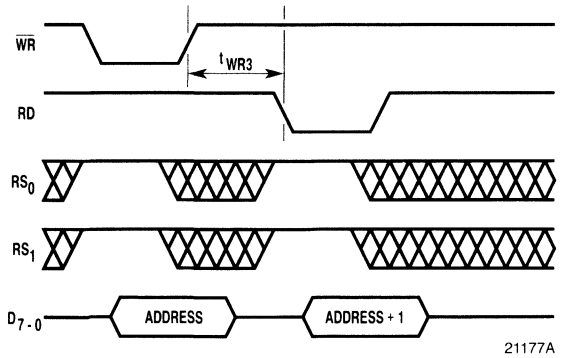


Figure 8. $\overline{\text{WRITE}}$ and $\overline{\text{READ}}$ Back Pixel Address Register ($\overline{\text{WRITE}}$ Mode)

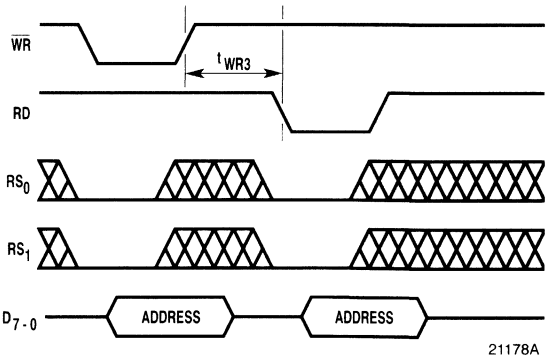


Figure 9. $\overline{\text{READ}}$ Color Value the $\overline{\text{READ}}$ Pixel Address Register ($\overline{\text{READ}}$ Mode)

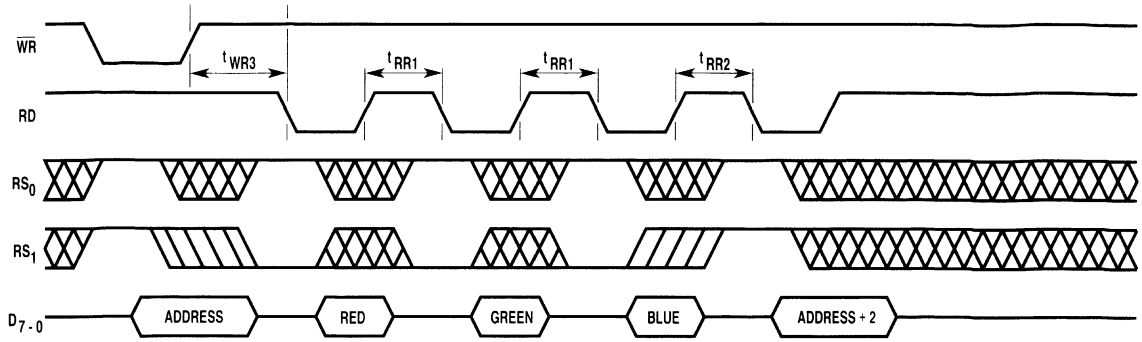


Figure 10. Color Value $\overline{\text{WRITE}}$ Followed by $\overline{\text{READ}}$

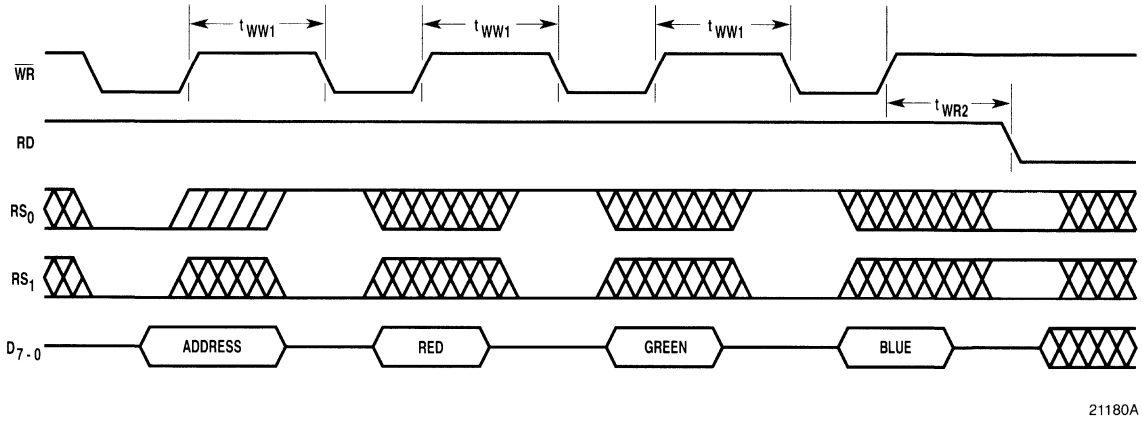


Figure 11. Color Value $\overline{\text{WRITE}}$ Followed by $\overline{\text{WRITE}}$

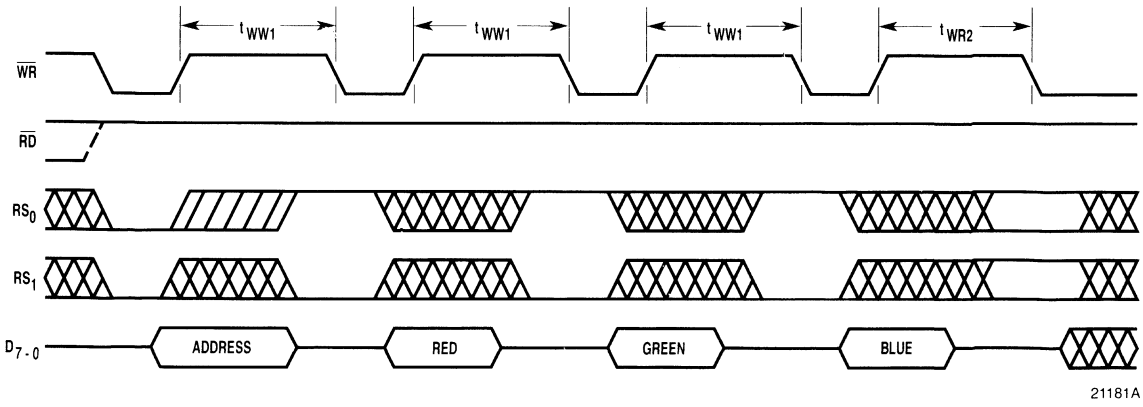


Figure 12. Color Value $\overline{\text{READ}}$ Followed by $\overline{\text{READ}}$

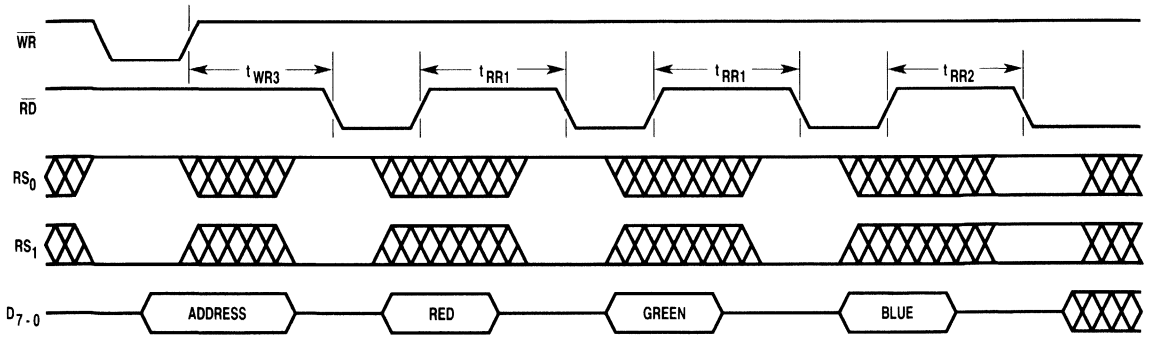
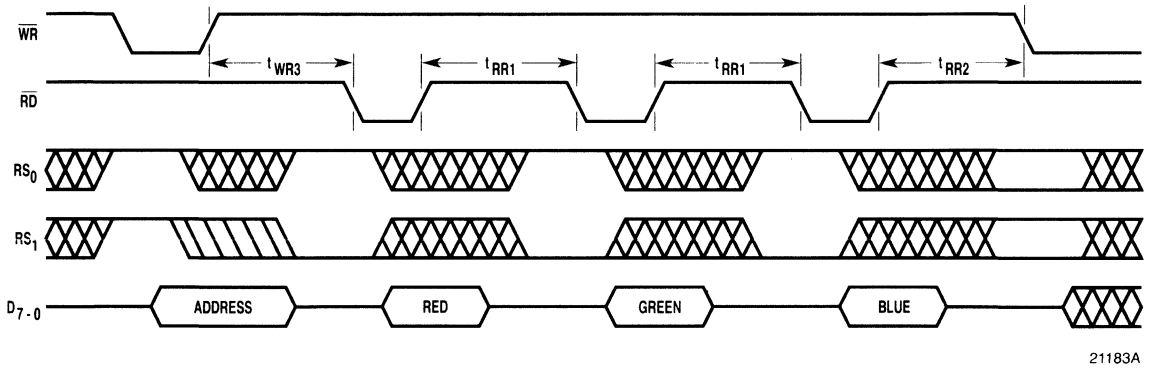


Figure 13. Color Value $\overline{\text{READ}}$ Followed by $\overline{\text{WRITE}}$



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to +7.0V
Temperature	
Operating, ambient	0°C to +70°C
Storage	−65 to +150°C

Note: 1. Stresses above those listed may damage the device permanently. Proper operation at these or any other conditions outside those listed in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating conditions

Parameter		Temperature Range: Standard, Min –	Min –4	Min –5	Min –6	Min –8	Max	Units
V_{CC}	Positive Supply Voltage (Measured to GND)	4.5	4.5	4.5	4.5	4.5	5.5	V
I_{REF}	Reference Input Current	−3	−3	−3	−3	−3	−10	mA
V_{IL}	Digital Input Voltage, Logic LOW	−0.5	−0.5	−0.5	−0.5	−0.5	0.8	V
V_{IH}	Digital Input Voltage, Logic HIGH	2.0	2.0	2.0	2.0	2.0	$V_{CC}+0.5$	V
I_{OL}	Output Current, Logic LOW						2.0	mA
I_{OH}	Output Current, Logic HIGH						−4.0	mA
t_{CLK}	PCLK Period	28	25	20	15	12		ns
Δt_C	PCLK Jitter [1]						±2.5	%
t_{PWL}	PCLK Width, LOW	9	8	6	5	4		ns
t_{PWH}	PCLK Width, HIGH	7	7	6	5	4		ns
t_S	Pixel Word or $\overline{BLANK}$ Setup Time [2]	5	4	4	3	3		ns
t_H	Pixel Word or $\overline{BLANK}$ Hold Time [2]	5	4	4	3	3		ns
t_{WWL}	$\overline{WR}$ Pulse Width, LOW	50	50	50	50	50		ns
t_{RWL}	$\overline{RD}$ Pulse Width, LOW	50	50	50	50	50		ns
t_{SR}	Register Select Setup Time	15	12	10	10	10		ns
t_{HR}	Register Select Hold TIme	15	12	10	10	10		ns
t_{SD}	$\overline{WR}$ Data Setup Time	15	12	10	10	10		ns
t_{HD}	$\overline{WR}$ Data Hold TIme	15	12	10	10	10		ns
t_{WW1}	Successive $\overline{WRITE}$ Interval	3	3	3	3	3		t_{CLK}
t_{WR1}	$\overline{WR}$ Followed by $\overline{READ}$ Interval	3	3	3	3	3		t_{CLK}
t_{RR1}	Successive $\overline{READ}$ Interval	3	3	3	3	3		t_{CLK}
t_{RW1}	$\overline{RD}$ Followed by $\overline{WRITE}$ Interval	3	3	3	3	3		t_{CLK}
t_{WW2}	$\overline{WR}$ after Color $\overline{WRITE}$ [3]	3	3	3	3	3		t_{CLK}
t_{WR2}	$\overline{RD}$ after Color $\overline{WRITE}$ [3]	3	3	3	3	3		t_{CLK}
t_{RR2}	$\overline{RD}$ after Color $\overline{READ}$ [3]	6	6	6	6	6		t_{CLK}
t_{RW2}	$\overline{WR}$ after Color $\overline{READ}$ [3]	6	6	6	6	6		t_{CLK}
t_{WR3}	$\overline{RD}$ after Read Address $\overline{WRITE}$ [3]	6	6	6	6	6		t_{CLK}
t_{TRW}	$\overline{READ}/\overline{WRITE}$ Enable Transition Time	50		50				ns
t_A	Ambient Temperature, Still Air	0	0	0	0	0	70	°C

Notes:
1. This parameter is the allowed variation in the pixel clock frequency. It does not permit the pixel clock period to vary below the minimum specified t_{CLK} value.
2. The color palette's pixel address must be valid for the specified minimum setup and hold times at each rising edge of PCLK (this requirement includes the blanking period).
3. This parameter allows synchronization between operations on the microprocessor interface and the pixel stream being processed by the color palette.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Temperature Range: Standard Max	Units
V_{OL}	Output Voltage, LOW	I_{OL} = Max		0.4	V
V_{OH}	Output Voltage, HIGH	I_{OH} = Max	2.4		V
C_I	Input Capacitance			7	pF
C_O	Output Capacitance			7	pF
C_{IO}	Input/Output Capacitance			16	pF
I_I	Input Leakage Current		−10	10	μA
I_{OZ}	Output Leakage Current		−10	10	μA
I_{CC}	Operating Supply Current	I_{OUT} = Max, Digital Outputs Unloaded, PCLK = 35MHz		150	mA
V_{REF}	Reference Voltage at I_{REF} Pin	V_{CC} = 4.5V, I_{REF} = 10mA	V_{CC} − 3		V
V_{OC}	Output Voltage Compliance	I_{OUT} < 10mA	1.5		V
I_{OC}	Output Current Compliance	V_{OUT} < 1V, I_{REF} < 10mA	21		mA
E_G	Absolute Gain Error [1]	ZL = 75Ω + 30pF, I_{REF} = 4.44mA or ZL = 37.5Ω + 30pF, I_{REF} = 8.88mA		±5	%
ΔI_{OUT}	DAC to DAC Mismatch [2]	ZL = 75Ω + 30pF, I_{REF} = 4.44mA		±1	%
E_{LI}	Integral Linearity, Terminal Based [3]	ZL = 75Ω + 30pF, I_{REF} = 4.44mA		±0.5	LSB
t_R	Rise TIme [4]	ZL = 75Ω + 30pF, I_{REF} = 4.44mA		8	ns
t_{SET}	Full-Scale Setting Time [5]	ZL = 75Ω + 30pF, I_{REF} = 4.44mA		28	ns
GA	Glitch Area [6]	ZL = 75Ω + 30pF, I_{REF} = 4.44mA		200	pV-sec
C_A	DAC Output Capacitance	$\overline{BLANK}$ = Logic LOW		10	pF
$V_{\overline{BLANK}}$	Blanking Output Voltage	$\overline{BLANK}$ = Logic LOW, ZL = 75Ω + 30pF, I_{REF} = 4.44mA		±0.5	LSB
E_{OF}	Unadjusted Output Offset Error	$\overline{BLANK}$ = Logic HIGH, ZL = 75Ω + 30pF, I_{REF} = 4.44mA		±0.5	LSB

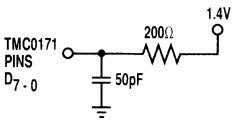
Notes:
1. Absolute gain error is defined as 100% (F.S.I_{OUT} − 2.1 • I_{REF})/2.1 • I_{REF} $V_{BLACK\ LEVEL}$ = 0V.
2. The listed value is relative to the midpoint of the full-scale distribution of the three DACs.
3. Zero and full-scale adjusted linearity error = [(V_{OUT} − V_{OFFSET}) − (DxVLSB)]/VLSB, where VLSB = ($V_{FULLSCALE}$ − V_{OFFSET})/63.
4. The rise time is measured for 10% to 90% of the full-scale transition.
5. The output signal's setting time is measured from a 2% change at the transition's initial value until it has settled to within 2% of the final value.
6. This value is determined using triangular approximation: glitch area = (area of positive transient) − (area of negative transient).

Switching characteristics within specified operating conditions

Parameter		Temperature Range: Standard – Min	– Max	–4 Min	–4 Max	–5 Min	–5 Max	–6 Min	–6 Max	–8 Min	–8 Max	Units
t_{DS}	PLCK to Valid DAC Output [1]	5	30	5	30	5	30	5	30	5	30	ns
Δt_{DS}	Differential Output Delay [2]		2		2		2		2		2	ns
t_{ENA}	Output Turn-On Delay	5		5		5		5		5		ns
t_{DIS}	Output Turn-Off Delay [3]		20		20		20		20		20	ns
t_{DO}	RD Enable Access Time		40		40		40		40		40	ns
t_{HO}	Output Hold Time	5		5		5		5		5		ns
FT_C	Clock Feedthrough [4]		–30		–30		–30		–30		–30	dB

Notes:
1. A valid analog output is defined as the 50% point between successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.
2. This applies to different analog outputs on the same device. This is a design parameter, not 100% tested.
3. Measured at ±200mV from initial steady state output voltage.
4. Reference to full-scale output.

AC Test Conditions



Input Pulse Levels	GND to 3V
Input Rise and Fall Times (10% to 90%)	2.5ns
Digital Input Timing Reference Level	1.5V
Digital Output Timing Reference Level	0.8V and 2.4V

21168A

Application Hints

Power Supply

The video DAC may draw large transient currents from the power supply. To ensure proper operation, use standard high frequency board layout techniques and power supply distribution.

The transient current required by the device dictates that the ground path impedance must be minimized by using decoupling capacitors, as shown in *Figure 14*. These capacitors' leads must be as short as possible. High-frequency decoupling is accomplished with a 0.1μF chip capacitor, C1. A bead tantalum, between 10μF to 47μF, should be used for C2.

A ground plane will minimize differential ground noise by holding the pin 14 voltage near 0 during the current transitions.

Analog Output-Line Driving

The output connections should be viewed as transmission lines. Impedance changes along these lines will reflect part of the video signal back to the DACs' outputs. To ensure good signal fidelity, RF design techniques should be observed. Any traces connecting the DAC to an onboard connector should form a transmission line of 75Ω impedance, unless the DAC's output termination resistor is placed at the output connector instead of the DAC's output pin. The coaxial cable that connects the outputs to a video monitor should have a characteristic impedance of 75Ω. Since connectors on the coaxial line can cause impedance changes, any connectors used must match the line's characteristic impedance.

The DACs use switched current sources that are summed together to generate the output current. Each 6-bit DAC consists of 63 current sources, each of

Analog Output-Line Driving (cont.)

which has a magnitude of 1/30 (I_{REF}). The digital input code determines the number of current sources that contribute to the total output current. This output current, in conjunction with a termination resistance connected between each DAC output and ground, sets the full-scale magnitude of the output voltage. There are four different methods of terminating the DAC outputs:

1. Single-Termination at the DAC (75Ω)
2. Single-Termination at the Destination (75Ω)
3. Double-Termination (37.5Ω)
4. Buffered Signal

1. Single-termination at the source places a single termination resistor at each DAC output. No other terminating load is present. Therefore, a high-input impedance monitor should be used. The AC load driven by each DAC's outputs is the transmission line impedance in parallel with the load resistor. The transmission line's impedance should match that of the load resistor. Thus, the DACs' output has an initial signal amplitude that is half the DC value expected. This half-amplitude signal is 100% reflected by the open circuit presented by the monitor input, restoring the signal amplitude to the expected value. The reflections from the monitor propogate back to the DAC output, where the load resistor presents a correctly terminated transmission line so that no further reflections occur. This arrangement is relatively tolerant of mismatches in the transmission line between the DAC and the monitor because no reflections occur at the DAC end of the transmission line. However, multiple monitors should not be connected in parallel, despite each monitor's high-input impedance.

2. Single-termination at the destination uses the termination impedance at the input of the monitor as both the load resistor for the DAC and the termination impedance of the cable (transmission line). If the connections are correctly terminated there will be no reflections. However, if there are any line impedance variations along the cable, reflections will occur and create "ghost images" on the display. This occurs because there is a reflection from the point where the mismatch occurs back to the DAC's output. The signal then reflects off the DAC's output back toward the monitor, causing an echo, or "ghosting".

3. Double-termination of the DAC outputs allows each end of the transmission line to be correctly matched. This results in the least amount of reflection and the highest signal and display fidelity. This termination method permits the fastest rise time. The DAC termination's RC time constant sets the outputs' rise time. The greater the time constant, the slower the rise time. Therefore, the rise time will be minimized since the impedance using this termination technique is less than that achieved with single-termination. With double-termination, it is necessary to increase I_{REF} to 8.8mA to ensure a full-scale output voltage of 700mV.

4. With a buffer at its outputs the DACs will be able to drive capacitive loads such as long lossy cables. A high-input impedance buffer, e.g., LM1201 or LM1203, is required. A 75Ω load is placed at the buffer's input.

   The buffer's low output impedance should be matched to the interconnecting cable with a series resistor. The cable should then be terminated with the same resistance at the monitor.

ESD Protection

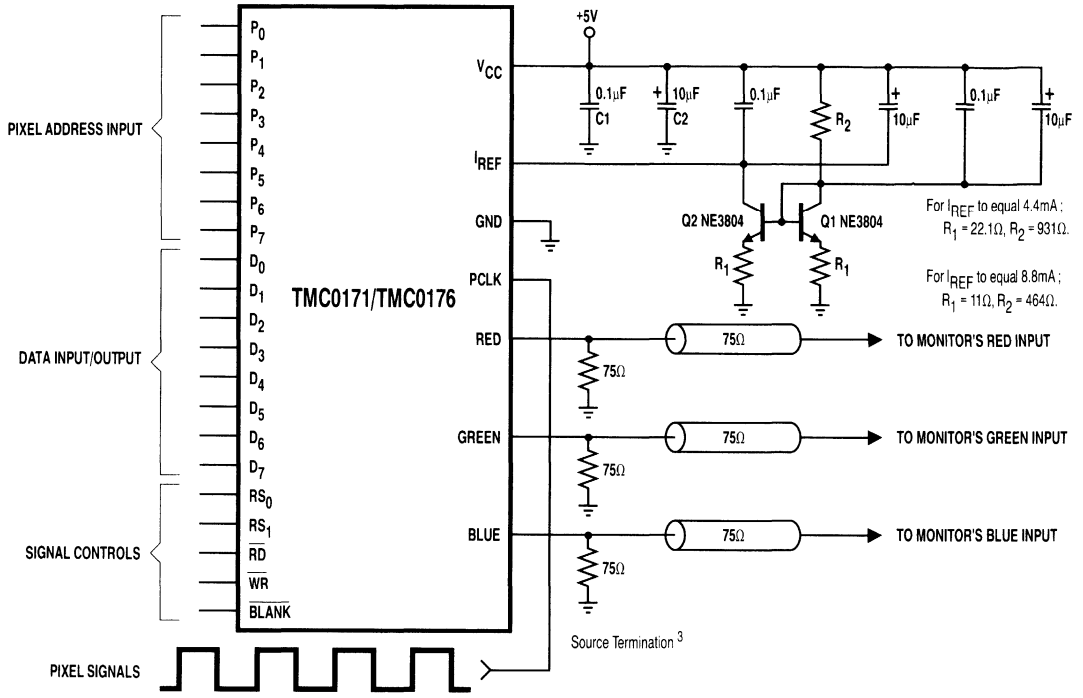
Although each pin has on-chip electrostatic discharge damage (ESD) protection, proper handling precautions during manufacturing will reduce the possibility of ESD.

Generating I_{REF}

An active I_{REF} current source will ensure that the video DAC has predictable and stable output currents. There are numerous methods available to generate the reference current. One of the simplest circuits is shown in *Figure 14*. As shown, this I_{REF} generator will sink −4.44mA (single-termination) with R1 = 22.1Ω and R2 = 931Ω.

For double-termination applications, R1 = 11Ω and R2 = 464Ω. The diode connected transistor, Q1, across Q2's base-emitter junction compensates for thermal variations to first order.

Figure 14. Typical Connection Showing I_{REF} Generator



NOTE: 1. Bead - style tantalum capacitors should be used for the 10µF devices.
2. Thermally connect the NPN transistors together.
3. For single termination, set I_{REF} to 4.44mA and use either source or destination termination resistors. For double termination, set I_{REF} to 8.88MA and use both source and destination resistors.

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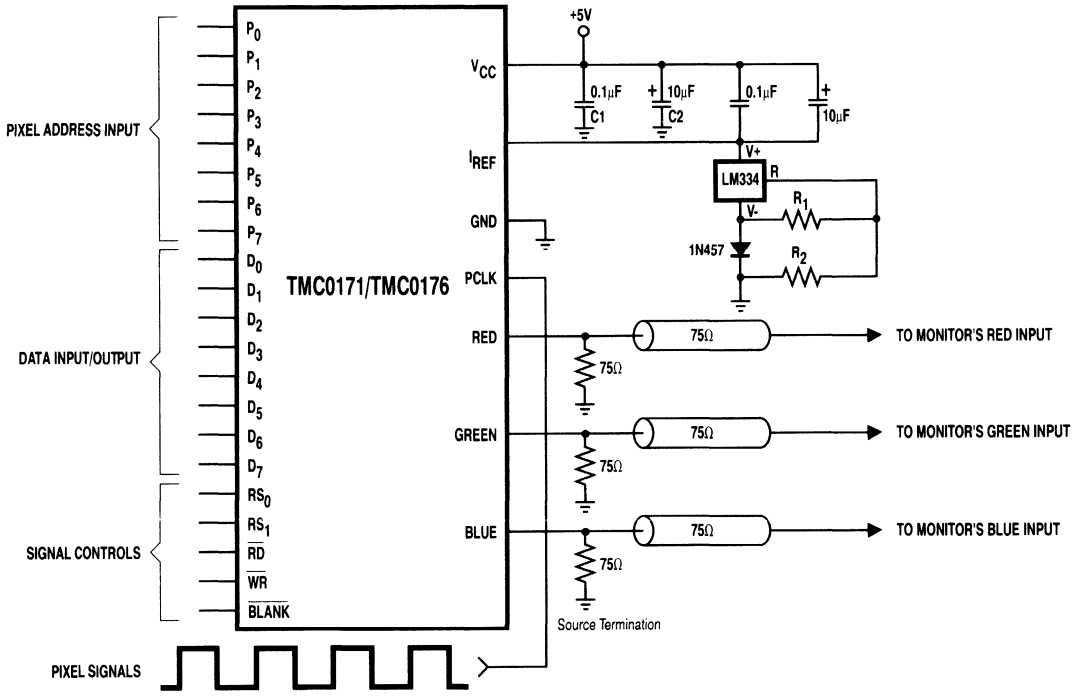
Figure 15 shows an alternative method of generating I_{REF}. The LM334 precision current source is used in a temperature compensated configuration. The reference current is set by a single resistor, R1, independent of V_{CC}. The current's value is:

$$I_{REF} = 130mV/R1$$

This current is not recommended for critical applications, particularly with double-termination.

Figure 15. Typical Connection with LM334 Current Source I_{REF} Generator



NOTE: 1. Bead - style tantalum capacitors should be used for the 10µF devices.
2. R_1 = 30Ω for I_{REF} 4.44mA;
R_2 = 10 times R_1
15Ω for I_{REF} = 8.88mA

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Figure 16 shows a TDC4611 and a discrete transistor generating a very stable I_{REF}.

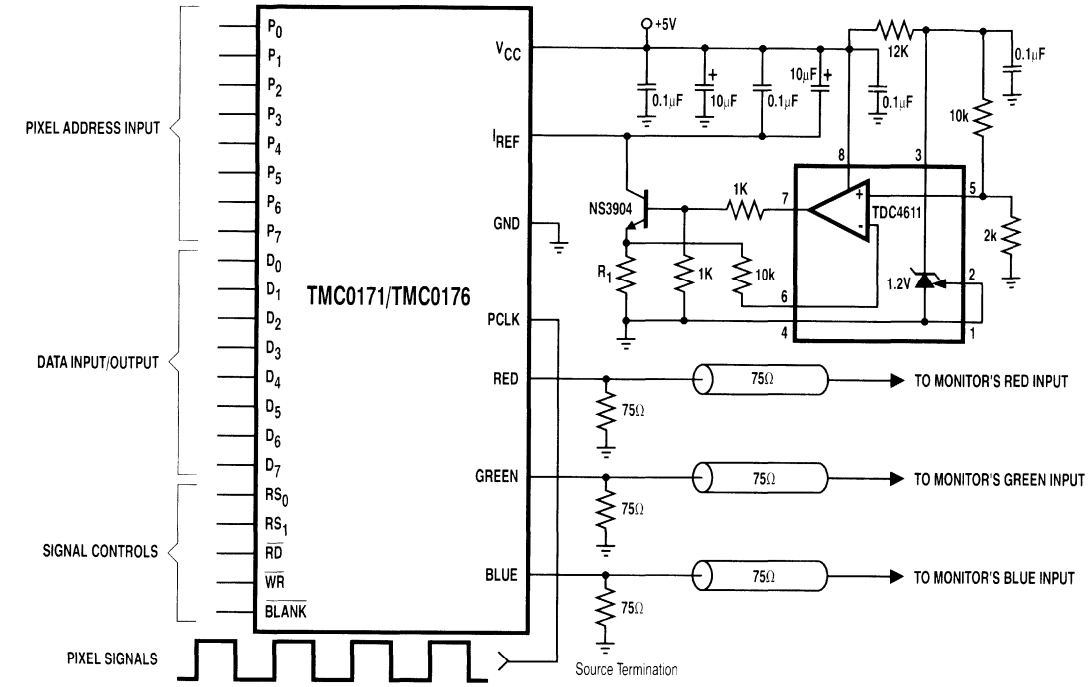
The TDC4611's on-board reference produces a nominal 1.24V. The voltage divider connected to the reference's output, pin 3, creates 200mV that is applied to R1.

Ignoring the small amount of base current, the discrete transistor's collector current (and therefore, I_{REF}) is:

$$I_{REF} = 200mV/R1$$

For $I_{REF} = 4.44mA$, R1 is, to the nearest 1% value 44.2Ω; $I_{REF} = 8.88mA$ gives an R1 of 22.1Ω.

Figure 16. Typical Connection with I_{REF} Generator Using TDC4611



Note: 1. Bead - style tantalum capacitors should be used for the 10µF devices.
2. For $I_{REF} = 4.4mA$, $R_1 = 4.42Ω$
For $I_{REF} = 8.88mA$, $R_1 = 22.1Ω$

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Decoupling I_{REF}

The DACs comprise switched current sources. Each current source is based on a current mirror that produces $(I_{REF})/30$ when active. The total output current is determined by the number of active current sources switched to the output and the magnitude of I_{REF}.

The magnitude of the current flowing through the internal current sources depends not only on I_{REF}, but also on the voltage at pin 4 relative to V_{CC}. Therefore, voltage variations between V_{CC} and the I_{REF} input can result in variations in the DAC's output current. These variations can be greatly attenuated by using a high-frequency capacitor to couple the I_{REF} input to V_{CC}. This allows the reference current input to track both high and low frequency variations in V_{CC}.

Ordering Information

Product Number	Speed (MHz)	Temperature Range	Screening	Package	Package Marking
TMC0171N6C	35	STD – T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	0171N6C
TMC0171N6C4	40	STD – T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	0171N6C4
TMC0171R2C	35	STD – T_A = 0°C to 70°C	Commercial	44 Lead Plastic J-Leaded Chip Carrier	0171R2C
TMC0176N6C4	40	STD – T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	0176N6C4
TMC0176N6C5	50	STD – T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	0176N6C5
TMC0176N6C6	66	STD – T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	0176N6C6
TMC0176N6C8	80	STD – T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	0176N6C8
TMC0176R2C4	40	STD – T_A = 0°C to 70°C	Commercial	44 Lead Plastic J-Leaded Chip Carrier	0176R2C4

TMC0458

Advance Information

Color Palette with Triple D/A Converter

8 bit, 200Msps

The TMC0458 is a 256 x 24 color palette which drives three 8-bit D/A converters to generate high-resolution analog graphics. The 5-way multiplexed data inputs permit the circuit to operate at 200Msps with TTL data input logic. A differential pseudo-ECL master clock input is provided. The device operates from a single +5V supply.

The dual-port palette can be read by the host asynchronously from the pixel clock through a standard microprocessor interface. Color overlay tables support menus, grids, cursors, and other enhancements. Bit planes may be masked or blinked. The TMC0458 is pin- and functionally-compatible with the BT458.

Fabricated in TRW's one micron OMICRON-C ™CMOS process, the TMC0458 is available in an 84 pin Plastic Leaded Chip Carrier (PLCC) or Plastic Pin Grid Array (PPGA).

Features

- Triple 8-Bit D/A Converters
- 256 Colors From A Palette Of 16.8 Million
- 200Msps Pixel Rate
- Multiplexed TTL Pixel Input
- Standard Microprocessor Interface
- RS343A-Compatible Outputs
- Single +5V Power Supply
- Monolithic
- Available In PPGA And PLCC
- Low Cost

Applications

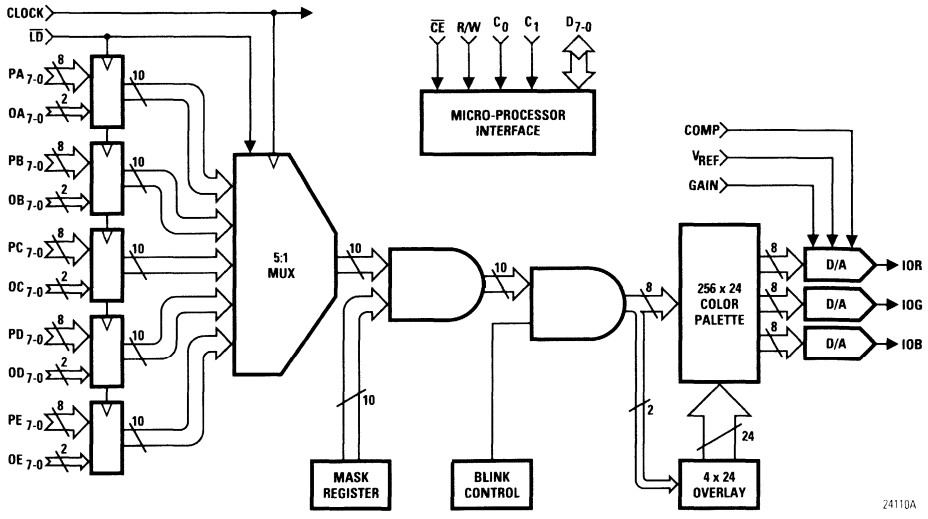
- High Resolution Graphics
- Image Processing Systems
- CAD/CAE/CAM

Associated Products

- TDC4611 Reference/Amplifier
- TMC2272 Color Space Converter

B

Simplified Block Diagram



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40G06714 Rev. A – 9/90
Printed in the U.S.A.

TDC1012

Monolithic Digital-To-Analog Converter
12-Bit, 20Msps

The TDC1012 is a TTL compatible, 12-bit monolithic D/A converter capable of converting digital data into an analog current or voltage at data rates in excess of 20 Mega-samples-per second (Msps).

The analog performance has been optimized for dynamic performance, with very low glitch energy. The dual outputs are able to drive 50Ω load with 1 Volt output levels while keeping a spurious-free-dynamic range greater than 70dB.

Data registers are incorporated on the TDC1012. This eliminates the temporal data skew encountered with external registers and latches and minimizes the glitches that can adversely affect performance in many applications.

Features

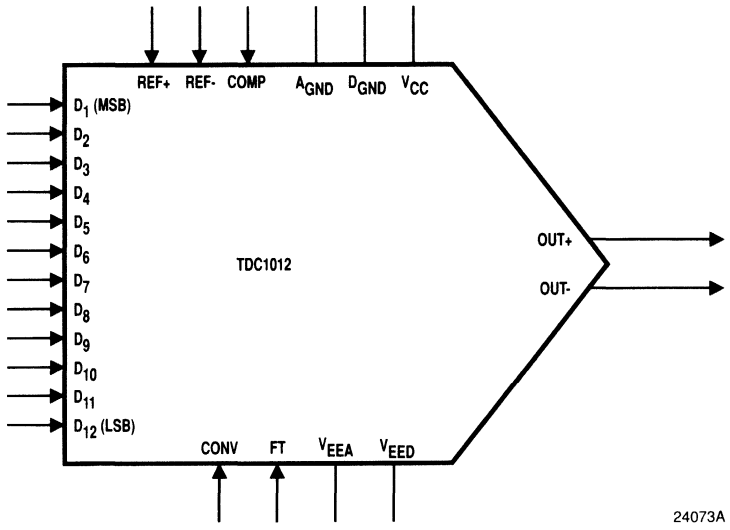
- 12-Bit Resolution
- 20 Msps Data Rate
- TTL Inputs
- Very Low Glitch With No Track And Hold Circuit Needed
- Dual +4dBm (1V Into 50Ω) Outputs Make Output Amplifiers Unnecessary In Many Applications
- 70dB Typical Spurious-Free Dynamic Range
- Available Compliant To MIL-STD-883

Applications

- Direct Digital RF Signal Generation
- Test Signal Generation
- Arbitrary Waveform Synthesis
- Broadcast And Studio Video
- High-Resolution A/D Converters

B

Interface Circuit



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40G02291 Rev. D – 9/90
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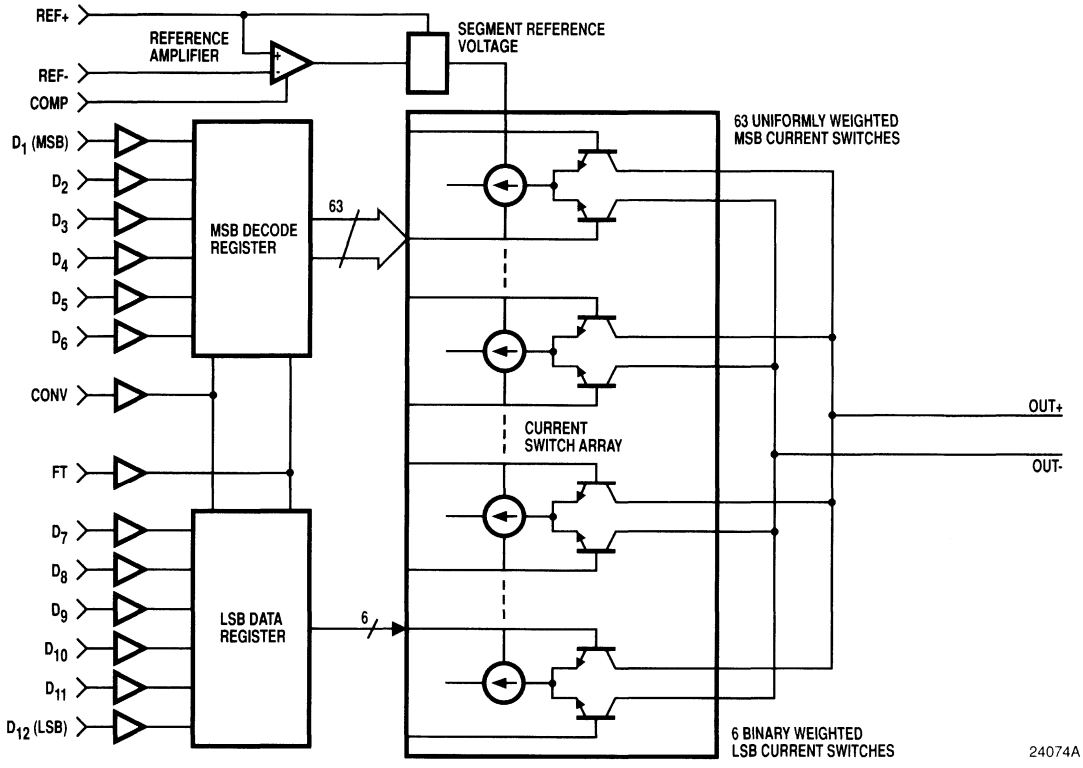
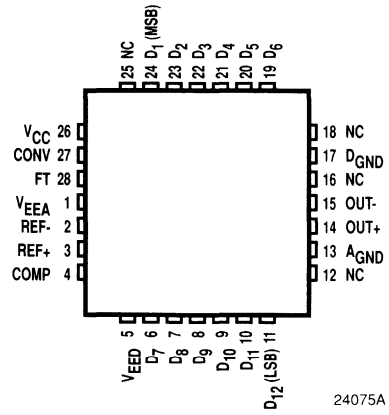
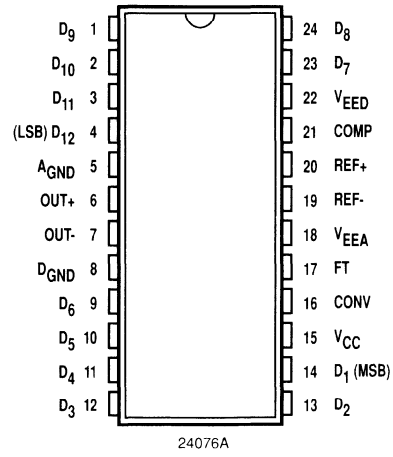
Functional Block Diagram



Pin Assignments



28 Contact Chip Carrier-C3 Package
28 Leaded Plastic Chip Carrier-R3 Package



24 Pin Hermetic Ceramic DIP-J7 Package
24 Pin Plastic DIP-N7 Package

Functional Description

General Information

The TDC1012 consists of five major circuit sections: the LSB data register, the MSB decode block, the decoded MSB register, the current switch array, and the reference amplifier. All data bits are registered just before the current switches to minimize the temporal skew that would generate glitches.

There are three major D/A architectures: segmentated, weighted current sources, and R-2R. In segmentated converters there is one current source for each possible output level. The current sources are equally weighted and for an input code of N, N current sources are turned on. An N bit segmented D/A has 2^N-1 current sources. A weighted current source D/A has one current source for each input bit, and a binary weighting for the current sources. In an R-2R D/A, there is one current source per bit and a resistor network which scales the current sources to have a binary weighting. When transitioning from a code of 011111111111 to 100000000000, both the R-2R D/A and Binary weighted D/A are turning some current sources on while turning others off. If the timing is not perfect, there is a moment where too many current sources are either on or off, resulting in a glitch. In a segmented architecture, 2047 of the current sources remain on, and one more is turned on to increment the output - no possibility of a glitch.

The TDC1012 uses an architecture with the 6 MSBs segmented and the 6 LSBs form a R-2R network. The result is a D/A converter which has very low-glitch energy, and a moderate die size.

Power, Grounds

The TDC1012 requires a –5.2V power supply and a +5.0V power supply. The analog (V_{EEA}) and digital (V_{EED}) supply voltages should be decoupled from each other, as shown in the ***Typical Interface Circuits***. The V_{CC} pin should be considered a digital power supply. The 0.1µF decoupling capacitors should be placed as close as possible to the power pins. The inductors are simple ferrite beads and are neither critical in value nor always required.

Reference

The TDC1012 has two reference inputs: REF+ and REF–. These are the inverting and noninverting inputs of the internal reference amplifier. An externally generated reference voltage is applied to the REF– pin. Current flows into the REF+ pin through an external current setting resistor (R_{REF}). This current is the reference current (I_{REF}) which serves as an internal reference for the current source array. The output current for an input code N from OUT+ is related to I_{REF} through the following relationship:

$$I_{OUT} = N \times \frac{I_{REF}}{64}$$

Where N is the value of the input code

This means that with an I_{REF} that is nominally 625µA, the full scale output is 40mA, which will drive a 50Ω load in parallel with a 50Ω transmission line (25Ω total load) with a 1V peak to peak signal. The impedance seen by the REF– and REF+ pins should be approximately equal so the effect of amplifier input bias current is minimized. The TDC1012 has been optimized to operate with a reference current of 625mA. Significantly increasing or decreasing this current may degrade the performance of the device.

The minimum and maximum values for V_{REF} and I_{REF} are listed in the table of ***Operating conditions***. The internal reference amplifier is externally compensated to assure stability. To compensate this amplifier, a 0.1µF capacitor should be connected between the COMP pin and V_{EEA}. The amplifier has been optimized to minimize the settling time, and as a result should be considered a DC amplifier. Performance of the TDC1012 operating in a multiplying D/A mode is not guaranteed.

Stable, adjustable reference circuits are shown in the *Typical Interface Circuits, 5, 6* and *7*.

Digital Inputs

The data inputs are TTL compatible. The TDC1012 is specified with two sets of setup and hold times. One of these pairs of specifications guarantees the performance of the TDC1012 to specifications listed in the ***Minimum*** and ***Maximum*** columns of the ***System performance characteristics*** table.

The second more rigid specification is recommended for applications where lowest possible glitch and highest SFDR are desired. The more stringent t_S and t_H ensure that the data will not be slewing during times critical to the TDC1012, and will minimize the effects of capacitively coupled data feedthrough and optimize SFDR performance.

Another method for reducing the effect of capacitive coupling is to slow down the slew rates of the digital inputs. This has been done in the circuit shown in the *Typical Interface Circuits* by the addition of 50Ω series resistors to the data lines.

Clock and Feedthrough Control

The TDC1012 requires a TTL clock signal (CONV) Data is synchronously entered on the rising edge of CONV. The CONV input is ignored in the Feedthrough (FT = HIGH) mode. The Feedthrough (FT) pin is normally held LOW, where the TDC1012 operates in a clocked mode (the output changes only after a clock rising edge). An internal pull-down resistor is provided,and this pin may be left open for clocked operation.

For certain applications, such as high-precision successive approximation A/D converters, throughput delay may be more important then glitch performance. In these cases, the FT pin may be brought HIGH, which makes the input registers transparent. This allows the analog output to change immediately and asynchronously in response to the digital inputs.

Since skew in the bits of the input word will result in glitches, and will affect settling time, it is recommended that the TDC1012 be operated in clocked mode for most applications.

Analog Outputs

Two simultaneous and complementary analog outputs are provided. Both of these outputs are full-power current sources. By driving the current source outputs into a resistive load, they may be used as voltage outputs. OUT+ provides a 0 to –40mA output current (0 to –1V when terminated in 25Ω) as the input code varies from 0000 0000 0000 to 1111 1111 1111. OUT– varies in a complementary manner from –40 to 0mA (–1 to 0V when terminated with 25Ω) over the same code range. (See the *Input Coding Table*.)

The output current is proportional to the reference current and the input code. The recommended output termination is 25Ω. This can be provided by placing a 50Ω source resistor between the output pin and ground, then driving a terminated 50Ω transmission line. With this load, the output voltage range of the converter is 0 to –1.0V.

If a load is capacitively coupled to the TDC1012, it is recommended that a 25Ω load at DC, as seen by the TDC1012, continue to be maintained. The output voltage should be kept within the output compliance voltage range, V_{OC}, as specified in the *Electrical characteristics table*, or the accuracy may be impaired.

Package Interconnections

Signal Type	Signal Name	Function	Value	J7 & N7 Package Pins	C3 & R3 Package Pins
Power	V_{CC}	Digital Supply Voltage	+5.0V	15	26
	A_{GND}	Analog Ground	0.0V	5	13
	D_{GND}	Digital Ground	0.0V	8	17
	V_{EEA}	Analog Supply Voltage	–5.2V	18	1
	V_{EED}	Digital Supply Voltage	–5.2V	22	5
Reference	REF–	Reference Voltage Input	–1.0V	19	2
	REF+	Reference Current Input	–625µA	20	3
	COMP	Compensation Capacitor	0.1µF, see text	21	4
Data Inputs	D_1 (MSB)	Most Significant Bit	TTL	14	24
	D_2		TTL	13	23
	D_3		TTL	12	22
	D_4		TTL	11	21
	D_5		TTL	10	20
	D_6		TTL	9	19
	D_7		TTL	23	6
	D_8		TTL	24	7
	D_9		TTL	1	8
	D_{10}		TTL	2	9
	D_{11}		TTL	3	10
	D_{12} (LSB)	Least Significant Bit	TTL	4	11
Feedthrough	FT	Feedthrough Mode Control	TTL	17	28
Convert	CONV	Convert (Clock) Input	TTL	16	27
Analog Output	OUT+	Analog Output	0 to 40mA	6	14
	OUT–	Analog Output	40 to 0mA	7	15

Input Coding Table[1]

Input Data MSB LSB	OUT+ (mA)	V_{OUT+}(mV)	OUT– (mA)	V_{OUT-}(mV)
0000 0000 0000	0.000	0.00	40.000	–1000.00
0000 0000 0001	0.009	–0.24	39.990	–999.75
0000 0000 0010	0.019	–0.49	39.980	–999.52
	•	•	•	•
	•	•	•	•
	•	•	•	•
	•	•	•	•
0111 1111 1111	19.995	–499.88	20.005	–500.12
1000 0000 0000	20.005	–500.12	19.995	–499.88
	•	•	•	•
	•	•	•	•
	•	•	•	•
1111 1111 1101	39.980	–999.52	0.019	–0.49
1111 1111 1110	39.990	–999.75	0.009	–0.24
1111 1111 1111	40.000	–1000.00	0.000	0.0

Note: 1. I_{REF} = 625µA, R_{LOAD} = 25Ω

Figure 1. Timing Diagram

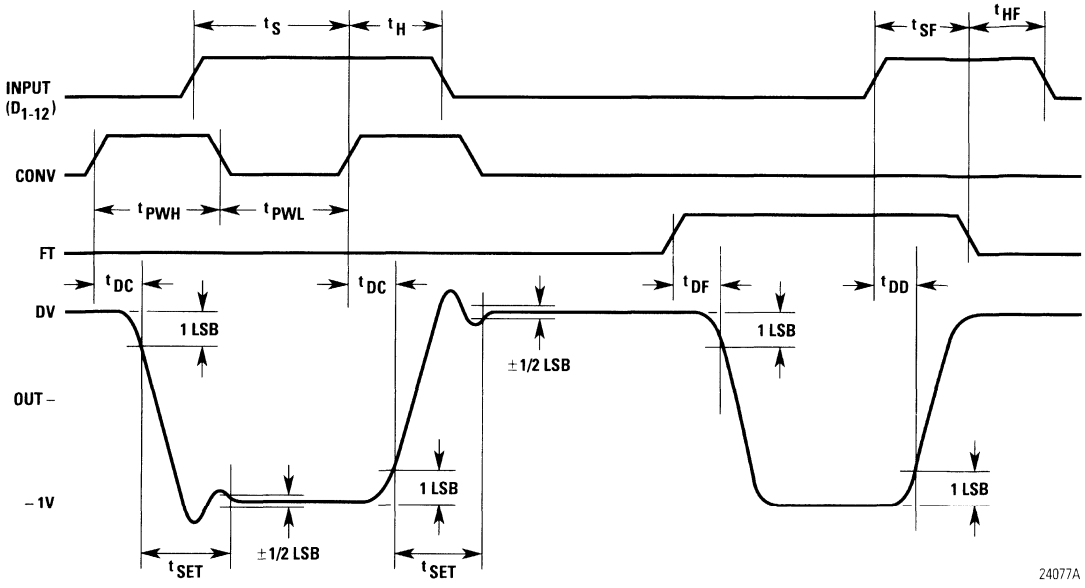


Figure 2. Equivalent Input Circuits

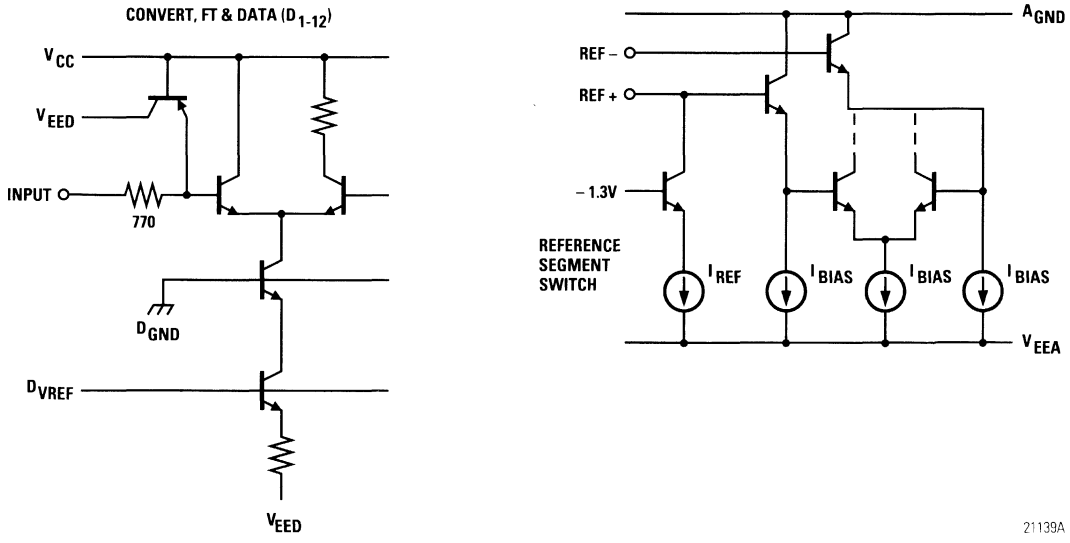


Figure 3. Equivalent Reference and Output Circuits

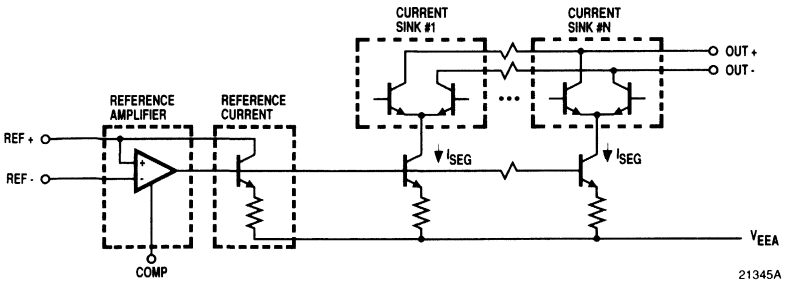
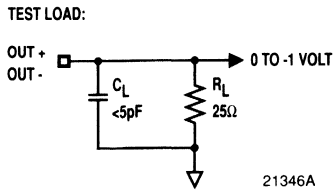


Figure 4. Output Test Load



B

Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltages

V_{CC}	(Measured to D_{GND})	–0.5 to +7.0V
V_{EEA}	(Measured to A_{GND})	–7.0 to +0.5V
V_{EEA}	(Measured to V_{EED})	–50 to +50mV
V_{EED}	(Measured to D_{GND})	–7.0 to +0.5V
A_{GND}	(Measured to D_{GND})	–0.5 to +0.5V

Inputs

CONV, FT, D_{1-12} (Measured to D_{GND})[2]	V_{CC} +0.5 to –0.5V
CONV, FT, D_{1-12} Current, Externally Forced[3]	±3mA
REF+, REF–, Applied Voltage (Measured to A_{GND})[3]	V_{EEA} to +0V
REF+, REF–, Current, Externally Forced[3]	±3mA

Outputs

OUT+, OUT–, Applied Voltage (Measured to A_{GND})[2]	–2.0 to +2.0V
OUT+, OUT–, Current, Externally Forced[3]	+50mA
Short-Circuit Duration (Single Output to GND)	unlimited

Temperature

Operating, Ambient	
(Plastic Package)	–20 to +90°C
(Ceramic Package)	–60 to +150°C
Junction	
(Plastic Package)	+140°C
(Ceramic Package)	+200°C
Lead, soldering (10 seconds)	+300°C
Storage	–65 to +150°C

Note: 1. Absolute maximum ratings are limited values applied individually while other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.

2. Applied voltage must be current limited to specified range.

3. Forcing voltage must be limited to specified range. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Positive Supply Voltage (Measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EED}	Negative Supply Voltage (Measured to D_{GND})	–4.9	–5.2	–5.5	–4.9	–5.2	–5.5	V
V_{EEA}	Negative Supply Voltage (Measured to A_{GND})	–4.9	–5.2	–5.5	–4.9	–5.2	–5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	–0.1	0.0	0.1	–0.1	0.0	0.1	V
V_{EEA}	Negative Supply Voltage (Measured to V_{EED})	–20	0	20	–20	0	20	mV
t_{PWL}	CONV Pulse Width LOW (to Meet Specification)	20			20			ns
t_{PWL}	CONV Pulse Width LOW (to Optimize SFDR)	20			20			ns
t_{PWH}	CONV Pulse Width HIGH (to Meet Specifications)	20			20			ns
t_{PWH}	CONV Pulse Width HIGH (to Optimize SFDR)	20			20			ns
t_S	Setup Time, Data to CONV (to Meet Specification)	25			25			ns
t_S	Setup Time, Data to CONV (to Optimize SFDR)	32			36			ns
t_H	Hold Time (to Meet Specifications)	1			1			ns
t_H	Hold Time (to Optimize SFDR)	4			6			ns
t_{SF}	Setup Time, Data to FT	5			7			ns
t_{HF}	Hold Time, Data to FT	28			32			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
V_{REF}	Reference Voltage (REF–)	–0.7	–1.0	–1.3	–0.7	–1.0	–1.3	V
I_{REF}	Reference Current (REF+)	550	625	700	575	625	675	µA
C_C	Compensation Capacitor	0.01	0.1			0.01	0.1	µF
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				–55		125	°C

Notes: 1. A common power supply isolated with ferrite bead inductors is recommended for V_{EEA} and V_{EED}. This is shown in the *Typical Interface Circuits*.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
$I_{EEA}+I_{EED}$		$V_{EEA}=V_{EED}$=Max,static					
		T_A=0 to 70°C		−180			mA
		T_A=70°C		−150			mA
		T_C=−55 to 125°C				−200	mA
		T_C=125°C				−150	mA
I_{CC}		V_{CC}=Max, Static		25			mA
		T_A=0 to 70°C					
		T_A=70°C		20			mA
		T_C=−55 to 125°C				35	mA
		T_C=125°C				24	mA
C_{REF}	Reference Input Capacitance			15		15	pF
C_I	Digital Input Capacitance			15		15	pF
V_{OC}	Compliance Voltage		−1.2	1.2	−1.2	1.2	V
R_O	Output Resistance		12		12		kΩ
C_O	Output Capacitance			45		45	pF
I_O	Full Scale Output Current	I_{REF}=Nominal	40		40		mA
I_{IL}	Input Current, Logic LOW	V_{CC}, V_{EE}=Max , V_I=0.4V	−10	50	−10	50	µA
I_{IH}	Input Current, Logic HIGH	V_{CC}, V_{EE}=Max, V_I=2.4V	−10	100	−10	100	µA
I_{IM}	Input Current, Max Input Voltage	V_{CC}, V_{EE}=Max, V_I=V_{CC} Max	−10	100	−10	100	µA
V_{TH}	Logic Input Threshold Voltage,Typical	V_{CC}, V_{EE}=Nom, T_A=25°C	1.25	1.55	1.25	1.55	V

Switching characteristics

Parameter		Test Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Typ	Max	Min	Typ	Max	
F_D	Maximum Data Rate	V_{EEA}, V_{EED}, V_{CC} = Min	20	25		20	23		MHz
t_{DC}	Clock to Output Delay	V_{EEA}, V_{EED}, V_{CC} = Min, F T =LOW			17			20	ns
t_{DD}	Data to Output Delay	V_{EEA}, V_{EED}, V_{CC} = Min, FT = HIGH			35			40	ns
t_{DF}	FT to Output Delay	V_{EEA}, V_{EED}, V_{CC} = Min			35			40	ns
t_R	Risetime	90% to 10% of FSR, FT = LOW			4			4	ns
t_F	Falltime	10% to 90% of FSR, FT = LOW			4			4	ns
t_{SET}	Settling Time, Voltage	FT = LOW, Full-Scale Voltage Transition on I_{OUT} to ±0.0188% FSR		20	30		20	35	ns

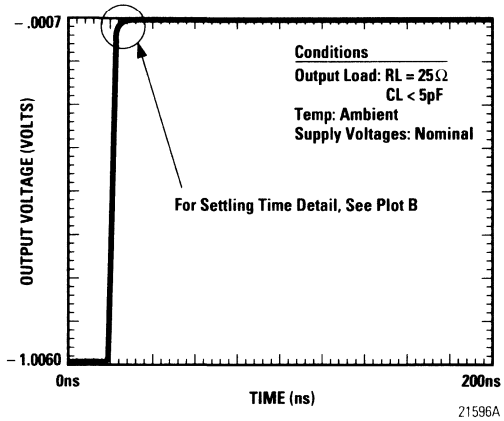
System performance characteristics

Parameter		Test Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Typ	Max	Min	Typ	Max	
E_{LD}	Differential Linearity Error	V_{EEA}, V_{EED}, V_{CC}, I_{REF}= Nom[1]			±0.012			±0.012	%
		TDC1012XXY3							
		TDC1012XXY2			±0.024			±0.024	%
		TDC1012XXY1			±0.048			±0.048	%
E_{LI}	Integral Linearity Error	V_{EEA}, V_{EED}, V_{CC}, I_{REF}= Nom[1]			±0.024			±0.024	%
		TDC1012XXY3							
		TDC1012XXY2			±0.048			±0.048	%
		TDC1012XXY1			±0.048			±0.048	%
V_{OS}	REF+ to REF– Offset Voltage		–10		+10	–10		+10	mV
I_B	REF– Input Bias Current				5			10	µA
E_G	Absolute Gain Error	V_{EEA}, V_{EED}, V_{CC}, I_{REF}= Nom	–5		5	–5		5	%
I_{OF}	Output Offset Current	V_{EEA}, V_{EED}, V_{CC}= Min, D_{1-12}=LOW	–5		+5	–5		+5	µA
PSRR	Power Supply Rejection Ratio	V_{EEA}, V_{EED}, V_{CC}, I_{REF}= Nom[2]			–50			–48	dB
PSS	Power Supply Sensitivity	V_{CC}, V_{EEA}, V_{EED}=4%, I_{REF}= Nom			–140			–140	µA/V
G_A	Peak Glitch Area			25	45		25	45	pV–sec
SFDR	Spurious Free Dynamic Range	I_{REF}=Nom, 20Msps, 10MHz bandwidth F_{out}=6MHz	60			60			dBc
		F_{out}=5MHz		70					dBc
		F_{out}=2MHz		75					dBc
		F_{out}=1MHz		78					dBc

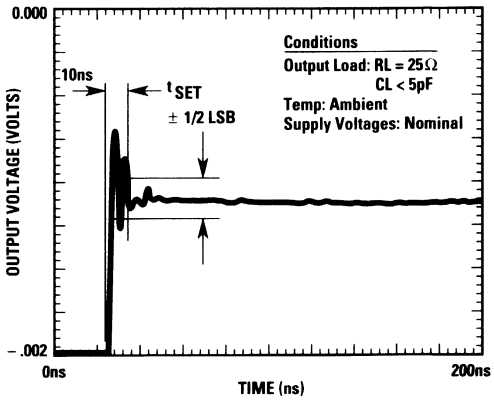
Notes: 1. OUT– connected to A_{GND}, OUT– driving virtual ground.
2. 120Hz, 600mV p-p ripple on V_{EE} and V_{CC}.

Typical Performance Curves (Typical Settling Time Characteristics)

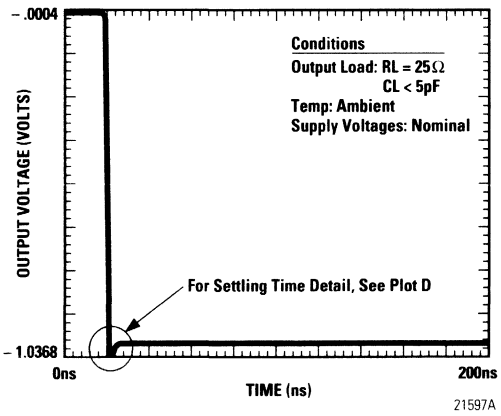
A. Full-Scale Output Transition, Rising Edge



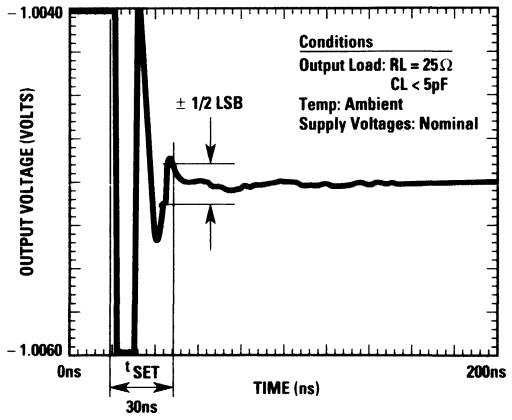
B. Settling Time, Full-Scale Output, Rising Edge



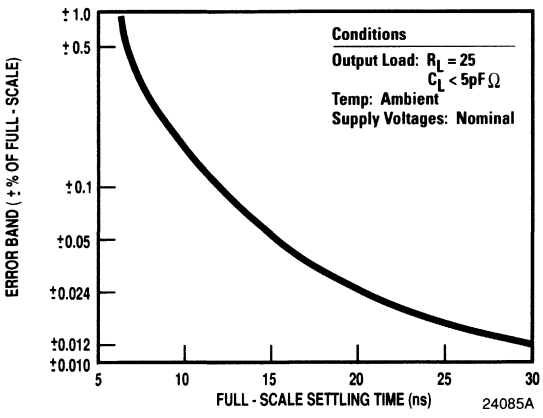
C. Full-Scale Output Transition, Falling Edge



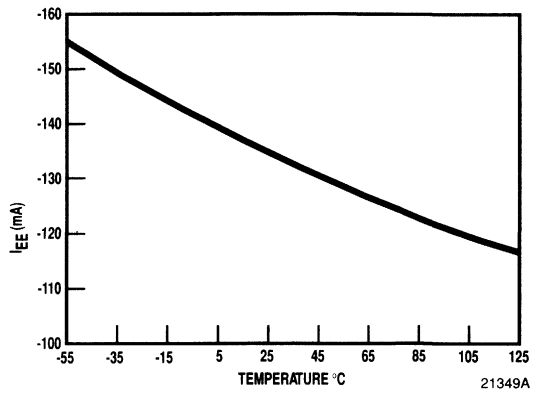
D. Settling Time, Full-Scale Output, Falling Edge



E. Typical Settling Time vs. Settling Accuracy



F. Typical Supply Current vs. Temperature



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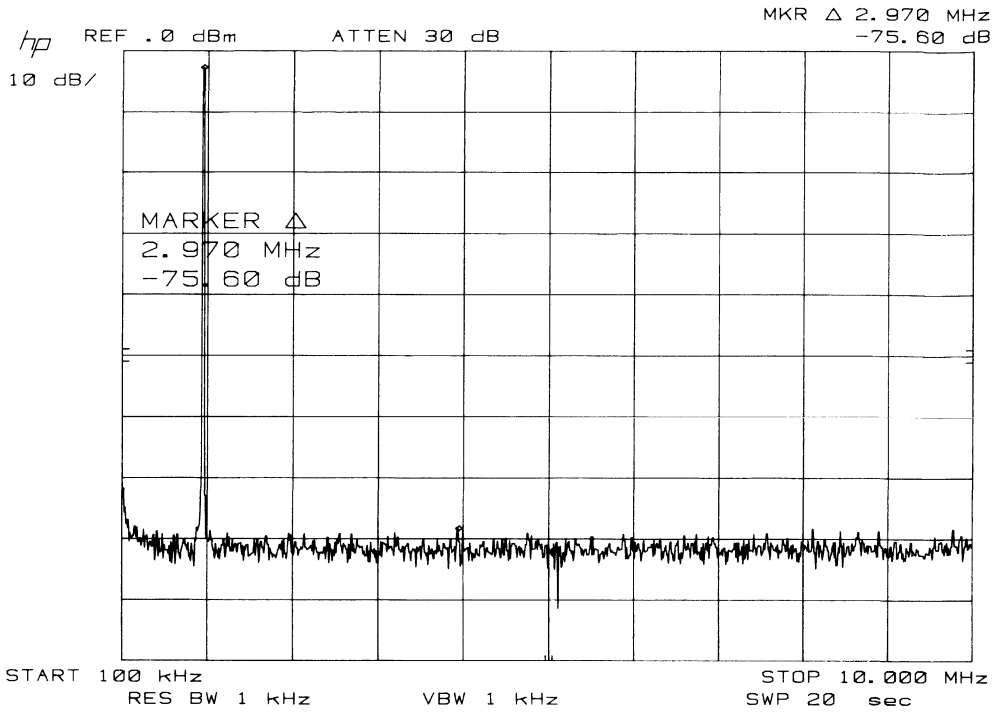
G. Typical Output Spectrum 20Msps 1MHz F_{OUT}



Applications Discussion

The TDC1012 is a high performance D/A converter. To get the best possible performance requires careful attention to the details of circuit design and layout.

Layout

The layout of grounds in any system is an important design consideration. Separate analog and digital grounds are provided at the TDC1012. All ground pins should be connected to a common low-noise, low-impedance groundplane. This groundplane should be common for the TDC1012 and all of its immediate interface circuitry, which includes all of the reference circuitry, the output load circuitry, and all of the power supply decoupling components.

The digital driving logic should use a separate system ground, and this ground should be connected to the analog groundplane in only one place. The analog and digital grounds may be connected in other ways if required by the user's system grounding plan, however, the voltage differential between the A_{GND} and D_{GND} pins must be held to within ±0.1 Volts.

The high slew-rates of digital data make capacitive coupling with the D/A output a potential problem. Since the digital signals contain high-frequency harmonics of the clock, as well as the signal that is being provided to the TDC1012, the result of data feedthrough often looks like harmonic distortion which degrades the Spurious-Free-Dynamic-Range (SFDR) performance of the D/A. Capacitive coupling can be minimized by keeping digital lines physically away from the analog output and reference. Another technique that can reduce capacitive data coupling is to use low slew rate digital drive circuits or slowing the driving edges with series resistors.

Direct Digital Synthesis Applications

For most synthesis applications, optimum signal purity is obtained with the use of a balun (a simple RF transformer made by wrapping a few turns of wire around a ferrite core) as shown in *Figure 5*. This configuration has the benefit of canceling common mode distortion. An output

amplifier is not recommended because any amplifier will add distortion, which is likely to be much greater than that present from the outputs of the TDC1012.

The strict adherence to at least the minimum input data setup and hold times is important for the realization of the optimal performance. Spur levels may decrease as setup and hold times are increased. It is possible to achieve even higher performance in some instances by carefully "tuning" the input data setup and hold times (slightly delaying or advancing the CONV signal in relation to the data) provided to the TDC1012. The ***Operating conditions*** table has two sets of data for t_S and t_H, one which guarantees performance of the device in most applications, and one, more conservative specification, which has been found to be optimal for DDS applications.

The actual digital-data waveform which represents a sinewave contains strong harmonics of that fundamental frequency. This can be seen by connecting a digital data line to the input of a spectrum analyzer. Data feedthrough to the analog output of a system due to improper board layout or system shielding and grounding will appear as additional harmonic distortion, adversely affecting SFDR.

Harmonic distortion may improve even further with reduced AC termination impedance values, at the expense of lowered output voltage. This is achieved by a balun used as an impedance transformer as shown in ***Figure 5***.

The purity of the output of the TDC1012 is greater than that which can be measured by many spectrum analyzers. The spectral plots shown in this data sheet were generated with an HP8568B, which has a noise floor just below that of the TDC1012. When making spectral measurements it is important to remember that the TDC1012 output power is +4dBm, which is greater power than many analyzers are equipped to handle without adding distortion of their own. Accordingly, it may be necessary to introduce an attenuator to the input of the spectrum analyzer.

The CONV signal provided to the TDC1012 must be as free from clock jitter as possible. Clock jitter is the random cycle-to-cycle variation in clock period. CONV clock jitter will effectively appear at the output as phase noise. A value of 10ps or less for clock jitter is recommended for the highest performance applications. Ordinary crystal oscillators are satisfactory. High-performance synthesizers, such as the HP8662, used to trigger a precision pulse generator, are also satisfactory.

The TMC2340 direct digital synthesizer is ideal for generating a digital sinusoid for the D/A converter. The TMC2340 automatically generates a carrier frequency which may then be digitally phase, frequency or amplitude modulated. Two outputs are provided which are 90° out of phase (quadrature outputs). For more information on direct digital synthesis, and other applications of the TDC1012, please see application note ***TP46*** and ***AB-8*** from TRW LSI Products.

Bipolar Output

See ***Figure 6*** for a suggested circuit for achieving a bipolar output voltage range. Optimum DC linearity is obtained by using a differential output, either with a balun or an operational amplifier in the differential mode. If it is desired that the TDC1012 be operated in a single-ended fashion, the unused output should be connected directly to ground as is shown in ***Figure 7***.

Figure 5. Typical Interface Circuit with Balum Output

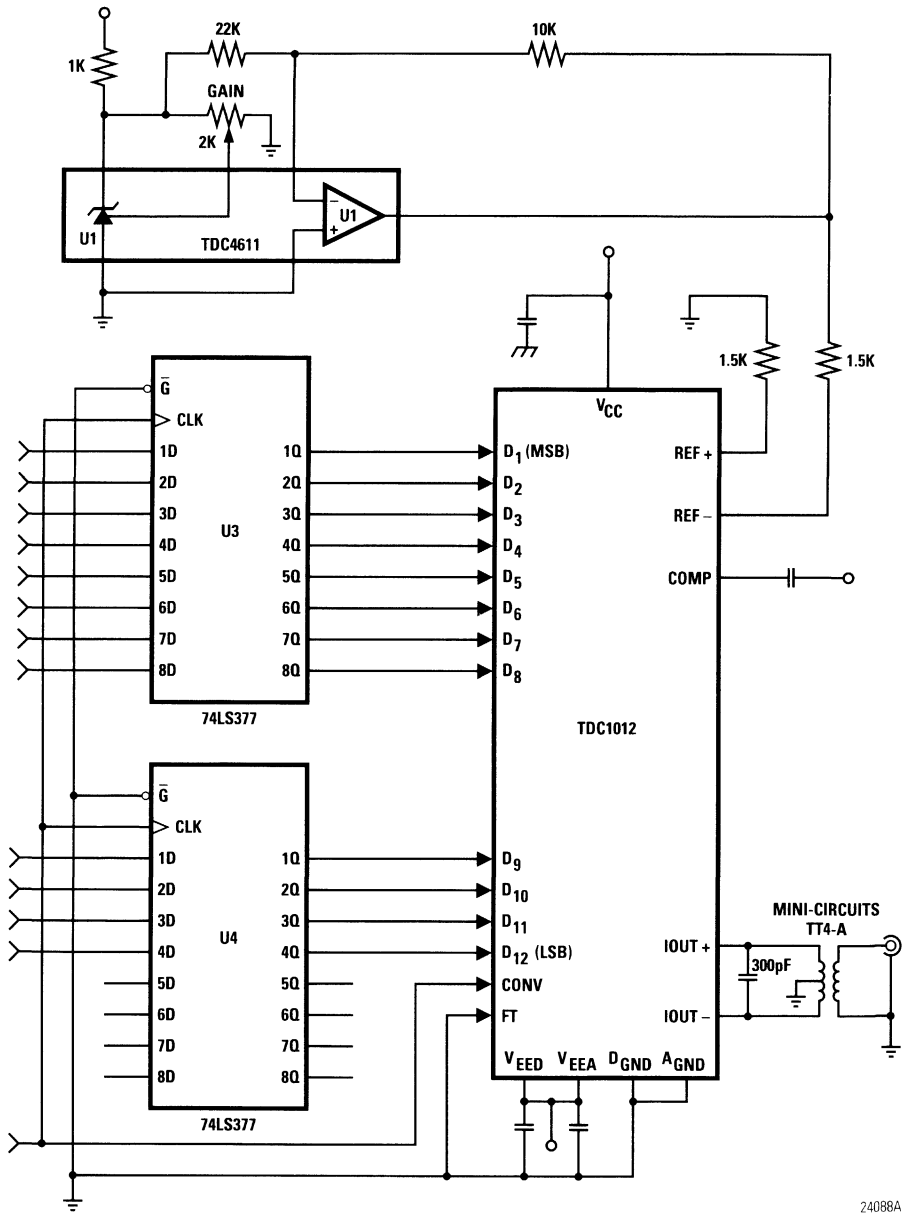


Figure 6. Typical Interface Circuit with Differential Amplifier Output

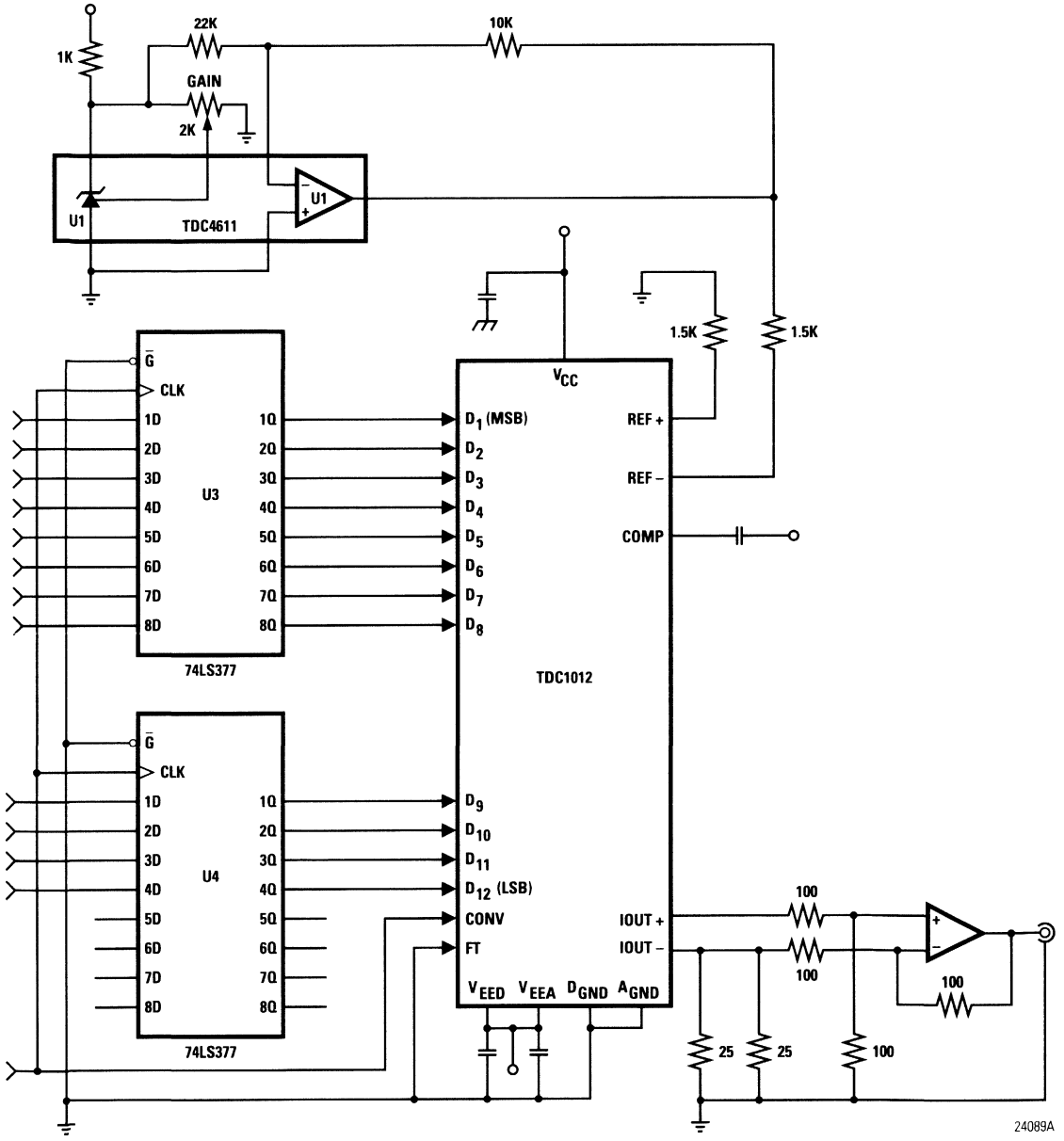
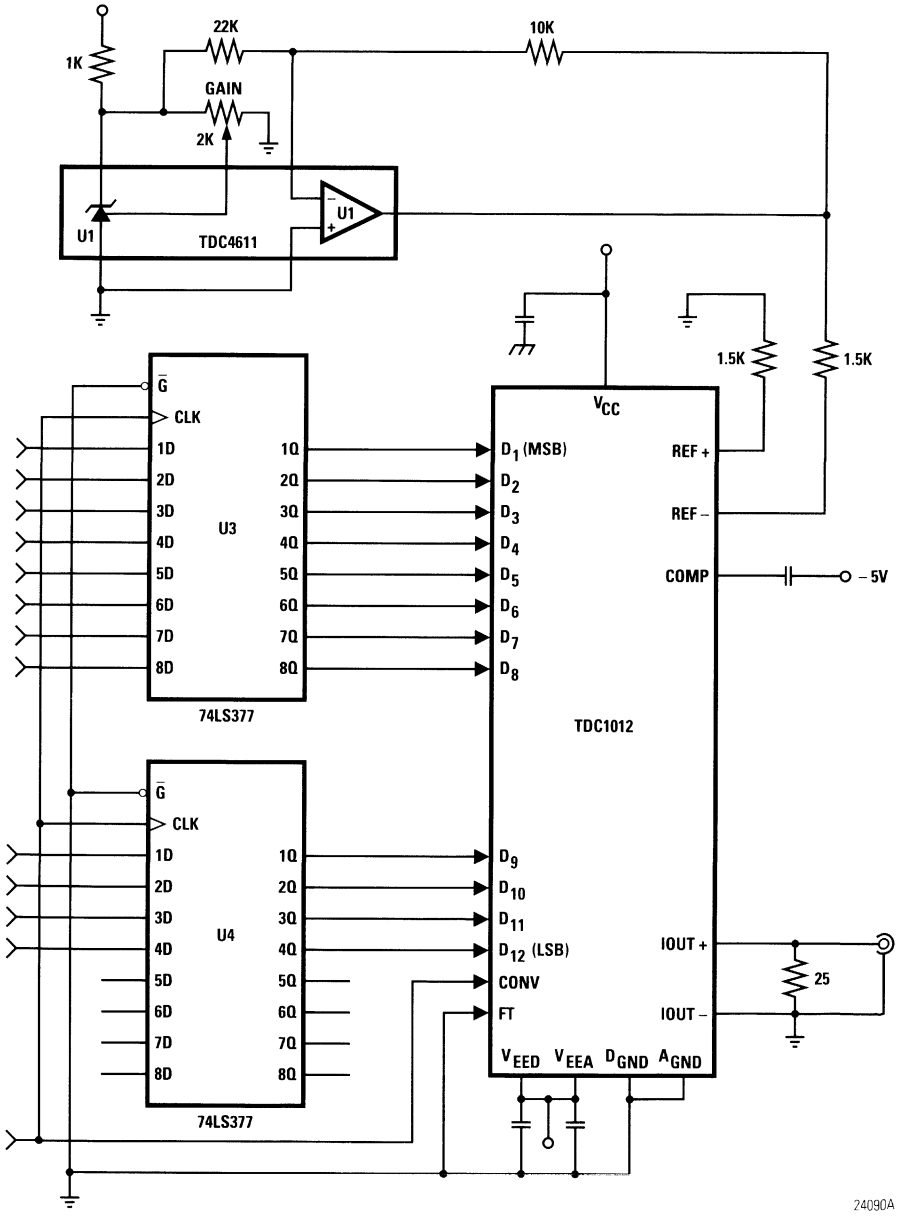


Figure 7. Typical Interface Circuit with Resistive Load Output



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1012N7CX	T_A=0°C to 70°C	Commercial	Plastic DIP	1012N7C-X
TDC1012J7CX	T_A=0°C to 70°C	Commercial	Ceramic DIP	1012J7C-X
TDC1012J7VX	T_C=−55°C to 125°C	MIL-STD-883	Ceramic DIP	1012J7V-X
TDC1012R3CX	T_A=0°C to 70°C	Commercial	Plastic Chip Carrier	1012R3C-X
TDC1012C3VX	T_C−55°C to 125°C	MIL-STD-883	Ceramic Chip Carrier	1012C3V-X

Linearity Grade (X)		None	1	2	3
E_{LD}	Linearity Error, Differential	±0.096% (4 LSB)	±0.048% (2 LSB)	±0.024% (1 LSB)	±0.012% (1/2 LSB)
E_{LI}	Linearity Error, Integral	±0.096% (4 LSB)	±0.048% (2 LSB)	±0.048% (2 LSB)	±0.024% (1 LSB)

B

All parameters contained in this specification are guaranteed by design, characterization, sample testing or 100% testing as appropriate. TRW reserves the right to change products and specifications without notice. This information does not convey any license under patent rights of TRW Inc. or others.

Life Support Policy

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I_{REF} =625A, R_{LOAD} = 25Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.Applied voltage must be current limited to specified range.Forcing Voltage must be limited to specified range. Current is specified as conventional current flowing into the device.

TDC1016

Video Speed D/A Converter
10-Bit, 20Msps

The TDC1016 is a bipolar monolithic digital-to-analog converter which can convert digital data into an analog voltage at rates up to 20Msps (Megasamples Per Second). The device includes an input data register and operates without an external deglitcher or amplifier.

Operating the TDC1016 from a single −5.2V power supply will bias the digital inputs for ECL levels, while operating from a dual ±5V power supply will bias the digital inputs for TTL levels.

All versions of the TDC1016 are 10-bit digital-to-analog converters, but are available with linearity specifications of either 8, 9, or 10 bits. The TDC1016 is patented under U.S. patent number 3283120 with other patents pending.

Features

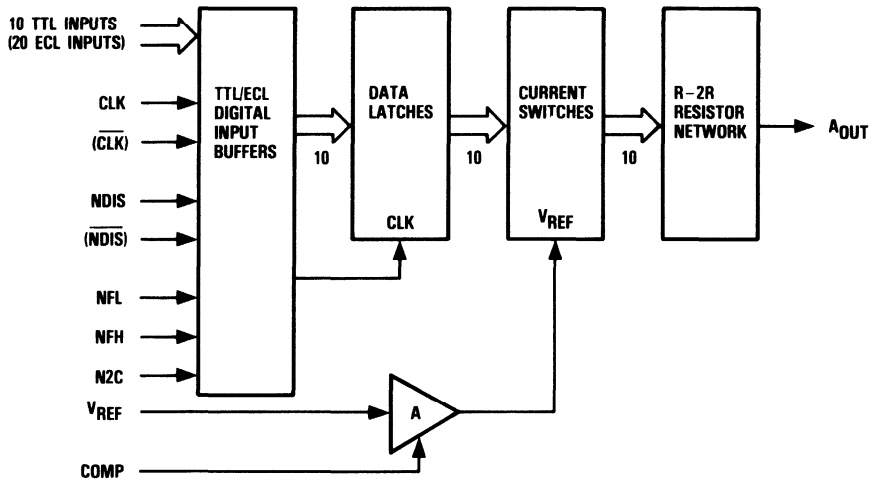
- 20Msps Conversion Rate
- 8, 9, Or 10-Bit Linearity
- Voltage Output, No Amplifier Required
- Single Supply Operation (−5.2V, ECL Compatible)
- Dual Supply Operation (±5.0V, TTL Compatible)
- Internal 10-Bit Latched Data Register
- Low Glitch Energy
- Disabling Controls, Forcing Full-Scale, Zero, And Inverting Input Data
- Binary Or Two's Complement Input Data Formats
- Differential Gain = 1.5%, Differential Phase = 1.0°

Applications

- Construction Of Video Signals From Digital Data 3x Or 4x NTSC Or PAL Color Subcarrier Frequency
- CRT Graphics Displays, RBG, Raster, Vector
- Waveform Synthesis

B

Functional Block Diagram



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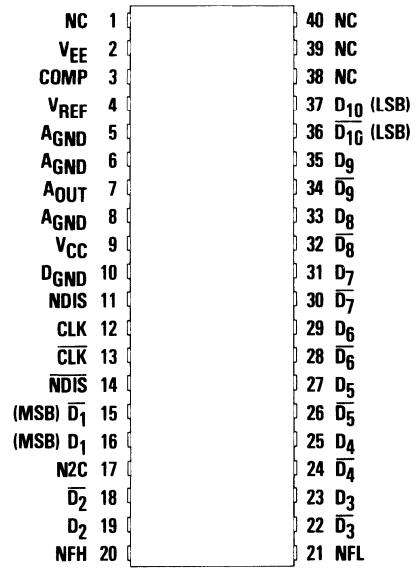
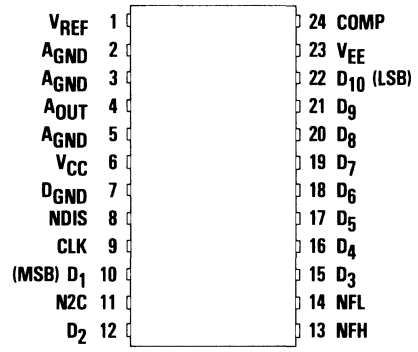
Printed in the U.S.A.

Pin Assignments



40 Pin CERDIP – B5 Package



24 Pin CERDIP – B7 Package

Functional Description

General Information

TTL/ECL buffers are used for all digital inputs to the TDC1016. Logic family compatibility depends upon the connection of power supplies. When single power supply (−5.2V) operation is employed, all data, clock, and disable inputs are compatible with differential ECL logic levels. All digital inputs become compatible with TTL levels when dual power supply (±5.0V) operation is used.

The internal 10-bit register latches data on the rising edge of the clock (CLK) pulse. Currents from the current sources are switched accordingly and combined in the resistor network to give an analog output voltage. The magnitude of the output voltage is directly proportional to the magnitude of the digital input word.

The NFL and NFH inputs can be used to simplify system calibration by forcing the analog output voltage to either its zero-scale or full-scale value. The TDC1016 can be operated in binary, inverse binary, two's complement, or inverse two's complement input data formats.

Power

The TDC1016 can be operated from a single −5.2V power supply or from a dual ±5.0V power supply. For single power supply operation, V_{CC} is connected to D_{GND} and all inputs to the device become ECL compatible. When V_{CC} is tied to +5.0V, the inputs are TTL compatible.

The return path for the output from the 10 current sources is A_{GND}. The current return path for the digital section is D_{GND}. D_{GND} and A_{GND} should be returned to system power supply ground by way of separate conductive paths to prevent digital ground noise from disturbing the analog circuitry of the TDC1016. All A_{GND} pins must be connected to system analog ground.

Reference

The reference input is normally set to −1.0V with respect to A_{GND}. Adjusting this voltage is equivalent to adjusting system gain. The temperature stability of the TDC1016 analog output (A_{OUT}) depends primarily upon the temperature stability of the applied reference voltage.

Reference (cont.)

The internal operational amplifier of the TDC1016 is frequency stabilized by an external 1 microfarad tantalum capacitor connected between the COMP pin and V_{EE}. A minimum of 1 microfarad is adequate for most applications, but 10 microfarads or more is recommended for optimum performance. The negative side of this capacitor should be connected to V_{EE}.

Controls

The NDIS inputs are used to disable the TDC1016 by forcing its output to the zero-scale value (current sources off). The NDIS inputs are asynchronous, active without regard to the CLK inputs. The other digital control inputs are synchronous, latched on the rising edge of the CLK pulse.

The rising edge of the CLK pulse transfers data from the input lines to the internal 10-bit register. In TTL mode, the inverted inputs for CLK, DATA, and NDIS are inactive and should be left open.

The *Input Coding Table* illustrates the function of the digital control inputs. A two's complement mode is created by activating N2C with a logic "0." When NFH and NFL are both activated with a logic "0," the input data to the 10-bit register is inverted.

Data Inputs

Data inputs are ECL compatible when single power supply operation is employed. The J5 and C2 packages allow for differential ECL inputs while the J7 and B7 packages have only single-ended inputs. When differential ECL data is used, any data input can be inverted simply by reversing the connections to the true and inverted data input pins. All inverted input pins should be left open if single-ended ECL or TTL modes are used. All data inputs have an internal 40 kOhm pull-up resistor to V_{CC}.

Analog Output

The analog output voltage is negative with respect to A_{GND} and varies proportionally with the magnitude of the input data word. The output resistance at this point is 80 Ohms, nominally.

No Connects

There are several pins labeled no connect (NC) on the TDC1016 J5 and C2 packages, which have no connections to the chip. These pins should be left open.

B

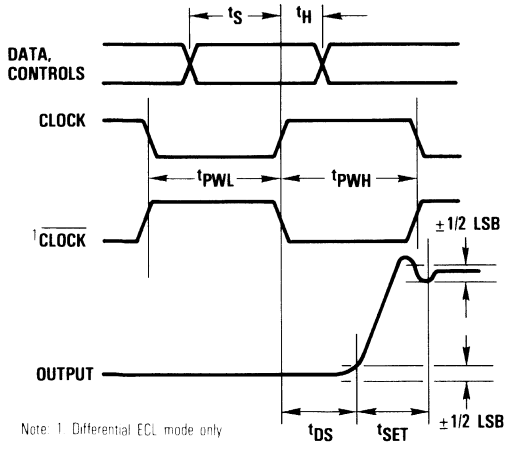
Package Interconnections

Signal Type	Signal Name	Function	Value	B5 Package Pins	B7 Package Pins
Power	V_{CC}	Positive Supply Voltage	+5.0V	9	6
	V_{EE}	Negative Supply Voltage	−5.0V	2	23
	A_{GND}	Analog Ground	0.0V	5, 6, 8	2, 3, 5
	D_{GND}	Digital Ground	0.0V	10	7
Reference	V_{REF}	Reference Voltage In	−1.0V	4	1
	COMP	Compensation	1μF	3	24
Controls	NDIS	Not Disable	TTL/ECL	11	8
	$\overline{\text{NDIS}}$	Not Disable (Inv)	ECL	14	
	CLK	Clock	TTL/ECL	12	9
	$\overline{\text{CLK}}$	Clock (Inv)	ECL	13	
	N2C	Not Two's Complement	TTL/ECL	17	11
	NFH	Not Force HIGH	TTL/ECL	20	13
	NFL	Not Force LOW	TTL/ECL	21	14

Package Interconnections (cont.)

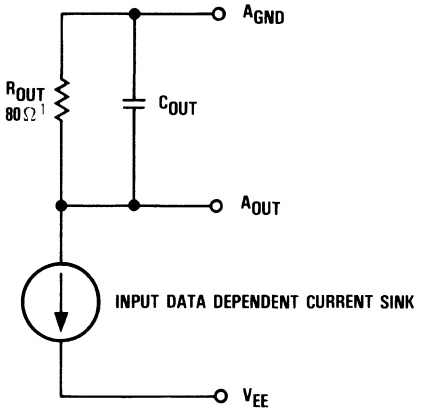
Signal Type	Signal Name	Function	Value	B5 Package Pins	B7 Package Pins
Data Inputs	D_1	Data Bit 1 (MSB)	TTL/ECL	16	10
	$\overline{D_1}$	Data Bit 1 (MSB Inv)	ECL	15	
	D_2		TTL/ECL	19	12
	$\overline{D_2}$		ECL	18	
	D_3		TTL/ECL	23	15
	$\overline{D_3}$		ECL	22	
	D_4		TTL/ECL	25	16
	$\overline{D_4}$		ECL	24	
	D_5		TTL/ECL	27	17
	$\overline{D_5}$		ECL	26	
	D_6		TTL/ECL	29	18
	$\overline{D_6}$		ECL	28	
	D_7		TTL/ECL	31	19
	$\overline{D_7}$		ECL	30	
	D_8		TTL/ECL	33	20
	$\overline{D_8}$		ECL	32	
	D_9		TTL/ECL	35	21
	$\overline{D_9}$		ECL	34	
	D_{10}	Data Bit 10 (LSB)	TTL/ECL	37	22
	$\overline{D_{10}}$	Data Bit 10 (LSB Inv)	ECL	36	
Analog Output	A_{OUT}	Analog Output Voltage	0V to −1V	7	4
No Connects	NC	No Connect	Open	1, 38, 39, 40	– –

Figure 1. Timing Diagram



Note: 1. Differential ECL mode only

Figure 2. Analog Output Equivalent Circuit, TTL and ECL Mode



Note: 1. 75Ω requires outside trim

Figure 3. Digital Input Equivalent Circuit, TTL Mode

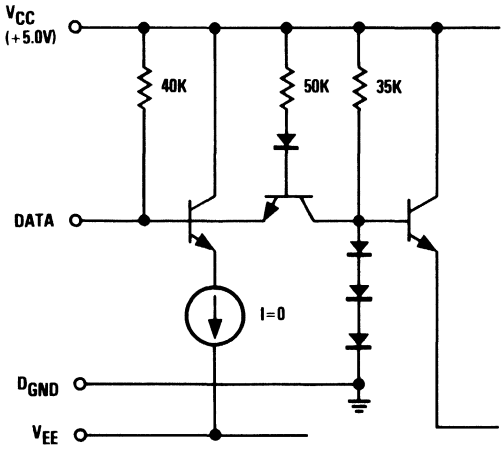
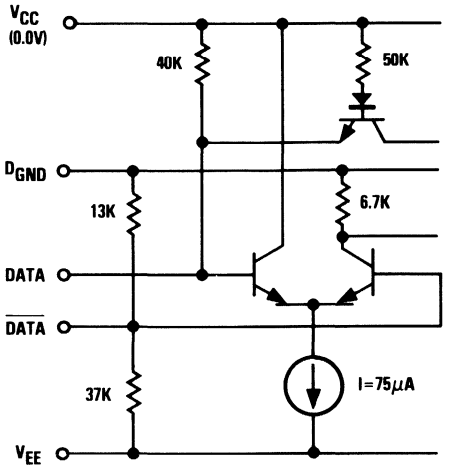


Figure 4. Digital Input Equivalent Circuit, ECL Mode



B

Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltages

V_{CC} (measured To D_{GND})	-0.5 to +7.0V
V_{EE} (measured To A_{GND})	+0.5 to -7.0V
A_{GND} (measured To D_{GND})	+0.5 to -0.5V

Input Voltages

Digital (measured To D_{GND})	+7.0 to -7.0V
Reference (measured To A_{GND})	-1.5 to +0.5V

Output

Applied voltage (measured To A_{GND})	+2.0 to -2.0V [2]
Short-circuit duration	indefinite

Temperature

Operating ambient	+125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	-65 to +150°C

Notes

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.

Operating conditions

Parameter			Temperature Range: Standard Min	Standard Nom	Standard Max	Extended Min	Extended Nom	Extended Max	Units
V_{CC}	Positive Supply Voltage	TTL Mode	4.75	5.0	5.25	4.50	5.0	5.50	V
		ECL Mode	-0.25	0.0	0.25	-0.25	0.0	0.25	V
V_{EE}	Negative Supply Voltage		-4.5	-5.0	-5.5	-4.5	-5.0	-5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})		-0.1	0.0	0.1	-0.1	0.0	0.1	V
t_{PWL}	CLK Pulse Width, LOW		15			20			ns
t_{PWH}	CLK Pulse Width, HIGH		15			20			ns
t_S	Input Register Set-up Time	TTL Mode	20			22			ns
		ECL Mode	25			27			ns
t_H	Input Register Hold Time		2			2			ns
V_{IL}	Logic "0"	TTL Mode	D_{GND}		0.8	D_{GND}		0.8	V
		ECL Mode			-1.67			-1.67	V
V_{IH}	Logic "1"	TTL Mode	2.0		V_{CC}	2.0[1]		V_{CC}	V
		ECL Mode	-1.0			-1.0			V
V_{REF}	Reference Voltage		-0.8	-1.0	-1.2	-0.8	-1.0	-1.2	V
C_{COMP}	Compensation Capacitor		1.0			1.0			μF
T_A	Ambient Temperature		0		70				°C
T_C	Case Temperature					-55		125	°C

Note:

1. V_{IH}/NDIS = 2.2 Min.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{CC}	Power Supply Current	TTL Mode, V_{CC} = Max, V_{EE} = Max		20		20	mA
I_{EE}	Power Supply Current	TTL Mode, V_{CC} = Max, V_{EE} = Max[1]		-130		-150	mA
I_{REF}	Reference Input Current	V_{EE} = Max, V_{REF} = -1.0V		10		10	μA
I_{IL}	Logic "0" Input Current	TTL Mode, V_{CC} = Max, V_{EE} = Max		-1.0		-1.0	mA
		ECL Mode, V_{CC} = 0.0, V_{EE} = Max		-300		-300	μA
I_{IH}	Logic "1" Input Current	TTL Mode, V_{CC} = Max, V_{EE} = Max		75		75	μA
		ECL Mode, V_{CC} = 0.0, V_{EE} = Max		350		350	μA
C_{OUT}	Output Capacitance	A_{OUT} to A_{GND} (Figure 2)		10		10	pF
C_{IN}	Digital Input Capacitance	Any Digital Input to D_{GND}		35		35	pF
R_{OUT}	Output Resistance	A_{OUT} to A_{GND} (Figure 2)	70	95	70	95	Ohms

Note:

1. Return current from V_{EE} flows through A_{GND}.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_C	Maximum Data Rate	TTL Mode Full-Scale Output Step	20		20		MSPS
		ECL Mode Full-Scale Output Step	17.8		17.8		MSPS
t_{DS}	Data Turn-on Delay	RL = 75 Ohms		30		30	ns
t_{SET}	Settling Time	TDC1016-8 to 0.2%		30		30	ns
		TDC1016-9 to 0.1%		35		35	ns
		TDC1016-10 to .05%		40		40	ns
t_{RV}	Output 10% to 90% Risetime	V_{EE} = Nom, RL = 75 Ohms, Full-Scale Step		5.5		5.5	ns

B

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
RES	Resolution	All TDC1016 Devices		10		10	Bits
ELI, ELD	Linearity Error Integral and Differential Terminal Based	TDC1016-8		0.2		0.2	% FS
		TDC1016-9		0.1		0.1	% FS
		TDC1016-10		0.05		0.05	% FS
V_{OFS}	Full-Scale Output Voltage	V_{EE} = Nom, RL $\geq$ 10 kOhms	-0.95	-1.05	-0.95	-1.05	V
		V_{REF} = -1.000V					
V_{OZS}	Zero-Scale Output Voltage	V_{EE} = Nom, RL $\geq$ 10 kOhms		±15		±15	mV
		V_{REF} = -1.000V					
DP	Differential Phase	NTSC 4x subcarrier [1]		1.0		1.0	Degree
DG	Differential Gain	NTSC 4x subcarrier [1]		1.5		1.5	%
GE	Glitch "Energy" (Area)	RL = 50 Ohms, Midscale	125		125		pV-sec
GV	Glitch Voltage	RL = 50 Ohms, Midscale		35		35	mV

Note:

1. In excess of theoretical DP and DG due to quantizing error.

Input Coding Table

NDIS	N2C	NFH	NFL	Data	Output	Description
0	x	x	x	xxxxxxxxxx	0.0	Output Disabled
1	1	1	1	1111111111	0.0	Binary (Default State for TTL
1	1	1	1	0000000000	−1.0	Mode Control) Inputs Open
1	1	0	0	1111111111	−1.0	Inverse Binary
1	1	0	0	0000000000	0.0	
1	0	1	1	0111111111	0.0	Two's Complement
1	0	1	1	1000000000	−1.0	
1	0	0	0	0111111111	−1.0	Inverse Two's Complement
1	0	0	0	1000000000	0.0	
1	x	0	1	xxxxxxxxxx	0.0	Force HIGH
1	x	1	0	xxxxxxxxxx	−1.0	Force LOW

Notes:
1. For TTL, $0.0 < V_{IL} < +0.8V$ is logic "0".
2. For TTL, $+2.0 < V_{IH} < +5.0V$ is logic "1".
3. For ECL, $-1.85 < V_{IL} < -1.67V$ is logic "0".
4. For ECL, $-1.0 < V_{IH} < -0.8V$ is logic "1".
5. x = "don't care".

Calibration

The TDC1016 is calibrated by adjusting the voltage reference to give the desired full-scale output voltage. The current switches can be turned on either by loading the data register with full-scale data or by bringing the NFH input to a logic zero. Note that all 10 current switches are activated by the NFH input and the resulting full-scale output voltage will be greater than if the system used only eight or nine bits for full-scale data.

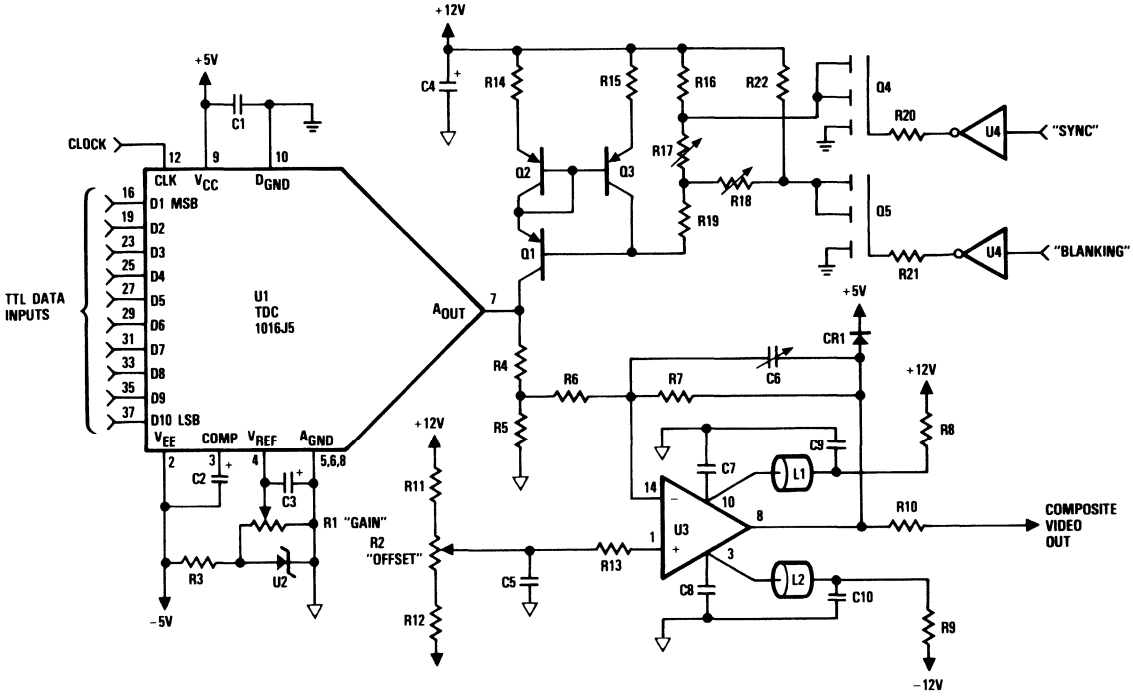
Typical Application

The *Typical Interface Circuit (Figure 5)* shows the TDC1016 in a typical application, reconstructing video signals from digital data. Television timing signals, SYNC and BLANKING, are added by injecting current from the Wilson current source into a resistor divider circuit at the output of the TDC1016.

The TDC1016 output and currents from the SYNC and BLANKING inputs are summed and amplified by the HA2539 wide-band operational amplifier. Note the careful power supply decoupling at the power input pins of the amplifier. The output of the circuit is a composite video signal with SYNC and BLANKING levels coming from external sources. This technique allows the TDC1016 to use its entire dynamic range for the video information while pulses are added by other means.

The reference for the TDC1016 is generated by dividing the output voltage from a two-terminal band-gap voltage reference. System gain is calibrated by adjusting variable resistor R1. Analog and digital grounds should be routed back to system power supply ground by separate paths.

Figure 5. Typical Interface Circuit



Parts List

Resistors

R1	5K	1/4W	10-turn
R2	1K	1/4W	10-turn
R3	1K	1/4W	5%
R4	43	1/4W	5%
R5	33	1/4W	5%
R6	330	1/4W	5%
R7	750	1/4W	5%
R8,R9	10	1/4W	5%
R10	75	1/4W	2%
R11,R12	10K	1/4W	5%
R13	220	1/4W	5%
R14,R15	100	1/4W	5%
R16,R22	390	1/4W	5%
R17,R18	2K	1/4W	10-turn
R19	1K	1/4W	5%
R20,R21	1K	1/4W	5%

Capacitors

C1	0.01μF	50V
C2	1.0μF	10V
C3	1.0μF	10V
C4	2.2μF	25V
C5	0.1μF	50V
C6	2-5 pF	50V
C7	0.1μF	50V
C8	0.1μF	50V
C9	0.1μF	50V
C10	0.1μF	50V

RF Chokes

L1,L2	Ferrite beads

Diodes

CR1	1N4001

Transistors

Q1	2N2907
Q2	2N2907
Q3	2N2907
Q4	2N6660
Q5	2N6660

Integrated Circuits

U1	TRW TDC1016
U2	LM113
U3	HA2539
U4	SN7404

Ordering Information [1]

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1016B5CX	STD – T_A = 0°C to 70°C	Commercial	40 Pin CERDIP	1016B5CX
TDC1016B5AX [3]	EXT – T_C = –55°C to 125°C	High Reliability	40 Pin CERDIP	1016B5AX
TDC1016B7CX	STD – T_A = 0°C to 70°C	Commercial	24 Pin CERDIP	1016B7CX
TDC1016B7AX [3]	EXT – T_C = –55°C to 125°C	High Reliability	24 Pin CERDIP	1016B7AX

Notes:
1. Per TRW document 70Z01757.
2. "X" in part and mark number indicates grade. The TDC1016 devices are available in three grades. Grade "8" is for 8-bit linearity, grade "9" for 9-bit linearity, and grade "10" for 10-bit linearity.
3. The TDC1016 with A screening is available in 8 or 9-bit linearity only.

TDC1018

Digital-to-Analog Converter
8-Bit, 200MHz

The TDC1018 is an 8-bit digital-to-analog converter, designed for 200MHz operation and capable of directly driving a 75 Ohm load to standard video levels. Most applications require no extra registering, buffering, or deglitching. Four special level controls make the device ideal for video applications. All data and control inputs are ECL compatible.

The TDC1018 is built with TRW's OMICRON-B™ 1-micron bipolar process. On-chip data registers and precise matching of propagation delays make the TDC1018 inherently low-glitching. The TDC1018 offers high performance, low power consumption, and video compatibility in a 24 pin DIP or a 28 contact chip carrier.

Features

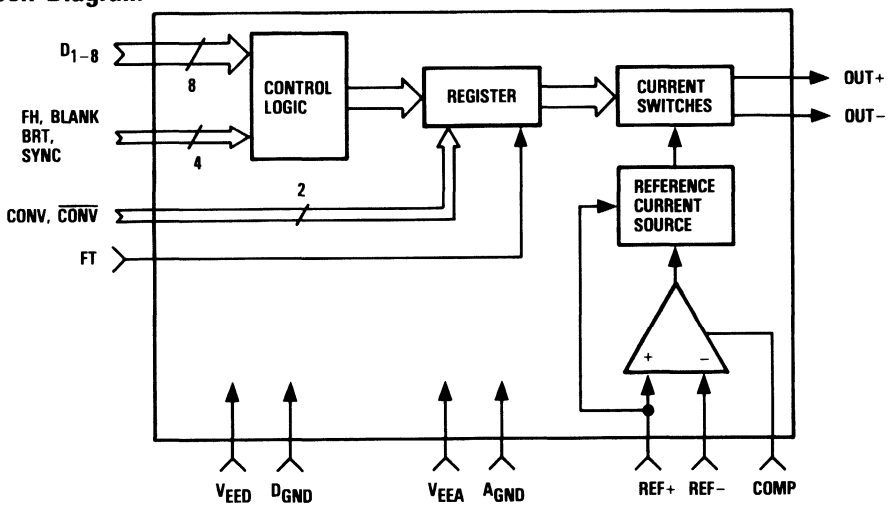
- Monolithic "Graphics-Ready"
- 125MHz Digital Update Rate, TDC1018
- 200MHz Digital Update Rate, TDC1018-1
- 8-Bit Resolution
- 1/2 LSB Linearity
- Registered Data And Video Controls
- Complementary Current Outputs
- Video Controls: SYNC, BLANK, BRight, Force High
- Inherently Low Glitch Energy
- ECL Compatible Inputs
- Multiplying Mode Capability
- Can Be Operated In TTL Systems
- Available In A 24 Pin DIP And 28 Contact Chip Carrier
- Single −5.2V Power Supply

B

Applications

- RGB Graphics
- High Resolution Video
- Raster Graphic Displays
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

Functional Block Diagram



TRW LSI Products Inc.
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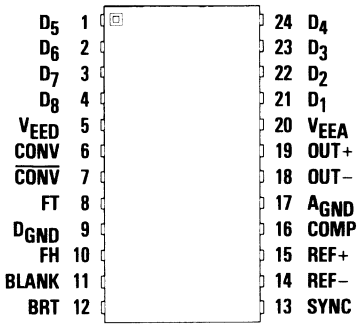
La Jolla, CA 92038

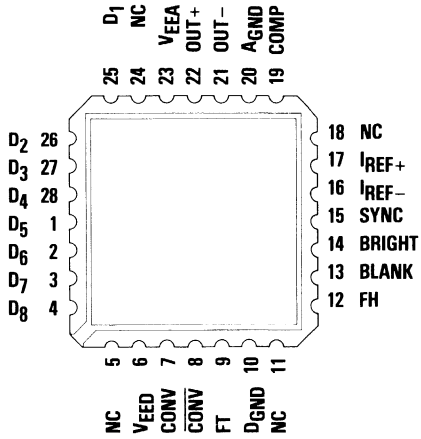
Phone: (619) 457-1000
FAX: (619) 455-6314

40G01211 Rev. G–11/90
Printed in the U.S.A.

Pin Assignments



24 Pin CERDIP – B7 Package



28 Contact Chip Carrier – C3 Package

Functional Description

General Information

The TDC1018 develops complementary analog output currents proportional to the product of the digital input data and analog reference current. All data and control inputs are compatible with standard ECL logic levels. FeedThrough control (FT) determines whether data and control inputs are synchronous or asynchronous. If FT is LOW, each rising edge of the CONVert clock (CONV) latches decoded data and control values into an internal D-type register. The registered values are then converted into the appropriate analog output by switched current sinks. When FT is HIGH, data and control inputs are not registered, and the analog output asynchronously tracks the input values. FT is the only asynchronous input, and is normally used as a DC control.

The TDC1018 uses a segmented approach in which the four MSBs of the input data are decoded into a parallel "Thermometer" code, which drives fifteen identical current sinks to produce sixteen coarse output levels. The LSBs of the input drive four binary-weighted current switches, with a total contribution of one-sixteenth of full-scale. The LSB and MSB currents are summed to provide 256 analog output levels.

Special control inputs, SYNC, BLANK, Force High (FH) and BRight (BRT), drive appropriately weighted current sinks which add to the output current to produce specific output levels especially useful in video applications.

Power

To provide highest noise immunity, the TDC1018 operates from separate analog and digital power supplies, V_{EEA} and V_{EED}, respectively. Since the required voltage for both V_{EEA} and V_{EED} is $-5.2V$, these may ultimately be connected to the same power source, but individual high-frequency decoupling for each supply is recommended. A typical decoupling network is shown in *Figure 7*. The return for I_{EED}, the current drawn from the V_{EED} supply, is D_{GND}. The return for I_{EEA} is A_{GND}. All power and ground pins MUST be connected.

Although the TDC1018 is specified for a nominal supply of $-5.2V$, operation from a $+5.0V$ supply is possible provided that the relative polarities of all voltages are maintained.

For additional information concerning the use of ECL D/A converters in a $+5V$ system, refer to *TRW Application Note TP-33 "Using the TDC1018 and TDC1034 in a TTL Environment."*

Reference

The TDC1018 has two reference inputs: REF+ and REF−, which are noninverting and inverting inputs of an internal reference buffer amplifier. The output of this operational amplifier serves as a reference for the current sinks. The feedback loop is internally connected around one of the current sinks to achieve high accuracy (see *Figure 4*).

The analog output currents are proportional to the digital data and reference current, I_{REF}. The full-scale output value may be adjusted over a limited range by varying the reference current. Accordingly, the stability of the analog output depends primarily upon the stability of the reference. A method of achieving a stable reference is shown in *Figure 7*.

The reference current is fed into the REF+ input, while REF− is typically connected to a negative reference voltage through a resistor chosen to minimize input offset bias current effects.

A COMPensation input (COMP), is provided for external compensation of the TDC1018's reference amplifier. A capacitor (C_C) should be connected between COMP and the V_{EEA} supply, keeping lead lengths as short as possible. The value of the compensation capacitor determines the effective bandwidth of the amplifier. In general, decreasing C_C increases bandwidth and decreases amplifier stability. For applications in which the reference is constant, C_C should be large, while smaller values of C_C may be chosen if dynamic modulation of the reference is required.

Controls

The TDC1018 has four special video control inputs: SYNC, BLANK, Force High (FH), and BRighT (BRT), in addition to a clock FeedThrough control (FT). All controls are standard ECL level compatible, and include internal pulldown resistors to force unused controls to a logic LOW (inactive) state.

Typically the TDC1018 is operated in the synchronous mode, which assures the highest conversion rate and lowest spurious output noise. By asserting FT, the input registers are disabled, allowing data and control changes to asynchronously feed-through to the analog output. Propagation delay from input change (control or data) to analog output is minimized in the asynchronous mode of operation.

In the synchronous mode, the video control inputs are registered by the rising edge of the CONV clock in a manner similar to the data inputs. The controls, like data, must be present at the inputs for a setup time of t_S (ns) before, and a hold time of t_H (ns) after the rising edge of CONV in order to be registered. In the asynchronous mode, the setup and hold times are irrelevant and minimum pulse widths HIGH and LOW become the limiting factor.

Asserting the video controls produces various output levels which are used for frame synchronization, horizontal blanking, etc., as described in video system standards such as RS-170 and RS-343A. The effect of the video controls on the analog outputs is shown in *Table 1*. Special internal logic governs the interaction of these controls to simplify their use in video applications. BLANK, SYNC, and Force High override the data inputs. SYNC overrides all other inputs, and produces full negative video output. Force High drives the internal digital data to full-scale, giving a reference white video level output. The BRT control creates a "whiter than white" level by adding 10% of the full-scale value to the present output level, and is especially useful in graphics displays for highlighting cursors, warning messages, or menus. For non-video applications, the special controls can be left unconnected.

Data Inputs

Data inputs to the TDC1018 are standard single-ended ECL level compatible. Internal pulldown resistors force unconnected data inputs to logic LOW. Input registers are provided for synchronous data entry and lowest differential data propagation delay (skew), which minimizes glitching.

In the registered mode, valid data must be present at the input a setup time t_S (ns) before, and a hold time t_H (ns) after the rising edge of CONV. When FT is HIGH, data input is asynchronous and the input registers are disabled. In this case the analog output changes asynchronously in direct response to the input data.

Convert

CONVert (CONV) is a differential ECL compatible clock input whose rising edge synchronizes data and control entry into the TDC1018. Within the constraints shown in *Figure 2*, the actual switching threshold of CONV is determined by $\overline{CONV}$. CONV may be driven single-ended by connecting $\overline{CONV}$ to a suitable bias voltage (V_{BB}). The bias voltage chosen will determine the switching threshold of CONV. However, for best performance, CONV must be driven differentially. This will minimize clock noise and power supply/output intermodulation. Both clock inputs must normally be connected, with $\overline{CONV}$ being the complement of CONV.

Analog Outputs

The two analog outputs of the TDC1018 are high-impedance complementary current sinks which vary in proportion to the input data, controls, and reference current values. The outputs are capable of directly driving a dual 75 Ohm load to standard video levels. The output voltage will be the product of the output current and effective load impedance, and will usually be between 0V and −1.07V in the standard configuration (see *Figure 5*). In this case, the OUT− output gives a DC shifted video output with "sync down." The corresponding output from OUT+ is also DC shifted and inverted, or "sync up."

Package Interconnections

Signal Type	Signal Name	Function	Value	B7 Package Pins	C3 Package Pins
Power	V_{EEA}	Analog Supply Voltage	−5.2V	20	23
	V_{EED}	Digital Supply Voltage	−5.2V	5	6
	A_{GND}	Analog Ground	0.0V	17	20
	D_{GND}	Digital Ground	0.0V	9	10
Reference	REF−	Reference Current− Input	Op-Amp Virtual Ground	14	16
	REF+	Reference Current+ Input	Op-Amp Virtual Ground	15	17
	COMP	COMPensation Input	C_C	16	19
Controls	FT	Register FeedThrough Control	ECL	8	9
	FH	Data Force High Control	ECL	10	12
	BLANK	Video BLANK Input	ECL	11	13
	BRT	Video BRighT Input	ECL	12	14
	SYNC	Video SYNC Input	ECL	13	15
Data Inputs	D_1	Data Bit 1 (MSB)	ECL	21	25
	D_2		ECL	22	26
	D_3		ECL	23	27
	D_4		ECL	24	28
	D_5		ECL	1	1
	D_6		ECL	2	2
	D_7		ECL	3	3
	D_8	Data Bit 8 (LSB)	ECL	4	4
Convert	CONV	CONVert Clock Input	ECL	6	7
	$\overline{CONV}$	CONVert Clock Input, Complement	ECL	7	8
Analog Outputs	OUT−	Output Current−	Current Sink	18	21
	OUT+	Output Current+	Current Sink	19	22

Figure 1. Timing Diagram

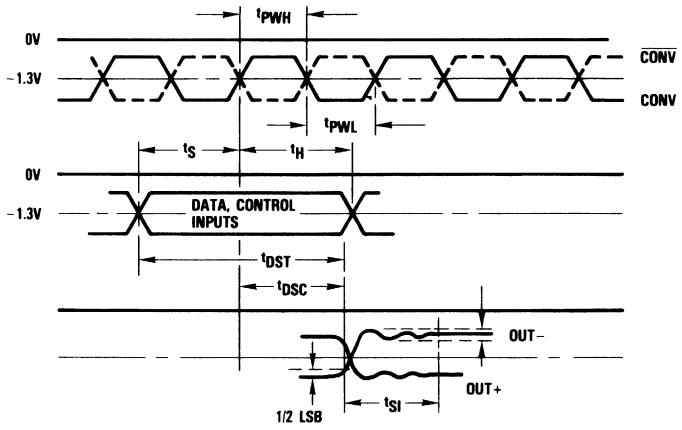


Figure 2. CONVert, $\overline{\text{CONV}}$ert Switching Levels

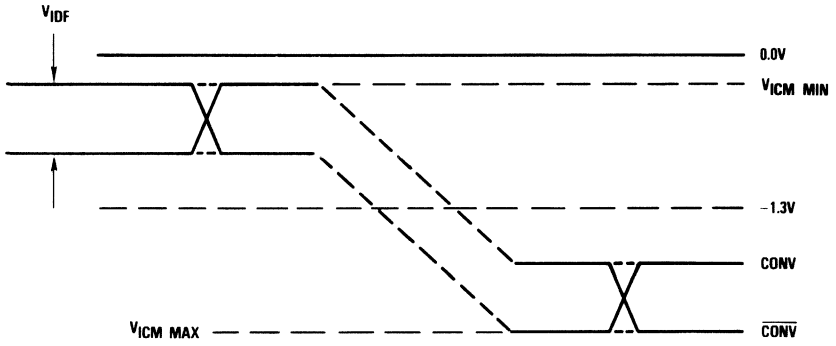


Figure 3. Equivalent Input Circuits

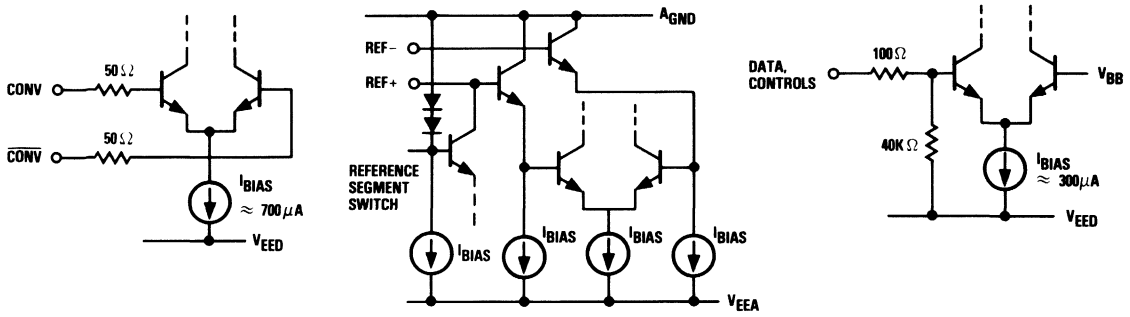


Figure 4. Equivalent Output Circuit

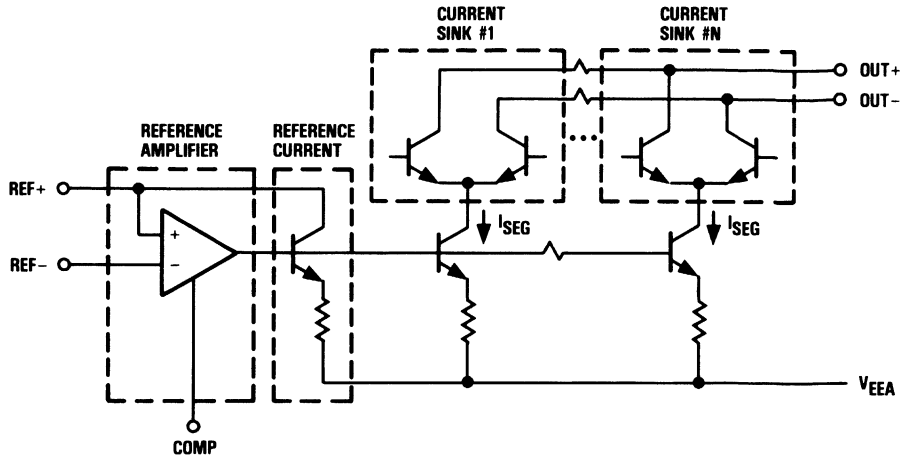
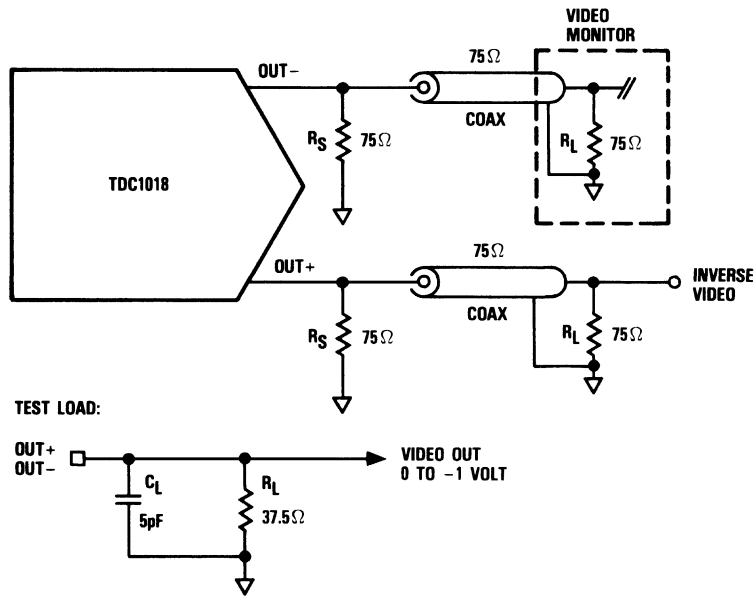


Figure 5. Standard Load Configuration



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{EED} (measured to D_{GND})	−7.0 to 0.5V
V_{EEA} (measured to A_{GND})	−7.0 to 0.5V
A_{GND} (measured to D_{GND})	−0.5 to 0.5V

Input Voltages

CONV, Data, and Controls (measured to D_{GND})	V_{EED} to 0.5V
Reference input, applied voltage (measured to A_{GND}) [2]	
REF+	V_{EEA} to 0.5V
REF−	V_{EEA} to 0.5V
Reference input, applied current, externally forced [3,4]	
REF+	6.0mA
REF−	0.5mA

Output

Analog output, applied voltage (measured to A_{GND})	
OUT+	−2.0 to +2.0V
OUT−	−2.0 to +2.0V
Analog output, applied current, externally forced [3,4]	
OUT+	50mA
OUT−	50mA
Short circuit duration	Unlimited sec

Temperature

Operating, ambient	−60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−60 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

Operating conditions

Parameter			Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{EED}	Digital Supply Voltage (measured to D_{GND})		-4.9	-5.2	-5.5	V
V_{EEA}	Analog Supply Voltage (measured to A_{GND})		-4.9	-5.2	-5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})		-0.1	0.0	+0.1	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential		-0.1	0.0	+0.1	V
V_{ICM}	CONV Input Voltage, Common Mode Range (Figure 2)		-0.5		-2.5	V
V_{IDF}	CONV Input Voltage, Differential (Figure 2)		0.4		1.2	V
t_{PWL}	CONV Pulse Width, LOW		4			ns
t_{PWH}	CONV Pulse Width, HIGH		4			ns
t_S	Setup Time, Data and Controls		3.5			ns
t_H	Hold Time, Data and Controls		0			ns
V_{IL}	Input Voltage, Logic LOW				-1.49	V
V_{IH}	Input Voltage, Logic HIGH		-1.045			V
I_{REF}	Reference Current	Video standard output levels[1]	1.059	1.115	1.171	mA
		8-bit linearity	1.0		1.3	mA
C_C	Compensation Capacitor		2000	3900		pF
T_A	Ambient Temperature, Still Air		0		70	°C

Note:

1. Minimum and Maximum values allowed by ±5% variation given in RS343A and RS170 after initial gain correction of device.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Units
$I_{EEA}+I_{EED}$	Supply Current	$V_{EEA} = V_{EED}$ = MAX, static[1]			
		T_A = 0°C to 70°C		170	mA
		T_A = 70°C		130	mA
C_{REF}	Equivalent Input Capacitance, REF+, REF-			5	pF
C_I	Input Capacitance, Data and Controls			5	pF
V_{OCP}	Compliance Voltage, + Output		-1.2	+1.5	V
V_{OCN}	Compliance Voltage, - Output		-1.2	+1.5	V
R_O	Equivalent Output Resistance		20		KOhms
C_O	Equivalent Output Capacitance			20	pF
I_{OP}	Max Current, + Output	V_{EEA} = NOM, SYNC = BLANK = 0, FH = BRT = 1		30	mA
I_{ON}	Max Current, - Output	V_{EEA} = NOM, SYNC = 1		30	mA
I_{IL}	Input Current, Logic LOW, Data and Controls	V_{EED} = MAX, V_I = -1.49V		200	μA
I_{IH}	Input Current, Logic HIGH, Data and Controls	V_{EED} = MAX, V_I = -1.045V		200	μA
I_{IC}	Input Current, Convert	V_{EED} = MAX, $-1.49V < V_I < -1.045V$		50	μA

Note:

1. Worst case over all data and control states

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Data Rate	V_{EEA}, V_{EED} = MIN			
		TDC1018	125		MSPS
		TDC1018-1	200		MSPS
t_{DSC}	Clock to Output Delay, Clocked Mode	V_{EEA}, V_{EED} = MIN, FT = 0		8	ns
t_{DST}	Data to Output Delay, Transparent Mode	V_{EEA}, V_{EED} = MIN, FT = 1		13	ns
t_{SI}	Current Settling Time, Clocked Mode	V_{EEA}, V_{EED} = MIN, FT = 0			
		0.2%		10	ns
		0.8%		8	ns
		3.2%		5	ns
t_{RI}	Risetime, Current	10% to 90% of Gray Scale		1.7	ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error Integral, Terminal Based	V_{EEA}, V_{EED}, I_{REF} = NOM		0.2	% of Gray Scale
E_{LD}	Linearity Error Differential	V_{EEA}, V_{EED}, I_{REF} = NOM		0.2	% of Gray Scale
I_{OF}	Output Offset Current	V_{EEA}, V_{EED} = MAX, SYNC = BLANK = 0, FH = BRT = 1		10	μA
E_G	Absolute Gain Error	V_{EEA}, V_{EED} = MIN, I_{REF} = NOM		±5	% of Gray Scale
TC_G	Gain Error Tempco			±0.024	% of Gray Scale/°C
BWR	Reference Bandwidth, -3dB	C_C = MIN, ΔV_{REF} = 1mV p-p	1		MHz
DP	Differential Phase	4 x NTSC		1.0	Degrees
DG	Differential Gain	4 x NTSC		2.0	%
PSRR	Power Supply Rejection Ratio	V_{EEA}, V_{EED}, I_{REF} = NOM [1]		45	dB
		V_{EEA}, V_{EED}, I_{REF} = NOM [2]		55	dB
PSS	Power Supply Sensitivity	V_{EEA}, V_{EED}, I_{REF} = NOM		120	μA/V
G_C	Peak Glitch Charge	Registered Mode [3,4]		800	fCoulomb
G_I	Peak Glitch Current	Registered Mode		1.2	mA
G_E	Peak Glitch "Energy" (Area)	Registered Mode [4]		30	pV-Sec
FT_C	Feedthrough Clock	Data = Constant [5]		-50	dB
FT_D	Feedthrough Data	Clock = Constant [5]		-50	dB

Notes:

1. 20KHz, ±0.3V ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
2. 60Hz, ±0.3V ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
3. fCoulombs = microamps x nanoseconds.
4. 37.5Ω load. Because glitches tend to be symmetric, average glitch area approaches zero.
5. dB relative to full gray scale, 250MHz bandwidth limit.

Table 1 Video Control Truth Table

Sync	Blank	Force High	Bright	Data Input	Out– (mA)[1]	Out– (V)[2]	Out– (IRE)[3]	Description[4]
1	X	X	X	X	28.57	–1.071	–40	Sync Level
0	1	X	X	X	20.83	–0.781	0	Blank Level
0	0	1	1	X	0.00	0.00	110	Enhanced High Level
0	0	1	0	X	1.95	–0.073	100	Normal High Level
0	0	0	0	000...	19.40	–0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	–0.073	100	Normal High Level
0	0	0	1	000...	17.44	–0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.00	110	Enhanced High Level

Notes:

1. Out+ is complementary to Out–. Current is specified as conventional current when flowing into the device.
2. Voltage produced when driving the standard load configuration (37.5 Ohms). See Figure 5.
3. 140 IRE units = 1.00V
4. RS-343-A tolerance on all control values is assumed.

Figure 6. Video Output Waveforms for Out– and Out+ with Standard Load Configuration

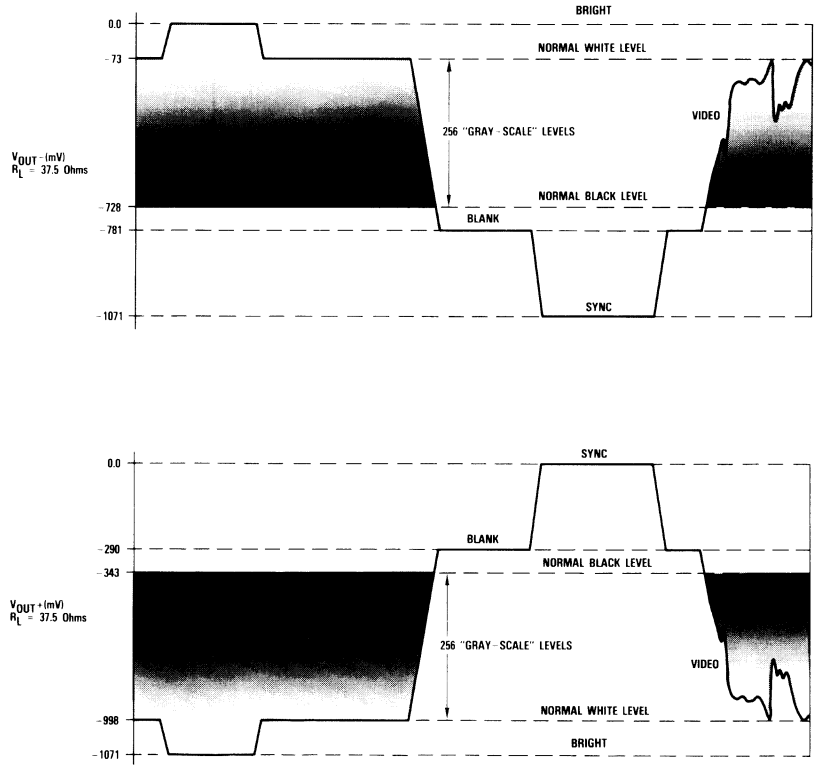
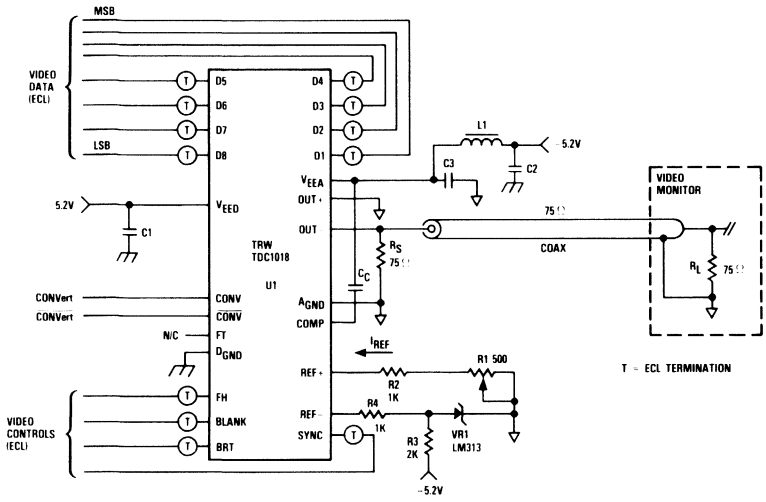


Figure 7. Typical Interface Circuit



Parts List

Integrated Circuits

U1 TDC1018 D/A Converter

Voltage References

VR1 LM113 or LM313 Bandgap Reference

Inductors

L1 Ferrite Bead Shield Inductor
Fair-Rite P/N 2743001112 or Similar

Resistors

R1	1KΩ	Pot	10 Turn
R2	1.00KΩ	1/8W	1% Metal Film
R3	2.00KΩ	1/8W	1% Metal Film
R4	1.00KΩ	1/8W	1% Metal Film

Capacitors

C1 – C3	0.1μF	50V	Ceramic Disc
C_C	0.01μF	50V	Ceramic Disc

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1018B7C	STD – T_A = 0°C to 70°C	Commercial	24 Pin CERDIP	1018B7C
TDC1018B7C1	STD – T_A = 0°C to 70°C	Commercial	24 Pin CERDIP	1018B7C1
TDC1018C3C	STD – T_A = 0°C to 70°C	Commercial	28 Contact Chip Carrier	1018C3C
TDC1018C3C1	STD – T_A = 0°C to 70°C	Commercial	28 Contact Chip Carrier	1018C3C1

TDC1034

Digital-to-Analog Converter
4-Bit, 200MHz

The TRW TDC1034 is a 4-bit D/A converter, designed for 200MHz operation and is capable of directly driving a 75 Ohm load to standard video levels. Most applications require no extra registering, buffering, or deglitching. Three special level controls make the device ideal for video applications. All data and control inputs are ECL compatible.

The TDC1034 is built with TRW's OMICRON-B™ 1-micron bipolar process. On-chip data registers and precise matching of propagation delays insure low glitch energy. The TDC1034 offers high performance, low power consumption, and video compatibility in an 18 pin CERDIP package.

Features

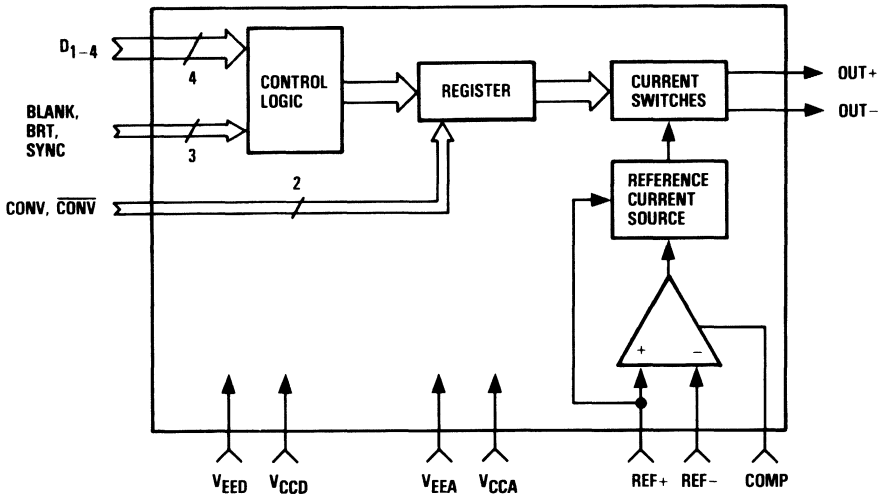
- "Graphics-Ready"
- 200MHz Conversion Rate
- 1/8 LSB Linearity
- Power Supply Noise Rejection >50dB
- Registered Data And Video Controls
- Differential Current Outputs
- Video Controls: SYNC, BLANK, BRighT
- Low Glitch Energy
- ECL Compatible, Can Be Used In TTL Systems
- Low Power Dissipation
- Available In An 18 Pin CERDIP Package
- Single −5.2V Power Supply

B

Applications

- CAD/CAM Workstations
- RGB Graphics
- Raster Scan Displays
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

Functional Block Diagram



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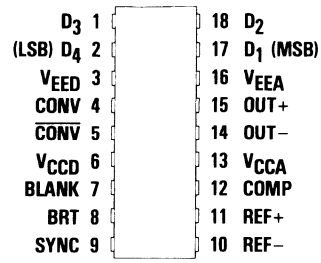
Pin Assignments



18 Pin CERDIP – B8 Package

Functional Description

General Information

The TDC1034 develops complementary analog output currents proportional to the product of the digital input data and analog reference current. All data and control inputs are compatible with standard ECL logic levels. Each rising edge of the CONVert clock (CONV) latches data and control values into an internal D-type register. The registered values are then converted into an analog output by switched current sinks.

The TDC1034 uses a segmented circuit design scheme in which the input data is decoded into a parallel "Thermometer" code, which drives fifteen identical current sinks to produce sixteen output levels.

Special control inputs, SYNC, BLANK and BRighT (BRT), drive appropriately weighted current sinks which add to the output current to produce specific output levels especially useful in video applications.

Power

To provide highest noise immunity, the TDC1034 operates from separate analog and digital power supplies, V_{EEA} and V_{EED}, respectively. Since the required voltage for both V_{EEA} and V_{EED} is −5.2V, these may ultimately be connected to the same power source, but high-frequency decoupling for each supply is recommended. A typical decoupling network is shown in *Figure 7*. The return for I_{EED}, the current drawn from the V_{EED} supply, is V_{CCD}. The return for I_{EEA} is V_{CCA}. All V_{EE} and V_{CC} pins MUST be connected.

Although the TDC1034 is specified for a nominal supply of −5.2V, operation from a +5.0V supply is possible provided that the relative polarities of all voltages are correctly maintained. For additional information concerning the use of ECL D/A converters in a +5V system, refer to *TRW Application Note TP-33 "Using the TDC1018 and TDC1034 in a TTL Environment."*

Reference

The TDC1034 has two reference inputs: REF+ and REF−, which are noninverting and inverting inputs to an internal reference buffer amplifier. The output of this operational amplifier serves as a reference for the current sinks. The feedback loop is internally connected around one of the current sinks to achieve high accuracy (see *Figure 4*).

The analog output currents are proportional to the digital data and reference current, I_{REF}. The full-scale output value may be adjusted over a limited range by varying the reference current. Accordingly, the stability of the analog output depends primarily upon the stability of the reference. A method of achieving a stable reference is shown in *Figure 7*.

The reference current flows into the REF+ input, while REF− is typically connected to a negative reference voltage through a resistor chosen to minimize input offset current effects.

A COMPensation input (COMP), is provided for external compensation of the TDC1034's reference amplifier. A capacitor (C_C) should be connected between COMP and the V_{EEA} supply, keeping lead lengths as short as possible. The value of the compensation capacitor determines the effective bandwidth of the amplifier. In general, decreasing C_C increases bandwidth and decreases amplifier stability. For applications in which the reference is constant, C_C should be large, while smaller values of C_C may be chosen when dynamic modulation of the reference is required.

Controls

The TDC1034 has three special video control inputs: SYNC, BLANK and BRighT (BRT). All controls are standard ECL level compatible, and include internal pulldown resistors to force unused controls to a logic LOW (inactive) state.

Controls (cont.)

The video control inputs are registered by the rising edge of the CONV clock in a manner similar to the data inputs. These inputs, like data, must be valid for a setup time of t_S before, and a hold time of t_H after the rising edge of CONV in order to be registered.

Asserting the video controls produces various output levels which are used for frame synchronization, horizontal blanking, etc., as described in video system standards such as RS-170 and RS-343A. The effect of the video controls on the analog outputs is shown in *Table 1*. Internal logic governs the interaction of these controls to simplify their use in video applications. BLANK and SYNC override the data inputs. SYNC overrides all other inputs, and produces full-scale output. The BRT control creates a "whiter than white" level by adding 10% of the full-scale value to the present output level, and is especially useful in graphics display for highlighting cursors, warning messages, or menus. For non-video applications, these controls may be left unconnected.

Data Inputs

Data inputs to the TDC1034 are standard single-ended ECL compatible. Internal pulldown resistors force unconnected data inputs to logic LOW. Input registers are provided for synchronous data entry and lowest differential data propagation delay (skew), which minimizes glitching.

Valid data must be present at the input a setup time t_S before, and a hold time t_H after the rising edge of CONV.

Convert

CONVert (CONV) is a differential ECL compatible clock input whose rising edge synchronizes data and control entry into the TDC1034. Within the constraints shown in *Figure 2*, the actual switching threshold of CONV is determined by $\overline{\text{CONV}}$. CONV may be driven single-ended by connecting $\overline{\text{CONV}}$ to a suitable bias voltage (V_{BB}). The bias voltage chosen will determine the switching threshold of CONV. However, for best performance, CONV must be driven differentially. This will minimize clock noise and power supply/output intermodulation. Both clock inputs must normally be connected.

Analog Outputs

The two analog outputs of the TDC1034 are high impedance complementary current sinks which vary in proportion to the input data, controls, and reference current values. The outputs are capable of directly driving dual 75 Ohm loads to standard video levels. The output voltage is the product of the output current and effective load impedance, and is usually between 0V and −1.07V in the standard configuration (see *Figure 5*). In this case, the OUT− output gives a DC shifted video output with "sync down." The corresponding output from OUT+ is also DC shifted and inverted, or "sync up."

Package Interconnections

Signal Type	Signal Name	Function	Value	B8 Package Pins
Power	V_{EEA}	Analog Supply Voltage	−5.2V	16
	V_{EED}	Digital Supply Voltage	−5.2V	3
	V_{CCA}	Analog Supply Voltage	0.0V	13
	V_{CCD}	Digital Supply Voltage	0.0V	6
Reference	REF−	Reference Current− Input	Op-Amp Virtual Ground	10
	REF+	Reference Current+ Input	Op-Amp Virtual Ground	11
	COMP	COMPensation Input	C_C	12
Controls	BLANK	Video BLANK Input	ECL	7
	BRT	Video BRighT Input	ECL	8
	SYNC	Video SYNC Input	ECL	9
Data Inputs	D_1	Data Bit 1 (MSB)	ECL	17
	D_2		ECL	18
	D_3		ECL	1
	D_4	Data Bit 4 (LSB)	ECL	2
Convert	CONV	CONVert Clock Input	ECL	4
	$\overline{CONV}$	CONVert Clock Input, Complement	ECL	5
Analog Outputs	OUT−	Output Current−	See Text	14
	OUT+	Output Current+	See Text	15

Figure 1. Timing Diagram

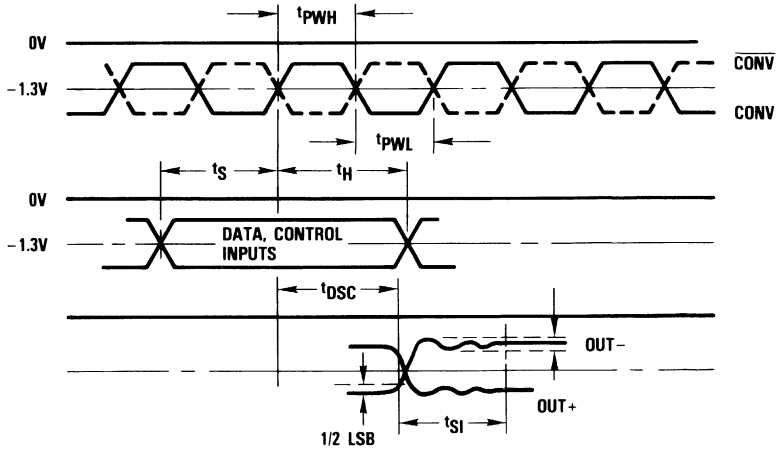


Figure 2. CONV, $\overline{CONV}$ Switching Levels

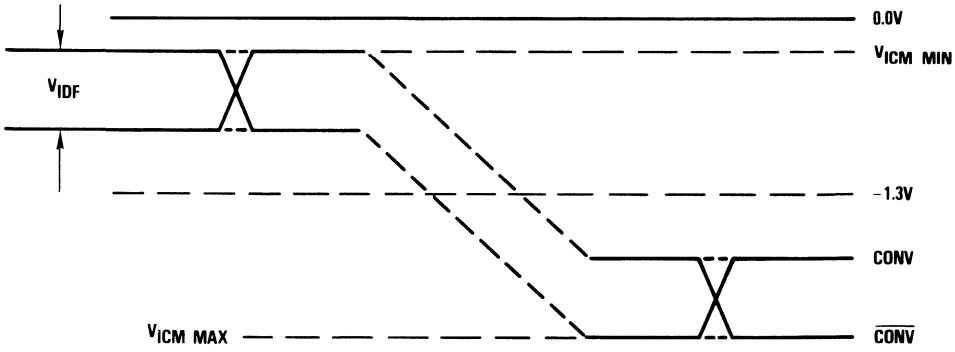


Figure 3. Equivalent Input Circuit

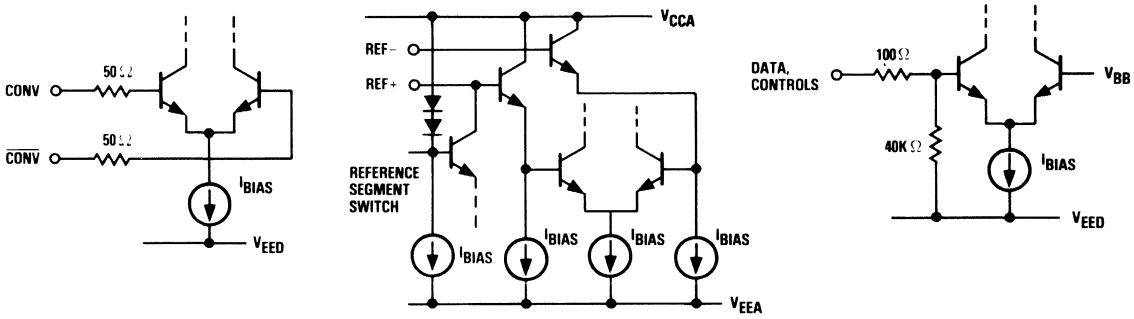


Figure 4. Equivalent Output Circuit

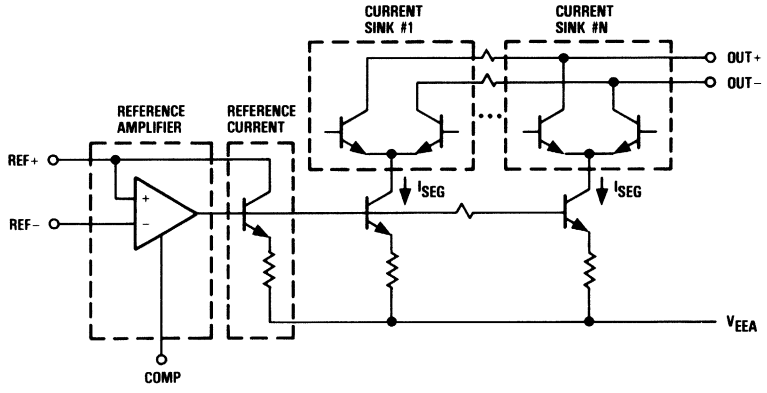
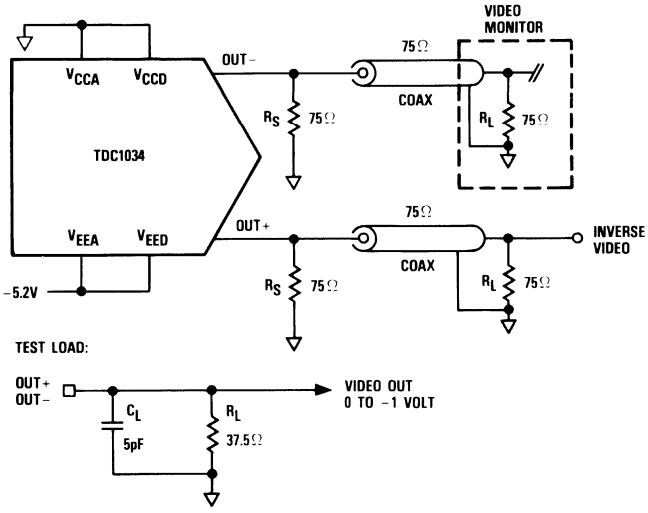


Figure 5. Standard Load Configuration



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{EED} (measured to V_{CCD})	-7.0 to 0.5V
V_{EEA} (measured to V_{CCA})	-7.0 to 0.5V
V_{EEA} (measured to V_{EED})	-0.5 to 0.5V
V_{CCA} (measured to V_{CCD})	-0.5 to 0.5V

Input Voltages

CONV, Data, and Controls (measured to V_{CCD})	V_{EED} to 0.5V
Reference input, applied voltage (measured to V_{CCA})[2]	
REF+	V_{EEA} to 0.5V
REF-	V_{EEA} to 0.5V
Reference input, applied current, externally forced[3,4]	
REF+	6.0mA
REF-	0.5mA

Output

Analog output, applied voltage (measured to V_{CCA})	
OUT+	-2.0 to +2.0V
OUT-	-2.0 to +2.0V
Analog output, applied current, externally forced[3,4]	
OUT+	50mA
OUT-	50mA
Short circuit duration	Unlimited sec

Temperature

Operating, ambient	-60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	-60 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{EED}	Digital Supply Voltage (measured to V_{CCD})	-4.75	-5.2	-5.5	V
V_{EEA}	Analog Supply Voltage (measured to V_{CCA})	-4.75	-5.2	-5.5	V
$V_{CCA}-V_{CCD}$	Supply Voltage Differential	-0.1	0.0	+0.1	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential	-0.1	0.0	+0.1	V
V_{ICM}	CONV Input Voltage, Common Mode Range (Figure 2)	-0.5		-2.5	V
V_{IDF}	CONV Input Voltage, Differential (Figure 2)	0.3		1.2	V
t_{PWL}	CONV Pulse Width, LOW	4			ns
t_{PWH}	CONV Pulse Width, HIGH	4			ns
t_S	Setup Time, Data and Controls	4.0			ns
t_H	Hold Time, Data and Controls	0			ns
V_{IL}	Input Voltage, Logic LOW			-1.49	V
V_{IH}	Input Voltage, Logic HIGH	-1.045			V
I_{REF}	Reference Current Video standard output levels[1]	1.10	1.17	1.24	mA
	6-bit linearity	1.0		1.3	mA
C_C	Compensation Capacitor	1000	2700		pF
T_A	Ambient Temperature, Still Air	0		70	°C

Note: 1. Minimum and Maximum values allowed by ±5% variation given in RS343A and RS170 after intitial gain correction of device.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Units
$I_{EEA}+I_{EED}$	Supply Current	$V_{EEA} = V_{EED}$ = Max, static[1]			
		T_A = 0°C to 70°C		-145	mA
		T_A = 70°C		-130	mA
C_{REF}	Equivalent Input Capacitance, REF+, REF-			5	pF
C_I	Input Capacitance, Data and Controls			5	pF
V_{OCP}	Compliance Voltage, + Output		-1.2	+1.5	V
V_{OCN}	Compliance Voltage, - Output		-1.2	+1.5	V
R_O	Equivalent Output Resistance		50		K
C_O	Equivalent Output Capacitance			20	pF
I_{OP}	Max Current, + Output	V_{EEA} = Nom, SYNC = BLANK = 0, BRT = 1	30		mA
I_{ON}	Max Current, - Output	V_{EEA} = Nom, SYNC = 1	30		mA
I_{IL}	Input Current, Logic LOW, Data and Controls	V_{EED} = Max, V_I = -1.49V		200	μA
I_{IH}	Input Current, Logic HIGH, Data and Controls	V_{EED} = Max, V_I = -1.045V		200	μA
I_{IC}	Input Current, Convert	V_{EED} = Max, $-2.5 < V_I < -0.5$		50	μA

Note:
1. Worst case over all data and control states

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Data Rate	V_{EEA}, V_{EED} = Min	200		MSPS
t_{DSC}	Clock to Output Delay	V_{EEA}, V_{EED} = Min		8	ns
t_{SI}	Current Settling Time, Clocked Mode	V_{EEA}, V_{EED} = Min, 3.2%		5	ns
t_{RI}	Rise Time, Current	10% to 90% of Gray Scale		2.0	ns

System performance characteristics within specified operating conditions

B

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error Integral, Terminal Based	V_{EEA}, V_{EED}, I_{REF} = Nom		0.8	% of Gray Scale
E_{LD}	Linearity Error Differential	V_{EEA}, V_{EED}, I_{REF} = Nom		0.8	% of Gray Scale
I_{OF}	Output Offset Current	V_{EEA}, V_{EED} = Max, SYNC = BLANK = 0, BRT = 1		10	μA
EG	Absolute Gain Error	V_{EEA}, V_{EED} = Min		6	% of Gray Scale
TC_G	Gain Error Tempco	I_{REF} = Nom		0.01	% of Gray Scale/°C
BWR	Reference Bandwidth, -3dB	C_C = Min, V_{REF} = 1mV p-p	1		MHz
PSRR	Power Supply Rejection Ratio	V_{EEA}, V_{EED}, I_{REF} = Nom[1]		45	dB
		V_{EEA}, V_{EED}, I_{REF} = Nom[2]		46	dB
PSS	Power Supply Sensitivity	V_{EEA}, V_{EED}, I_{REF} = Nom		120	μA/V
G_C	Peak Glitch Charge[3,4]			800	fCoulomb
G_I	Peak Glitch Current			1.2	mA
G_E	Peak Glitch "Energy" (Area)[4]			30	pV-Sec
FT_C	Feedthrough Clock[5]	Data = Constant BW = 250MHz		-36	dB
		BW = 50MHz		-50	dB
FT_D	Feedthrough Data[5]	CONV = Constant BW = 250MHz		-42	dB
		BW = 50MHz		-50	dB

Notes:

1. 20KHz, 0.75V p-p ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
2. 60Hz, 0.75V p-p ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
3. fCoulombs = microamps x nanoseconds.
4. 37.5 Ω load. Because glitches tend to be symmetric, average glitch energy approaches zero.
5. dB relative to full gray scale.

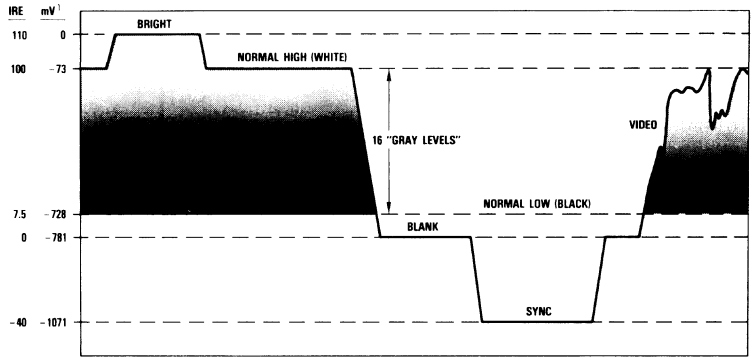
Table 1 Video Control Truth Table

Sync	Blank	Bright	Data Input	Out– (mA)[1]	Out– (V)[2]	Out– (IRE)[3]	Description[4]
1	X	X	X	28.57	–1.071	–40	Sync Level
0	1	X	X	20.83	–0.781	0	Blank Level
0	0	0	0000	19.40	–0.728	7.5	Normal Low Level
0	0	0	1111	1.95	–0.073	100	Normal High Level
0	0	1	0000	17.44	–0.654	7.5	Enhanced Low Level
0	0	1	1111	0.00	0.00	110	Enhanced High Level

Notes:

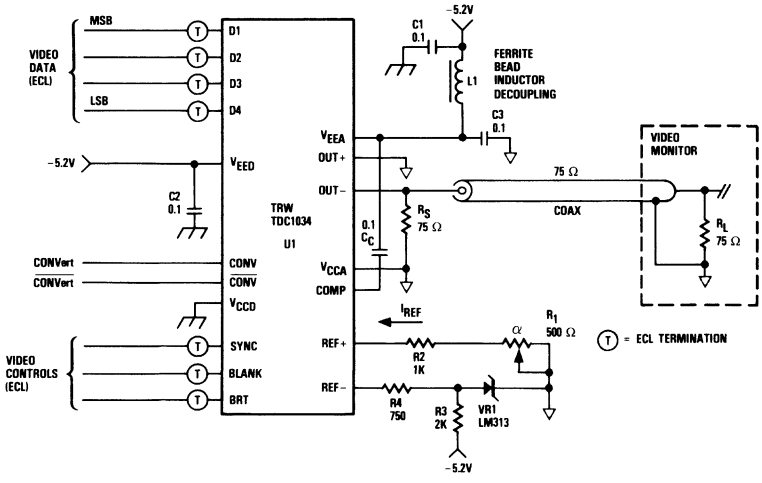
1. Out+ is complementary to Out–. Current is specified as conventional current when flowing into the device.
2. Voltage produced when driving the standard load configuration (37.5 Ohms to V_{CCA}). See Figure 5.
3. 140 IRE units = 1.00V.
4. RS-343-A tolerance on all control values is assumed.

Figure 6. Video Output Waveform for Out– and Standard Load Configuration



Note: 1. Output voltage is measured with standard load connected between Out– and V_{CCA}.

Figure 7. Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1034B8C	STD – T_A = 0°C to 70°C	Commercial	18 Pin CERDIP	1034B8C

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TDC1041 Monolithic Digital To Analog Converter
10 Bit, 20Msps, 12ns Settling Time

The TDC1041 is a TTL compatible, 10-bit monolithic D/A converter capable of converting digital data into an analog current or voltage at data rates in excess of 20 Mega-samples-per second (Msps).

The analog circuitry has been optimized for dynamic performance, with very low glitch energy. The output is able to drive a 50Ω load with a 1 Volt output level while maintaining low harmonic distortion.

Data registers are incorporated on the TDC1041. This eliminates data skew encountered with external registers and latches and minimizes the glitches that can adversely affect many applications.

Features

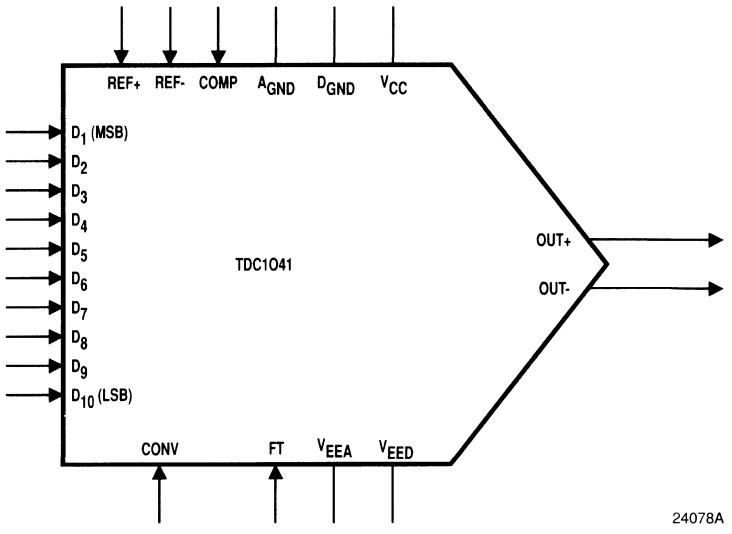
- 10-Bit Resolution
- 20 Msps Data Rate
- TTL Inputs
- Very Low-Glitch With No Track And Hold Circuit Needed
- Dual +4dBm (1V Into 50Ω) Outputs Make Output Amplifiers Unnecessary In Many Applications

Applications

- Test Signal Generation
- Arbitrary Waveform Synthesis
- Broadcast And Studio Video
- High-Resolution A/D Converters

B

Interface Diagram



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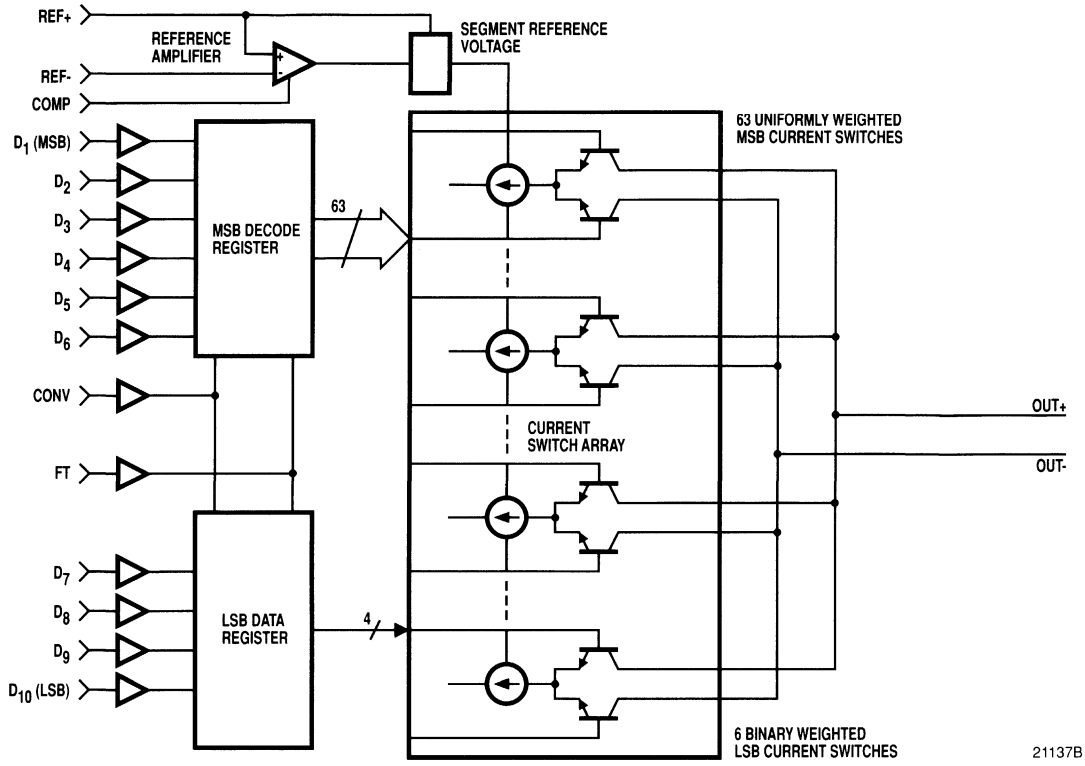
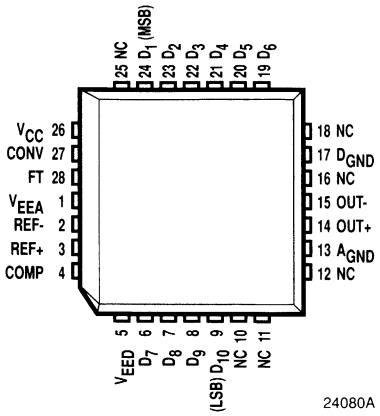
Functional Block Diagram



Pin Assignments



28 Leaded Plastic Chip Carrier – R3 Package

Functional Description

General Description

The TDC1041 consists of five major circuit sections: the LSB data register, the MSB decode block, the decoded MSB register, the current switch array, and the reference amplifier. All data bits are registered just before the current switches to minimize the temporal skew that would generate glitches.

Power, Grounds

The TDC1041 requires a –5.2V power supply and a +5.0V power supply. The analog (V_{EEA}) and digital (V_{EED}) supply voltages should be decoupled from each other, as shown in the *Typical Interface Circuit*. The V_{CC} pin should be considered a digital power supply. The 0.1µF decoupling capacitors should be placed as close as possible to the power pins. The inductors are simple ferrite beads and are neither critical in value nor always required.

Reference and Compensation

The TDC1041 has two reference inputs: REF+ and REF– These are the inverting and noninverting inputs of the internal reference amplifier. An externally generated reference voltage is applied to the REF- pin. Current flows into the REF+ pin through an external current setting resistor (R_{REF}). This current is the reference current (I_{REF}) which serves as an internal reference for the current source array. The output current for an input code N from OUT+ is related to I_{REF} through the following relationship:

$$I_{OUT} = N \times \frac{I_{REF}}{16}$$

Where N is the value of the input code.

This means that with an I_{REF} that is nominally 625μA, the full-scale output is 40mA, which will drive a 50Ω load in parallel with a 50Ω transmission line (25Ω total load) with a 1V peak to peak signal. The impedance seen by the REF– and REF+ pins should be approximately equal so that the effect of amplifier input bias current is minimized. When driving a 75Ω load, the reference current must be reduced. This can be done by increasing the value of the resistor from REF+ to ground.

The internal reference amplifier is externally compensated to ensure stability. A 0.1μF capacitor should be connected between the COMP pin and V_{EEA}.

Digital Inputs

The data inputs are TTL compatible. One of the effects that leads to degradation of the dynamic performance of the device is the capacitive feedthrough from the digital inputs to the analog output of the device. One method of reducing the effect of capacitive coupling is to slow down the slew rates of the digital inputs. This can be done in many ways, starting with the selection of a logic family that is no faster than what is needed, and can include the addition of 50Ω series resistors to the data lines.

Clock and Feedthrough Control

The TDC1041 requires a TTL clock signal (CONV). Data is synchronously entered on the rising edge of CONV. The CONV input is ignored in the Feedthrough (FT = HIGH) mode. The Feedthrough (FT) pin is normally held LOW, where the TDC1041 operates in a clocked mode (the output changes only after a clock rising edge). An internal pull-down resistor is provided, and this pin may be left open for clocked operation.

For certain applications, such as high-precision successive approximation A/D converters, throughput delay may be more important than glitch performance. In these cases, the FT pin may be brought HIGH, which makes the input registers transparent. This allows the analog output to change immediately and asynchronously in response to the digital inputs.

Since skew in the bits of the input word will result in glitches, and will affect settling time, it is recommended that the TDC1041 be operated in clocked mode for most applications.

Analog Outputs

Two simultaneous and complementary analog outputs are provided. Both of these outputs are full-power current sources. By loading the current source outputs with a resistive load, they may be used as voltage outputs. OUT+ provides a 0 to –40mA output current (0 to –1V when terminated in 25Ω) as the input code varies from 00 0000 0000 to 11 1111 1111. OUT– varies in a complementary manner from –40 to 0mA (–1 to 0V when terminated with 25Ω) over the same code range. (See the *Input Coding Table*.) The output current is proportional to the reference current and the input code.

No Connect

These pins have no internal connection and should be left open for optimal performance.

Package Interconnections

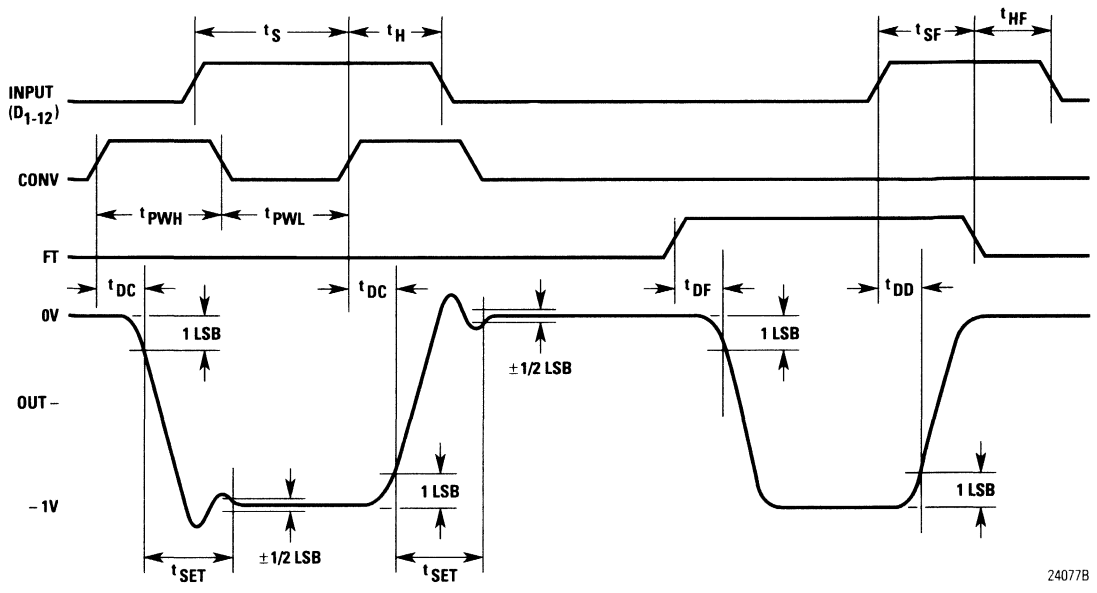
Signal Type	Signal Name	Function	Value	R3 Package Pins
Power	A_{GND}	Analog Ground	0.0V	13
	D_{GND}	Digital Ground	0.0V	17
	V_{EEA}	Analog Supply Voltage	–5.2V	1
	V_{EED}	Digital Supply Voltage	–5.2V	5
	V_{EED}	Digital Supply Voltage	–5.2V	26
Reference	REF–	Reference Voltage Input	–1.0V	2
	REF+	Reference Current Input	–625µA	3
	COMP	Compensation Capacitor	0.1µF, see text	4
Data Inputs	D_1 (MSB)	Most Significant Bit	TTL	24
	D_2		TTL	23
	D_3		TTL	22
	D_4		TTL	21
	D_5		TTL	20
	D_6		TTL	19
	D_7		TTL	6
	D_8		TTL	7
	D_9		TTL	8
	D_{10} (LSB)	Least Significant Bit	TTL	9
Feedthrough	FT	Feedthrough Mode Control	TTL	28
Convert	CONV	Convert (Clock) Input	TTL	27
Analog Output	OUT+	Analog Output	0 to 40mA	14
	OUT–	Analog Output	40 to 0mA	15
No Connect	NC	No Internal Connection	Open	10,11,12,16,18,25

Input Coding Table[1]

Input Data MSB LSB	OUT+ (mA)	V_{OUT+}(mV)	OUT– (mA)	V_{OUT-}(mV)
00 0000 0000	0.000	0.00	40.000	–1000.00
00 0000 0001	0.039	–0.97	39.961	–998.05
00 0000 0010	0.078	–1.95	39.922	–998.05
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
0111 1111 11	19.961	–499.03	20.000	–500.00
1000 0000 00	20.000	–500.00	19.961	–499.03
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
1111 1111 01	39.922	–998.05	0.078	–1.95
1111 1111 10	39.961	–999.03	0.039	–0.97
1111 1111 11	40.000	–1000.00	0.000	0.0

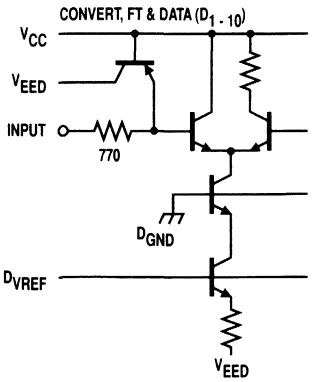
Note: 1. I_{REF} = 625µA, R_{LOAD} = 25Ω

Figure 1. Timing Diagram



B

Figure 2. Equivalent Reference and Output Circuits



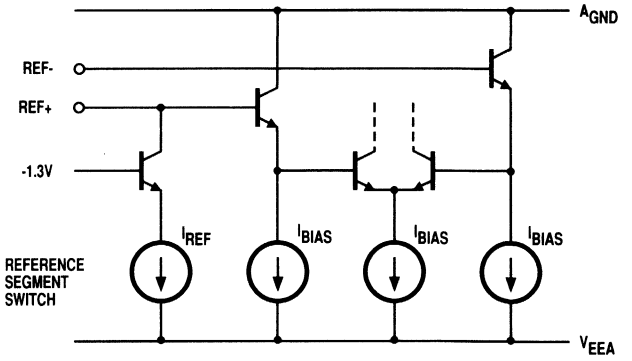


Figure 3. Simplified Reference and Output Circuits

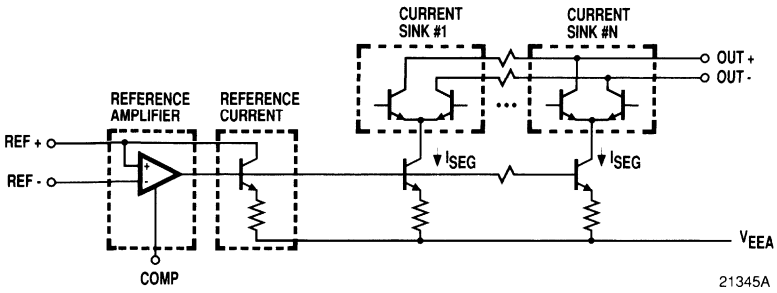
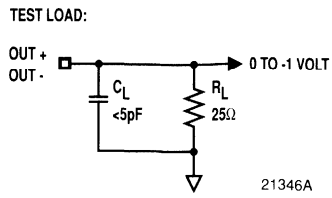


Figure 4. Output Test Load



Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltages

V_{CC}	(measured to D_{GND})	–0.5 to +7.0V
V_{EEA}	(measured to A_{GND})	–7.0 to +0.5V
V_{EEA}	(measured to V_{EED})	–50 to +50mV
V_{EED}	(measured to D_{GND})	–7.0 to +0.5V
A_{GND}	(measured to D_{GND})	–0.5 to +0.5V

Inputs

CONV, FT, $D_{1\text{-}10}$ (measured to D_{GND})[2]	V_{CC} +0.5 to –0.5V
CONV, FT, $D_{1\text{-}10}$ Current, externally forced[3]	±3mA
REF+, REF-,applied voltage (measured to A_{GND})[3]	V_{EEA} to +0.5V
REF+, REF-, current, externally forced[3]	±3mA

Outputs

OUT+, OUT–, applied voltage (measured to A_{GND})[2]	–2.0 to +2.0V
OUT+, OUT–, current, externally forced[3]	+50mA
Short-circuit duration (single output to GND)	unlimited

Temperature

Operating, ambient	
(Plastic Package)	–20 to +90°C
(Ceramic Package)	–60 to +150°C
Junction	
(Plastic Package)	+140°C
(Ceramic Package)	+200°C
Lead, soldering (10 seconds)	+300°C
Storage	–65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{CC}	Positive Supply Voltage (Measured to D_{GND})	4.75	5.0	5.25	V
V_{EED}	Negative Supply Voltage (Measured to D_{GND})	–4.9	–5.2	–5.5	V
V_{EEA}	Negative Supply Voltage (measured to A_{GND})	–4.9	–5.2	–5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	–0.1	0.0	0.1	V
V_{EEA}	Negative Supply Voltage (Measured to V_{EED})[1]	–20	0	20	mV
t_{PWL}	CONV Pulse Width LOW (to Meet Specification)	20			ns
t_{PWH}	CONV Pulse Width HIGH (to Meet Specifications)	20			ns
t_S	Setup Time, Data to CONV (to Meet Specification)	25			ns
t_H	Hold Time (to Meet Specifications)	1			ns
t_{SF}	Setup Time, Data to FT	5			ns
t_{HF}	Hold Time, Data to FT	28			ns
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
V_{REF}	Reference Voltage (REF–)	–0.7	–1.0	–1.3	V
I_{REF}	Reference Current (REF+)	400	625	700	µA
C_C	Compensation Capacitor	0.01	0.1		µF
T_A	Ambient Temperature, Still Air	0		70	°C

Note 1 A common power supply isolated with ferrite bead inductors is recommended for V_{EEA} and V_{EED}. This is shown in the *Typical Interface Circuit*.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Units
$I_{EEA}+I_{EED}$		$V_{EEA}=V_{EED}$=Max, static T_A=0 to 70°C		–180	mA
		T_A=70°C		–150	mA
I_{CC}		V_{CC}=Max, Static T_A=0 to 70°C		25	mA
		T_A=70°C		20	mA
C_{REF}	Reference Input Capacitance			15	pF
C_I	Digital Input Capacitance			15	pF
V_{OC}	Compliance Voltage		–1.2	1.2	V
R_O	Output Resistance		12		kΩ
C_O	Output Capacitance			45	pF
I_O	Full-Scale Output Current	I_{REF}=Nominal	40		mA
I_{IL}	Input Current, Logic LOW	V_{CC},V_{EE}=Max , V_I=0.4V	–10	50	µA
I_{IH}	Input Current, Logic HIGH	V_{CC},V_{EE}=Max, V_I=2.4V	–10	100	µA
I_{IM}	Input Current, Max Input Voltage	V_{CC},V_{EE}=Max, V_I=V_{CC} Max	–10	100	µA
V_{TH}	Logic Input Threshold Voltage,Typical	V_{CC},V_{EE}=Nom, T_A=25°C	1.25	1.55	V

Switching characteristics

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Typ	Standard Max	Units
F_D	Maximum Data Rate	V_{EEA}, V_{EED}, V_{CC}=Min	20	25		MHz
t_{DC}	Clock to Output Delay	V_{EEA}, V_{EED}, V_{CC}=Min, FT=LOW			17	ns
t_{DD}	Data to Output Delay	V_{EEA}, V_{EED}, V_{CC}=Min, FT=HIGH			35	ns
t_{DF}	FT to Output Delay	V_{EEA}, V_{EED}, V_{CC}=Min			35	ns
t_R	Risetime	90% to 10% of FSR, FT=LOW			4	ns
t_F	Falltime	10% to 90% of FSR, FT=LOW			4	ns
t_{SET}	Settling Time, Voltage	FT=LOW, Full-Scale Voltage transition on I_{OUT} to ±0.0188%FSR		20	30	ns

System performance characteristics

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Typ	Standard Max	Units
E_{LD}	Differential Linearity Error	V_{EEA}, V_{EED}, I_{REF} = Nom[1]				
		TDC1041			±0.1	%
		TDC1041-1			±0.05	%
E_{LI}	Integral Linearity Error	V_{EEA}, V_{EED}, I_{REF} = Nom[1]				
		TDC1041			±0.1	%
		TDC1041-1			±0.05	%
V_{OS}	REF+ to REF- Offset Voltage		-10		+10	mV
I_B	REF- Input Bias Current				5	µA
E_G	Absolute Gain Error	V_{EEA}, V_{EED}, V_{CC}, I_{REF}= Nom	-5		5	%
I_{OF}	Output Offset Current	V_{EEA}, V_{EED}, V_{CC}= Min, $D_{1\text{-}10}$=LOW	-5		+5	A
PSRR	Power Supply Rejection Ratio	V_{EEA}, V_{EED}, V_{CC},I_{REF}= Nom[2]			-50	dB
PSS	Power Supply Sensitivity	V_{CC}, V_{EEA}, V_{EED}=4%, I_{REF}= Nom			-140	µA/V
G_A	Peak Glitch Area			25	45	pV-sec
SFDR	Spurious Free Dynamic Range	I_{REF}=Nom, 20 Msps, 10MHz bandwidth F_{out}=6MHz	60			dBc
		F_{out}=5MHz		70		dBc
		F_{out}=2MHz		75		dBc
		F_{out}=1MHz		78		dBc

Note: 1. OUT– connected to A_{GND}, OUT– driving virtual ground.

2. 120Hz, 0.6Vp-p ripple on V_{EEA} and V_{EED}. dB relative to 0.6Vp-p ripple input.

Applications Information

There are three major D/A architectures: segmented, weighted current sources, and R-2R. In segmented there is one current source for each possible output level. The current sources are equally weighted and for an input code of N, N current sources are turned on. An N bit segmented D/A has 2^N current sources. A weighted current source D/A has one current source for each bit of input with a binary weighting for the current sources. In an R-2R D/A, there is one current source per bit, and a resistor network which scales the current sources to have a binary weighting.

When transitioning from a code of 0111111111 to 100000000000, both the R-2R D/A and Binary weighted D/A are turning some current sources on while turning others off. If the timing is not perfect, there is a moment where all current sources are either on or off, resulting in a glitch. In a segmented architecture, 511 of the current sources remain on, and one more is turned on to increment the output no possibility of a glitch.

The TDC1041 uses a hybrid architecture with the 6 MSBs segmented, and the 4 LSBs from a R-2R network. The result is a converter which has very low-glitch energy, and a moderate die size.

Layout, Power and Grounding

The layout of grounds in any system is an important design consideration. Separate analog and digital grounds are provided at the TDC1041. All ground pins should be connected to a common low-noise, low-impedance groundplane. This groundplane should be common for the TDC1041 and all of its immediate interface circuitry, which includes all of the reference circuitry, the output load circuitry, and all of the power supply decoupling components.

The digital driving logic should use a separate system ground, and this ground should be connected (typically through a ferrite bead inductor) to the analog groundplane in only one place. The analog and digital grounds may be connected in other ways if required by the user's system grounding plan, however, the voltage differential between the A_{GND} and D_{GND} pins must be held to within ±0.1 Volts.

Direct Digital Synthesis Applications

There are many factors that can influence the system performance of a direct digital synthesizer. The following comments are directed at getting the best possible performance from the TDC1041, as measured by Spurrious Free Dynamic Range (SFDR).

The termination of the output pins has an effect on DAC performance. For most synthesis applications, optimum signal purity is obtained with the use of a balun (a simple RF transformer made by wrapping a few turns of wire around a ferrite core). This configuration has the benefit of cancelling common mode distortion.

Harmonic distortion may improve even further with reduced AC termination impedance values, at the expense of lowered output voltage.

An output amplifier is not recommended because any amplifier will add extra distortion of its own, which is likely to be much greater than that present from the direct outputs of the TDC1041.

One detrimental effect in DAC performance is capacitive coupling of the digital data into the output terminal. The actual digital-data waveform which represents a sine wave contains strong harmonics of that sine wave. This can be seen by connecting a digital data line to the input of an analog spectrum analyzer. Therefore data feedthrough to the analog output of a system due to improper board layout or system shielding and grounding will appear as additional harmonic distortion, adversely affecting SFDR.

The strict adherence to at least the minimum input data setup and hold times is important for the realization of the optimal performance. Spur levels may decrease as setup and hold times are increased. It is possible to achieve even higher performance in some instances by carefully "tuning" the input data setup and hold times (slightly delaying or advancing the CONV signal in relation to the data) fed to the TDC1041. The ***Operating conditions*** table has two sets of data for t_S and t_H, one which guarantees performance of the device in most applications, and one, more conservative specification which has been found to be optimal for DDS applications.

The purity of the output of the TDC1041 is greater than that which can be measured by many spectrum analyzers. The spectral plots shown in this data sheet were generated with an HP8568B, which has a noise floor barely below that of the TDC1041, once the TDC1041 performance has been optimized. When making spectral measurements it is important to remember that the TDC1041 output power is +4dBm, which is greater power than many analyzers are

equipped to handle without adding distortion of their own. Accordingly, it may be necessary to introduce an attenuator to the input of the spectrum analyzer to see the true DAC performance.

Output Termination

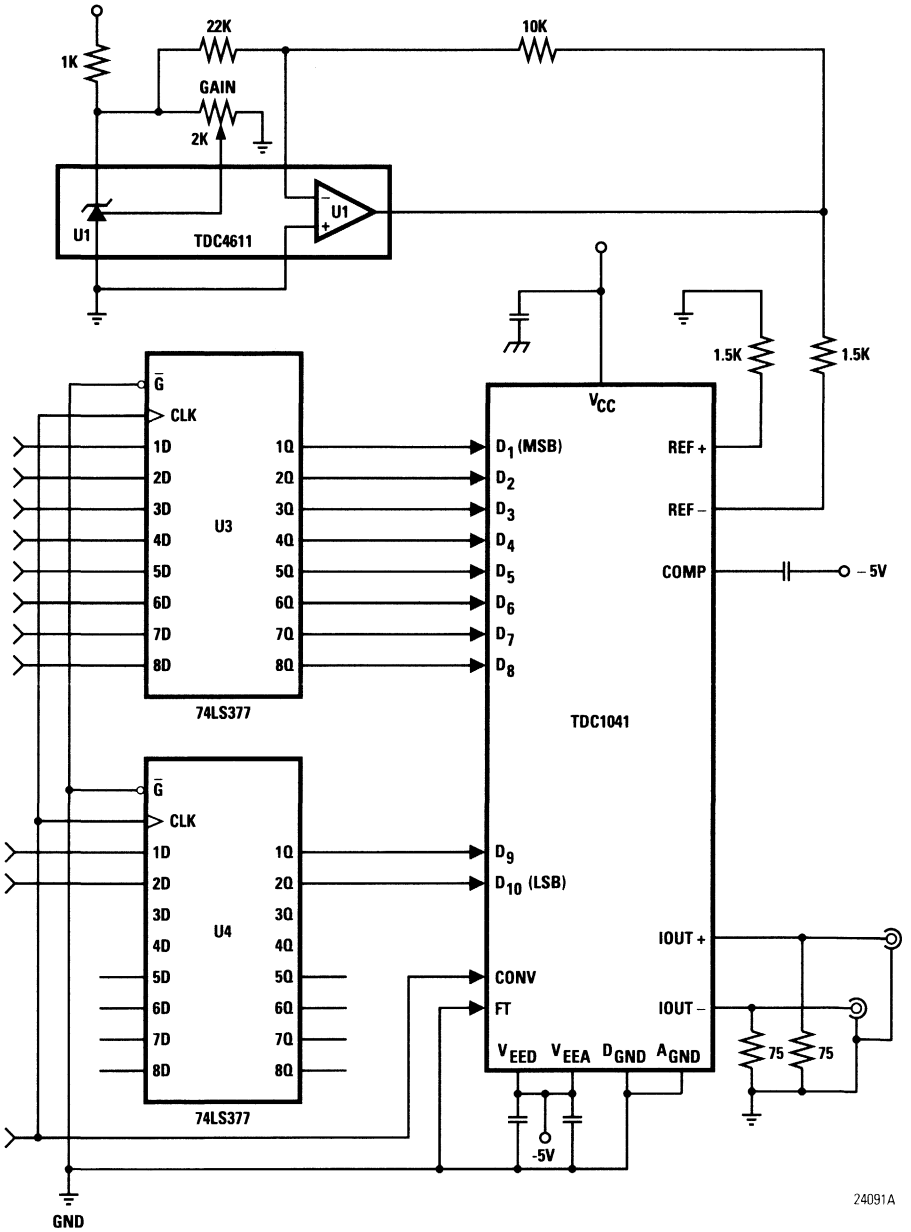
The recommended output termination is 25Ω. This can be provided by placing a 50Ω source resistor between the output pin and ground, then driving a 50Ω transmission line. With this load, the output voltage range of the converter is 0 to –1.0V. If a load is capacitively coupled to the TDC1041, it is recommended that a 25Ω load at DC, as seen by the TDC1041, continue to be maintained. The output voltage should be kept within the output compliance voltage range, V_{OC}, as specified in the ***Electrical Characteristics*** table, or the accuracy may be impaired.

Optimum DC linearity is obtained by using a differential output either with a balun, or an operational amplifier in the differential mode. If it is desired that the TDC1041 be operated in a single ended fashion, the unused output should be connected directly to ground as is shown in ***Figure 5***. The CONV signal provided to the TDC1041 must be as free from clock jitter as possible. Clock jitter is the random cycle-to- cycle variation in clock period. CONV clock jitter will effectively appear at the output as phase noise. A value of 10ps or less for clock jitter is recommended for the highest performance applications. Ordinary crystal oscillators are satisfactory. High-performance synthesizers, such as the HP8662, used to trigger a precision pulse generator, are also satisfactory, although not as jitter free as a crystal oscillator.

Driving a 75Ω Transmission line

The TDC1041 has been optimized to operate with a reference current of 625μA. Significantly increasing or decreasing this current may degrade the performance of the device. If it is desired that the device drive a 37.5Ω load (75Ω source termination driving 75Ω transmission line) rather than the 25Ω suggested load, then V_{REF} should be held at 1V and I_{REF} reduced to 417μA. This will result in a 1V p-p voltage being generated at the DAC output.

Figure 5. Typical Interface Circuit



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1041R3C	T_A=0°C to 70°C	Commercial	Plastic Chip Carrier	1041R3C
TDC1041R3C1	T_A=0°C to 70°C	Commercial	Plastic Chip Carrier	1041R3C1

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Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded. Applied voltage must be current limited to specified range. Forcing voltage must be limited to specified range. Current is specified as conventional current flowing into the device.

TDC1112

Monolithic D/A Converter

12-Bit, 50Msps
12ns Settling Time to 0.1%, 70dB SFDR

The TDC1112 is an ECL compatible, 12-bit monolithic D/A converter capable of converting digital data into an analog current at data rates in excess of 50Msps (MegaSample Per Second).

The analog performance has been optimized for dynamic performance, with very low glitch energy. The output is able to drive a 50Ω load with 1V outputs while keeping a spurious-free-dynamic range greater than 70dB.

Data registers are incorporated on the chip. This eliminates the temporal data skew encountered with external registers and latches and minimizes the glitches that can adversely affect many applications.

Features

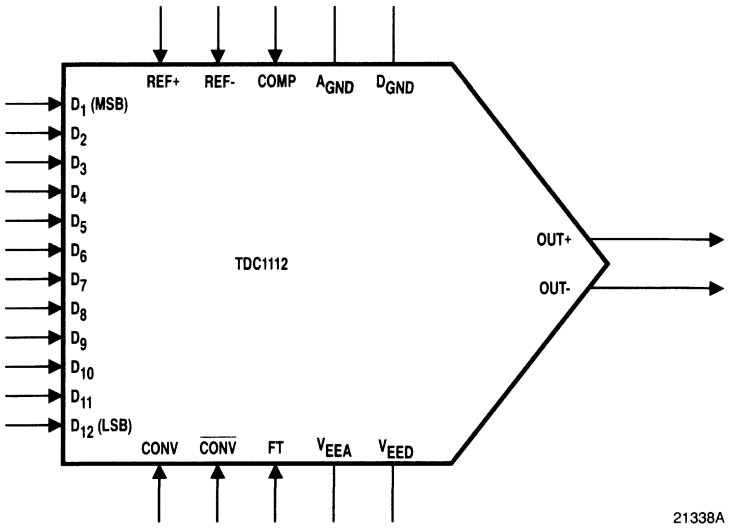
- 12-Bit Resolution
- 50Msps Data Rate
- ECL Inputs
- Very Low Glitch – No Track And Hold Circuit Needed
- Dual +4dBm (1V Into 50Ω) Outputs Make Output Amplifiers Unnecessary In Many Applications
- 70dB Typical Spurious-Free-Dynamic-Range
- Available Compliant To MIL-STD-883C

Applications

- Direct Digital RF Signal Generation
- Test Signal Generation
- Arbitrary Waveform Synthesis
- Broadcast And Studio Video
- High-Resolution A/D Converters

B

Interface Diagram



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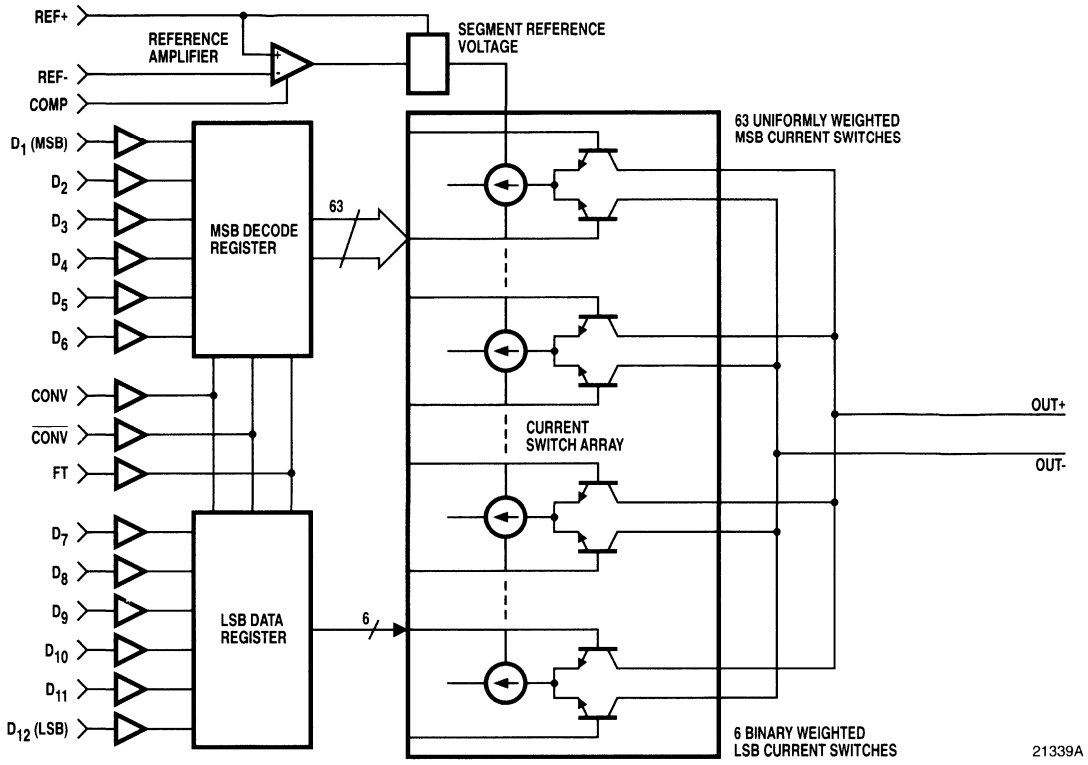
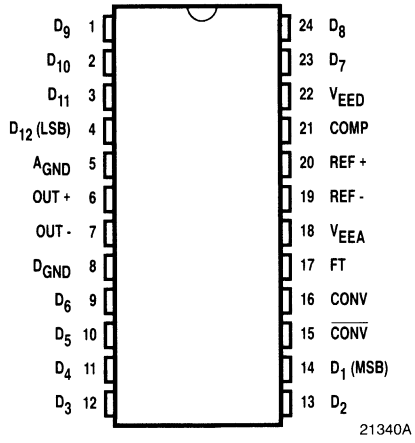
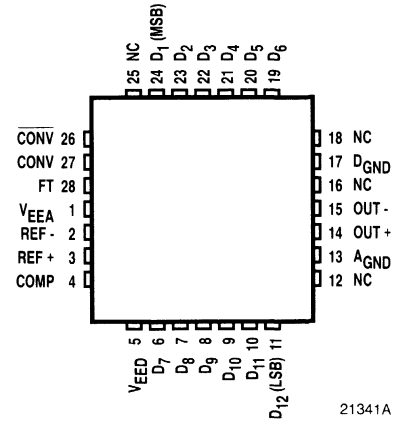
Functional Block Diagram



Pin Assignments



24 Pin Hermetic Ceramic DIP – J7 Package
24 Pin Plastic DIP – N7 Package



28 Contact Chip Carrier – C3 Package
28 Leaded Plastic Chip Carrier – R3 Package

Functional Description

General Information

The TDC1112 consists of five major circuit sections: the LSB data register, the MSB decode block, the decoded MSB register, the current switch array, and the reference amplifier. All data bits are registered just before the current switches to minimize the temporal skew that would generate glitches.

There are three major D/A architectures: thermometer code segmentation, weighted current sources, and R−2R. In thermometer code segmentation there is one current source for each possible output level. The current sources are equally weighted and for an input code of N, N current sources are turned on. An N bit segmented D/A has 2^N current sources. A weighted current source D/A has one current source for each bit of input with a binary weighting for the current sources. In an R−2R D/A, there is one current source per bit, and a resistor network which scales the current sources to have a binary weighting.

When transitioning from a code of 011111111111 to 100000000000, both the R−2R D/A and binary weighted D/A are turning some current sources on while turning others off. If the timing is not perfect, there is a moment where all current sources are either on or off, resulting in a glitch. In a segmented architecture, 2047 of the current sources remain on, and one more is turned on to increment the output-no possibility of a glitch.

The TDC1112 uses a hybrid architecture with the 6 MSBs segmented, and the 6 LSBs from a R−2R network. The result is a converter which has very low glitch energy, and a moderate die size.

Power, Grounds, and Layout

The TDC1112 requires a single −5.2V power supply. The analog (V_{EEA}) and digital (V_{EED}) supply voltages should be decoupled from each other, as shown in the ***Typical Interface Circuits***, to provide the highest noise immunity. The 0.1μF decoupling capacitors should be placed as close as possible to the power pins. The inductors are simple ferrite beads and are neither critical in value nor always required.

The high slew-rates of digital data make capacitive coupling with the D/A output a real problem. Since the digital signals contain high-frequency harmonics of the clock, as well as the signal that is being provided to the DAC, the result of data feedthrough often looks like harmonic distortion which degrades the Spurious-Free-Dynamic-Range (SFDR) performance of the D/A.

The layout of grounds in any system is an important design consideration. Separate analog and digital grounds are provided at the TDC1112. All ground pins should be connected to a common low-noise, low-impedance groundplane. This groundplane should be common for the TDC1112 and all of its immediate interface circuitry, which includes all of the reference circuitry, the output load circuitry, and all of the power supply decoupling components.

The digital driving logic should use a separate system ground, and this ground should be connected (typically through a ferrite bead inductor) to the analog groundplane in only one place. The analog and digital grounds may be connected in other ways if required by the user's system grounding plan, however, the voltage differential between the A_{GND} and D_{GND} pins must be held to within ±0.1V.

Reference

The TDC1112 has two reference inputs: REF+ and REF−. These are the inverting and noninverting inputs of the internal reference amplifier. An externally generated reference voltage is applied to the REF− pin. Current flows into the REF+ pin through an external current setting resistor (R_{REF}). This current is the reference current (I_{REF}) which serves as an internal reference for the current source array. The output current for an input code N from OUT+ is related to I_{REF} through the following relationship:

$$I_{OUT}\,(\text{Input Code N}) = N \times \frac{I_{REF}}{64}$$

This means that with an I_{REF} that is nominally 625μA, the full scale output is 40mA, which will drive a 50Ω load in parallel with a 50Ω transmission line (25Ω load total) with a 1V peak-to-peak signal. The impedance seen by the REF− and REF+ pins should be approximately equal so that the effect of amplifier input bias current is minimized.

Reference (cont.)

The TDC1112 has been optimized to operate with a reference current of 625μA. Significantly increasing or decreasing this current may degrade the performance of the device. The minimum and maximum values for V_{REF} and I_{REF} are listed in the ***Operating Conditions Table***.

The internal reference amplifier is externally compensated to assure stability. To compensate this amplifier, a 0.1μF capacitor should be connected between the COMP pin and V_{EEA}. The amplifier has been optimized to minimize the TDC1112 settling time, and as a result should be considered a DC amplifier. Performance of the TDC1112 operating in a multiplying D/A mode is not guaranteed.

A typical interface circuit that includes a stable, adjustable reference circuit is shown in ***Figures 9a-c***.

Digital Inputs

The data inputs are single-ended ECL compatible. The TDC1112 is specified with two sets of setup and hold times. One of these pairs of specifications guarantees the performance of the TDC1112 to specifications listed in the minimum and maximum columns of the ***System Performance Characteristics Table***. The second more rigid specification is recommended for applications where lowest possible glitch and highest SFDR are desired. The more stringent t_S and t_H insure that the data will not be slewing during times critical to the TDC1112, and will hence minimize the effects of capacitively coupled data feedthrough and optimize SFDR performance. Another method reducing the effect of capacitive coupling is to slow down the slew rates of the digital inputs. This has been done in the circuit shown in ***Figures 9a-c*** by the addition of 50Ω series resistors to the data lines.

Clock and Feedthrough Control

The TDC1112 requires an ECL clock signal (CONVert and $\overline{\text{CONVert}}$). Even though complementary operation is preferred, a single-ended signal may be used if either unused CONV input is biased at a DC voltage midway between the active input's V_{IH} and V_{IL} levels.

Data is synchronously entered on the rising edge of CONV (the falling edge of $\overline{\text{CONV}}$). The CONV input is ignored in the Feedthrough (FT=HIGH) mode.

The Feedthrough (FT) pin is normally held LOW, in which case the TDC1112 operates in a clocked mode (the output changes only after a clock rising edge). An internal pull-down resistor is provided, and this pin may be left open for clocked operation. For certain applications, such as high-precision successive approximation A/D converters, speed may be more important then glitch performance. In these cases, the FT pin may be brought HIGH, which makes the input registers transparent. This allows the analog output to change immediately and asynchronous in response to the digital input, without the need for a clock.

Since skew in the bits of the input word will result in glitches, and may affect settling time, it is recommended that the TDC1112 be operated in clocked mode for most applications.

Analog Outputs

Two simultaneous and complementary analog outputs are provided. Both of these outputs are full-power current sources. By loading the current source outputs with a resistive load, they may be used as voltage outputs. OUT+ provides a 0 to −40mA output current (0 to −1V when terminated in 25Ω) as the input code varies from 0000 0000 0000 to 1111 1111 1111. OUT− varies in a complementary manner from −40 to 0mA (−1 to 0V when terminated with 25Ω) over the same code range. (See the ***Output Coding Table***.) The output current is proportional to the reference current and the input code.

The recommended output termination is 25Ω. This can be provided by placing a 50Ω source resistor between the output pin and ground, then driving a 50Ω transmission line. With this load, the output voltage range of the converter is 0 to −1.0V. If a load is capacitively coupled to the TDC1112, it is recommended that a 25Ω load at DC, as seen by the TDC1112, continue to be maintained. The output voltage should be kept within the output compliance voltage range, V_{OC}, as specified in the ***Electrical Characteristics Table***, or the accuracy may be impaired.

See ***Figure 9b*** for a suggested circuit for achieving a bipolar output voltage range. Optimum DC linearity is obtained by using a differential output either with a balun, or an operational amplifier in the differential mode. If it is desired that the TDC1112 be operated in a single ended fashion, the unused output should be connected directly to ground as is shown in ***Figure 9c***.

Package Interconnections

Signal Type	Signal Name	Function	Value	J7, N7 Package Pins	C3, R3 Package Pins
Power	V_{EEA}	Analog Supply Voltage	−5.2V	18	1
	V_{EED}	Digital Supply Voltage	−5.2V	22	5
	A_{GND}	Analog Ground	0.0V	5	13
	D_{GND}	Digital Ground	0.0V	8	17
Reference	REF−	Reference Voltage Input	−1.0V	19	2
	REF+	Reference Current Output	−0.625mA	20	3
	COMP	Compensation Capacitor	0.1μF, See Text	21	4
Data Input	D_1 (MSB)	Most Significant Bit Input	ECL	14	24
	D_2		ECL	13	23
	D_3		ECL	12	22
	D_4		ECL	11	21
	D_5		ECL	10	20
	D_6		ECL	9	19
	D_7		ECL	23	6
	D_8		ECL	24	7
	D_9		ECL	1	8
	D_{10}		ECL	2	9
	D_{11}		ECL	3	10
	D_{12} (LSB)	Least Significant Bit Input	ECL	4	11
Feedthrough	FT	Feedthrough Mode Control	ECL	17	28
Convert (Clock)	CONV	Convert (Clock) Input	ECL	16	27
	$\overline{CONV}$	Convert (Clock) Input	ECL	15	26
Analog Output	OUT+	Analog Output	0 to −40mA	6	14
	OUT−	Analog Output	−40 to 0mA	7	15

B

Output Coding Table [1]

Input Data MSB		D_{1-12} LSB	OUT+ (mA)	V_{OUT+} (mV)	OUT− (mA)	V_{OUT-} (mV)
0000	0000	0000	0.000	0.00	40.000	−1000.00
0000	0000	0001	0.009	−0.24	39.990	−999.75
0000	0000	0010	0.019	−0.49	39.980	−999.52
	•		•	•	•	•
	•		•	•	•	•
	•		•	•	•	•
0111	1111	1111	19.995	−499.88	20.005	−500.12
1000	0000	0000	20.005	−500.12	19.995	−499.88
	•		•	•	•	•
	•		•	•	•	•
	•		•	•	•	•
1111	1111	1101	39.980	−999.52	0.019	−0.49
1111	1111	1110	39.990	−999.75	0.009	−0.24
1111	1111	1111	40.000	−1000.00	0.000	0.00

Note: 1. $I_{REF} = 625\mu A$, $R_{LOAD} = 25\Omega$.

Figure 1. Timing Diagram

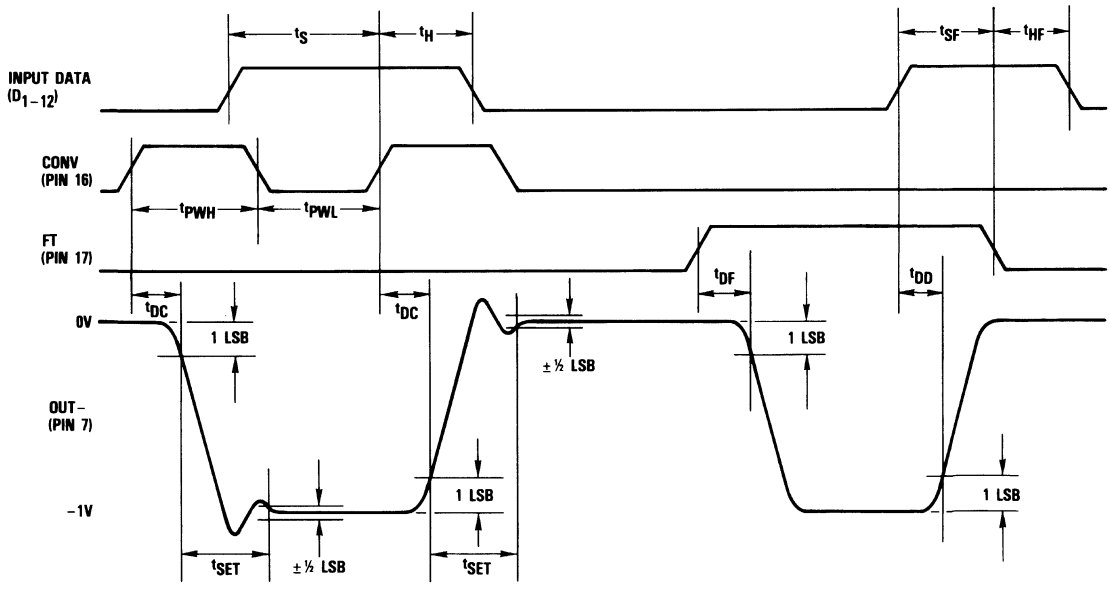


Figure 2a. Equivalent Input Circuit (Data and FT)

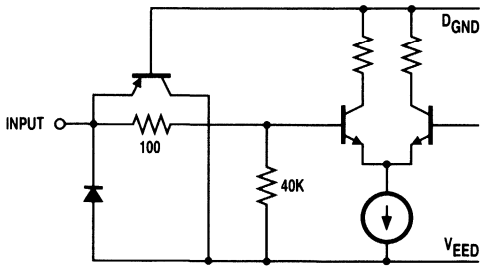
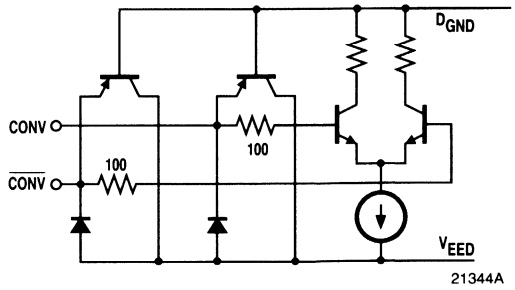


Figure 2b. Equivalent Input Circuit (CONV and $\overline{CONV}$)



B

Figure 3. Equivalent Reference and Output Circuits

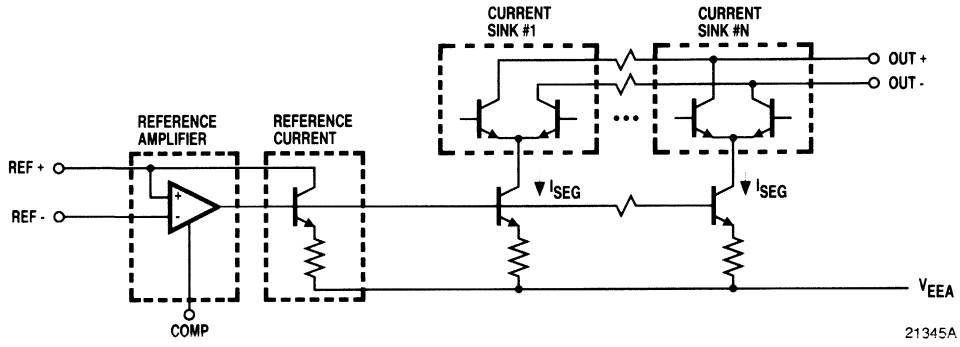


Figure 4. Standard Test Load

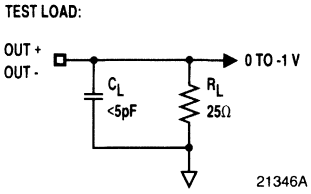
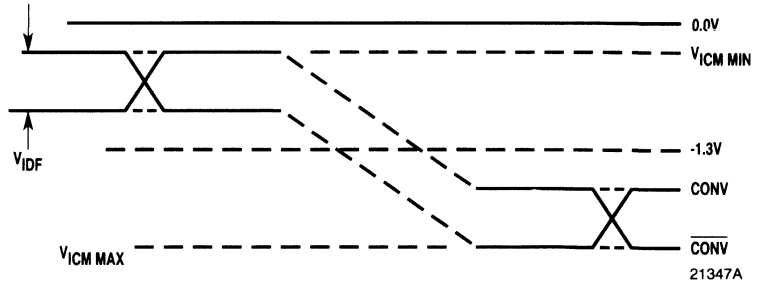


Figure 5. CONV and $\overline{CONV}$ Switching Levels



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{EEA} (measured to A_{GND})	−7.0 to +0.5V
V_{EEA} (measured to V_{EED})	−50 to +50mV
V_{EED} (measured to D_{GND})	−7.0 to +0.5V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Inputs

Applied voltage	
CONV, $\overline{CONV}$, FT, $D_{1\text{-}12}$ (measured to D_{GND}) [2]	V_{EED} to +0.0V
REF+, REF− (measured to A_{GND}) [2]	V_{EEA} to +0.0V
Applied current	
REF+, REF−, externally forced (measured to A_{GND}) [3,4]	±3mA
Digital inputs	±3mA

Outputs

Applied voltage	
OUT+, OUT− (measured to A_{GND}) [2]	−2.0 to +2.0V
Applied current	
OUT+, OUT−, externally forced (measured to A_{GND}) [3,4]	+50mA
Short-circuit duration (single output to GND)	Unlimited

Temperature

Operating, ambient (plastic package)	−20 to +90°C
(ceramic package)	−60 to +150°C
junction (plastic package)	+140°C
(ceramic package)	+200°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Commercial			Military			
		Min	Nom	Max	Min	Nom	Max	
F_S	Clock Frequency	0		50	0		50	MHz
V_{EEA}	Analog Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{EEA}	Analog Supply Voltage (measured to V_{EED}) [1]	−20	0.0	+20	−20	0.0	+20	mV
V_{EED}	Digital Supply Voltage (measured to D_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
V_{REF}	Reference Voltage, REF−	−0.7	−1.0	−1.3	−0.7	−1.0	−1.3	V
I_{REF}	Reference Current, REF+	0.550	0.625	0.700	0.575	0.625	0.675	mA
C_C	Compensation Capacitor	0.01	0.1		0.01	0.1		μF
V_{IL}	Digital Input Voltage, Logic LOW			−1.55			−1.60	V
V_{IH}	Digital Input Voltage, Logic HIGH	−1.05			−1.00			V
t_S	Input Data Setup Time	17			18			ns
t_S	Input Data Setup Time [2]	24			24			ns
t_H	Input Data Hold Time	0			0			ns
t_H	Input Data Hold Time [2]	4			4			ns
t_{SF}	Setup Time, Data to FT			7			7	ns
t_{HF}	Hold Time, Data to FT			24			24	ns
V_{ICM}	CONV Input Voltage, Common Mode Range [3]	−0.5		−2.0	−0.5		−2.0	V
V_{IDF}	CONV Input Voltage, Differential [3]	0.4		1.2	0.4		1.2	V
t_{PWL}	CONV Pulse Width LOW							
	≥ 40Msps	10.5			10.5			ns
	< 40Msps	11			11			ns
t_{PWL}	CONV Pulse Width LOW [2]	18			18			ns
t_{PWH}	CONV Pulse Width HIGH							
	≥ 40Msps	8.0			8.5			ns
	< 40Msps	9.0			9.0			ns
t_{PWH}	CONV Pulse Width HIGH [2]	11			11			ns
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Notes:
1. A common power supply, isolated simply with ferrite bead inductors, is recommended for V_{EEA} and V_{EED}. See the Typical Interface Circuits, Figures 9a-c.
2. SFDR sensitive applications.
3. See Figure 5., CONV, CONV Switching Levels.

Electrical characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Commercial		Military		
			Min	Max	Min	Max	
I_{EE}	Supply Current ($I_{EEA}+I_{EED}$) [2]	V_{EEA} = Max [3]		−180		−195	mA
		T_A = 70 °C		−150			mA
		T_C = 125°C				−145	mA
C_{REF}	Reference Input Capacitance	REF+, REF−		15		15	pF
C_I	Digital Input Capacitance	$D_{1\text{-}12}$, FT, CONV, $\overline{CONV}$		15		15	pF
I_{IL}	Digital Input Current, Logic LOW	V_{EED} = Max, V_I = −1.85V	−10	200	−10	250	μA
I_{IH}	Digital Input Current, Logic HIGH	V_{EED} = Max, V_I = −0.8V	−10	200	−10	250	μA
I_{IC}	CONV Input Current	V_{EED} = Max, −1.85V < V_I < −0.8V		50		50	μA
R_O	Output Resistance	OUT+, OUT−	12		12		kOhms
C_O	Output Capacitance	OUT+, OUT−		45		45	pF
V_{OC}	Output Compliance Voltage	OUT+, OUT−	−1.2	+1.2	−1.2	+1.2	V
I_O	Full-Scale Output Current	OUT+, OUT−	40		40		mA

Notes:
1. Worst case over all data and control states.
2. See the Typical Supply Current vs. Temperature graph (Figure 6) for typical values.
3. Standard test load, Figure 4.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range						Units
			Commercial			Military			
			Min	Typ	Max	Min	Typ	Max	
F_S	Maximum Clock Rate [1,2,3]	V_{EEA}, V_{EED} = Min, FT = LOW	50			50			Msps
t_{DC}	Clock to Output Delay [2,3]	V_{EEA}, V_{EED} = Min, FT = LOW			20			20	ns
t_{DD}	Data to Output Delay [2,4]	V_{EEA}, V_{EED} = Min, FT = HIGH			25			25	ns
t_{DF}	FT to Output Delay [2]	V_{EEA}, V_{EED} = Min			30			30	ns
t_R	Output Risetime [3]	90% to 10% of FSR, FT = LOW		2	4		2	4	ns
t_F	Output Falltime [3]	10% to 90% of FSR, FT = LOW		2	4		2	4	ns
t_{SET}	Output Voltage Settling Time [2,5,6]	FT = LOW, Worst Case Full-Scale Voltage Transition on OUT−							
		to 0.1% FS (4 LSB or 10 Bits)		12	20		13		ns
		to 0.05% FS (2 LSB)		17			14		ns
		to 0.0188% FS (3/4 LSB)		20	30		18	35	ns
		to 0.0125% FS (1/2 LSB)		25	35		25		ns

Notes:
1. F_S is limited only by t_{PWL}, t_{PWH}, t_S and t_H requirements.
2. See Figure 1., Timing Diagram.
3. Clock Mode.
4. Feedthrough Mode.
5. Standard test load, Figure 4.
6. See the Typical Output Voltage Settling Time vs. Settling Accuracy curve.

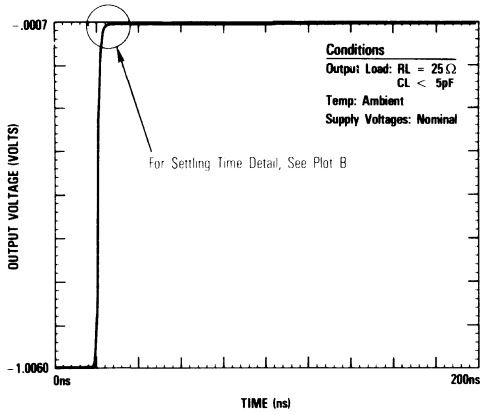
System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range						Units
			Commercial			Military			
			Min	Typ	Max	Min	Typ	Max	
E_{LI}	Linearity Error, Integral (Terminal Based)	Note 1,							
		TDC1112			±0.096			±0.096	%
		TDC1112–1			±0.048			±0.048	%
		TDC1112–2			±0.048			±0.048	%
		TDC1112–3			±0.024			±0.024	%
E_{LD}	Linearity Error, Differential	Note 1,							
		TDC1112			±0.096			±0.096	%
		TDC1112–1			±0.048			±0.048	%
		TDC1112–2			±0.024			±0.024	%
		TDC1112–3			±0.012			±0.012	%
SFDR	Spurious–Free Dynamic Range [2]	32Msps,							
		F_{OUT} = 12MHz	55	67			67		dB
		F_{OUT} = 10MHz		68		54	68		dB
		40Msps,							
		F_{OUT} = 16MHz		63			63		dB
		F_{OUT} = 5MHz		70			70		dB
		F_{OUT} = 1MHz		72			72		dB
E_G	Absolute Gain Error	Note 3		±1	±5		±1	±5	%
TC_{EG}	Gain Error Temperature Coefficient	Note 3		±30			±30		ppm/°C
I_{OF}	Output Offset Current	Note 4		±0.1	±5		±0.1	±5	μA
TC_{OF}	Offset Temperature Coefficient	Note 5		±2			±2		μV/°C
V_{OS}	REF+ to REF– Offset Voltage			±1.5	±10		±1.5	±10	mV
I_B	REF– Input Bias Current				5			10	μA
PSRR	Power Supply Rejection Ratio	Note 6			–50			–48	dB
PSS	Power Supply Sensitivity	Note 7			–140			–140	μA/V
DP	Differential Phase	Note 8		0.2					Degree
DG	Differential Gain	Note 8		0.3					%
G_A	Peak Glitch Area [9]	FT = LOW		20	35		20	45	pV-sec

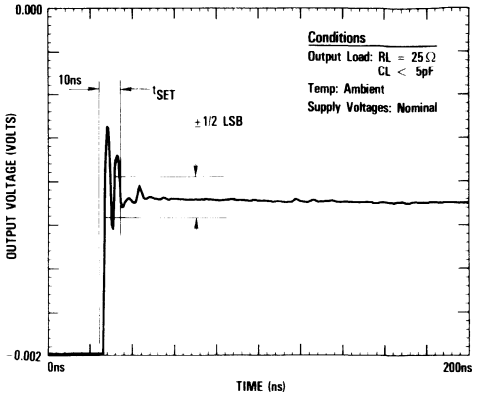
Notes:
1. OUT– connected to A_{GND}, OUT– driving virtual ground. V_{EEA}, V_{EED}, I_{REF} = Nom.
2. Circuit as shown in Figure 9a., I_{REF} = Nom.
3. V_{EED}, V_{EEA}, V_{REF} = Nom.
4. V_{EEA}, V_{EED} = Min, $D_{1\text{-}12}$ = LOW.
5. V_{EEA}, V_{EED} = Max, $D_{1\text{-}12}$ = LOW.
6. 120Hz, 0.6Vp-p ripple on V_{EEA} and V_{EED}. dB relative to 0.6Vp-p ripple input. V_{EEA}, V_{EED}, I_{REF} = Nom.
7. V_{EEA}, V_{EED} = ±4%, I_{REF} = Nom.
8. F_S = 4 x NTSC Subcarrier.
9. Worst case 1 LSB transition.

Typical Performance Curves (Typical Settling Time Characteristics)

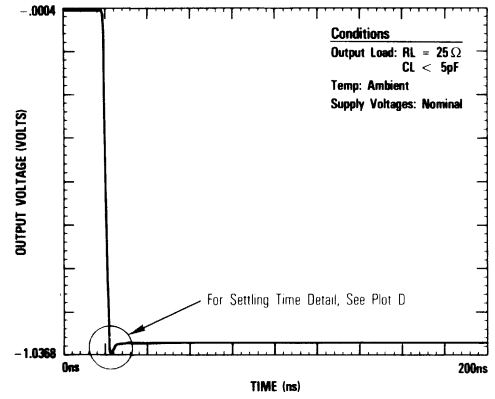
A. Full-Scale Output Transition, Rising Edge



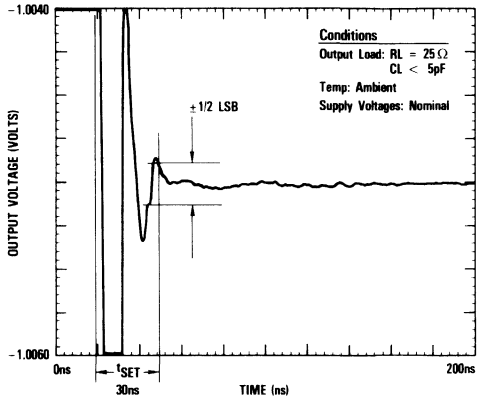
B. Settling Time, Full-Scale Output, Rising Edge



C. Full-Scale Output Transition, Falling Edge



D. Settling Time, Full-Scale Output, Falling Edge



E. Typical Settling Time vs. Settling Accuracy

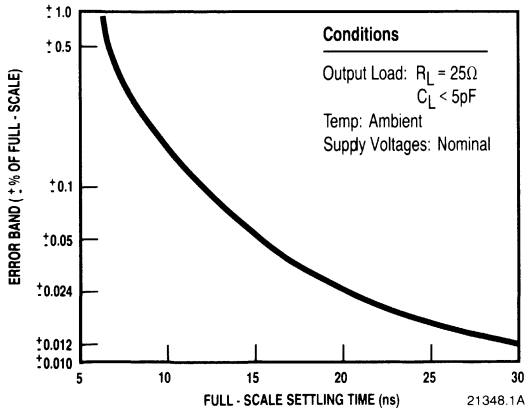


Figure 6. Typical Supply Current vs. Temperature

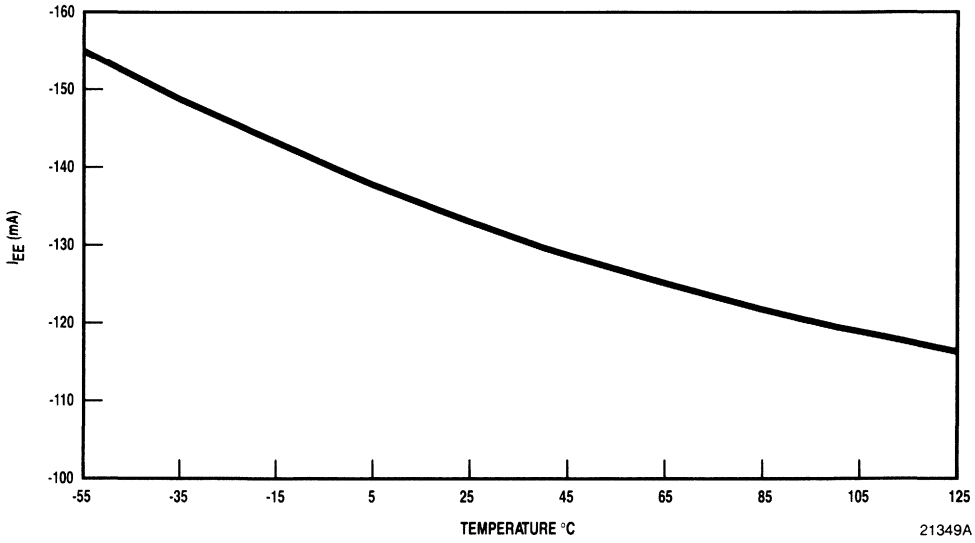


Figure 7. Typical Output Spectrum, 40MSPS, 13.336MHz F_{OUT}

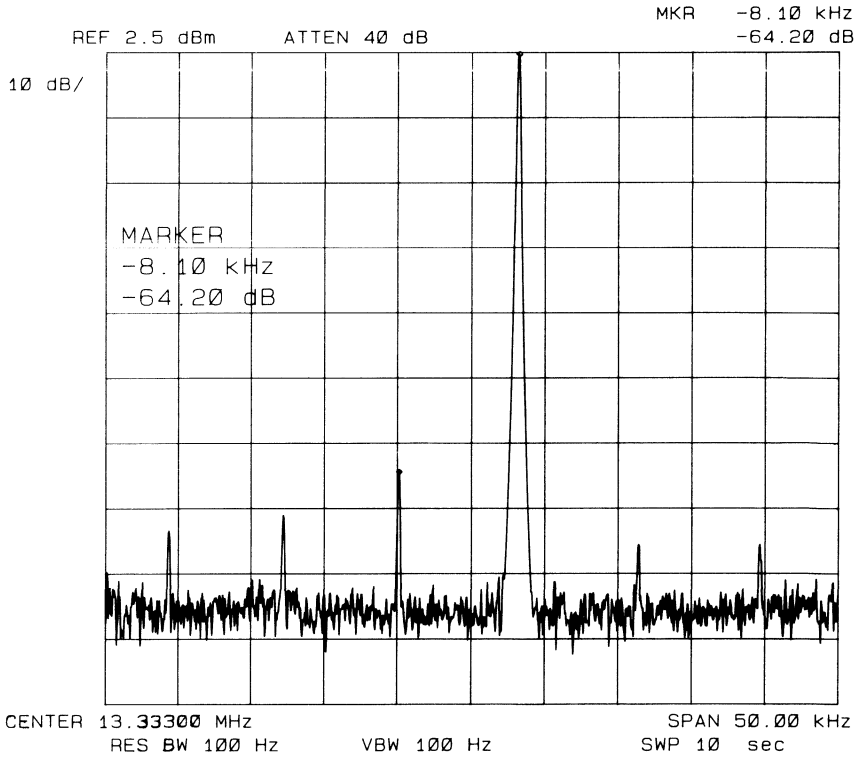
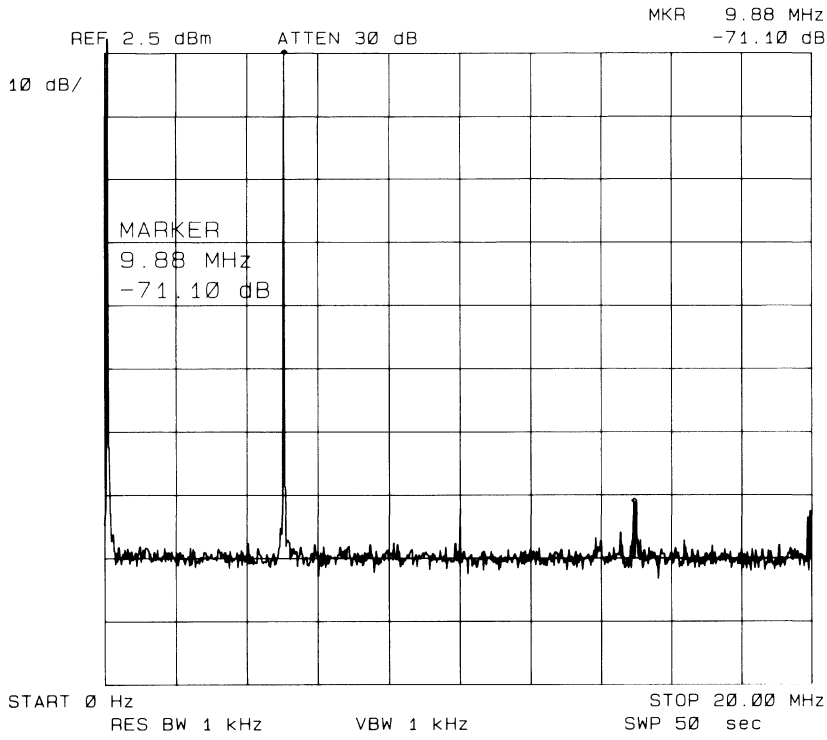


Figure 8. Typical Output Spectrum, 40Msps, 5MHz F_{OUT}



Application Discussion

Direct Digital Synthesis Applications

For most synthesis applications, optimum signal purity is obtained with the use of a balun (a simple RF transformer made by wrapping a few turns of wire around a ferrite core) as shown in ***Figure 9a***. This configuration has the benefit of cancelling common mode distortion.

An output amplifier is not recommended because any amplifier will add extra distortion of its own, which is likely to be much greater than that present from the direct outputs of the TDC1112.

The strict adherence to at least the minimum input data setup and hold times is important for the realization of the optimal performance. Spur levels may decrease as setup and hold times are increased. It is possible to achieve even higher performance in some instances by carefully "tuning" the input data setup and hold times (slightly delaying or advancing the CONV signal in relation to the data) fed to the TDC1112. The ***Operating Conditions Table*** has two sets of data for t_S and t_H, one which guarantees performance of the device in most applications, and one, more conservative specification which has been found to be optimal for DDS applications.

The actual digital-data waveform which represents a sine wave contains strong harmonics of that sinewave. This can be seen by connecting a digital data line to the input of an analog spectrum analyzer. Therefore, data feedthrough to the analog output of a system due to improper board layout or system shielding and grounding will appear as additional harmonic distortion, adversely affecting SFDR.

Harmonic distortion may improve even further with reduced AC termination impedance values, at the expense of lowered output voltage.

The purity of the output of the TDC1112 is greater than that which can be measured by many spectrum analyzers.

Direct Digital Synthesis Applications (cont.)

The spectral plots shown in *Figures 7 and 8* were generated with an HP8568B, which has a noise floor barely below that of the TDC1112, once the TDC1112 performance has been optimized. When making spectral measurements it is important to remember that the TDC1112 output power is +4dBm, which is greater power than many analyzers are equipped to handle without adding distortion of their own. Accordingly, it may be necessary to introduce an attenuator to the input of the spectrum analyzer to see the true DAC performance.

The CONV signal provided to the TDC1112 must be as free from clock jitter as possible. Clock jitter is the random cycle-to-cycle variation in clock period. CONV clock jitter will effectively appear at the output as phase noise. A value of 10ps or less for clock jitter is recommended for the highest performance applications. Ordinary crystal oscillators are satisfactory. High-performance synthesizers, such as the HP8662, used to trigger a precision pulse generator, are also satisfactory, although not as jitter free as a crystal oscillator.

B

Figure 9a. Typical Interface Circuit with Balun Output

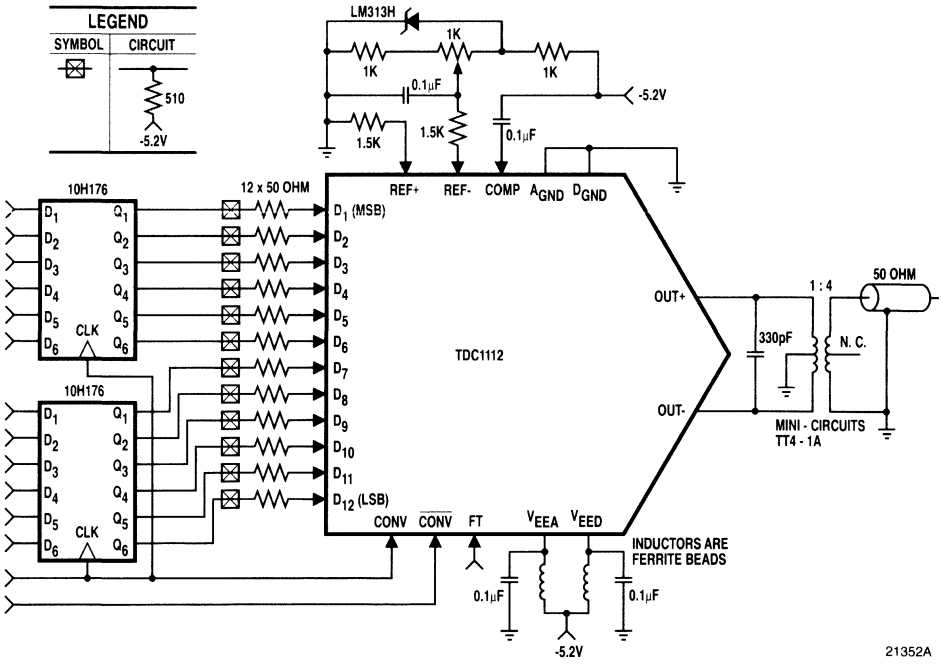


Figure 9b. Typical Interface Circuit with Bipolar, Differential Mode Operational Amplifier Output

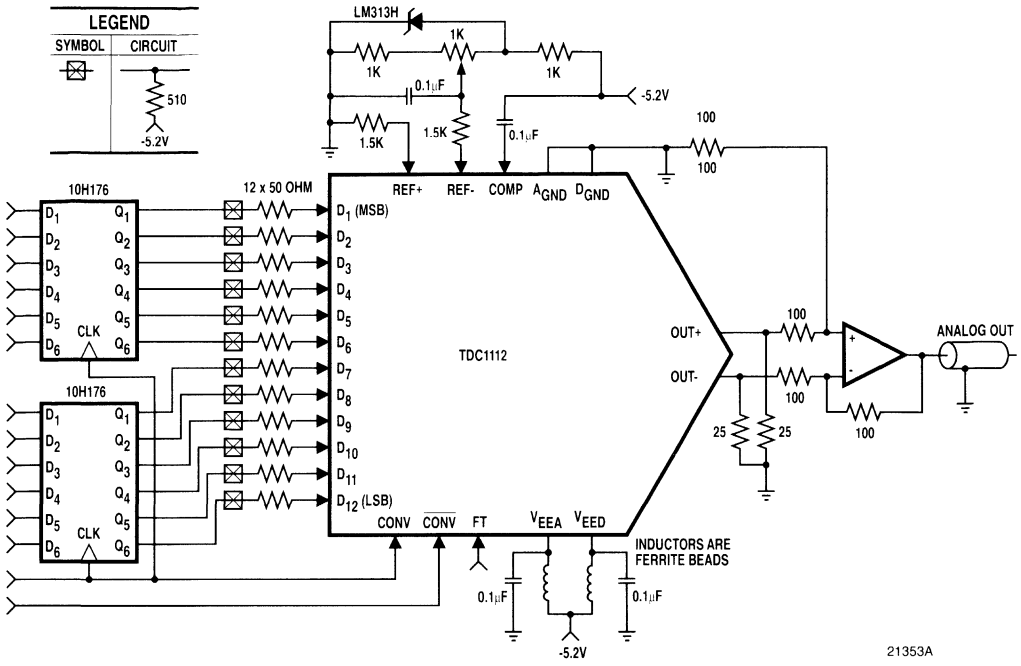
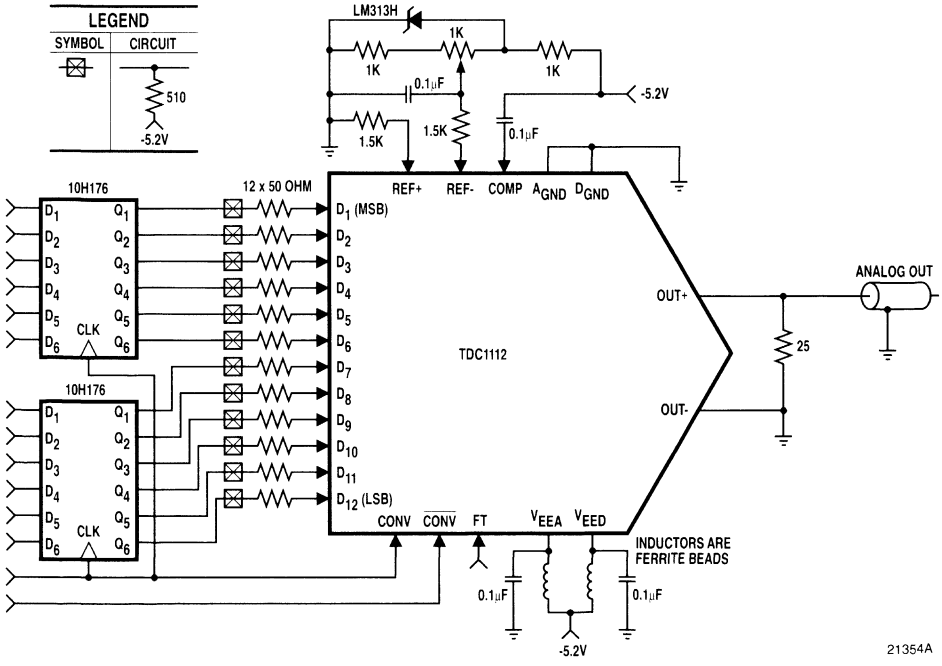


Figure 9c. Typical Interface Circuit with Resistive Load Output



Ordering Information

Product [1] Number	Temperature Range	Screening	Package	Package [1] Marking
TDC1112J7CX	STD – T_A = 0°C to 70°C	Commercial	24 Pin Hermetic Ceramic DIP	1112J7C-X
TDC1112J7VX	EXT – T_C = –55°C to 125°C	MIL-STD-883	24 Pin Hermetic Ceramic DIP	1112J7V-X
TDC1112N7CX	STD – T_A = 0°C to 70°C	Commercial	24 Pin Plastic DIP	1112N7C-X
TDC1112C3VX	EXT – T_C = –55°C to 125°C	MIL-STD-883	28 Contact Chip Carrier	1112C3V-X
TDC1112R3CX	STD – T_A = 0°C to 70°C	Commercial	28 Leaded Plastic Chip Carrier	1112R3C-X

Note: 1. The "X" in the product designation denotes the linearity grade, guaranteed over the operating temperature range, per the following table:

B

Linearity Grade (X)	None	1	2	3
E_{LD} Linearity Error, Differential	±0.096% (4 LSB)	±0.048% (2 LSB)	±0.024% (1 LSB)	±0.012% (1/2 LSB)
E_{LI} Linearity Error, Integral	±0.096% (4 LSB)	±0.048% (2 LSB)	±0.048% (2 LSB)	±0.024% (1 LSB)

Not every grade is available in every package/screening/temperature range combination. Consult factory for availability.

TDC1141 Monolithic Digital To Analog Converter
10 Bit, 50Msps, 12ns Settling Time

The TDC1141 is an ECL compatible, 10-bit monolithic D/A converter capable of converting digital data into an analog current or voltage at data rates in excess of 50 Mega-samples-per second (Msps).

The analog circuitry has been optimized for dynamic performance, with very low glitch energy. The output is able to drive a 50Ω load with 1V output levels while maintaining large spurious-free-dynamic range.

Data registers are incorporated on the TDC1141. This eliminates data skew encountered with external registers and latches and minimizes the glitches that can adversely affect many applications.

Features

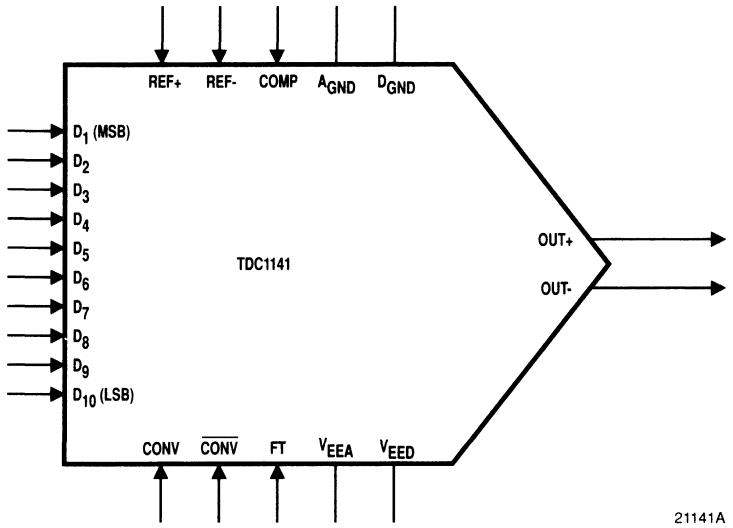
- 10-Bit Resolution
- 50 Msps Data Rate
- ECL Inputs
- Very Low Glitch With No Track And Hold Circuit Needed
- Dual +4dBm (1V Into 50Ω) Outputs Make Output Amplifiers Unnecessary In Many Applications

Applications

- Direct Digital RF Signal Generation
- Test Signal Generation
- Arbitrary Waveform Synthesis
- Broadcast And Studio Video
- High-Resolution A/D Converters

B

Interface Diagram



TRW LSI Products Inc.
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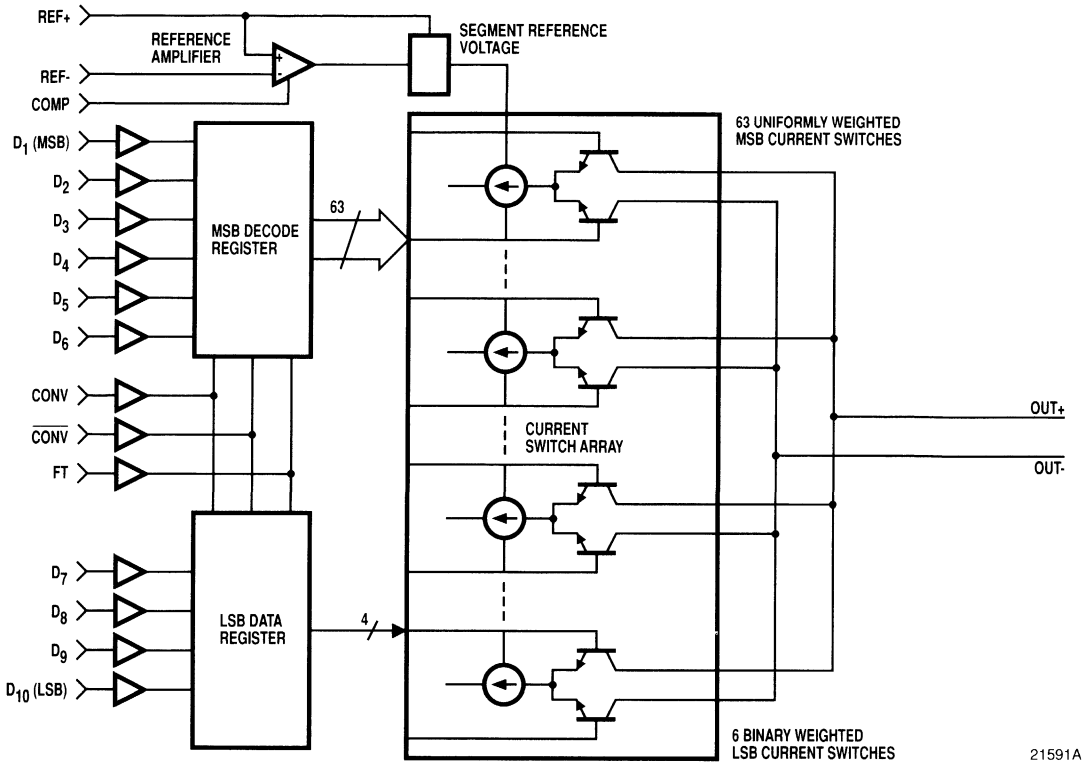
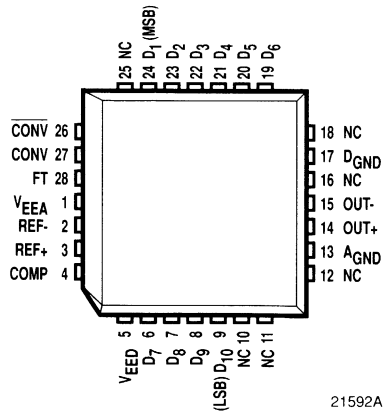
Phone: (619) 457-1000
FAX: (619) 455-6314

40G06718 Rev. A – 9/90
Printed in the U.S.A.

Functional Block Diagram



Pin Assignments



28 Leaded Plastic Chip Carrier – R3

Functional Description

General Description

The TDC1141 consists of five major circuit sections: the LSB data register, the MSB decode block, the decoded MSB register, the current switch array, and the reference amplifier. All data bits are registered just before the current switches to minimize the temporal skew that would generate glitches.

Power and Grounds

The TDC1141 requires a single –5.2V power supply. This supply is divided into analog (V_{EEA}) and digital (V_{EED}) supply pins which should be decoupled from each other. An example of this decoupling is shown in the *Typical Interface Circuit*. The 0.1µF decoupling capacitors should be placed as close as possible to the power pins. The

inductors are simple ferrite beads and are neither critical in value nor always required.

Reference and Compensation

The TDC1141 has two reference inputs: REF+ and REF–. These are the inverting and noninverting inputs of the internal reference amplifier. An externally generated reference voltage is applied to the REF– pin. Current flows into the REF+ pin through an external current setting resistor (R_{REF}). This current is the reference current (I_{REF}) which serves as an internal reference for the current source array. The output current for an input code N from OUT+ is related to I_{REF} through the following relationship:

$$I_{OUT} = N \times \frac{I_{REF}}{16}$$

Where N is the input code to the D/A converter

This means that with an I_{REF} that is nominally 625μA, the full-scale output is 40mA, which will drive a 50Ω load in parallel with a 50Ω transmission line (25Ω load total) with a 1V peak to peak signal. The impedance seen by the REF– and REF+ pins should be approximately equal so that the effect of amplifier input bias current is minimized.

The internal reference amplifier is externally compensated to ensure stability. A 0.1μF capacitor should be connected between the COMP pin and V_{EEA}.

Digital Inputs

All digital inputs including the FT, CONV and Data Inputs are compatible with ECL logic. Input registers are provided on the data input lines to minimize the effect of glitching caused by data skew.

Clock and Feedthrough Control

The TDC1141 requires a differential ECL clock signal (CONVert and $\overline{\text{CONV}}$ert). Even though complementary operation is preferred, a single-ended signal may be used if either unused CONV input is biased at a DC voltage midway between the active input's V_{IH} and V_{IL} levels.

Data is synchronously entered on the rising edge of CONV (the falling edge of $\overline{\text{CONV}}$). The CONV input is ignored in the Feedthrough (FT = HIGH) mode.

The Feedthrough (FT) pin is normally held LOW, in which case the TDC1141 operates in a clocked mode (the output changes only after a clock rising edge). An internal pull-down resistor is provided, and this pin may be left open for clocked operation. For certain applications, such as high-precision successive approximation A/D converters, output delay may be more important than glitch performance. In these cases, the FT pin may be brought HIGH, which makes the input registers transparent. This allows the analog output to change immediately and asynchronously in response to the digital input, without the need for a clock.

B

Analog Outputs

Two simultaneous and complementary analog outputs are provided. Both of these outputs are full-power current sources. By loading the current source outputs with a resistive load, they may be used as voltage outputs. OUT+ provides a 0 to –40mA output current (0 to –1V when terminated in 25Ω) as the input code varies from 00 0000 0000 to 11 1111 1111. OUT– varies in a complementary manner from –40 to 0mA (–1 to 0V when terminated with 25Ω) over the same code range. (See the *Input Coding Table*.) The output current is proportional to the reference current and the input code.

No Connect

These pins have no internal connection and should be left open for optimal performance.

Package Interconnections

Signal Type	Signal Name	Function	Value	R3 Package Pins
Power	A_{GND}	Analog Ground	0.0V	13
	D_{GND}	Digital Ground	0.0V	17
	V_{EEA}	Analog Supply Voltage	–5.2V	1
	V_{EED}	Digital Supply Voltage	–5.2V	5
Reference	REF–	Reference Voltage Input	–1.0V	2
	REF+	Reference Current Input	–625μA	3
	COMP	Compensation Capacitor	0.1μF, see text	4
Data Inputs	D_1 (MSB)	Most Significant Bit	ECL	24
	D_2		ECL	23
	D_3		ECL	22
	D_4		ECL	21
	D_5		ECL	20
	D_6		ECL	19
	D_7		ECL	6
	D_8		ECL	7
	D_9		ECL	8
	D_{10} (LSB)	Least Significant Bit	ECL	9
Feedthrough	FT	Feedthrough Mode control	ECL	28
Convert	CONV	Convert (Clock) Input	ECL	27
	$\overline{CONV}$	Convert Complement	ECL	26
Analog Output	OUT+	Analog Output	0 to 40mA	14
	OUT–	Analog Output	40 to 0mA	15
No Connect	NC	No Internal Connection	Open	10,11,12,16,18,25

Input Coding Table[1]

Input Data MSB LSB	OUT+ (mA)	V_{OUT+}(mV)	OUT– (mA)	V_{OUT-}(mV)
00 0000 0000	0.000	0.00	40.000	–1000.00
00 0000 0001	0.039	–0.97	39.961	–998.05
00 0000 0010	0.078	–1.95	39.922	–998.05
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
0111 1111 11	19.961	–499.03	20.000	–500.00
1000 0000 00	20.000	–500.00	19.961	–499.03
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
1111 1111 01	39.922	–998.05	0.078	–1.95
1111 1111 10	39.961	–999.03	0.039	–0.97
1111 1111 11	40.000	–1000.00	0.000	0.0

Note: 1. I_{REF} = 625μA, R_{LOAD} = 25Ω

B

Figure 1. Timing Diagram

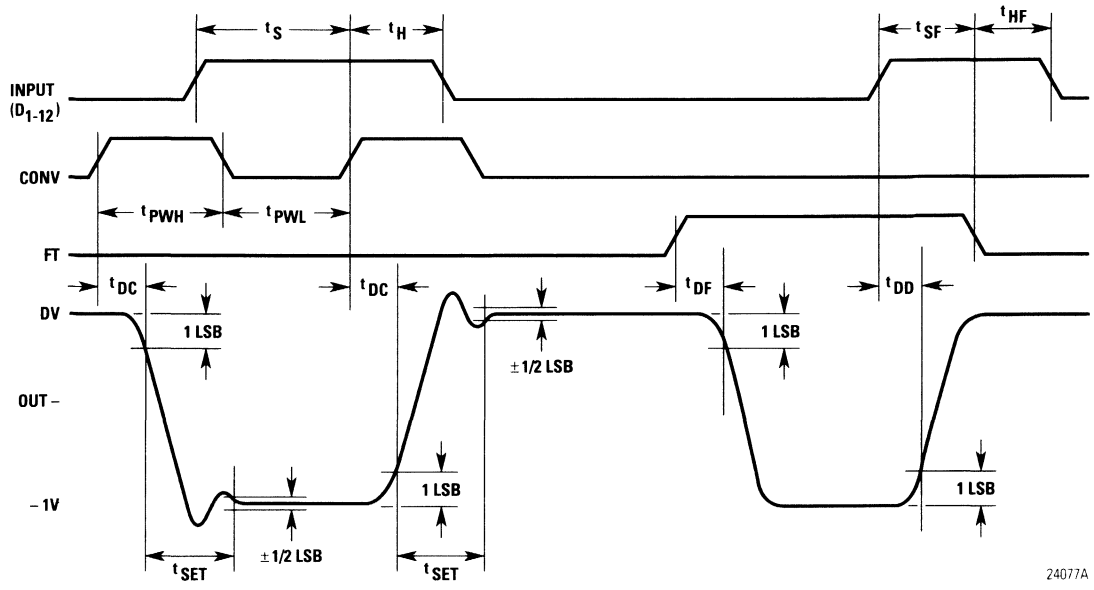


Figure 2. Equivalent Input Circuit (Data and FT)

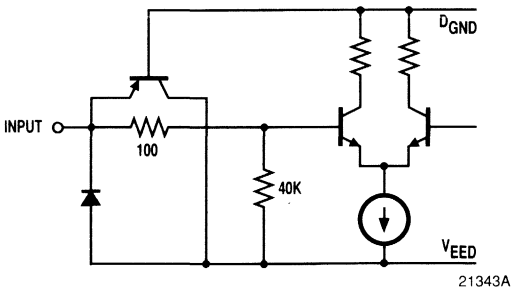


Figure 3. Equivalent Input Circuit (CONV and $\overline{CONV}$)

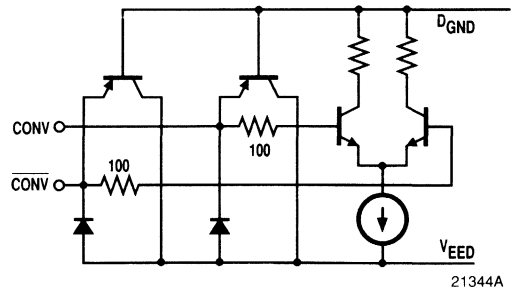


Figure 4. Equivalent Reference and Output Circuits

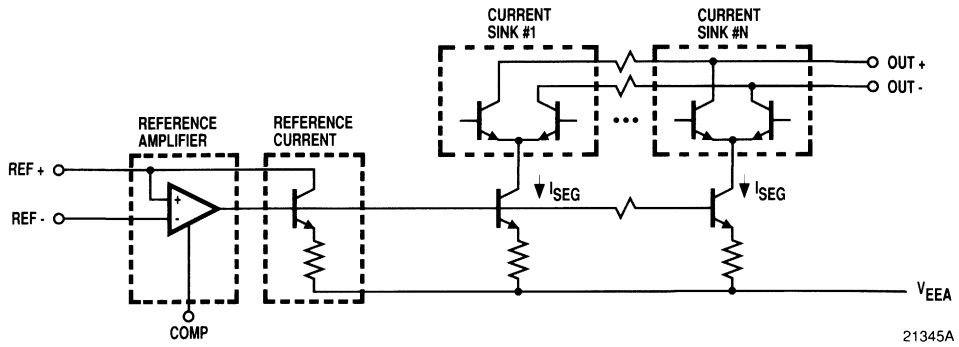


Figure 5. Standard Test Load

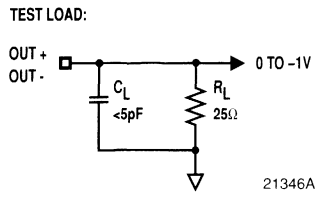
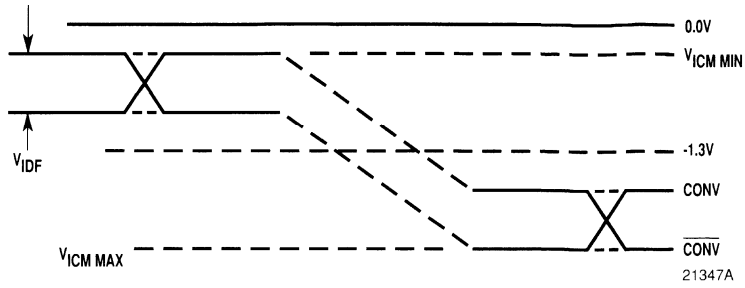


Figure 6. CONV and $\overline{CONV}$ Switching Levels



Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltages

V_{EEA}	(Measured to A_{GND})	–7.0 to +0.5V
V_{EEA}	(Measured to V_{EED})	–50 to +50mV
V_{EED}	(Measured to D_{GND})	–7.0 to +0.5V
A_{GND}	(Measured to D_{GND})	–0.5 to +0.5V

Inputs

CONV, $\overline{CONV}$, FT, $D_{1\text{-}12}$ (Measured to D_{GND})[2]	V_{EED} to +0.5V
REF+, REF-, Applied Voltage (Measured to A_{GND})[2]	V_{EEA} to +0.5V
REF+, REF–, Current, Externally Forced[3,4]	±3mA

Outputs

OUT+, OUT–, Applied Voltage (Measured to A_{GND})[2]	–2.0 to +2.0V
OUT+, OUT–, Current, Externally Forced[3,4]	+50mA
Short-Circuit Duration (Single Output to GND)	unlimited

Temperature

Operating, ambient (Plastic Package)	–20 to +90°C
Operating, ambient (Ceramic Package)	–60 to +150°C
Junction (Plastic Package)	+140°C
Junction (Ceramic Package)	+200°C
Lead, Soldering (10 Seconds)	+300°C
Storage	–65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
F_S	Clock Frequency	0		50	Msps
V_{EED}	Negative Supply Voltage (Measured to D_{GND})	–4.9	–5.2	–5.5	V
V_{EEA}	Negative Supply Voltage (Measured to A_{GND})	–4.9	–5.2	–5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	–0.1	0.0	0.1	V
V_{EEA}	Negative Supply Voltage (Measured to V_{EED})[1]	–20	0	20	mV
t_{PWL}	CONV Pulse Width LOW ($F_S \geq 40$ Msps)	10.5			ns
	CONV Pulse Width LOW ($F_S < 40$ Msps)	11			ns
t_{PWH}	CONV Pulse Width HIGH ($F_S \geq 40$ Msps)	8			ns
	CONV Pulse Width HIGH ($F_S < 40$ Msps)	9			ns
t_S	Setup Time, Data to CONV	17			ns
t_H	Hold Time	0			ns
t_{SF}	Setup Time, Data to FT	7			ns
t_{HF}	Hold Time, Data to FT	24			ns
V_{IL}	Input Voltage, Logic LOW			–1.55	V
V_{IH}	Input Voltage, Logic HIGH	–1.05			V
V_{REF}	Reference Voltage (REF–)	–0.7	–1.0	–1.3	V
I_{REF}	Reference Current (REF+)	400	625	700	µA
C_C	Compensation Capacitor	0.01	0.1		µF
T_A	Ambient Temperature, Still Air	0		70	°C

Note: 1. A common power supply isolated with ferrite bead inductors is recommended for V_{EEA} and V_{EED}. This is shown in the *Typical Interface Circuits*.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Units
$I_{EEA}+I_{IEED}$		$V_{EEA}=V_{EED}$=Max,static T_A=0 to 70°C		–180	mA
		T_A=70°C		–150	mA
C_{REF}	Reference Input Capacitance			15	pF
C_I	Digital Input Capacitance			15	pF
V_{OC}	Compliance Voltage		–1.2	1.2	V
R_O	Output Resistance		12		kΩ
C_O	Output Capacitance			45	pF
I_O	Full-Scale Output Current	I_{REF}=625µA	40		mA
I_{IL}	Input Current, Logic LOW	V_{EE}=Max, V_I=0.4V	–10	200	µA
I_{IH}	Input Current, Logic HIGH	V_{EE}=Max, V_I=2.4V	–10	200	µµA

Switching characteristics

Parameter		Test Conditions	Temperature Range Standard Min	Typ	Max	Units
t_{DC}	Clock to Output Delay	V_{EEA}, V_{EED}=Min, FT=LOW			20	ns
t_{DD}	Data to Output Delay	V_{EEA}, V_{EED}=Min, FT=HIGH			25	ns
t_{DF}	FT to Output Delay	V_{EEA}, V_{EED}=Min			30	ns
t_R	Risetime[1]	90% to 10% of FSR, FT=LOW		2	4	ns
t_F	Falltime[1]	10% to 90% of FSR, FT=LOW		2	4	ns
t_{SET}	Settling Time, Voltage	FT=LOW, Full-Scale Voltage transition on I_{OUT} to 0.1% FSR		12	20	ns

Note: 1. Clocked Mode

System performance characteristics

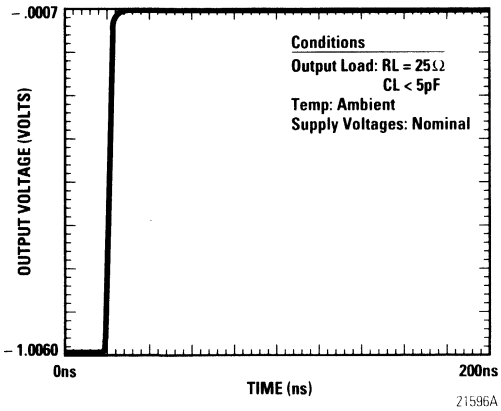
Parameter		Test Conditions	Temperature Range Standard Min	Typ	Max	Units
E_{LD}	Differential Linearity Error	V_{EEA}, V_{EED}, I_{REF} = Nom[1]				
		TDC1141			±0.1	%
		TDC1141-1			±0.05	%
E_{LI}	Integral Linearity Error	V_{EEA}, V_{EED}, I_{REF} = Nom[1]				
		TDC1141			±0.1	%
		TDC1141-1			±0.05	%
V_{OS}	REF+ to REF– Offset Voltage		–10		+10	mV
I_B	REF- Input Bias Current			5	µA	
E_G	Absolute Gain Error	V_{EEA}, V_{EED}, I_{REF} = Nom	–5		5	%
I_{OF}	Output Offset Current	V_{EEA}, V_{EED}= Max, D_{1-12} = LOW	–5		+5	µA
PSRR	Power Supply Rejection Ratio	V_{EEA}, V_{EED}, I_{REF} = Nom[2]			–50	dB
PSS	Power Supply Sensitivity	V_{EEA}, V_{EED} = ±4%, I_{REF} = Nom			–140	µA/V
G_A	Peak Glitch Area				40	pV– sec

Note: 1. OUT– connected to A_{GND}, OUT– driving virtual ground.

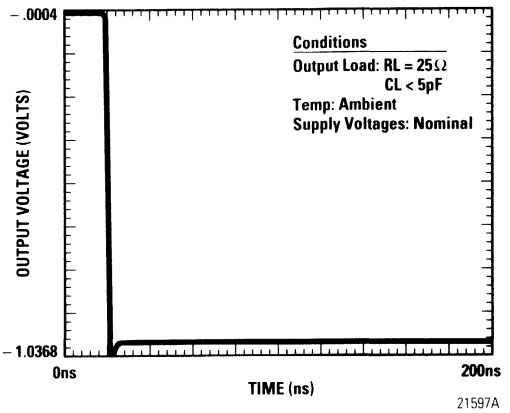
2. 120Hz, 600mV p-p ripple on V_{EE} and V_{CC}.

Typical Performance Curves (Typical Settling Time Charactersitics)

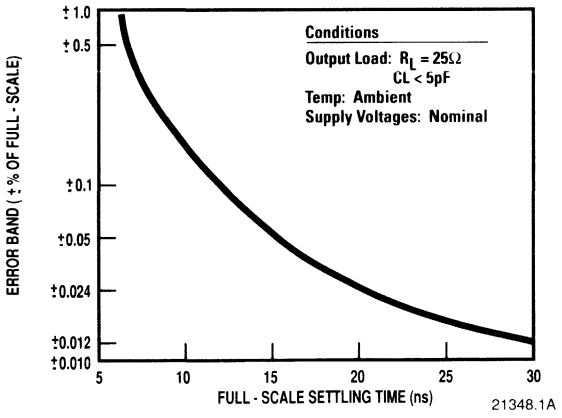
A. Full-Scale Output Transition, Rising Edge



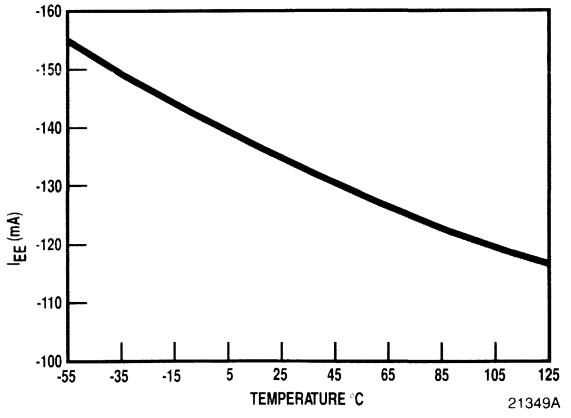
B. Full-Scale Output Transition, Falling Edge



C. Typical Settling Time vs. Settling Accuracy



D. Typical Supply Current vs. Temperature



Applications Information

There are three major D/A architectures: segmented, weighted current sources, and R-2R. In segmentated D/A converters there is one current source for each possible output level. The current sources are equally weighted and for an input code of N, N current sources are turned on. An N bit segmented D/A has 2^N current sources. A weighted current source D/A has one current source for each bit of input with a binary weighting for the current sources. In an R-2R D/A, there is one current source per bit, and a resistor network which scales the current sources to have a binary weighting.

When transitioning from a code of 0111111111 to 1000000000, both the R-2R D/A and Binary weighted D/A are turning some current sources on while turning others off. If the timing is not perfect, there is a moment where all current sources are either on or off, resulting in a glitch. In a segmented architecture, 511 of the current sources remain on, and one more is turned on to increment the output with no possibility of a glitch.

The TDC1141 uses a hybrid architecture with the 6 MSBs segmented, and the 4 LSBs from a R-2R network. The result is a converter which has very low glitch energy, and a moderate die size.

Layout, Power and Grounding

The layout of grounds in any system is an important design consideration. Separate analog and digital grounds are provided on the TDC1141. All ground pins should be connected to a common low-noise, low-impedance groundplane. This groundplane should be common for the TDC1141 and all of its immediate interface circuitry, which includes all of the reference circuitry, the output load circuitry, and all of the power supply decoupling components.

The digital driving logic should use a separate system ground, and this ground should be connected (typically through a ferrite bead inductor) to the analog groundplane in only one place. The analog and digital grounds may be connected in other ways if required by the user's system grounding plan, however, the voltage differential between the A_{GND} and D_{GND} pins must be held to within ±0.1 Volt.

Output Termination

The recommended output termination is 25Ω. This can be provided by placing a 50Ω source resistor between the output pin and ground, then driving a 50Ω transmission line. With this load, the output voltage range of the converter is 0 to –1.0V. If a load is capacitively coupled to the TDC1141, it is recommended that a 25Ω load at DC, as seen by the TDC1141, continue to be maintained. The output voltage should be kept within the output compliance voltage range, V_{OC}, as specified in the *Electrical Characteristics Table*, or the accuracy may be impaired.

See *Figure 8* for a suggested circuit for achieving a bipolar output voltage range. Optimum DC linearity is obtained by using a differential output either with a balun, or an operational amplifier in the differential mode. If it is desired that the TDC1141 be operated in a single ended fashion, the unused output should be connected directly to ground as is shown in *Figure 9*. The CONV signal provided to the TDC1141 must be as free from clock jitter as possible. Clock jitter is the random cycle-to-cycle variation in clock period. CONV clock jitter will effectively appear at the output as phase noise. A value of 10ps or less for clock jitter is recommended for the highest performance applications. Ordinary crystal oscillators are satisfactory. High-performance synthesizers, such as the HP8662, used to trigger a precision pulse generator, are also satisfactory, although not as jitter free as a crystal oscillator.

Driving a 75Ω Transmission line

The TDC1141 has been optimized to operate with a reference current of 625μA. Significantly increasing or decreasing this current may degrade the performance of the device. If it is desired that the device drive a 37.5Ω load (75Ω source termination driving 75Ω transmission line) rather than the 25Ω suggested load, then V_{REF} should be held at 1V and I_{REF} reduced to 417μA. This will result in a 1V p-p voltage being generated at the DAC output.

Figure 7. Typical Interface Circuit with Balun Output

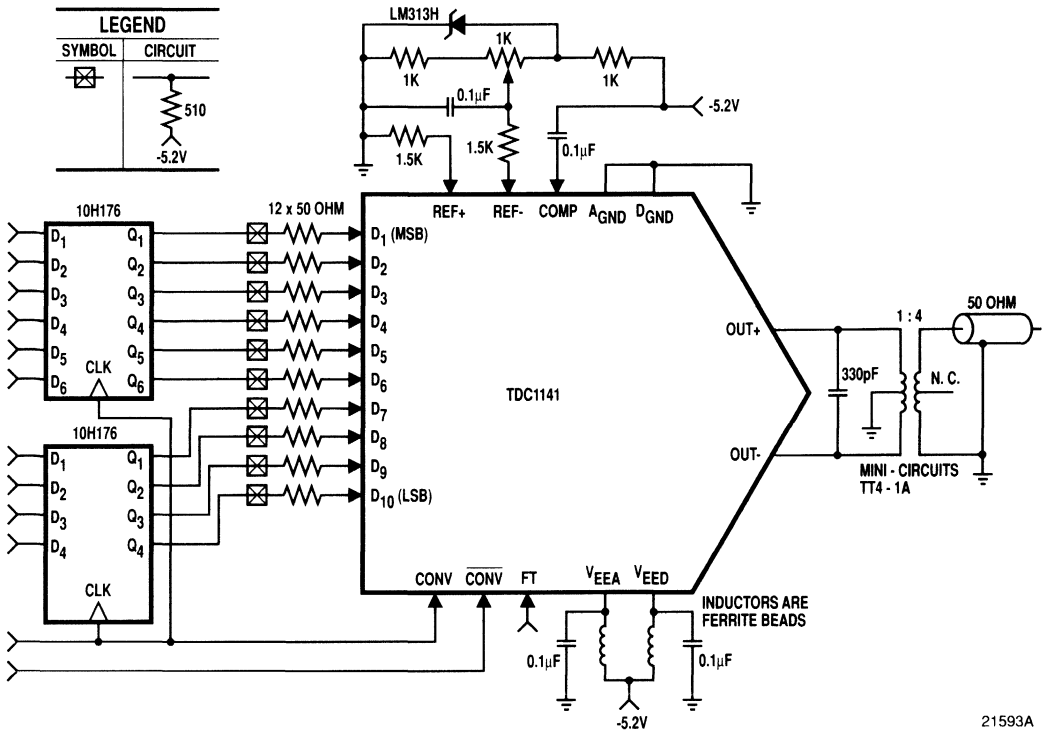


Figure 8. Typical Interface Circuit with Bipolar, Differential Mode Operational Amplifier Output

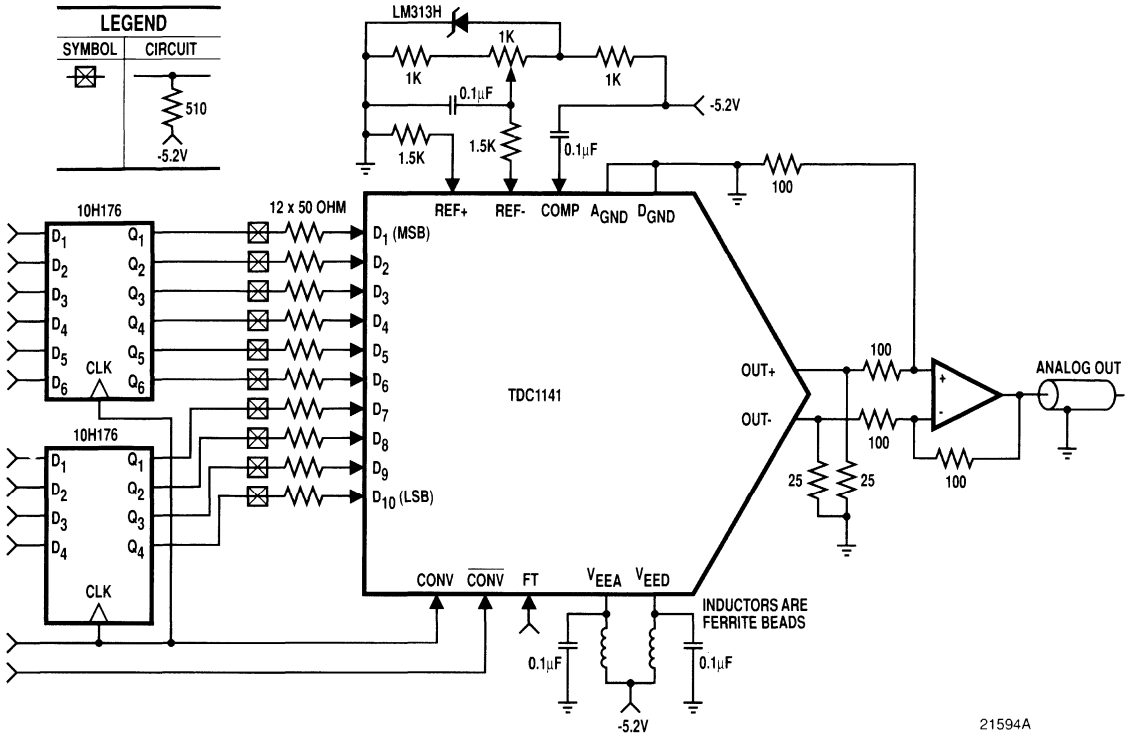
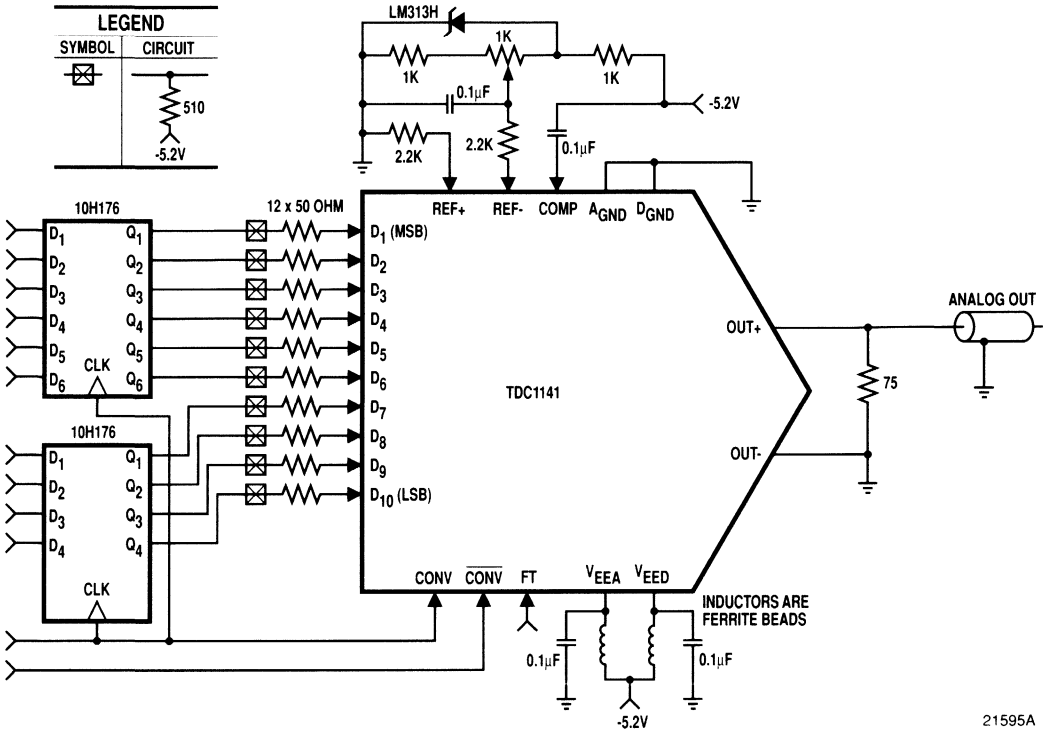


Figure 9. Typical Interface Circuit with Resistive Load Output



B

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1141R3C	T_A=0°C to 70°C	Commercial	Plastic Chip Carrier	1141R3C
TDC1141R3C1	T_A=0°C to 70°C	Commercial	Plastic Chip Carrier	1141R3C-1

TDC1318

Digital-to-Analog Converter
Triple 8-Bit, 200MHz

The TDC1318 consists of three separate 8-bit video D/A converters in a single monolithic integrated circuit. The TDC1318 is designed for 200MHz operation and is ECL compatible. Each of the three D/A converters has complementary current-sinking outputs that can directly drive 75 Ohm lines to 1Vp-p.

Video controls, SYNC and BLANK, are included for setting video output levels during synchronization and CRT blanking intervals. OVERLAY, a 110% white control, is useful for emphasizing portions of a CRT display and for cursor identification. All data and control inputs to the TDC1318 are internally registered on the rising edge of the clock (CONV).

A single band-gap voltage source is the reference for all three D/A converters and a single external resistor determines the reference current. The pinout of the TDC1318 allows for optimum board layout and minimizes digital feedthrough. Analog and digital grounds are kept separate for maximum system ground flexibility.

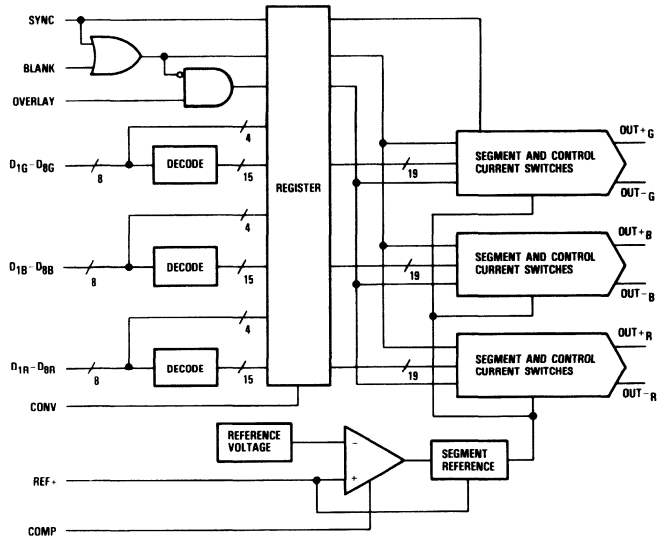
Features

- Complete, Monolithic, "Graphics-Ready"
- Three 8-Bit D/A Converters
- Registered Data Inputs
- Registered SYNC, BLANK And OVERLAY Controls
- On-Board Voltage Reference
- Linearity Error Less Than 1/2 LSB
- 200MHz Operation, ECL Compatible Inputs
- Complementary Current Outputs
- Single −5.2V Power Supply Required
- Can Be Operated In TTL Systems
- Available In A 40 Pin DIP

Applications

- Raster Scan Displays
- Bit-Mapped Graphics
- PC Graphics Systems
- CAD/CAM Workstations

Functional Block Diagram



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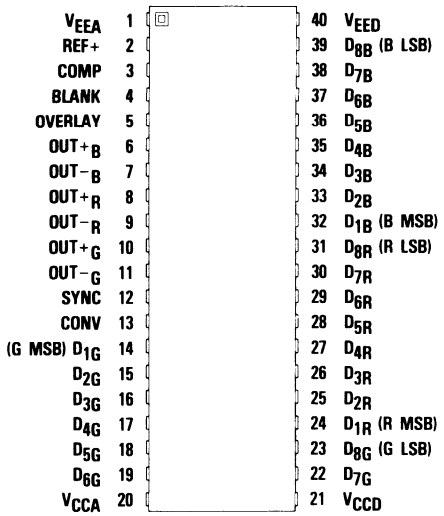
Phone: (619) 457-1000
FAX: (619) 455-6314

40G02411 Rev. E−11/90
Printed in the U.S.A.

Pin Assignments



40 Pin CERDIP – B5 Package

Functional Description

General Information

The TDC1318 has three pairs of complementary analog current outputs for directly driving the 75 Ohm red, green and blue inputs of an RGB color video monitor. The current flowing into each output terminal is proportional to the product of the 8-bit input data and the analog reference current. All digital inputs are compatible with standard (10K) ECL logic levels. The rising edge of CONVert latches all data and control inputs into an internal register. These binary data values are then converted into analog output current by a set of matched current switches.

Power

For optimum noise immunity, the TDC1318 operates from separate −5.2V analog and digital power inputs, V_{EEA} and V_{EED}. These may be connected to the same power source but separate power supply decoupling for each power input is recommended. The return path for I_{EED}, the current drawn from the V_{EED} supply, is V_{CCD}. The return path for I_{EEA} is V_{CCA}. All power input terminals must be connected.

Although the TDC1318 is specified for a −5.2V supply, operation from +5V is possible provided that the correct polarity of all voltages are maintained. For additional information concerning the use of ECL D/A converters in a +5V system, refer to *TRW Application Note TP-33 "Using The TDC1018 And TDC1034 In A TTL Environment."*

Reference

The TDC1318 has an on-board band-gap voltage source (−1.3V, nominal) that is referenced to V_{CCA}. The reference input, REF+, is the noninverting input of the reference amplifier. This amplifier provides a reference voltage for all of the current switches.

The analog output current is proportional to the digital data and the reference current, I_{REF}. The full-scale output current may be adjusted by varying the reference current. A compensation input, COMP, is provided to externally compensate the internal reference amplifier. A capacitor, C_C, should be connected between COMP and V_{EEA}.

Convert

The TDC1318 CONV clock is a single-ended ECL compatible input whose rising edge synchronizes the internal data transfer from the data encoder into the current switches of the three D/A converters.

Video Controls

The TDC1318 has three video control inputs: SYNC, BLANK and OVERLAY. Internal logic simplifies the use of these controls in video applications. All are ECL compatible and include internal pull-down resistors to force any unused control to the inactive state. The video controls are registered on the rising edge of the CONV clock input. Video control inputs must be valid for the set-up time, t_S, before and for the hold time, t_H, after the rising edge of CONV.

Asserting the video controls produces output levels for synchronization and blanking intervals and the 110% white overlay function. The effects of the video controls on the analog outputs are shown in the *Input Coding Table*. SYNC overrides data, BLANK and OVERLAY, producing a full-scale output on $OUT-_G$ and $OUT+_G$ only while forcing the remaining four outputs to the

Video Controls (cont.)

blanking level. BLANK overrides data and OVERLAY producing a "blacker than black" video level on all three D/A converters. OVERLAY overrides input data and forces the output of all three D/A converters to a level 10% whiter than white.

Analog Outputs

The red, green and blue analog outputs of the TDC1318 are each high-impedance complementary current sinks whose currents vary in proportion to the input data, video control inputs and reference current. All outputs are capable of directly driving 75 Ohm lines to standard video levels shown in ***Figures 1 and 2***. The voltage produced across the load is the product of the output current and the net load impedance. This voltage varies between 0 and −1V when driving a 75 Ohm line with source and destination termination. For optimum dynamic performance all six analog outputs should have the same load resistance.

The $OUT-_G$ terminal will produce a "sync down" waveform while the $OUT+_G$ terminal will produce a "sync up" waveform. SYNC applies only to the green channel ($OUT-_G$, $OUT+_G$). When SYNC is asserted, only the green channel will output the standard sync level. The red and blue channels output the blanking level. The ***Input Coding Table*** and ***Figures 1 and 2*** show this effect.

Data Inputs

The data inputs to the TDC1318 are single-ended and ECL compatible with internal pull-down resistors to force unused pins to the inactive state. The names red, green and blue are arbitrarily assigned to the three D/A converters but the SYNC control affects only the one named green.

The eight data bits for each D/A converter are decoded prior to being latched in the data register. This reduces glitch energy caused by small differences in propagation delay (skew) in the path to the current switches. On the rising edge of CONV, all data is synchronously transferred to the three D/A converters. Data must be valid for a set-up time, t_S, before and a hold time, t_H, after the rising edge of CONV.

B

Package Interconnections

Signal Type	Signal Name	Function	Value	B5 Package Pins
Power	V_{CCA}	Positive Analog Power Input	0.0V	20
	V_{CCD}	Positive Digital Power Input	0.0V	21
	V_{EEA}	Negative Analog Power Input	−5.2V	1
	V_{EED}	Negative Digital Power Input	−5.2V	40
Reference	REF+	Reference Current Input		2
	COMP	Compensation Capacitor	C_C	3
Convert	CONV	Convert (Clock) Input	ECL	13
Video Controls	SYNC	Video SYNC Data Input	ECL	12
	BLANK	Video BLANK Data Input	ECL	4
	OVERLAY	Video OVERLAY Data Input	ECL	5
Analog Outputs	$OUT-_G$	Green Channel − Output Current	Figure 1	11
	$OUT+_G$	Green Channel + Output Current	Figure 2	10
	$OUT-_R$	Red Channel − Output Current	Figure 1	9
	$OUT+_R$	Red Channel + Output Current	Figure 2	8
	$OUT-_B$	Blue Channel − Output Current	Figure 1	7
	$OUT+_B$	Blue Channel + Output Current	Figure 2	6

Package Interconnections (cont.)

Signal Type	Signal Name	Function	Value	B5 Package Pins
Data Inputs	D_{1G}	Green Channel MSB Data Input	ECL	14
	D_{2G}		ECL	15
	D_{3G}		ECL	16
	D_{4G}		ECL	17
	D_{5G}		ECL	18
	D_{6G}		ECL	19
	D_{7G}		ECL	22
	D_{8G}	Green Channel LSB Data Input	ECL	23
	D_{1R}	Red Channel MSB Data Input	ECL	24
	D_{2R}		ECL	25
	D_{3R}		ECL	26
	D_{4R}		ECL	27
	D_{5R}		ECL	28
	D_{6R}		ECL	29
	D_{7R}		ECL	30
	D_{8R}	Red Channel LSB Data Input	ECL	31
	D_{1B}	Blue Channel MSB Data Input	ECL	32
	D_{2B}		ECL	33
	D_{3B}		ECL	34
	D_{4B}		ECL	35
	D_{5B}		ECL	36
	D_{6B}		ECL	37
	D_{7B}		ECL	38
	D_{8B}	Blue Channel LSB Data Input	ECL	39

Input Coding Tables

Green Channel ($OUT-_G$, $OUT+_G$)

SYNC	BLANK	OVERLAY	DATA MSB LSB	I_{OUT-} (mA)	V_{OUT-} (mV)	I_{OUT+} (mA)	V_{OUT+} (mV)	OUTPUT
0	0	1	XXXXXXXX	0.00	0	−28.56	−1071	110% White
0	0	0	11111111	−1.95	−73	−26.61	−998	Ref. White
0	0	0	00000000	−19.41	−728	−9.15	−343	Ref. Black
0	1	X	XXXXXXXX	−20.83	−781	−7.73	−290	Blank
1	X	X	XXXXXXXX	−28.56	−1071	0.00	0	Sync

Red and Blue Channels ($OUT-_R$, $OUT-_B$, $OUT+_R$, $OUT+_B$)

SYNC	BLANK	OVERLAY	DATA MSB LSB	I_{OUT-} (mA)	V_{OUT-} (mV)	I_{OUT+} (mA)	V_{OUT+} (mV)	OUTPUT
0	0	1	XXXXXXXX	0.00	0	−20.83	−781	110% White
0	0	0	11111111	−1.95	−73	−18.88	−708	Ref. White
0	0	0	00000000	−19.41	−728	−1.42	−53	Ref. Black
0	1	X	XXXXXXXX	−20.83	−781	0.00	0	Blank
1	X	X	XXXXXXXX	−20.83	−781	0.00	0	Blank

Note: 1. V_{OUT} is measured across a 37.5 Ohm load resistor connected between the output terminal and V_{CCA}.

Figure 1. Video Output Waveforms For All OUT− Terminals

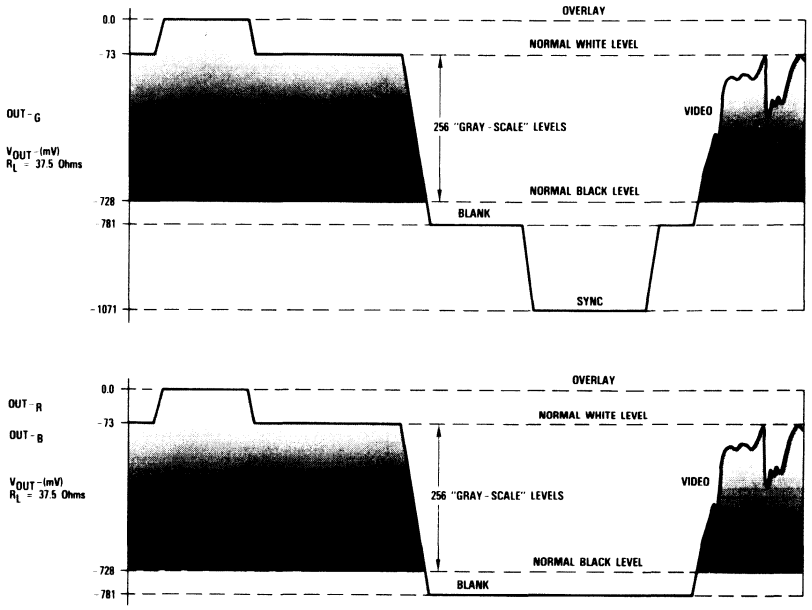


Figure 2. Video Output Waveforms For All OUT+ Terminals

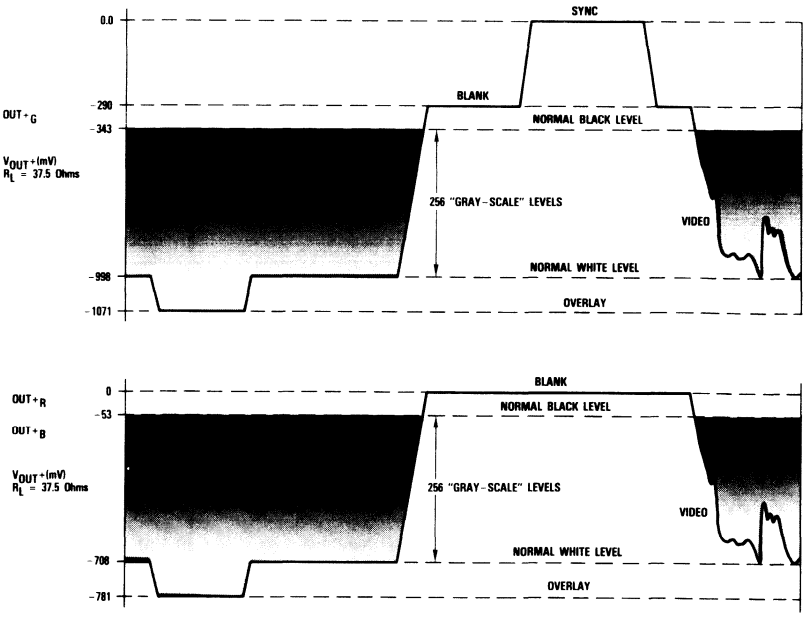


Figure 3. Timing Diagram

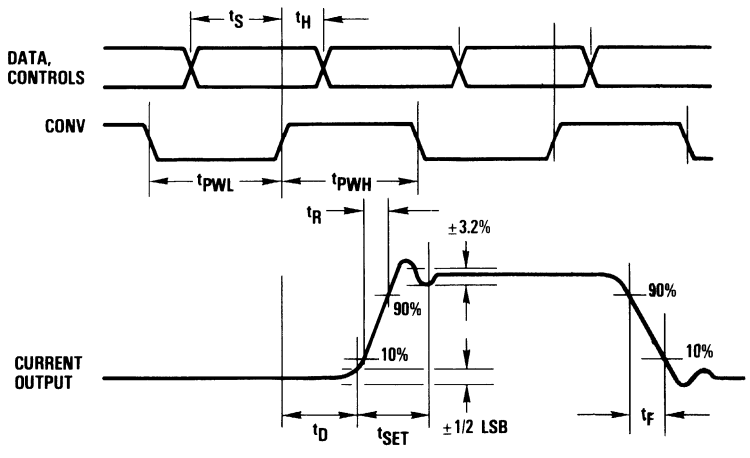
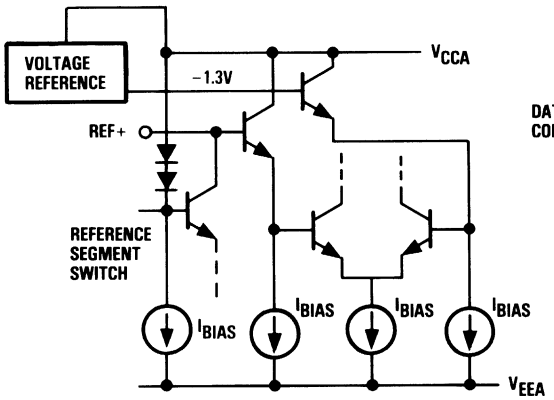


Figure 4. Equivalent Input Circuits



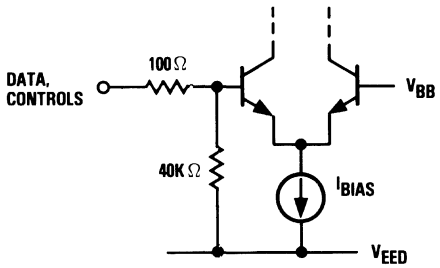


Figure 5. Equivalent Reference And Output Circuits

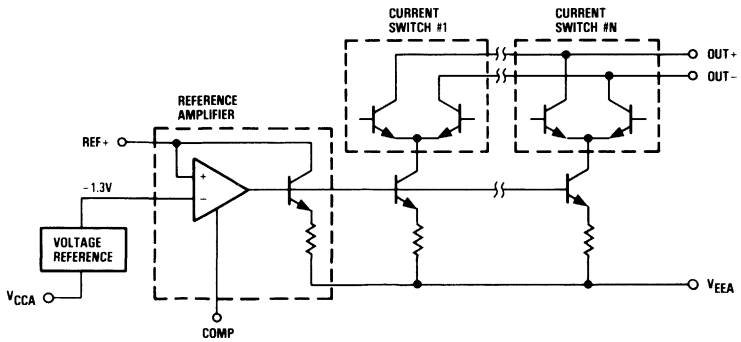
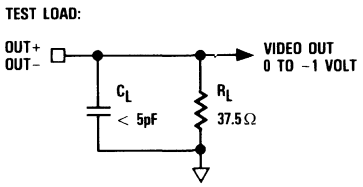


Figure 6. Output Test Load



Absolute maximum ratings (beyond which the device may be damaged) [1]

Power Supply Voltages

V_{EEA} (measured to V_{CCA})	+0.5 to −7.0V
V_{EED} (measured to V_{CCD})	+0.5 to −7.0V
V_{CCA} (measured to V_{CCD})	+0.5 to −0.5V
V_{EEA} (measured to V_{EED})	+0.5 to −0.5V

Inputs

Digital Inputs, applied voltage (measured to V_{CCD}) [2]	+0.5 to V_{EED}V
REF+, applied voltage (measured to V_{CCA}) [2]	+0.5 to V_{EEA}V
REF+, applied current [3,4]	6.0mA

Outputs

Applied voltage (measured to V_{CCA}) [2]	+2.0 to −2.0V
Applied current [3,4]	50mA
Short circuit duration	Unlimited

Temperature

Operating, ambient	−60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−60 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{EED}	Digital Supply Voltage (measured to V_{CCD})	−4.8	−5.2	−5.5	V
V_{EEA}	Analog Supply Voltage (measured to V_{CCA})	−4.8	−5.2	−5.5	V
$V_{CCA}-V_{CCD}$	Supply Voltage Differential	−0.1	0.0	+0.1	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential	−0.1	0.0	+0.1	V
V_{IL}	Input Voltage, Logic LOW			−1.49	V
V_{IH}	Input Voltage, Logic HIGH	−1.00			V
t_{PWL}	CONV Pulse Width, LOW	48	50	52	% Duty Cycle
t_{PWH}	CONV Pulse Width, HIGH	48	50	52	% Duty Cycle
t_S	Setup Time, Digital Inputs	2.0			ns
t_H	Hold Time, Digital Inputs	2.0			ns
I_{REF}	Reference Current	1.00	1.115	1.30	mA
C_C	Compensation Capacitor	2700	10,000		pF
T_A	Ambient Temperature	0		70	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
$I_{EEA} + I_{EED}$	Supply Current	$V_{EEA} = V_{EED}$ = MAX, static [1]			
		T_A = 0°C to 70°C		-380	mA
		T_A = 70°C		-350	mA
C_O	Output Capacitance			20	pF
I_O	Max Output Current	V_{EEA} = NOM, SYNC = HIGH		30	mA
V_{OC}	Compliance Voltage	Measured to V_{CCA}	-1.2	+1.5	V
I_{IL}	Input Current, Logic LOW	V_{EED} = MAX, V_{IN} = -1.45V		250	μA
I_{IH}	Input Current, Logic HIGH	V_{EED} = MAX, V_{IN} = -1.00V		310	μA
I_{IC}	Input Current, Controls	V_{EED} = MAX, $-1.45 < V_{IN} < -1.0$		510	μA
C_{IN}	Input Capacitance, Digital			15	pF

Note:

1. Worst case over all data and control states.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Data Rate	V_{EEA}, V_{EED} = Min	200		MHz
t_D	Clock to Output Delay	V_{EEA}, V_{EED} = Min		7	ns
t_R	Rise Time, Current	10% to 90% of Gray Scale		2.0	ns
t_F	Fall Time, Current	90% to 10% of Gray Scale		1.3	ns
t_{SET}	Current Settling Time	V_{EEA}, V_{EED} = Min, to 3.2%		5	ns

System performance characteristics within specified operating conditions

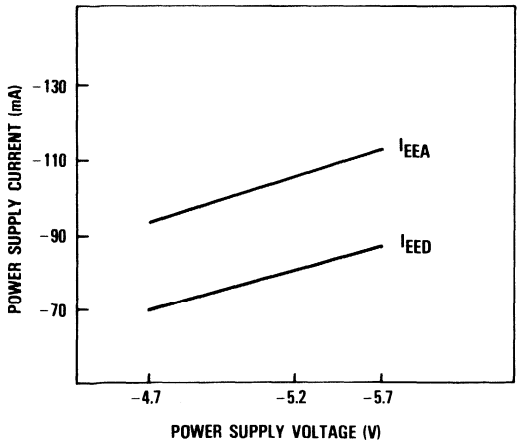
Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error Integral, Terminal Based	V_{EEA}, V_{EED}, I_{REF} = Nom		0.2	% of Gray Scale
E_{LD}	Linearity Error Differential	V_{EEA}, V_{EED}, I_{REF} = Nom		0.2	% of Gray Scale
I_{OF}	Output Offset Current	V_{EEA}, V_{EED} = Max, SYNC = BLANK = LOW OVERLAY = HIGH		10	μA
E_G	Absolute Gain Error	V_{EEA}, V_{EED} = Min		7	% of Gray Scale
TC_G	Gain Error Tempco	I_{REF} = Nom		.06	% of Gray Scale/°C
PSRR	Power Supply Rejection	@20kHz, V_{EEA}, V_{EED}, I_{REF} = Nom [1]	45		dB [3]
		@60Hz, V_{EEA}, V_{EED}, I_{REF} = Nom [2]	46		dB [3]
PSS	Power Supply Sensitivity	V_{EEA}, V_{EED}, I_{REF} = Nom		120	μA/V
G_C	Peak Glitch Charge			800	fCoulomb [4]
G_I	Peak Glitch Current			1.2	mA
G_E	Peak Glitch Energy (Area) [5]			30	pV-sec

Notes:

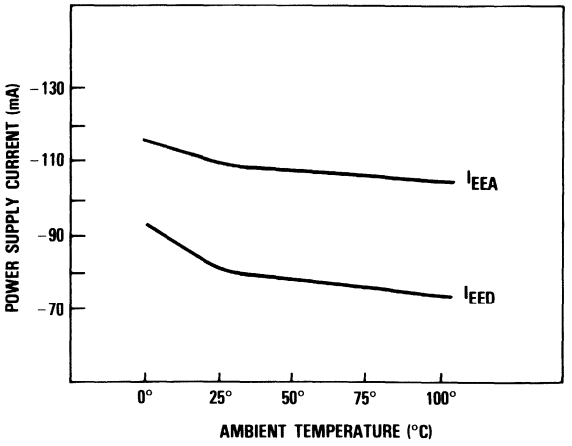
1. 20kHz, 0.75 Volts p-p superimposed on V_{EEA} and V_{EED}. Units (dB) are relative to full gray scale.
2. 60Hz, 0.75 Volts p-p superimposed on V_{EEA} and V_{EED}. Units (dB) are relative to full gray scale.
3. Units (dB) are relative to full gray scale.
4. fCoulomb = femtocoulombs = microamps x nanoseconds.
5. 37.5 Ohm resistive load. Glitches tend to be symmetric, average glitch energy approaches zero.

Typical Performance Curves

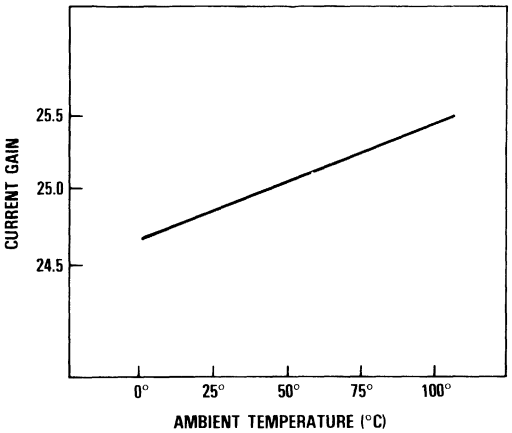
A. Power Supply Current vs. Power Supply Voltage



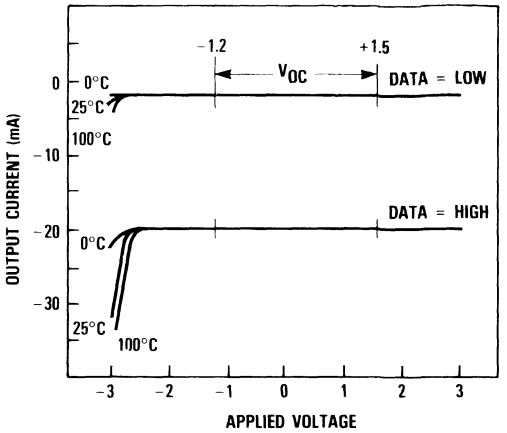
B. Power Supply Current vs. Temperature



C. Current Gain vs. Temperature

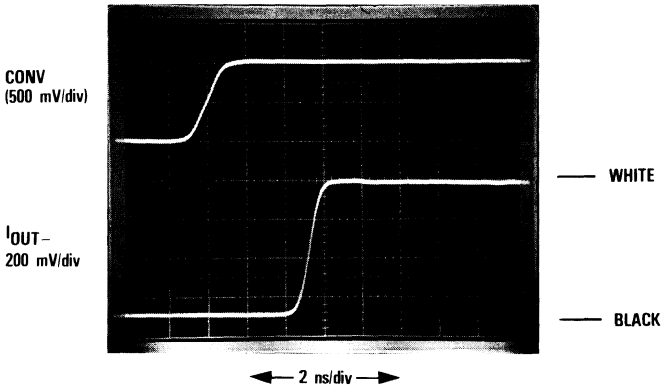


D. Output Current vs. Applied Voltage
(Output Voltage Compliance)



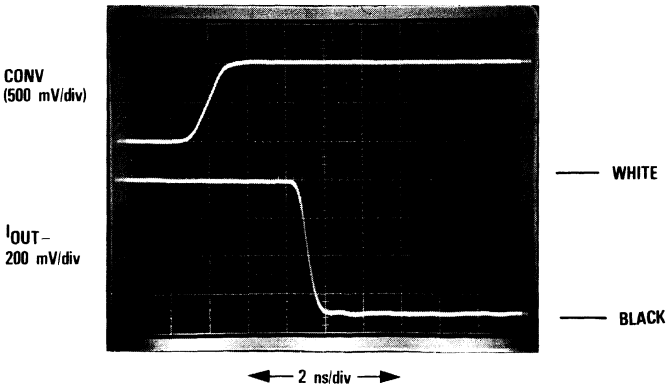
E. V_{OUT} Risetime (Scope Photo)

Video "Black-to-White" Transition.



F. V_{OUT} Falltime (Scope Photo)

Video "White-to-Black" Transition.



Typical Interface Circuit

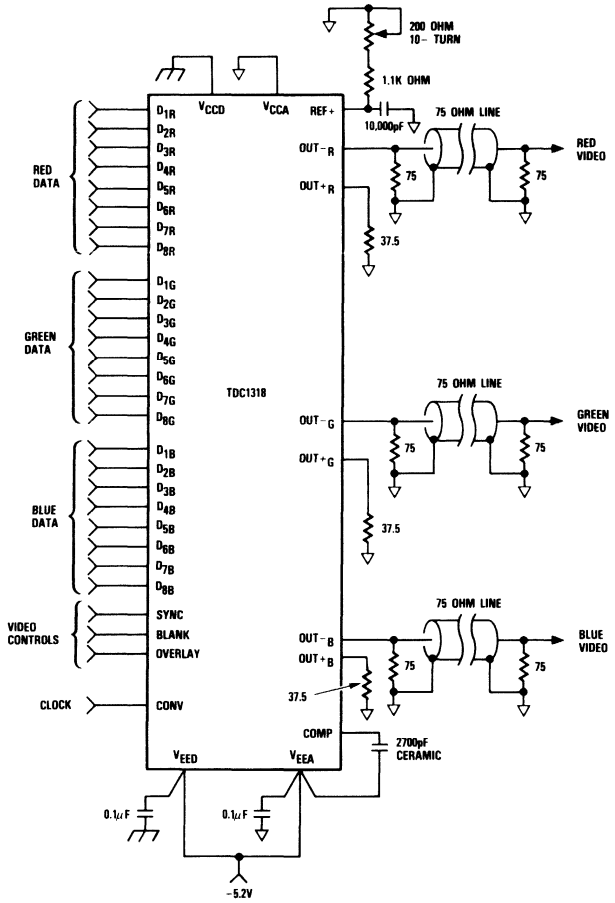
Figure 7 shows the basic connections to the TDC1318 as it might appear in a color CRT graphics system. The device is powered from a single -5.2 Volt power supply and is connected to separate analog and digital grounds. All digital inputs are single-ended and ECL compatible. Standard ECL termination practice should be used with all digital inputs to the TDC1318. The series resistor network between the REF+ input and analog ground is useful for adjusting the overall gain of all three D/A converters.

In this application, all three D/A converters are connected to drive 75 Ohm lines to inputs of a color monitor. Source and destination terminating resistors are required for optimum dynamic performance. Using the OUT- terminals, a "sync down" waveform will be provided at the monitor inputs. The unused outputs (in this case $OUT+_R$, $OUT+_G$ and $OUT+_B$) should be connected to analog ground through 37.5 Ohm resistors.

The TDC1318 can be operated in TTL systems by connecting the V_{CC} inputs to the +5 Volt power supply and the V_{EE} inputs to ground. Digital input and analog output level-shifting techniques described the TRW Application Note TP-33 "Using The TDC1018 And TDC1034 In A TTL Environment" should be followed.

B

Figure 7. Typical Interface Circuit



Calibration

The TDC1318 is easy to use and calibrate. The *Typical Interface Circuit (Figure 7)* has only one adjustment. The variable resistor in the series network connected to REF+ will allow a ±10% variation in the overall gain of the device. Since all three D/A converters are operated from the same reference current, adjusting the variable resistor will change the gain of all three D/A converters.

The circuit of *Figure 7* is best calibrated by enabling either BLANK or SYNC and adjusting the reference current until the voltage at the monitor input is −781mV (BLANK) or −1071mV (SYNC, green channel) with respect to analog ground. Depending upon system to system matching requirements, a fixed value resistor (approximately 1.1kOhm) may be connected between REF+ and analog ground eliminating the need to calibrate the TDC1318 at all.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1318B5C	STD−T_A=0°C to 70°C	Commercial	40 Pin CERDIP	1318B5C

TDC1334

Digital-to-Analog Converter
Triple 4-Bit, 200MHz

The TDC1334 consists of three separate 4-bit D/A converters in a single monolithic integrated circuit. The TDC1334 is designed for 200MHz operation and is ECL compatible. Each of the three D/A converters has complementary current-sinking outputs that can directly drive 75 Ohm lines.

Video controls, SYNC and BLANK, are included for setting video output levels during synchronization and CRT blanking intervals. BRIGHT, a 10% brightness enhancement control, is useful for emphasizing portions of a CRT display and for cursor identification. All data and control inputs to the TDC1334 are internally registered on the rising edge of the clock (CONV).

A single band-gap voltage source is the reference for all three D/A converters and a single external resistor determines the reference current. The pinout of the TDC1334 allows for optimum board layout and minimizes digital feedthrough. Analog and digital grounds are kept separate for maximum system ground flexibility.

Features

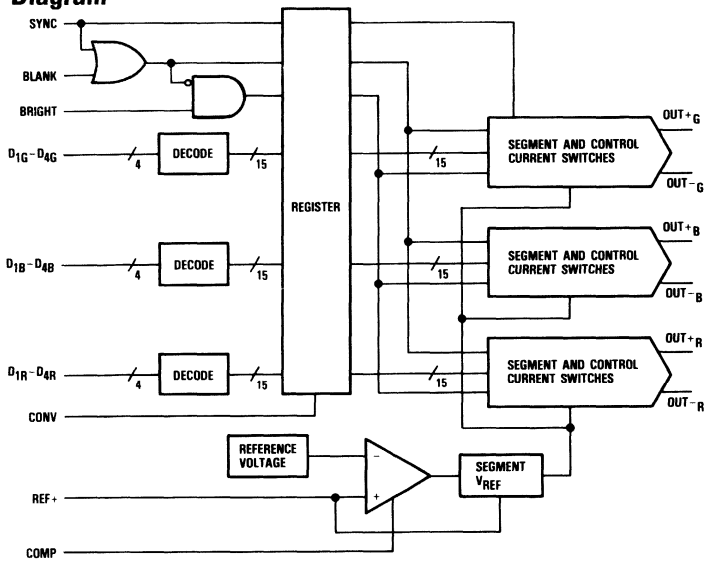
- Complete Monolithic "Graphics-Ready"
- Three 4-Bit D/A Converters
- Registered Data Inputs
- Registered SYNC, BLANK And BRIGHT Controls
- On-Board Voltage Reference
- Linearity Error Less Than 1/8 LSB
- Guaranteed Monotonicity
- 200MHz Operation, ECL Compatible Inputs
- Can Be Operated In TTL Systems
- Complementary Current Outputs
- Single −5.2V Power Supply Required
- Available In A 28 Pin CERDIP Package

Applications

- Raster Scan Displays
- Bit-Mapped Graphics
- PC Graphics Systems
- CAD/CAM Workstations

B

Functional Block Diagram



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La Jolla, CA 92038

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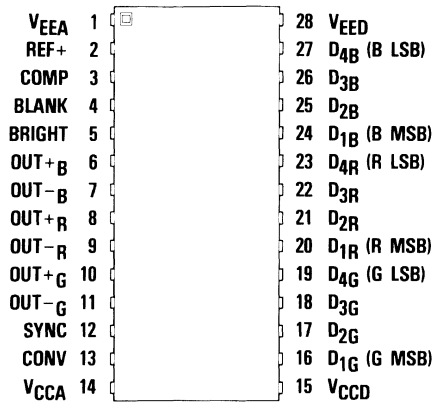
Printed in the U.S.A.

Pin Assignments



28 Pin CERDIP – B6 Package

Functional Description

General Information

The TDC1334 has three pairs of complementary analog current outputs for directly driving the 75 Ohm red, green and blue inputs of a RGB color video monitor. The amplitude of the current flowing into each output terminal is proportional to the product of the 4-bit input data and the analog reference current. All digital inputs are compatible with standard (10K) ECL logic levels. The rising edge of CONVert clocks all data and control bits into an internal register. These binary data values are then converted into analog output current by a set of matched current switches.

Power

For optimum noise immunity, the TDC1334 operates from separate analog and digital power inputs, V_{EEA} and V_{EED}, which require −5.2V. These may be connected to the same power source but power supply decoupling for each power input is recommended. The return path for I_{EED}, the current drawn from the V_{EED} supply, is V_{CCD}. The return path for I_{EEA} is V_{CCA}. All power input pins must be connected.

Although the TDC1334 is specified for a −5.2V supply, operation from +5V is possible, provided that the correct polarity of all voltages are maintained. For additional information concerning the use of ECL D/A converters in a +5V system, refer to *TRW Application Note TP-33 "Using The TDC1018 And TDC1034 In A TTL Environment."*

Reference

The TDC1334 has an on-board band-gap voltage source (−1.4V, nominal) that is referenced to V_{CCA}. The reference input, REF+, is the noninverting input of the reference amplifier. This amplifier provides a reference voltage for all of the current switches.

The analog output currents are proportional to the digital data and the reference current, I_{REF}. The full-scale output value may be adjusted by varying the reference current. Since the reference can be varied dynamically, the stability of the analog output depends upon the stability of I_{REF}.

A compensation input, COMP, is provided to externally compensate the internal reference amplifier. A capacitor, C_C, should be connected between COMP and V_{EEA}.

Video Controls

The TDC1334 has three video control inputs: SYNC, BLANK and BRIGHT. Internal logic simplifies the use of these controls in video applications. All are ECL compatible and include internal pull-down resistors to force any unused control to the inactive state. The video controls are registered on the rising edge of the CONV clock input. Video control inputs must be valid a set-up time, t_S, before and a hold time, t_H, after the rising edge of CONV.

Asserting the video controls produces output levels for synchronization and blanking intervals, and 10% brightness enhancement. The effects of the video controls on the analog outputs are shown in the *Input Coding Table*. SYNC overrides data, BLANK and BRIGHT, producing a full-scale output on OUT−G and OUT+G only. BLANK overrides data and BRIGHT producing a "blacker than black" video level on all three D/A converters. BRIGHT creates an enhanced video level by adding 10% to the present value of the red, green and blue data.

Data Inputs

The data inputs to the TDC1334 are single-ended and ECL compatible with internal pull-down resistors to force unused pins to the inactive state. The names, red, green

Data Inputs (cont.)

and blue, are arbitrarily assigned to the three D/A converters but the SYNC control affects only the one named green. The four data bits for each D/A converter are decoded prior to being latched in the data register, reducing glitch energy caused by small differences in propagation delay (skew) in the path to the current switches. On the rising edge of CONV, all data is synchronously transferred to the three D/A converters. Data must be valid for a set-up time, t_S, before and a hold time, t_H, after the rising edge of CONV.

Convert

The TDC1334 CONV clock is a single-ended ECL compatible input whose rising edge is used to synchronize the internal data transfer from the data encoder into the current switches of the three D/A converters.

Analog Outputs

The red, green and blue analog outputs of the TDC1334 are each high-impedance complementary current sinks whose currents vary in proportion to the input data, video control inputs and reference current. All outputs are capable of directly driving 75 Ohm lines to normal video levels. The voltage produced across the load is the product of the output current and the net load impedance. This voltage varies between 0 and −1V when driving a 75 Ohm line with source and destination termination. The $OUT-_G$ terminal will produce a "sync down" waveform while the $OUT+_G$ terminal will produce a "sync up" waveform. SYNC applies only to the green channel ($OUT-_G$, $OUT+_G$). There is no SYNC circuitry for the red and blue channels. This results in no SYNC offset on the $OUT+_R$ and $OUT+_B$ terminals. The *Input Coding Table* shows this effect.

B

Package Interconnections

Signal Type	Signal Name	Function	Value	B6 Package Pins
Power	V_{CCA}	Positive Analog Power Input	0.0V	14
	V_{CCD}	Positive Digital Power Input	0.0V	15
	V_{EEA}	Negative Analog Power Input	−5.2V	1
	V_{EED}	Negative Digital Power Input	−5.2V	28
Reference	REF+	Reference Current Input	1.17mA Nom.	2
	COMP	Compensation Capacitor	2700pF	3
Video Controls	SYNC	Video Sync Input	ECL	12
	BLANK	Video Blanking Input	ECL	4
	BRIGHT	Brightness Enhancement Input	ECL	5
Data Inputs	D_{1G}	Green Channel MSB Data Input	ECL	16
	D_{2G}		ECL	17
	D_{3G}		ECL	18
	D_{4G}	Green Channel LSB Data Input	ECL	19
	D_{1R}	Red Channel MSB Data Input	ECL	20
	D_{2R}		ECL	21
	D_{3R}		ECL	22
	D_{4R}	Red Channel LSB Data Input	ECL	23
	D_{1B}	Blue Channel MSB Data Input	ECL	24
	D_{2B}		ECL	25
	D_{3B}		ECL	26
	D_{4B}	Blue Channel LSB Data Input	ECL	27

Package Interconnections (cont.)

Signal Type	Signal Name	Function	Value	B6 Package Pins
Convert	CONV	Convert (Clock) Input	ECL	13
Analog Outputs	$OUT-_G$	Green Channel – Output Current	Figure 1	11
	$OUT+_G$	Green Channel + Output Current	Figure 2	10
	$OUT-_R$	Red Channel – Output Current	Figure 1	9
	$OUT+_R$	Red Channel + Output Current	Figure 2	8
	$OUT-_B$	Blue Channel – Output Current	Figure 1	7
	$OUT+_B$	Blue Channel + Output Current	Figure 2	6

Input Coding Tables

Green Channel ($OUT-_G$, $OUT+_G$)

SYNC	BLANK	BRIGHT	DATA	I_{OUT-} (mA)	V_{OUT-} (mV)	I_{OUT+} (mA)	V_{OUT+} (mV)	Description
0	0	1	1111	0.00	0	−28.56	−1071	Enhanced White
0	0	0	1111	−1.95	−73	−26.61	−998	Normal White
0	0	1	0000	−17.44	−654	−11.12	−417	Enhanced Black
0	0	0	0000	−19.41	−728	−9.15	−343	Normal Black
0	1	X	XXXX	−20.83	−781	−7.73	−290	Blank Level
1	X	X	XXXX	−28.56	−1071	0.00	0	Sync Level

Red and Blue Channels ($OUT-_R$, $OUT-_B$, $OUT+_R$, $OUT+_B$)

SYNC	BLANK	BRIGHT	DATA	I_{OUT-} (mA)	V_{OUT-} (mV)	I_{OUT+} (mA)	V_{OUT+} (mV)	Description
0	0	1	1111	0.00	0	−20.83	−781	Enhanced White
0	0	0	1111	−1.95	−73	−18.88	−708	Normal White
0	0	1	0000	−17.44	−654	−3.39	−127	Enhanced Black
0	0	0	0000	−19.41	−728	−1.42	−53	Normal Black
0	1	X	XXXX	−20.83	−781	0.00	0	Blank Level
1	X	X	XXXX	−20.83	−781	0.00	0	Blank Level

Note: 1. V_{OUT} is measured across a 37.5 Ohm load resistor connected between the output terminal and V_{CCA}.

Figure 1. Video Output Waveforms All OUT– Terminals

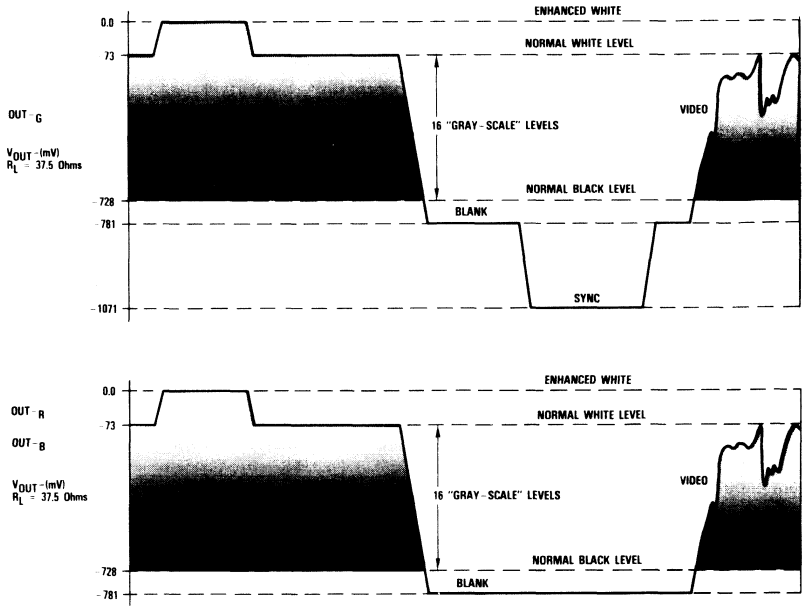


Figure 2. Video Output Waveforms For All OUT+ Terminals

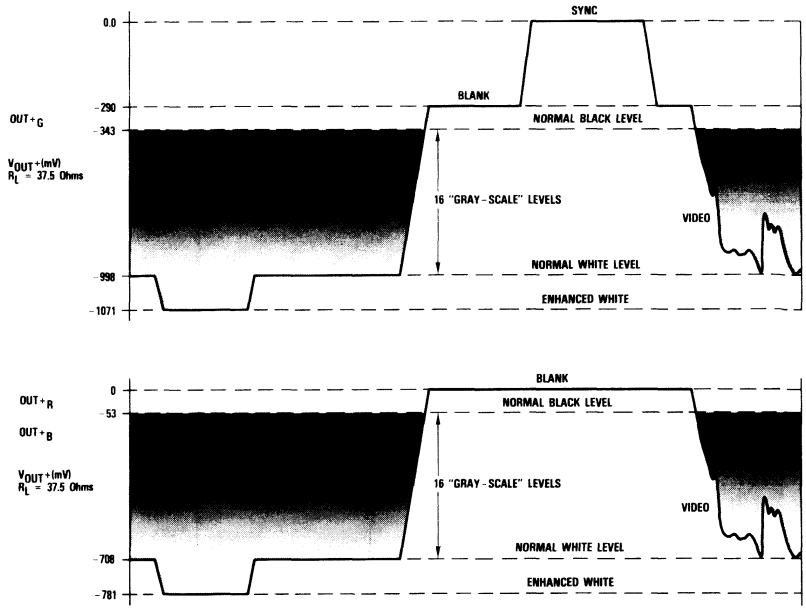


Figure 3. Timing Diagram

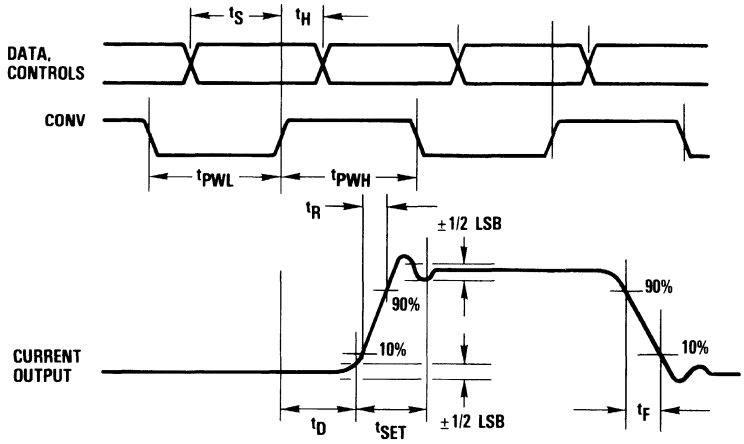


Figure 4. Equivalent Input Circuits

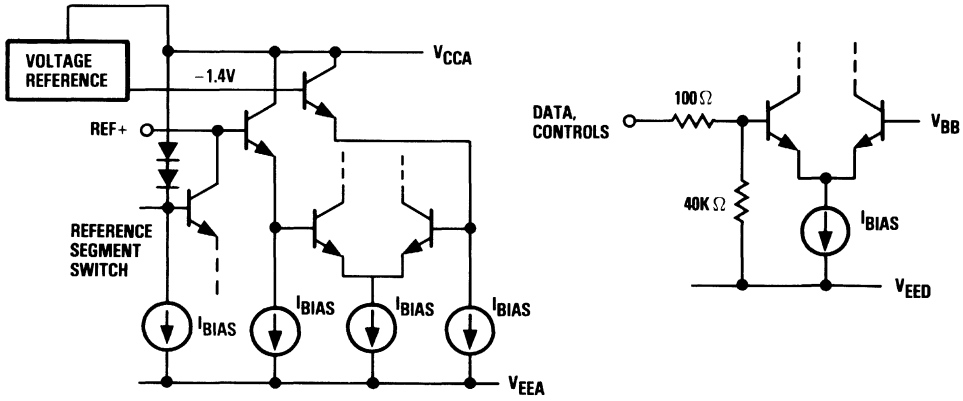


Figure 5. Equivalent Reference And Output Circuits

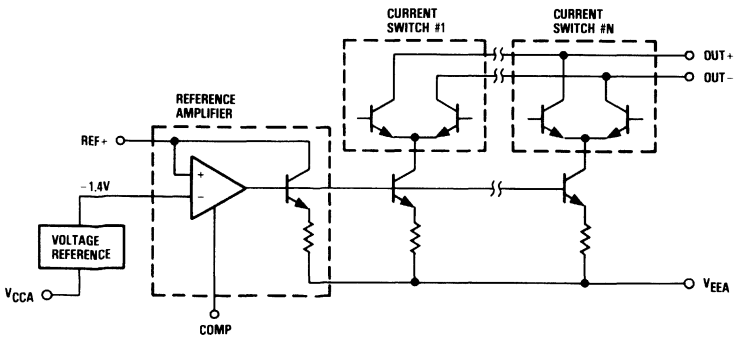
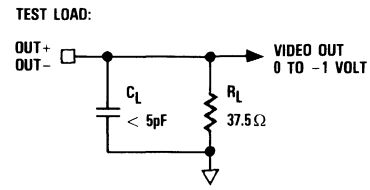


Figure 6. Output Test Load



Absolute maximum ratings (beyond which the device may be damaged) [1]

Power Supply Voltages

V_{EEA} (measured to V_{CCA})	+0.5 to −7.0V
V_{EED} (measured to V_{CCD})	+0.5 to −7.0V
V_{CCA} (measured to V_{CCD})	+0.5 to −0.5V
V_{EEA} (measured to V_{EED})	+0.5 to −0.5V

Inputs

Digital Inputs, applied voltage (measured to V_{CCD})[2]	+0.5 to V_{EED}V
REF+, applied voltage (measured to V_{CCA})[2]	+0.5 to V_{EEA}V
REF+, applied current[3,4]	6.0mA

Outputs

Applied voltage (measured to V_{CCA})[2]	+2.0 to −2.0V
Applied current[3,4]	50mA
Short circuit duration	Unlimited

Temperature

Operating, ambient	−60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−60 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{EED}	Digital Supply Voltage (measured to V_{CCD})	−4.7	−5.2	−5.5	V
V_{EEA}	Analog Supply Voltage (measured to V_{CCA})	−4.7	−5.2	−5.5	V
$V_{CCA}-V_{CCD}$	Supply Voltage Differential	−0.1	0.0	+0.1	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential	−0.1	0.0	+0.1	V
V_{IL}	Input Voltage, Logic LOW			−1.49	V
V_{IH}	Input Voltage, Logic HIGH	−1.045			V
t_{PWL}	CONV Pulse Width, LOW	4			ns
t_{PWH}	CONV Pulse Width, HIGH	4			ns
t_S	Setup Time, Digital Inputs	0			ns
t_H	Hold Time, Digital Inputs	2			ns
I_{REF}	Reference Current	1.00	1.17	1.30	mA
R_{REF}	Reference Resistor		1200		Ω
C_C	Compensation Capacitor	1000	2700		pF
T_A	Ambient Temperature	0		70	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Temperature Range: Standard Max	Units
$I_{EEA} + I_{EED}$	Supply Current	$V_{EEA} = V_{EED}$ = Max, static[1]			
		T_A = 0°C to 70°C		−290	mA
		T_A = 70°C		−220	mA
R_O	Output Resistance		50		kOhm
C_O	Output Capacitance			20	pF
I_O	Max Output Current	V_{EEA} = Nom, SYNC = HIGH		30	mA
V_{OC}	Compliance Voltage	Measured to V_{CCA}	−1.2	+1.5	V
I_{IL}	Input Current, Logic LOW	Data, CONV V_{EED} = Max, V_{IN} = −1.49V		135	μA
I_{IH}	Input Current, Logic HIGH	Data, CONV V_{EED} = Max, V_{IN} = −1.045V		150	μA
I_{IC}	Input Current	Video Controls V_{EED} = Max, $-1.045 < V_{IN} < -1.49$		380	μA
C_{REF}	Input Capacitance, REF+			5	pF
C_{IN}	Input Capacitance, Digital			5	pF

Notes:

1. Worst case over all data and control states.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Temperature Range: Standard Max	Units
F_S	Maximum Data Rate	V_{EEA}, V_{EED} = Min	200		MHz
t_D	Clock to Output Delay	V_{EEA}, V_{EED} = Min		8	ns
t_R	Rise Time, Current	10% to 90% of Gray Scale		2	ns
t_F	Fall Time, Current	90% to 10% of Gray Scale		2	ns
t_{SET}	Current Settling Time	V_{EEA}, V_{EED} = Min, to 3.2%		5	ns

System performance characteristics within specified operating conditions

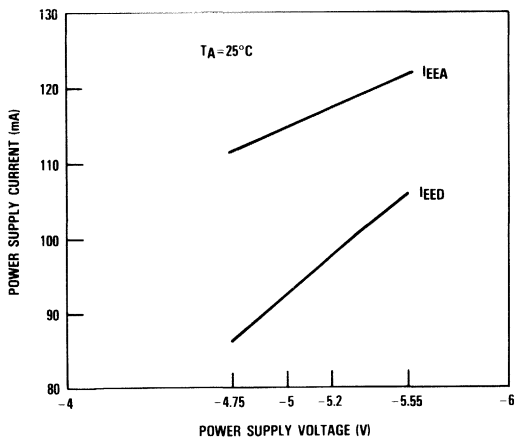
Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error Integral	V_{EEA}, V_{EED}, I_{REF} = Nom		0.8	% of Gray Scale
E_{LD}	Linearity Error Differential	V_{EEA}, V_{EED}, I_{REF} = Nom		0.8	% of Gray Scale
I_{OF}	Output Offset Current	V_{EEA}, V_{EED} = Max, SYNC = BLANK = LOW Data = BRIGHT = HIGH, OUT− Terminals		10	μA
E_G	Absolute Gain Error	V_{EEA}, V_{EED} = Min		6	% of Gray Scale
TC_G	Gain Error Tempco	I_{REF} = Nom		.02	% of Gray Scale/°C
BWR	Reference Bandwidth	C_C = Min	0.5		MHz
PSRR	Power Supply Rejection	@20kHz, V_{EEA}, V_{EED}, I_{REF} = Nom [1]	45		dB
		@60Hz, V_{EEA}, V_{EED}, I_{REF} = Nom [2]	46		dB
PSS	Power Supply Sensitivity	V_{EEA}, V_{EED}, I_{REF} = Nom		500	μA/V
G_C	Peak Glitch Charge [3]			800	fCoulomb
G_I	Peak Glitch Current			1.2	mA
G_E	Peak Glitch Energy (Area) [4]			30	pV−sec

Notes:

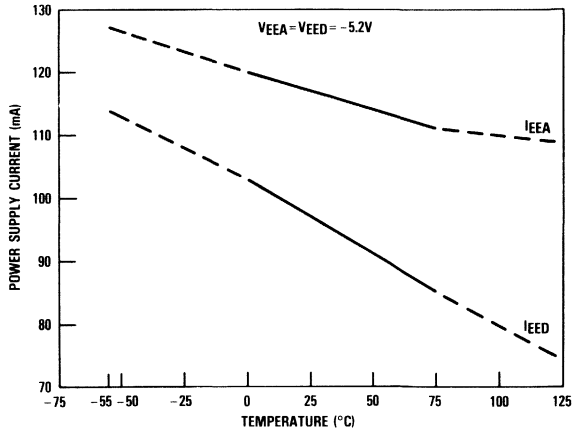
1. 20kHz, 0.75 Volts p−p superimposed on V_{EEA} and V_{EED}. Units (dB) are relative to full gray scale.
2. 60Hz, 0.75 Volts p−p superimposed on V_{EEA} and V_{EED}. Units (dB) are relative to full gray scale.
3. fCoulomb = femtocoulombs = microamps x nanoseconds.
4. 37.5 Ohm resistive load. Glitches tend to be symmetric, average glitch energy approaches zero.

Typical Performance Curves

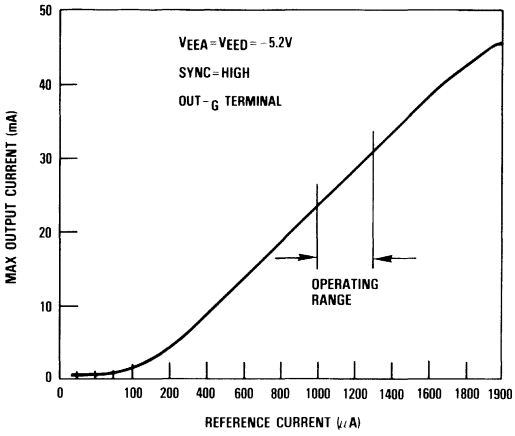
A. Power Supply Current vs. Power Supply Voltage



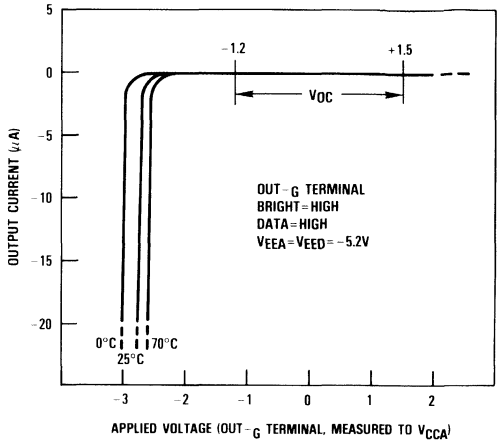
B. Power Supply Current vs. Temperature



C. Max Output Current vs. Reference Current

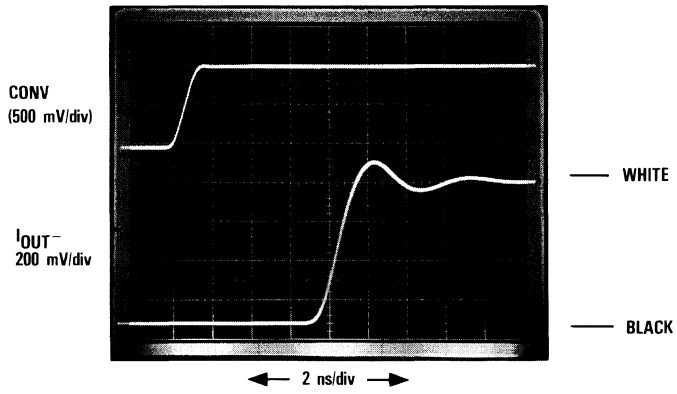


D. Output Current vs. Output Voltage (Output Voltage Compliance)



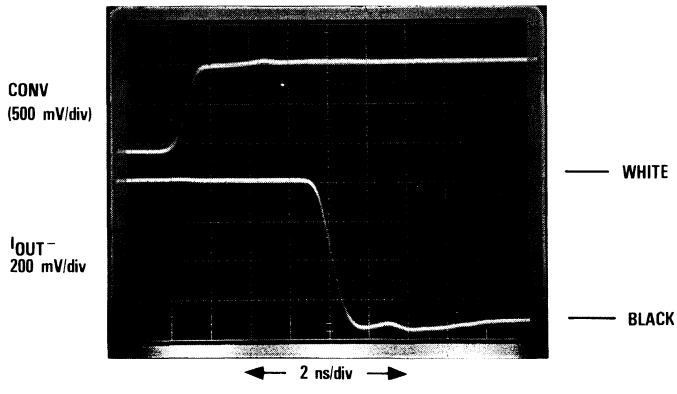
E. V_{OUT} Risetime (Scope Photo)

Video "Black-to-White" Transition.



F. V_{OUT} Falltime (Scope Photo)

Video "White-to-Black" Transition.



Typical Interface Circuit

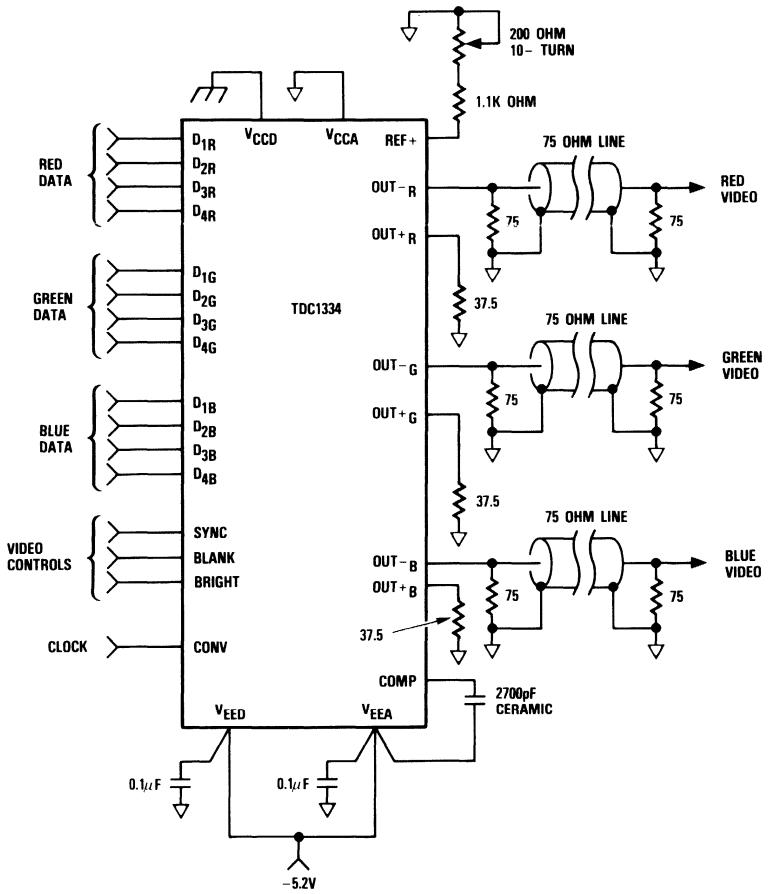
Figure 7. shows the basic connections of the TDC1334 as it might appear in a color CRT graphics system. The device is powered from a single -5.2 Volt power supply and is connected to separate analog and digital grounds. All digital inputs are single-ended and ECL compatible. Standard ECL termination practice should be used with all digital inputs to the TDC1334. The series resistor network between the REF+ input and analog ground is useful for adjusting the overall gain of all three D/A converters simultaneously.

In this application, all three D/A converters are connected to drive 75 Ohm lines to inputs of a color monitor. Source and destination terminating resistors are required for optimum dynamic performance. Using the OUT- terminals, a "sync down" waveform will be provided at the monitor inputs. The unused outputs ($OUT+_R$, $OUT+_G$ and $OUT+_B$ in this case) should be connected to analog ground through a 37.5 Ω resistor.

The TDC1334 can be operated in TTL systems by connecting the V_{CC} inputs to the +5 Volt power supply and the V_{EE} inputs to ground. Digital input and analog output level-shifting techniques described the TRW Application Note TP-33 "Using The TDC1018 And TDC1034 In A TTL Environment" should be followed.

B

Figure 7. Typical Interface Circuit



Calibration

The TDC1334 is very easy to use and calibrate. The *Typical Interface Circuit (Figure 7)* has only one adjustment. The variable resistor in the series network connected to REF+ will allow a ±10% variation in the overall gain of the device. Since all three D/A converters are operated from the same reference current, adjusting the variable resistor will change the gain of all three D/A converters simultaneously. The circuit of *Figure 7* is best calibrated by enabling either BLANK or SYNC and adjusting the reference current until the voltage at the monitor input is −781mV (BLANK) or −1071mV (SYNC, green channel only) with respect to analog ground. Depending upon system to system matching requirements, a fixed value resistor (approximately 1.2kOhm) may be connected between REF+ and analog ground eliminating the need to calibrate the TDC1334 at all.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1334B6C	STD−T_A=0°C to 70°C	Commercial	28 Pin CERDIP	1334B6C

Linear Products

TRW provides a selection of linear products that support and enhance the performance of our data conversion products.

Voltage references are needed by all A/D and D/A converters. These may be included in the converter (as with the THC-series from TRW), may be derived from the power supply (not very stable or quiet), or may be provided externally. A converter is only as good as its reference. For the most demanding applications (such as with the TMC1241/TMC1251 family) the 3ppm/°C TMC4169 is excellent. For less demanding applications (4-10 bits) the TDC4611 and TDC4614 provide a cost-effective solution, and offer the convenience of integrated amplifiers for reference shifting and buffering.

A Track/Hold circuit can usually improve the performance of a flash A/D converter at high input frequencies. Depending on your system performance requirements, the THC4940 may be just the thing to extend signal bandwidth and reduce distortion.

TRW's D/As are designed to drive terminated lines (with impedances as low as 25Ω) directly. At times, however, an amplifier is needed. The THC4940 is the best high-speed high-voltage video bandwidth buffer available.

Product	Output[1] Voltage (V)	Tolerance[1] (±%)	Temperature[1] Coefficient (ppm/°C)	Package		Grade[2]	Notes	Page
References								
TDC4611	−0.7 to +6.3	N/A	20	B4, NH	8 Pin DIP	C, F	Adjustable.	C23
				ME	14 Pin SOIC	C	Includes Operational Amplifier.	
TDC4614	+1.2 to +6.3	N/A	20	B9, N9	16 Pin DIP	C, F	Adjustable.	C41
				M9	16 Pin SOIC	C	Includes 4 Operational Amplifiers.	
TDC4169-3	+10.000	±0.05%	3	Y8	8 Pin Metal Can	C, F	High Precision.	C3
				NH	8 Pin DIP	C	Laser Trimmed.	
-2	+10.000	±0.05%	5	Y8	8 Pin Metal Can	C, F		
				NH	8 Pin DIP	C		
-1	+10.000	±0.05%	10	NH	8 Pin DIP	C		
	+10.000	±0.10%	30	MH	8 Pin SOIC	C, F		
				NH	8 Pin DIP	C		
				Z3	3 Pin Plastic	C		

Product	−3dB Bandwidth (MHz)	Slew Rate (V/ns)	Settling Time[1] (ns to .1%)	Input Offset Voltage[1] (mV)	Gain Flatness (dB)	Package	Grade[2]	Notes	Page
Amplifier									
THC4231	120	1.8	22	4.5	0.6	X1 12 Lead Metal Can	C, V	Current Feedback. Constant Bandwidth with Gain changes.	C11

Product	−3dB Bandwidth (MHz)	Acquisition Time[1] (ns to .1%)	Settling Time[1] (ns to 1mV)	Pedestal Offset[1] (mV)	Aperture Jitter[1] (ps_{RMS})	Package	Grade[2]	Notes	Page
Track/Hold									
THC4940	110	22	18	8	1.6	X2 24 Pin DIP	B, A	Very Fast Sampling. Wideband T/H Amplifier.	C59

Notes: 1. Guaranteed. See product specifications for test conditions.

2. A = High Reliability, $T_C = -55°C$ to 125°C.
B = Industrial, $T_C = -25°C$ to 85°C.
C = Commercial, $T_A = 0°C$ to 70°C.
F = Extended Temperature Range, $T_C = -55°C$ to 125°C.
V = MIL-STD-883 Compliant, $T_C = -55°C$ to 125°C

TDC4169

Precision +10.000 Volt Voltage Reference

The TDC4169 is a voltage reference offering exceptional accuracy and stability over a wide range of temperature and power supply conditions. The TDC4169 produces a reference voltage of +10.000 Volts generated from a power supply input voltage from +13 to +17 Volts. The TDC4169 also operates from a current source of 2mA.

Laser-trimmed temperature compensation circuits reduce the temperature coefficient of the output voltage to 1ppm/°C. The TDC4169 is trimmed by cutting resistors open to eliminate the effect of ageing caused by electromigration on the integrated circuit. The device also exhibits exceptional stability as supply voltage and current are varied. The reference can be operated either in series or in shunt mode and the output is short circuit protected.

The device is available in three package styles: 8-pin metal can, 8-pin plastic DIP, 8-pin SOIC, and 3-pin plastic TO-92. In all packages but the TO-92 there is an additional pin that can be used as a fine adjustment to the reference voltage. The TDC4169 is available in both commercial (0°C to 70°C) and military (–55°C to 125°C) temperature ranges.

Features

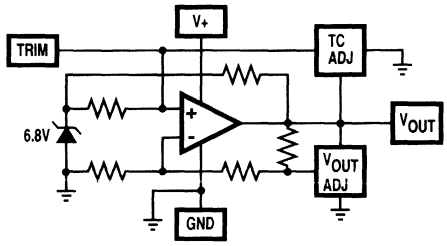
- Initial Voltage Accuracy 0.05%
- Temperature Stability 1.5ppm/°C, Guaranteed
- Power Supply Rejection Better Than 2ppm/V
- Very Low Noise

Applications

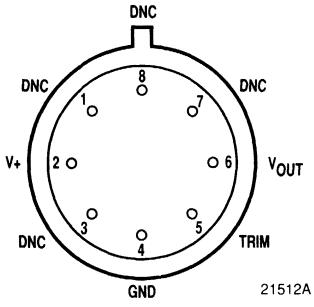
- High Resolution A/D Converters
- Precision Offset Control

C

Functional Block Diagram

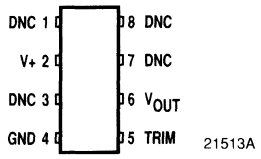


Pin Assignments



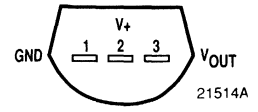
TOP VIEW

8 Pin Metal Can – Y8 Package



TOP VIEW

8 Pin Plastic DIP – NH Package
8 Pin Plastic SOIC – MH Package



TOP VIEW

3 Pin Plastic – Z3 Package

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40G06719 Rev. A – 8/90
Printed in the U.S.A.

Functional Description

The THC4169 precision voltage reference is based upon an internal buried Zener diode and output amplifier. The amplifier serves several functions in the THC4169 including gain (A_V = ~+1.47), temperature coefficient compensation and output current source or sink. Advanced trim techniques applied to thin-film resistors establish the initial accuracy of the THC4169 and ensure long-term stability, low noise, and low sensitivity to variations in temperature and input voltage.

The V+ pin supplies the power to the TDC4169. When used in series mode, the potential at this pin should be between +13 and +35 Volts. When used in shunt mode, the current through V_{IN} must be limited to 50mA. The GND pin serves as the zero Volt reference point for the circuitry of the TDC4169 and as the current sink for the V+ current. The V_{OUT} pin provides +10.000 Volts referred to the GND pin.

The TRIM pin can be used to adjust the V_{OUT} voltage slightly (approximately 15mV per μA of current flowing into TRIM). This pin can also be used to filter the reference noise by the adding a low-leakage capacitor connected from TRIM to GND.

There are several pins which are used at the factory to adjust output voltage and temperature coefficient. These pins should be left unconnected and may be removed from the package if desired.

Package Interconnections

Signal Type	Signal Name	Function	Value	Pin (Z3 package)	Pin NH, MH, Y8 Package
Power, Ground	V+	Power Supply	15V	2	2
	GND	Ground	0V	1	4
Output	V_{OUT}	Reference Output	10.000V	3	6
Input	TRIM	Fine Adjust of V_{OUT}	Open	—	5
No Connection	DNC	Do Not Connect	Open	—	1,3,7,8

Absolute maximum ratings (beyond which the device may be damaged)

Supply Voltage (V+ measured to GND) ..... –0.3 to 35V

Reverse Current (Shunt mode) 5mA

Power Dissipation 600mW

Storage Temperature Range ..... –60°C to +150°C

Soldering Information

- NH Package (10 seconds) ..... +260°C
- Y8 Package (10 seconds) ..... +300°C
- MH Package, Vapor Phase (60 seconds) ..... +215°C
- MH Package, Infrared (15 seconds) ..... +220°C

ESD Tolerance 100 pF, 1.5 kΩ, Human Body Model 800V

Operating conditions

Parameter		Min	Nom	Max	Unit
V+	Power Supply Voltage	13	15	17	V
I_{OUT}	Output Load Current			1	mA
C_L	Load Capacitance			200	pF
T_J	Junction Temperature (F-grade)	–55		125	°C
T_J	Junction Temperature (C-grade)	0		70	°C

Electrical characteristics within specified operating conditions [1,5]

Parameter		Test Conditions	Temperature Range						Unit
			Standard			Extended			
			Min	Typ	Max	Min	Typ	Max	
I+	Power Supply Current[9]	–1, –2, –3 grades		1.4	2.0		1.4	2.0	mA
		MHC, NHC, Z3C		1.5	2.4				mA
ΔI_{+V}	I+ Sensitivity, (ΔI+ vs V+) [9]	V+ = 13 to 30 Volts							
		–1, –2, –3 Grades		0.06	0.2		0.06	0.2	mA
		MHC, NHC, Z3C		0.08	0.3				mA
I_{SC}	Short Circuit Current[9]	–1, –2, –3 Grades	11	27	65	11	27	65	mA
		MHC, NHC, Z3C	10	27	65				mA
θ_{JC}	Thermal Resistance, Junction to Case	Y8 Package		75			75		°C/W
θ_{JA}	Thermal Resistance, Junction to Ambient	Y8 Package		150			150		°C/W
		NH Package		160					°C/W
		MH Package		180					°C/W
		Z3 Package		160					°C/W

System performance characteristics within specified operating conditions [1,5]

Parameter	Test Conditions	Temperature Range						Unit
		Standard			Extended			
		Min	Typ	Max	Min	Typ	Max	
V_{OUT} Output Voltage[7]	–1, –2, –3 Grades	9.995	10.000	10.005	9.995	10.000	10.005	V
	MHC, NHC, Z3C	9.990	10.000	10.010				V
ΔVO_T Temperature Coefficient (ΔV_{OUT} / ΔTemp) [4,7,9]	–3 Grade		1.5	3		1.5	3	ppm/°C
	–2 Grade		2.7	5		2.7	5	ppm/°C
	–1 Grade		6	10				ppm/°C
	MHC, NHC, Z3C		5	30				ppm/°C
ΔVO_V Power Supply Sensitivity, Line Regulation, (ΔV_{OUT} / $\Delta V+$) [9]	V+ = 13 to 30 Volts							
	–1, –2, –3 Grades		2.0	8.0		2.0	8.0	ppm/V
	MHC, NHC, Z3C		2.4	12.0				ppm/V
ΔVO_{I+} Load Regulation, (ΔV_{OUT} / ΔI_{OUT+}) [2,6,8,9]	I_{OUT} = 0 to 10mA							
	–1, –2, –3 Grades		3.0	20.0		3.0	20.0	ppm/mA
	MHC, NHC, Z3C		3.0	25.0				ppm/mA
ΔVO_{I-} Load Regulation, (ΔV_{OUT} / ΔI_{OUT-}) [2,6,8]	I_{OUT} = 0 to –10mA		80	160		80	160	ppm/mA
ΔVO_t Long-Term Stability, Non-Cumulative, (ΔV_{OUT} vs time) [7]	1000 Hours, $T_j < T_{MAX}$							
	–1, –2, –3 Grades		6			6		ppm
	MHC, NHC, Z3C		8					ppm
ΔVO_{TRM} TRIM Pin Sensitivity, (ΔV_{OUT} / ΔI_{TRIM})	–1, –2, –3 Grades		1500	2600		1500	2600	ppm/µA
	MHC, NHC, Z3C		1500	2800				ppm/µA
ΔVO_P Thermal Regulation, (ΔV_{OUT} / ΔPower) [3,8]	10ms After Load Applied, Sourcing I_{OUT}							
	–1, –2, –3 Grades		3	±20		3	±20	ppm/100mW
	MHC, NHC, Z3C		4	±25				ppm/100mW
	Sinking I_{OUT}							
	–1, –2, –3 Grades		3			3		ppm/100mW
	MHC, NHC, Z3C		4					ppm/100mW
HYS_T Temperature Hysteresis of V_{OUT}	ΔT = 25°C							
	–1, –2, –3 Grades		3			3		ppm
	MHC, NHC, Z3C		5					ppm
V_N Noise Voltage	10Hz to 1KHz		10	30		10	30	µVrms
	0.1Hz to 10Hz		4			4		µVrms
	10Hz to 10KHz		4			4		µVrms
	C_{filter} = 0.1µF							

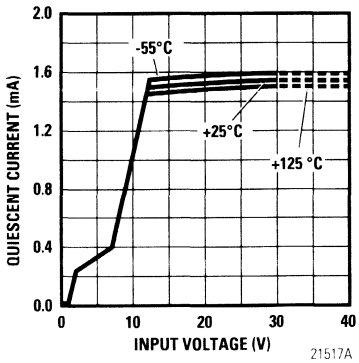
Notes on specification tables

1. Guaranteed specifications apply for T_J = +25°C, V+ = +13 to +17 Volts, I_{OUT} = 0.0 to 1.0mA, C_L <200pF, unless otherwise specified (Note 9).
2. The Class-B output stage of the TDC4169 will exhibit transients at its crossover point (when sinking approximately 1mA). It is advantageous to load the output with a resistor to V+ or GND to avoid the crossover point.
3. The change in output voltage at a time, t, after a 100mW step change of power dissipation.
4. Worst-case change in V_{OUT} measured at specified temperatures divided by the total span of the temperature range. Specified temperatures are not necessarily at the extremes of the temperature range.
5. Electrical characteristics are guaranteed only within *Operating conditions*.
6. Measured at constant temperature using low duty cycle pulse testing. Measurements are made on V_{OUT} pin, 1/8" from package bottom. Does not include effects of heating such as V_{OUT} Temperature Coefficient and Thermal Regulation.
7. Consult factory for availability of THC4169 with guaranteed long-term stability, lower initial V_{OUT} accuracy, or lower Temperature Coefficient.
8. When sinking current, a 0.1µF tantalum capacitor should be connected between V_{OUT} and GND.
9. Specification guaranteed over full temperature range.

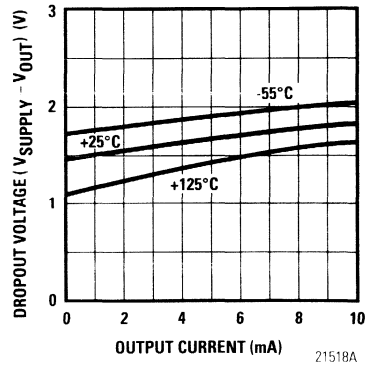
C

Typical Performance Characteristics

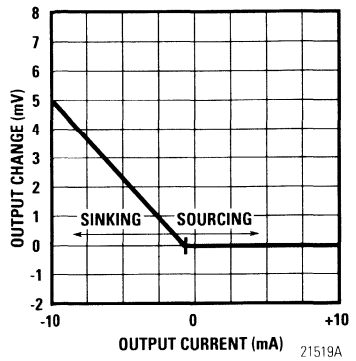
A. Quiescent Current vs Input Voltage and Temperature



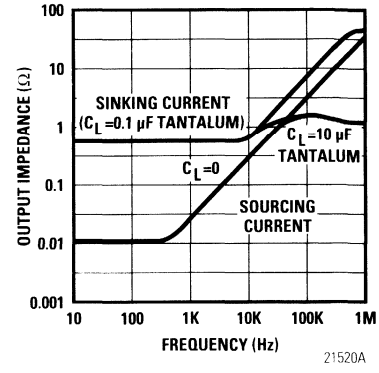
B. Dropout Voltage vs Output Current (Series Mode Sourcing Current)



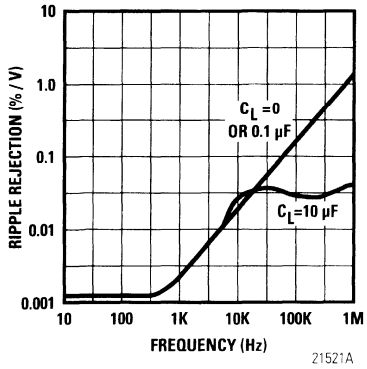
C. Output Change vs Output Current



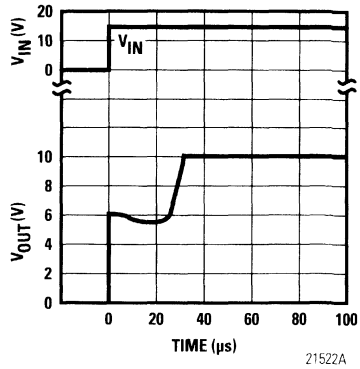
D. Output Impedence vs Frequency



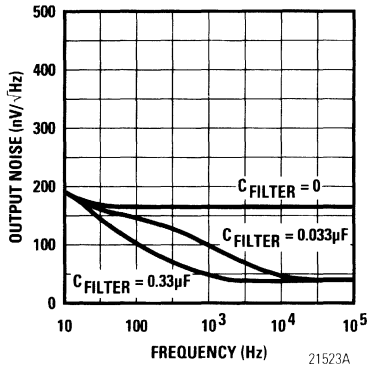
E. Ripple Rejection vs Frequency



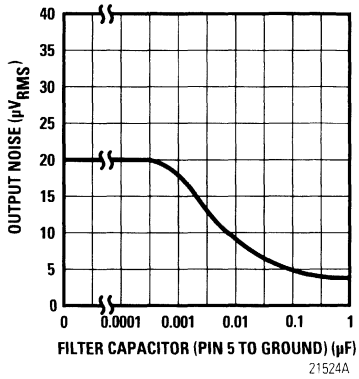
F. Start-up Response



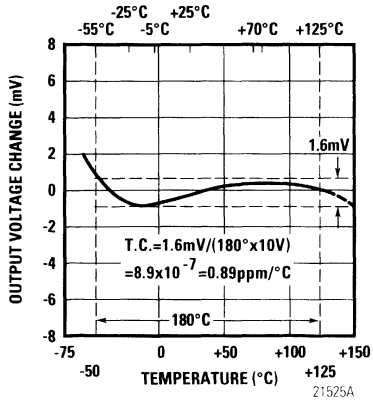
G. Output Noise vs Frequency



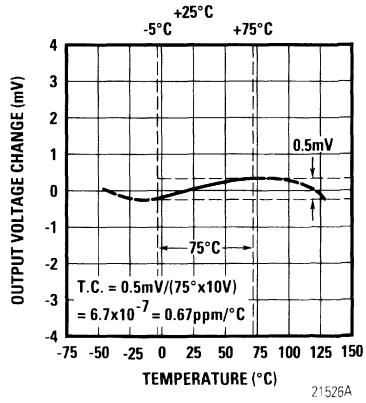
H. Output Noise vs Filter Capacitor



I. Temperature Coefficient



J. Temperature Coefficient



Applications Information

The exceptional stability and low noise of the TDC4169 make the device ideally suited to use as the reference for a high-resolution A/D converters and other precision analog circuits.

Minimizing Noise

The TRIM pin of the TDC4169 can be used to reduce broadband noise by connecting a low-leakage 0.1 to 0.3μF capacitor between TRIM and GND. The capacitor should exhibit low-leakage since current drawn from the TRIM pin alters the output reference voltage. For a temperature range of 0 to 50°C a polyester or Mylar dielectric capacitor is recommended. For higher temperatures, a polypropylene dielectric may be needed. To operate at temperatures up to 125°C a Teflon capacitor is recommended for its low-leakage characteristics. Ceramic capacitors should be avoided since they can convert mechanical stress and vibration into current via their piezo-electric characteristics, which will increase the noise voltage of the output reference voltage.

Do Not Connect

There are several pins labeled "DNC". These are used in the manufacturing pr°Cess to trim the reference voltage and temperature coefficient of the TDC4169. These pins should be left unconnected and protected from leakage currents and noise coupling. They may be removed from the package, if desired. A guard ring can be placed around the DNC and TRIM pins and connected to ground to further shield them from leakage and noise. This will effectively prevent AC transients from degrading the output reference voltage.

Output Loading

The V_{OUT} output can source as well as sink current, however the output impedance is greater when sinking current. When operating in shunt mode (reference is sinking current), a 0.1μF capacitor should be connected from the V_{OUT} to GND. A tantalum capacitor is recommended. Although the output can sink as well as source current, since the output has a class-B output stage there is a crossover transient when I_{OUT} is close to 0. In applications where I_{OUT} is likely to pass through 0 it is recommended that the output be preloaded with a small bias current to avoid this transient.

The TDC4169 is capable of output currents as large as ±10mV, however there is an error induced in the output by the current passing through the parasitic resistance of the package pins. Larger currents also tend to cause the die to heat up, adding to the error in the reference output. For highest accuracy it is suggested that the reference current be kept below 1μA.

The device will not be damaged by a short circuit to ground or to the power supply, but if the device is at an elevated temperature, the additional power dissipation is likely to raise the junction temperature above safe operating limits.

TRIM Pin

The output voltage of the TDC4169 can be adjusted by providing current to or drawing current from the TRIM pin. The nominal output voltage on the TRIM pin is +6.8 Volts. The reference voltage changes approximately 15 mV for each μA of current. Because of this sensitivity it is highly recommended that the TRIM pin be protected from noise and leakage, as these will have an adverse effect upon reference performance. The range over which the output is adjusted should not exceed ±10mV. Trimming over a lager range will result in a degradation of temperature coefficient. The expected degradation is about 1ppm/°C for each 10mV of trim.

Typical Interface Circuits

The typical interface circuits shown below depict the common configurations in which the TDC4169 is used.

Figure 1. Series Regulator with Optional Filtering for Noise Reduction

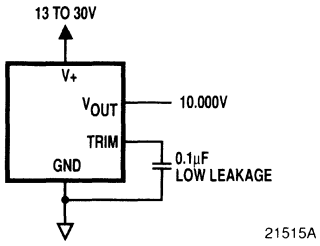
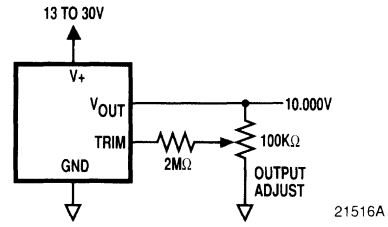


Figure 2. Series Regulator with Optional Trim for V_{OUT} Adjustment



Ordering Information

Product Number	Temperature Coefficient	Temperature Range	Screening	Package	Package Marking
TDC4169Y8F2	5ppm/°C	–55°C to 125°C	Commercial	8 Pin Metal Can	4169Y8F-2
TDC4169Y8F3	3ppm/°C	–55°C to 125°C	Commercial	8 Pin Metal Can	4169Y8F-3
TDC4169Y8C2	5ppm/°C	0°C to 70°C	Commercial	8 Pin Metal Can	4169Y8C-2
TDC4169Y8C3	3ppm/°C	0°C to 70°C	Commercial	8 Pin Metal Can	4169Y8C-3
TDC4169MHC	30ppm/°C	0°C to 70°C	Commercial	8 Pin Plastic SOIC	4169MHC
TDC4169NHC	30ppm/°C	0°C to 70°C	Commercial	8 Pin Plastic DIP	4169NHC
TDC4169NHC1	10ppm/°C	0°C to 70°C	Commercial	8 Pin Plastic DIP	4169NHC-1
TDC4169NHC2	5ppm/°C	0°C to 70°C	Commercial	8 Pin Plastic DIP	4169NHC-2
TDC4169NHC3	3ppm/°C	0°C to 70°C	Commercial	8 Pin Plastic DIP	4169NHC-3
TDC4169Z3C	30ppm/°C	0°C to 70°C	Commercial	3 Pin Plastic	4169Z3C

THC4231

Wide Bandwidth Fast Settling Operational Amplifier

165MHz Closed Loop Bandwidth

The THC4231 is a wide bandwidth fast settling operational amplifier designed specifically for high-speed, low-gain applications. The op amp design is based on current feedback architecture, a topology that eliminates the gain-bandwidth trade-off of voltage feedback designs while permitting outstanding high-speed performance.

The THC4231 op amp is the ideal design alternative to low-precision open-loop buffers and conventional oscillation prone op amps. The THC4231 offers precise gains from ±1.000 to ±5.000 and linearity that is a true .1% – even in demanding 50 Ohm applications. Traditional open-loop buffers typically have a gain of .95 and linearity of only 3%. And open loop buffer settling time is usually specified with an unrealistically large load resistance or neglecting thermal tail effects. The THC4231 current feedback op amp settles to .05% in 15ns with a 100 Ohm load.

Offsets and drifts were not ignored in the THC4231; the input offset voltage is 1mV and input offset voltage drift is only 10μV/°C. The THC4231 is stable and oscillation-free across the entire gain range and since it's internally compensated, the user is saved the trouble of designing external compensation networks and having to tweak them in production. The absence of a gain-bandwidth trade-off in the THC4231 allows performance to be easily predicted.

The THC4231 is constructed using thin-film resistor/bipolar technology. The THC4231X1B is specified over an ambient range of –25°C to 85°C, while the THC4231X1V operates with guaranteed performance over the –55°C to 125°C case operating range, is manufactured in facilities certified to MIL-STD-1772 and is screened to MIL-STD-883 for military applications. Both are packaged in a 12 lead metal can (TO-8/MO-12 style).

Features

- Current Feedback Architecture
- 165MHz Closed-Loop -3dB Bandwidth
- 15ns Settling To 0.05%
- 1mV Input Offset Voltage, 10μV/°C Drift
- 100mA Output Current
- Excellent AC And DC Linearity
- Available Tested To MIL-STD-883

Applications

- Buffer For Flash A/D Converter
- DAC Current-To-Voltage Conversion
- Precision Line Driving
- Low-Power, Low-Gain, High-Speed Applications

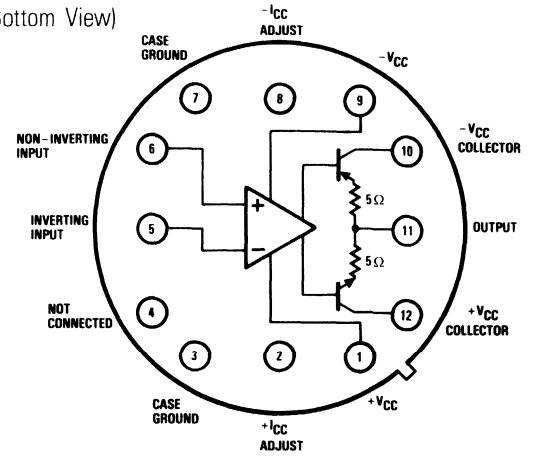
C

Typical Performance

Parameter	Gain Settings 1	2	5	-1	-2	-5	Units
-3dB Bandwidth	180	165	130	165	150	115	MHz
Rise Time (2V)	1.8	2.0	2.5	2.0	2.2	2.9	ns
Slew Rate	2500	3000	3000	3000	3000	3000	V/μs
Settling Time (to .1%)	12	12	12	12	12	15	ns

Pin Assignments and Functional Block Diagram

(Bottom View)



12 Lead Metal Can – X1 Package
(TO-8/MO-12 Style)

TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

40G05913 Rev. B – 11/90
Printed in the U.S.A.

Functional Description

General Information

The THC4231 op amp is based on current feedback instead of the traditional voltage feedback topology. The use of the THC4231 is basically the same as that of the conventional op amp, including active filters and differential amplifiers. (Refer to *Current Feedback vs. Voltage Feedback: A Comparison* for theory of operation.) However, to prevent oscillations, active circuit elements should not be used inside the feedback loop.

The THC4231 is designed specifically for low gain applications. The best performance is obtained when the circuit is used at gains between ± 1 and ± 5. Unlike conventional voltage feedback op amps, the current feedback THC4231 bandwidth is relatively unaffected by the gain setting. Optimum overall performance is achieved and all specifications are guaranteed with a 250 Ohm feedback resistor.

Supply Voltage

The THC4231 is designed to operate from ± 15V supplies although it can operate with supplies reduced as low as ± 5V. See *Current Adjust* for operation with reduced supply voltages. Low and high frequency decoupling capacitors (3.9μF and 0.1μF) should be connected in parallel from the $\pm V_{CC}$ supply pins to the analog ground plane. The 0.1μF capacitors should be less than 0.15" from pins 1 and 9 while the 3.9μF capacitors are within 1" of these pins.

Collector Supply

The $\pm V_{CC}$ collector pins are connected to the $\pm V_{CC}$ supplies via 33 Ohm resistors. High frequency decoupling capacitors of .01μF should be connected from $\pm V_{CC}$ collector supply pins to the analog ground. This resistor and capacitor combination provide optimum settling performance with minimum distortion.

Current Adjust

To regain the full bandwidth lost when operating with supplies below ± 10V, it is necessary to increase the V_{CC} supply currents by shorting the $\pm I_{CC}$ adjust (pins 2 and 8) to the respective $\pm V_{CC}$ supply voltage (pins 1 and 9). The plot of bandwidth vs. V_{CC} shows the effect of shorting I_{CC} adjust pins to V_{CC} supply pins. Care should be taken to not exceed the maximum junction temperature. For this reason, this technique must not be used with supplies exceeding ± 10V. For intermediate values of V_{CC}, external resistors between pins 1 and 2 and pins 8 and 9 can be used. When operating with ± 15V supplies, pins 2 and 8 must remain open-circuit.

Case Ground

Case ground pins should be connected to the system analog ground.

Inverting and Non-Inverting Input

To prevent output peaking, the ground plane should be removed from the pc board in the vicinity of the inverting and non-inverting input pins.

Output

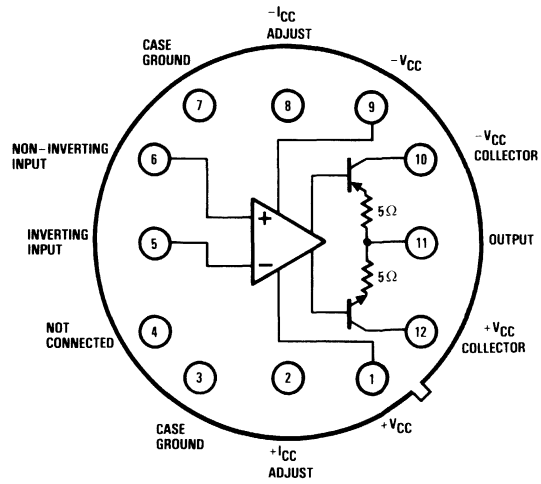
The analog output is capable of swinging $V_{CC}-3$V to $-V_{CC}+3$V at up to 100mA output current. To prevent output peaking, the ground plane should be removed from the vicinity of the output pin.

No Connect

The No Connect pin is not connected internally to any portion of the circuit.

Pin Assignments and Functional Block Diagram

(Bottom View)



12 Lead Metal Can (TO-8/MO-12 Style) – X1 Package

Package Interconnections

Signal Type	Signal Name	Function	Value	12 Lead Metal Can Package Leads
Power	$+V_{CC}$	Positive Supply Voltage	+15V	1
	$+V_{CC}$ Collector	Positive Collector Voltage	+15V	12
	$-V_{CC}$	Negative Supply Voltage	−15V	9
	$-V_{CC}$ Collector	Negative Collector Voltage	−15V	10
	GND	Case Ground	0.0V	3, 7
Current Adjust	$+I_{CC}$ Adjust	Positive Low-Voltage Adjust	See Text	2
	$-I_{CC}$ Adjust	Negative Low-Voltage Adjust	See Text	8
Input	IN+	Non-Inverting	±12V	6
	IN−	Inverting	±12V	5
Output	V_{OUT}	Analog Output	±12V	11
No Connect	NC	None	–	4

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Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

$\pm V_{CC}$ ..... ±20V

Input

Inverting and Non-inverting input ..... See Diagram

Voltage ..... See Diagram

Output Current ..... ±100mA

Temperature

Operating, case ..... −65 to +130°C

junction ..... +175°C

Lead, soldering (10 seconds) ..... +300°C

Storage ..... −65 to +150°C

Reliability

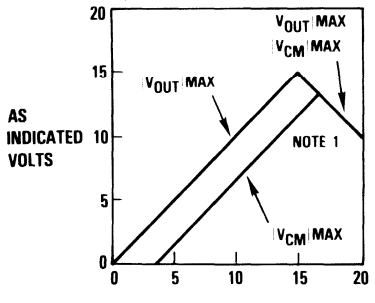
Mean Time Between Failure [2] ..... 2.9×10^6 Hours

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. V-grade, GF @ $T_C = 70°C$, per MIL-HDBK-217D.

Absolute Maximum Rating

Input and Common Mode Voltage Limits



Note: 1. These ratings protect against damage to the input stage caused by saturation of either the input or output stages at lower supply voltages, and against exceeding transistor collector-emitter breakdown ratings at high supply voltages. V_{OUT} (Max) is calculated by assuming no output saturation. Saturation is allowed to occur up to this calculated level of $V_{OUT} - V_{CM}$ is defined as the voltage at the non-inverting input, pin 6.

Operating conditions

Parameter		Temperature Range						Units
		Industrial			Extended			
		Min	Nom	Max	Min	Nom	Max	
$\pm V_{CC}$	Supply Voltage	±5	±15		±5	±15		V
GND	Case Ground		0.0			0.0		V
IN+, IN−	Inputs		$\|V_{CC}\|-3$			$\|V_{CC}\|-3$		V
V_{OUT}	Output		$\pm V_{CC}$			$\pm V_{CC}$		V
T_A	Ambient Temperature	−25		85				°C
T_C	Case Temperature				−55		125	°C

DC Electrical characteristics within specified operating conditions

(R_L = 100 Ohms, R_f = 250 Ohms, V_{CC} = ±15V, A_V = +2)

Parameter		Test Conditions	Temperature Range						Units
			Industrial			Extended			
			Min	Typ	Max	Min	Typ	Max	
I_{CC}	Supply Current	V_{CC} = ±15V, No Load		18	22		18	22	mA
R_{IN}	Input Resistance	Non-Inverting	100	400		100	400		kOhms
C_{IN}	Input Capacitance	Non-Inverting		1.3	2.5		1.3	2.5	pF
V_{IO}	Input Offset Voltage			1	4.5		1	4.5	mV
T_{CIO}	Temp Coefficient, Input Offset Voltage			10	25		10	25	µV/°C
I_{IB}	Input Bias Current	Non-Inverting		5	31		5	31	µA
		Inverting		10	35		10	35	µA
T_{CIB}	Temp Coefficient, Input Bias Current	Non-Inverting		50	125		50	125	nA/°C
		Inverting		125	200		125	200	nA/°C
V_{OUT}	Output Voltage Range	No Load	±11	±12		±11	±12		V

AC Electrical characteristics within specified operating conditions

(R_L = 100 Ohms, R_f = 250 Ohms, V_{CC} = ±15V, A_V = +2)

Parameter		Test Conditions	Temperature Range						Units
			Industrial			Extended			
			Min	Typ	Max	Min	Typ	Max	
SSBW	Small Signal Bandwidth [1]	V_{OUT} = 2Vp-p	120	165		120	165		MHz
FPBW	Full Power Bandwidth [1]	V_{OUT} = 10Vp-p	60	95		60	95		MHz
E_{GPL}	Gain Flatness Peaking, LOW Frequency	V_{OUT} = 2Vp-p, 0.1≤f≤50MHz		0.1	0.6		0.1	0.6	dB
E_{GPH}	Gain Flatness Peaking, HIGH Frequency	V_{OUT} = 2Vp-p, f>50MHz		0.1	1.5		0.1	1.5	dB
E_{GR}	Gain Flatness Rolloff	V_{OUT} = 2Vp-p, Note 2		0.4	1.0		0.4	1.0	dB
T_{GD}	Group Delay	f≤100MHz		3.5 ± .5			3.5 ± .5		ns
E_P	Linear Phase Deviation	f≤100MHz		0.5	2.0		0.5	2.0	Degrees
RI_{NI}	Reverse Isolation, Non-Inverting	f≤100MHz	43	53		43	53		dB
RI_{IN}	Reverse Isolation, Inverting	f≤100MHz	26	36		26	36		dB
R_{OUT}	Output Resistance	f_{OUT} = 100MHz		5			5		Ohms
L_{OUT}	Output Inductance	f_{OUT} = 100MHz		37			37		nH
t_{RS}	Rise Time, Small Signal	2V Output Step		2	2.7		2	2.7	ns
t_{RL}	Rise Time, Large Signal	10V Output Step		5	7.0		5	7.0	ns
t_{FS}	Fall Time, Small Signal	2V Output Step		2	2.7		2	2.7	ns
t_{FL}	Fall Time, Large Signal	10V Output Step		5	7.0		5	7.0	ns
t_S	Settling Time	5V Output Step to .05%		15			15		ns
		2.5V Output Step to .1%		12	22		12	22	ns
E_{OS}	Overshoot	5V Output Step		5	15		5	15	%
SR	Slew Rate	Input Overdriven	1.8	3		1.8	3		V/ns
t_{OR}	Overload Recovery	Note 3		120			120		ns
HD2	Second Harmonic Distortion	0 dBm, 20MHz	−47	−55		−47	−55		dBc
HD3	Third Harmonic Distortion	0 dBm, 20MHz	−47	−59		−47	−59		dBc
	Equivalent Input Noise								
	Noise Floor	>5MHz	−150	−153		−150	−153		dBm(1Hz)
	Integrated	5MHz to 200MHz		70	100		70	100	μVrms
PSRR	Power Supply Rejection Ratio		45	50		45	50		dB
CMRR	Common Mode Rejection Ratio		40	46		40	46		dB

Notes:
1. −3dB bandwidth.
2. f = 100MHz.
3. < 50ns pulse, 200% overdrive, to < 1% error.

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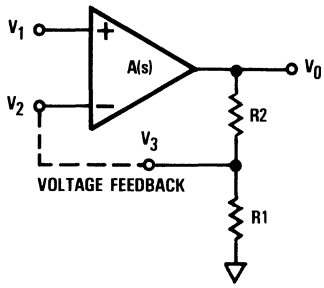
Current Feedback vs. Voltage Feedback: A Comparison

To fully understand the advantages of the THC4231 current feedback op amp, it is helpful to compare its theory of operation to that of the traditional voltage feedback op amp.

Voltage Feedback Op Amp

Traditional voltage feedback op amps have a differential, high input impedance stage followed by several gain stages. The open loop output of this op amp is:

$$V_O = A(s)[V_1 - V_2]$$

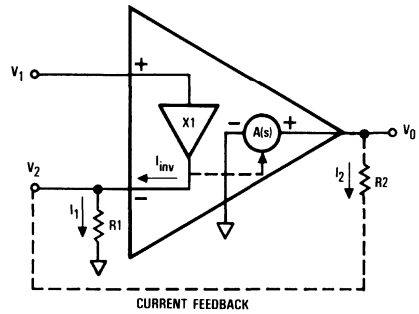


With the feedback connection made, a feedback voltage is applied to the inverting input and the closed loop gain is:

$$\frac{V_O}{V_1} = \frac{\frac{R_1 + R_2}{R_1}}{1 + \frac{\frac{R_1 + R_2}{R_1}}{A(s)}}$$

Current Feedback Op Amp

The current feedback op amp has a unity gain voltage buffer amplifier across the inverting and non-inverting inputs. This buffer forces the voltage at V_2 to be identical to the voltage applied at V_1 independent of any external feedback. Because the inverting input is actually the output of the buffer, this node has a very low input impedance, which is further reduced when the feedback resistor (R2) is installed. With respect to V_1, the inverting input is truly a virtual ground and current easily flows into or out of this node.



The transimpedance amplifier is the gain stage inside the THC4231. It senses the current flowing into or out of the inverting input and transforms this current into an output voltage. The transfer function of the transimpedance amplifier is A(s) and the units are Ohms.

The open loop gain of thie amplifier is:

$$V_O = I_{inv}\, A(s)$$

With the feedback resistor installed, the closed loop gain equation is:

$$\frac{V_O}{V_1} = \frac{\frac{R_1 + R_2}{R_1 R_2}}{\frac{1}{R_2} + \frac{1}{A(s)}} = \frac{1 + \frac{R_2}{R_1}}{1 + \frac{R_2}{A(s)}}$$

Voltage Feedback Op Amp (cont.)

Substituting $G = (R_1 + R_2)/R_1$

$$\frac{V_O}{V_1} = \frac{G}{1 + \frac{G}{A(s)}}$$

Substituting $A(s) = \frac{N(s)}{D(s)}$ yields:

$$\boxed{\frac{V_O}{V_1} = G \frac{N(s)}{N(s) + (G)\,D(s)}}$$

Now the two topologies can be compared. In the voltage feedback op amp transfer function, the circuit gain and pole locations are both dependent upon G = (R1 + R2)/R1. Therefore, changing the gain of the circuit causes the pole locations to move. In practice, for a high gain setting, the poles will be at a lower frequency than for a low gain setting. This is shown in the illustration below. Frequency response that depends upon the circuit gain is the biggest drawback of voltage feedback op amps.

Current Feedback Op Amp (cont.)

Substituting $G = 1 + \frac{R_2}{R_1}$

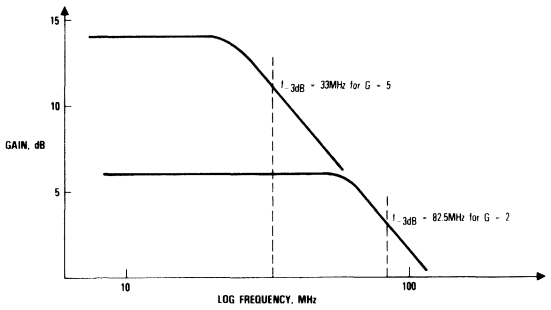
$$\frac{V_O}{V_1} = \frac{G}{1 + \frac{R_2}{A(s)}}$$

Substituting $A(s) = \frac{N(s)}{D(s)}$ yields:

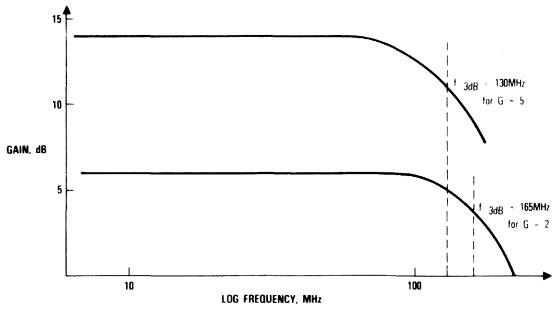
$$\boxed{\frac{V_O}{V_1} = G \frac{N(s)}{N(s) + R_2 D(s)}}$$

By comparison, the current feedback op amp also has circuit gain dependent upon G = (R1 + R2)/R1, but this time the pole locations are dependent only on R_2. This is the advantage of the current feedback topology over voltage feedback topology: frequency response is independent of the circuit gain. In practice, it is easy to keep R2 constant for various gain settings and therefore maintain the frequency response of the op amp. In fact, the design of the THC4231 has been optimized for R2 = 250 Ohms and all specifications are guaranteed with this value of feedback resistor.

Voltage Feedback Op Amp



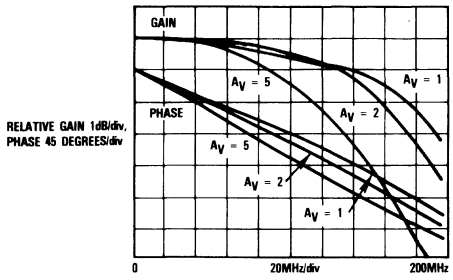
Current Feedback Op Amp



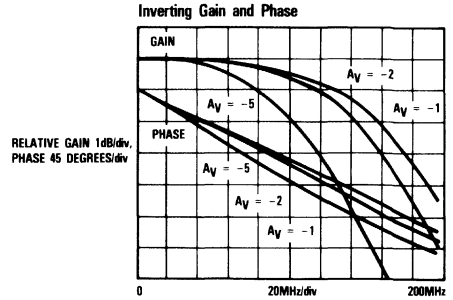
Typical Performance Curves

($T_A = 25°C$, $A_V = +2$, $V_{CC} = \pm 15V$, $R_L = 100$ Ohms, $R_f = 250$ Ohms)

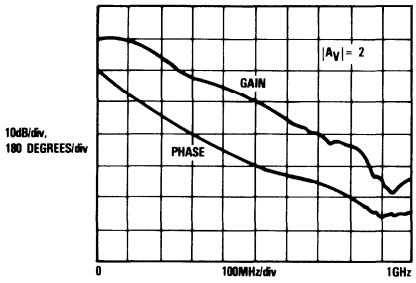
Non-Inverting Gain and Phase



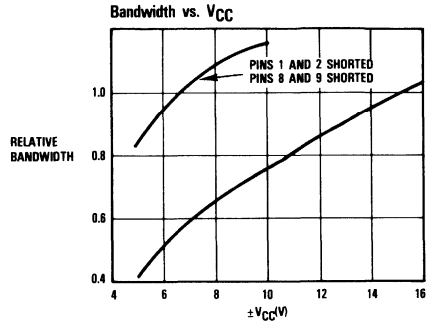
Inverting Gain and Phase



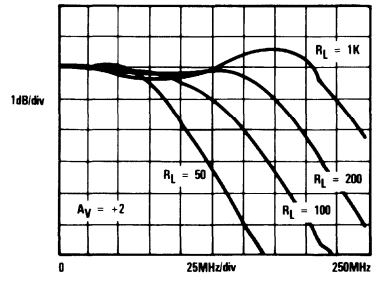
Broadband Gain and Phase



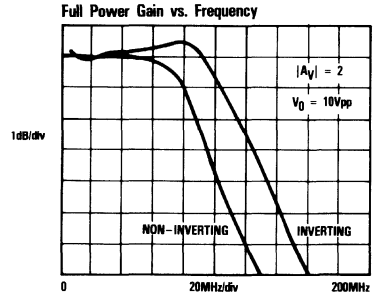
Bandwidth vs. V_{CC}



Gain vs. Frequency for Various R_Ls

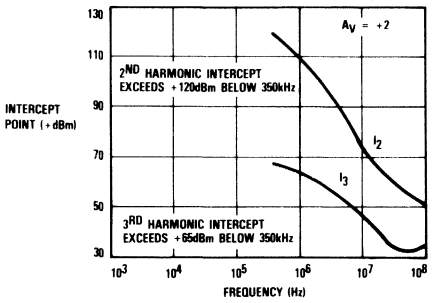


Full Power Gain vs. Frequency

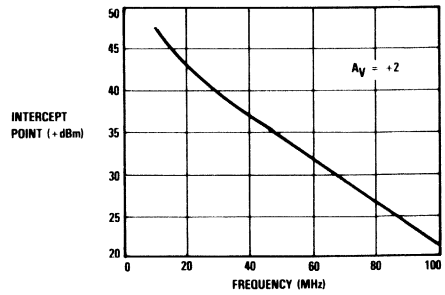


Typical Performance Curves (cont.)

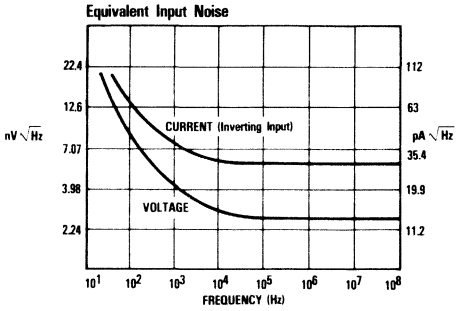
2nd and 3rd Harmonic Distortion Intercept



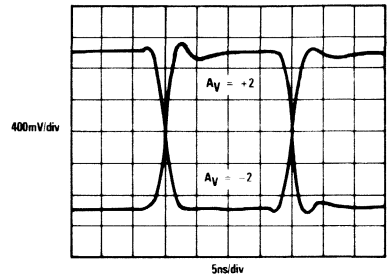
2-Tone 3rd Order Intermodulation Intercept



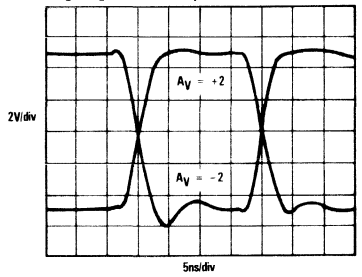
Equivalent Input Noise



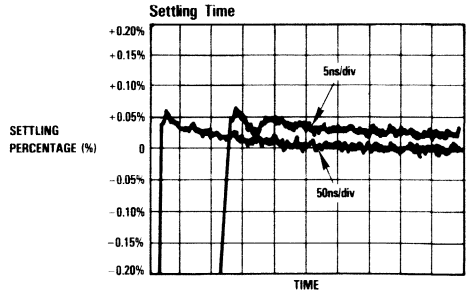
Small Signal Pulse Response



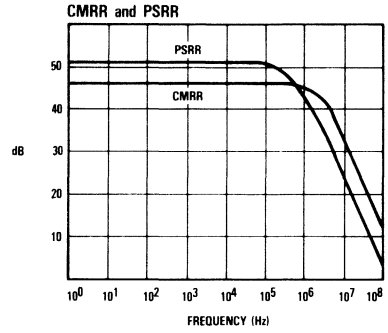
Large Signal Pulse Response



Settling Time



CMRR and PSRR



Layout Considerations

To assure optimum performance from the THC4231, the surrounding circuitry should follow good high-frequency layout practices which minimize unwanted coupling of signals between nodes. When breadboarding, point-to-point wiring should be used, keeping lead lengths less than 0.25". Solid ground plane is recommended. Sockets with small, short pin receptacles or individual high-frequency pins may be used with only slight performance degradation. For optimum performance, the THC4231 leads should be soldered, not socketed.

For printed circuit board layout, all traces should be kept as short and direct as possible. The body of the gain-setting resistor (R_G) should be kept as close to the inverting input (pin 5) as possible to reduce capacitance at that point. Ground plane should be removed from the pc board in the vicinity of the inverting, non-inverting and output pins. To prevent signal distortion caused by reflections from impedance mismatches, terminated microstrip or coaxial cable should be used whenever the signal must traverse more than one inch.

A ground return path for current from the load resistor to the power supply bypass capacitors must be provided. High frequency (surface mount if possible) ceramic capacitors of 0.01 to 0.1μF (with short leads) should be less than .15" from pins 1 and 9. Larger 3.9μF tantalum capacitors should be placed within 1" of these pins. $\pm V_{CC}$ collector supply connections (pins 10 and 12) can be made directly from pins 9 and 1, but better supply rejection and settling time performance are obtained if they are seperately bypassed with 0.01μF capacitors and 33 Ohm resistors as shown in the *Typical Application Circuits*.

Since the pc board forms such an integral portion of the circuit, it is recommended that a prototype board containing just the THC4231 circuitry is built and evaluated before commiting to a final pc board layout.

Typical Application Circuits

Figure 1. Non-Inverting Gain Circuit

$$A_V = 1 + \frac{R_F}{R_G}$$

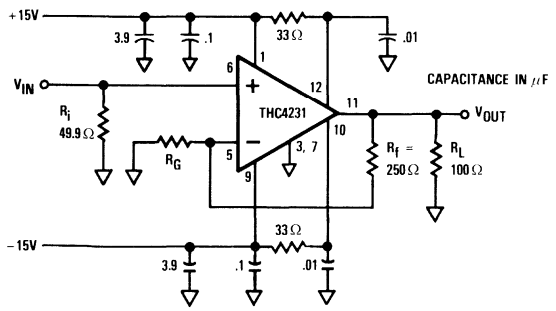
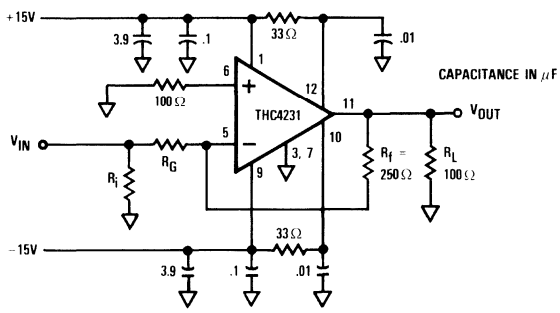


Figure 2. Inverting Gain Circuit

$$A_V = 1 - \frac{R_F}{R_G}$$



Distortion And Noise

The graphs of intercept point, I_2 and I_3, versus frequency make it easy to predict the distortion at any frequency given the output voltage of the THC4231. First, convert the output voltage (V_O) to V_{RMS} = ($V_{p\text{-}p}/2\sqrt{2}$) and then to P = [(10log$_{10}$ ($20V_{RMS}^2$)] to get the power output in dBm. At the frequency of interest, its 2nd harmonic will be S_2 = (I_2 – P)dB below the level of P. Its third harmonic will be S_3 = 2(I_3 – P)dB below P, as will the two-tone third order intermodulation products. These approximations are useful for P < –1dB compression levels.

Approximate noise figure can be determined for the THC4231 using the equivalent input noise graph. The following equation can be used to determine noise figure (F) in dB.

$$F = 10\log\left[1 + \frac{i_n^2 R_F^2}{\frac{V_n^2 + A_V^2}{4kTR_S\,\Delta f}}\right]$$

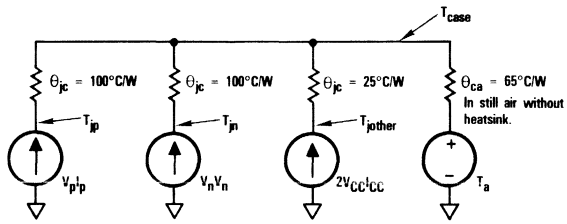
Where V_n is the rms noise voltage and I_n is the rms noise current. Beyond the breakpoint of the curves (i.e., where they are flat), the broadband noise figure equals the spot noise figure, so Δf should equal one (1) and V_n and I_n should be read directly from the graph. Below the breakpoint, the noise must be integrated and Δf set to the appropriate bandwidth.

C

Thermal Considerations

At high ambient temperatures or large internal power dissipations, heat sinking is required to maintain acceptable junction temperatures. The thermal model below can be used to predict junction temperatures. Many styles of heat sinks are available for TO-8 packages such as Wakefield 215 and Thermalloy 2240. Radial fin heat sinks cover the circuit board and may interfere with external components unless surface mounted resistors and capacitors are used. A 0.1" spacer can be installed under the TO-8 package so that conventional components can be used with sufficient clearance.

Thermal Model



$P_{circuit}$ = I_{CC} [(+V_{CC}) – (–V_{CC})] where I_{CC} = 16mA at ±15V

P_{xxx} = [(+V_{CC}) – V_{OUT} – (I_{col})(R_{col} + 4)](I_{col})(% duty cycle)

For positive V_O and V_{CC}, this is the power in the npn output stage.

For negative V_O and V_{CC}, this is the power in the pnp output stage.

I_{col} = V_{OUT} / R_{load} or 4mA whichever is greater. (Include feedback R in R_{load}.)

R_{col} is a resistor (33 Ohms recommended) between the xxx collector and ±V_{CC}.

$T_{j(pnp)}$ = P_{pnp} (100 + θ_{ca}) + (P_{cir} + P_{npn})θ_{ca} + T_a.
Similar for $T_{j(npn)}$.

$T_{j(cir)}$ = P_{cir} (48 + θ_{ca}) + (P_{pnp} + P_{npn}) θ_{ca} + T_a.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
THC4231X1B	IND–T_A = –25°C to 85°C	Industrial	12 Lead Metal Can (TO-8/MO-12)	THC4231X1B
THC4231X1V	EXT–T_C = –55°C to 125°C	MIL-STD-883	12 Lead Metal Can (TO-8/MO-12)	THC4231X1V

TDC4611

Adjustable Voltage Reference with Operational Amplifier

The TDC4611 comprises a precision adjustable voltage reference and a single general purpose operational amplifier on the same monolithic integrated circuit. This combination of circuit functions is ideally suited for complete reference circuits for A/D and D/A converters.

The voltage reference of the TDC4611 uses a band-gap reference source and built-in amplifier to enable the output voltage to be set with one pair of external resistors.

A separate operational amplifier is included on the TDC4611 for use with the voltage reference circuit in generating complete voltage reference circuits for A/D and D/A converters. The input common-mode range of the operational amplifier extends to the negative power supply voltage for additional application flexibility.

The TDC4611 is available in both commercial (0°C to +70°C) and extended (–55°C to +125°C) temperature ranges and in 8-pin CERDIP and plastic DIP as well as 14-pin plastic SOIC packages.

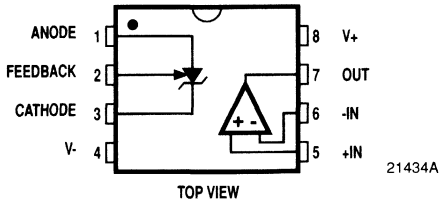
Features

- Low Drift, Adjustable Voltage Reference
- Low Offset Voltage Operational Amplifier
- Wide Common-Mode Input And Power Supply Voltage Range
- Wide Reference Voltage Range and Amplifier Output Voltage Swing
- Low Power Dissipation

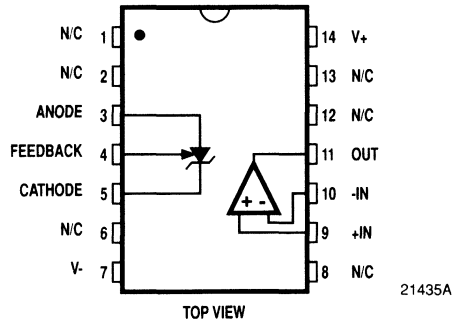
Applications

- Complete Voltage References For A/D And D/A Converters
- AC and DC Signal-Conditioning
- Active Filters With Offset Control
- Miniaturized, Reduced Chip Count Circuitry

Interface Diagrams



8 Pin CERDIP – B4 Package
8 Pin Plastic DIP – NH Package



14 Pin Plastic SOIC – ME Package

TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

40G06686 Rev. A – 7/90
Printed in the U.S.A.

Figure 1. Operational Amplifier Simplified Schematic Diagram

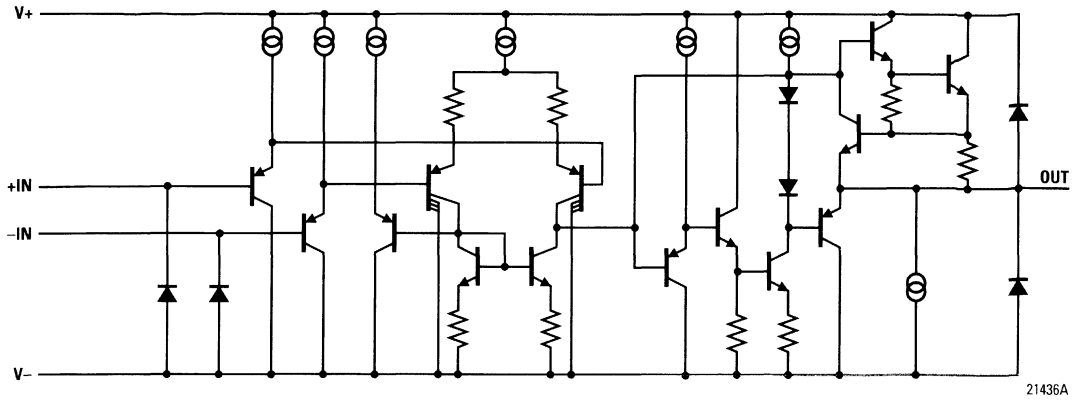


Figure 2. Reference Simplified Schematic Diagram

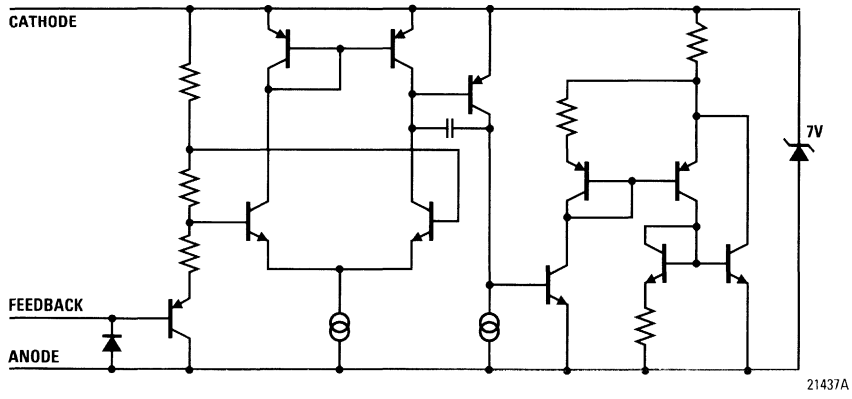
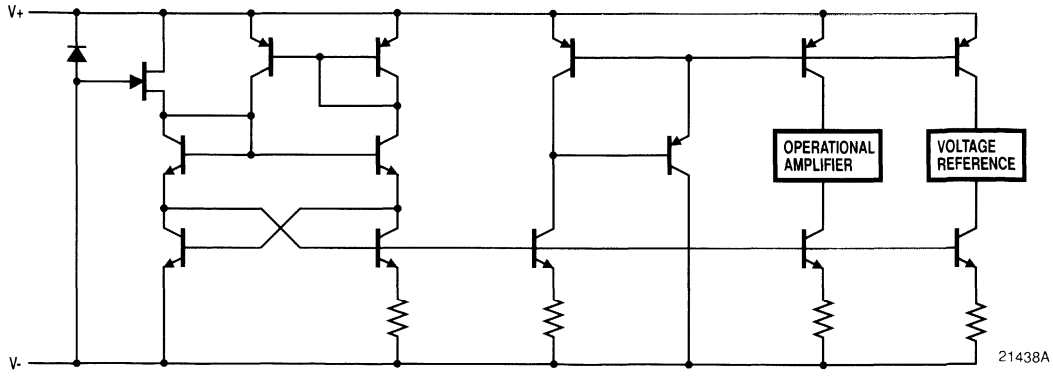


Figure 3. Bias Circuit Simplified Schematic Diagram



Functional Description

The TDC4611 is made up of an operational amplifier and an adjustable voltage reference on the same monolithic integrated circuit. The operational amplifier is a general purpose voltage feedback amplifier designed for DC and low-frequency applications. The voltage reference is a three-terminal band-gap voltage source with its own built-in amplifier.

Power

The TDC4611 has two power supply input terminals, V+ and V–, and will operate with a wide range of power supply voltages. The TDC4611 will operate with either V+ or V– grounded. The substrate of the TDC4611 is biased at the most negative potential, V–.

Voltage Reference

The TDC4611 voltage reference employs band-gap shunt-regulator topology that can be modeled as a Zener diode. When current flow in this diode is in the forward direction (from ANODE to CATHODE), it exhibits a normal diode exponential transfer characteristic. Current flowing in the reverse direction generates a constant voltage (CATHODE positive with respect to ANODE). The magnitude of this voltage is set by a pair of external resistors connected between ANODE and CATHODE with a common connection to FEEDBACK. When FEEDBACK is connected directly to ANODE, the voltage between CATHODE and ANODE is its minimum value of approximately 1.2 Volts.

Operational Amplifiers

The operational amplifier of the TDC4611 is a general purpose voltage-feedback amplifiers with PNP input transistors. The PNP input stage allows a common-mode input range that includes the negative power supply, V–. The inputs, –IN and +IN, are diode-clamped to V– but not clamped to V+ or to each other, allowing large differential input voltages.

The amplifier is unity-gain stable with low input bias and power supply currents. The amplifier and voltage reference share the same integrated circuit and their only common point is the substrate which is biased at V–. If the amplifier is not used, it should be connected so that both inputs and the output are within their recommended operating conditions (i.e., –IN connected to OUT, and +IN connected to FEEDBACK).

The output structure of the TDC4611 has a deadband voltage of approximately one diode V_{be}. The crossover distortion generated by this deadband can be eliminated by the use of a pull-up or pull-down resistor between the output and V+ or V–. The resistor increases output current and reduces crossover distortion. The value of this resistor should be determined so that the current through it is 1mA, nominally. Crossover distortion will be minimized and the amplifier will then also be frequency-stable while driving capacitive loads as large as 200pF.

Package Interconnections

Signal Type	Signal Name	Function	Value	Pin (SOIC)	Pin (DIP)
Power	V+	Positive Supply Voltage	+5V Nominal	14	8
	V–	Negative Supply Voltage	0V Nominal	7	4
Operational Amplifier	+IN	Non-Inverting Operational Amplifier Input	V– to V+ – 1.4V	9	5
	–IN	Inverting Operational Amplifier Input	V– to V+ – 1.4V	10	6
	OUT	Operational Amplifier Output	V– +1V to V+ –1.9V	11	7
Reference	Anode	Reference Anode	0V	3	1
	Cathode	Reference Cathode	1.2V to 6.3V	5	3
	Feedback	Reference Control	VCATHODE–1.2V	4	2

Absolute maximum ratings (beyond which the device may be damaged)

Supply Voltage (V+ measured to V–)	–0.3 to 36V
Applied Voltage any pin except CATHODE, measured to V–[1]	–0.3 to 36V
Applied Current, externally forced (any pin)	±20mA
Differential Input Voltage (+IN to –IN)	±36V
Output Short Circuit duration[2]	Indefinite
ESD Tolerance 120pF, 1.5KΩ[3]	±1kV

Notes:
1. The failure is caused not by exessive voltage but rather by excessive current flow. If any pin has a potential less than one diode drop below V– then this allows a parasitic NPN transistor to turn on and conduct current to V–. No damage to the device will occur if this current is limited to the absolute maximum ratings, however the device operation while this parasitic transistor is conducting is undefined and unpredictable.
2. Simultaneous short circuit of Reference and Operational Amplifier with higher power supply voltages may cause the junction temperature to rise above the maximum and thus should not be continuous.
3. Human Body Model

Operating conditions

Parameter	Min	Nom	Max	Unit
V+ Measured to V–	3	5	32	V
Common Mode Input Range (Operational Amplifier)	V–+1		V+–1.9	V
Reference Voltage	1.2		6.3	V
Ambient Temperature	0		70	°C

Electrical characteristics (Operational Amplifier)[1]

Parameter		Test Conditions	Temperature Range: Standard Min	Temperature Range: Standard Max	Temperature Range: Extended Min	Temperature Range: Extended Max	Unit
V_{OS}	Offset Voltage	$4V \le V+ \le 32V$		±7		±5	mV
V_{OS}	Offset Voltage	$V+ = 30V, 0V \le V_{CM} \le 28.6V$		±7		±5	mV
$V_{OS}TC$	Offset Temperature Coefficient			±30		±25	µV/°C
I_B	Input Bias Current	I_{B+IN} and I_{B-IN}		±40		±25	nA
I_{OS}	Input Offset Current	$I_{OS} = I_{B+IN} - I_{B-IN}$		±5		±4	nA
$I_{OS}TC$	I_{OS} Temperature Coefficient	Average value between 25°C and temperature extremes		±4		±4	pA/°C
R_{IN}	(Differential)	$T_A = 25°C$	1800		1800		MΩ
R_{IN}	(Common-Mode)	$T_A = 25°C$	3800		3800		MΩ
C_{IN}		Capacitance to ground, Non-Inverting input of follower, $T_A = 25°C$		6		6	pF
A_{VOL}	Open Loop Voltage Gain	$R_L = 10K\Omega$ to GND, V+ = 30V, $5V \le V_{OUT} \le 25V$, Open Loop $A_{VOL} = \Delta V_{OUT}/\Delta V_{INDIFF}$	92		92		dB
V_{OH}	Voltage Swing HIGH	$R_L = 10K\Omega$ to GND, V+ = 32V	V+ −1.9		V+ −1.8		V
V_{OL}	Voltage Swing LOW	$R_L = 10K\Omega$ to V+, V+ = 32V	V− +1.0		V− +1.0		V
I_{OUT+}	Current Sink	$V_{OUT} = 1.6V$, $V_{+IN} = 0V$, $V_{-IN} = 0.3V$	11		8		mA
I_{OUT-}	Current Source	$V_{OUT} = V+ - 2.5V$, $V_{+IN} = 0V$ $V_{-IN} = -0.3V$		−13		−13	mA
I_{SC}	Short Circuit Current	$V_{OUT} = 0V$, $V_{+IN} = 3V$ $V_{-IN} = 2V$	−50		−46		mA

Note: 1. Unless otherwise specified, these specifications apply for V−=0V, V+=5V, $V_{CM}=V+/2$, $V_{OUT}=V+/2$.

Electrical characteristics (Reference)[1]

Parameter		Test Conditions	Temperature				Unit
			Standard		Extended		
			Min	Max	Min	Max	
V_{REF}	Reference Voltage		1.21919	1.2689	1.2390	1.2490	V
$V_{REF}TC$	Temperature Coefficient			20		150	PPM/°C
$V_{REF}LT$	Long Term Stability (Typical)	T_j = 40°C		400		400	PPM/ 1000 HR
$V_{REF}LT$	Long Term Stability	T_j = 150°C		1000		1000	PPM/ 1000 HR
$V_{REF}HS$	Hysteresis[2]			±3.2		±3.2	µV/°C
ΔV/ΔI	V_{REF} Change with Current	I_{REF} 16µA to 100µA I_{REF} 100µA to 10mA		1.1 5.5		1.0 5.0	mV mV
PSS	V_{REF} Change with V+	V_{REF} vs V+ Change for V+ from 5 to V+MAX		86		88	dB
$V_{REF}AS$	V_{REF} Change with Anode Voltage	V+ = V+MAX, V_{anode} from GND to V+ – 1V		3.0		5.0	mV
I_{FS}	Feedback Bias Current	$V_{anode} \leq V_{FS} \leq 5.06V$		–55		–40	nA
$V_{REF}N$	Noise	10Hz – 10KHz, V_{FS} = 0 Typical Specification		30		30	µVRMS

Notes: 1. Unless otherwise specified, these specifications apply for V– = 0V, V+ = 5V, V_{CM} = V+/2, V_{OUT} = V+/2.

2. Hysteresis is $\Delta V_{RO}/\Delta T_J$ where ΔV_{RO} is the change in V_{RO} caused by a change in T_J after the reference has been "dehysterized" by spiraling the junction temperature in towards 25°C.

System performance characteristics (Operational Amplifier)

Parameter		Test Conditions	Temperature Range					Unit
			Standard			Extended		
			Min	Typ	Max	Min	Max	
GBW	Gain-Bandwidth Product	Closed loop, Gain = –1000, C_L = 30pF, Bandwidth = –3dB Frequency.		.52				MHz
SR	Slew Rate	V+ = 30V[1]	±.45	±.65		±.45		V/µs
N_V	Voltage Noise	100Hz, Input Referred		74				nV/√Hz
N_C	Current Noise	100Hz, Bias Current Noise		58				fA/√Hz
CMRR	Common Mode Rejection Ratio	V+ = 30V, 0V≤V_{CM}≤(V+–1.4V), CMRR = 20log{ΔV+/≤V_{OS}}	75	90		80		dB
PSRR	Power Supply Rejection Ratio	4V≤V+≤30V, V_{CM} = 1/2V+, PSRR = 20log{ΔV+/≤V_{OS}}	70	100		80		dB

Note: 1. Slew rate is measured with the Operational Amplifier in voltage follower mode. For rising slew rate, the input voltage is driven from 5V to 25Vand the output voltage transition is sampled at 10V and 20V. For falling slew rate, the input is driven from 25V to 5V, and the output is sampled at 20V and 10V.

Applications Information

Voltage Reference

The CATHODE voltage to the TDC4611 may be set anywhere with the range of –0.7 to +6.3 Volts with respect to ANODE. Poor voltage regulation will result when the CATHODE voltage is set to greater than +6.3 Volts. The *Reference Equivalent Circuit* shows how external resistors, R1 and R2, determine the gain of the built-in amplifier and, therefore, the total voltage (V_{REF}) between ANODE and CATHODE. The 7 Volt Zener diode limits the usable ANODE-to-CATHODE voltage to 6.3 Volts.

A capacitor connected between CATHODE and FEEDBACK will aid noise reduction. The *Typical Performance Curves* show values of capacitance and reverse current for optimum results. Keeping the reverse current between 20μA and 3mA ensures the stability of the reference regardless of capacitance.

A *Typical Interface Circuit* is shown for using the TDC4611 with 8-bit flash A/D converters such as the TDC1048 and TDC1038. The PNP transistor in the feedback loop of the TDC4611 is used to sink the reference current of the A/D converter. A *Typical Interface Circuit* is also shown for using the TDC4611 and TRW's 12-bit D/A converter, the TDC1012 (TDC1112, TDC1041, and TDC1141, too). The reference voltage applied to the REF– input of the TDC1012 determines the reference current flowing through the resistor on the REF+ input.

Operational Amplifiers

The output of the operational amplifier is very versatile and may be optimized in different ways.

Crossover Distortion

In applications where low crossover distortion is required from the operational amplifier, a pull-up or pull-down resistor should be added between the output and V+ or V–. The value of the resistor should be selected to pull an additional 1mA from the amplifier output. This additional class-A current flowing in the TDC4611 output stage will increase power dissipation slightly and minimize crossover distortion.

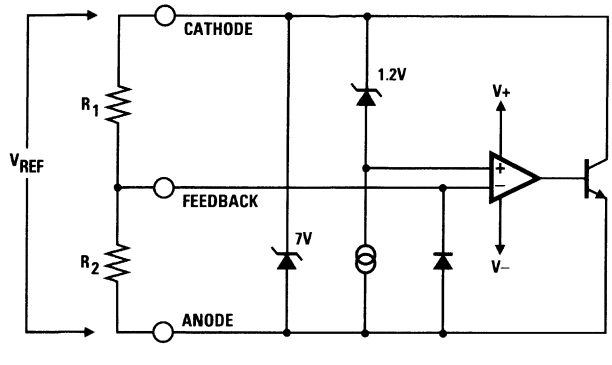
Driving of Capacitive Loads

The output resistance of the amplifier in combination with the capacitive load determines the dominant pole of the amplifier and limits its frequency stability. When driving a capacitance of 200pF, pull-up or pull-down resistors used to improve crossover distortion will also ensure frequency stability.

Output Voltage Swing

Unloaded, the TDC4611 amplifier outputs can swing to within 300mV of the negative power supply voltage, V–. A resistor connected between the output and V– will increase the voltage swing, closer to V–. If the output load is referred to V+, the negative-going output swing is increased but bandwidth and slew-rate are reduced.

Figure 4. Reference Equivalent Circuit



$$V_{REF} = 1.2\left(1 + \frac{R_2}{R_1}\right)$$

Figure 5. Typical Application of TDC4611 as Reference for a Flash A/D Converter

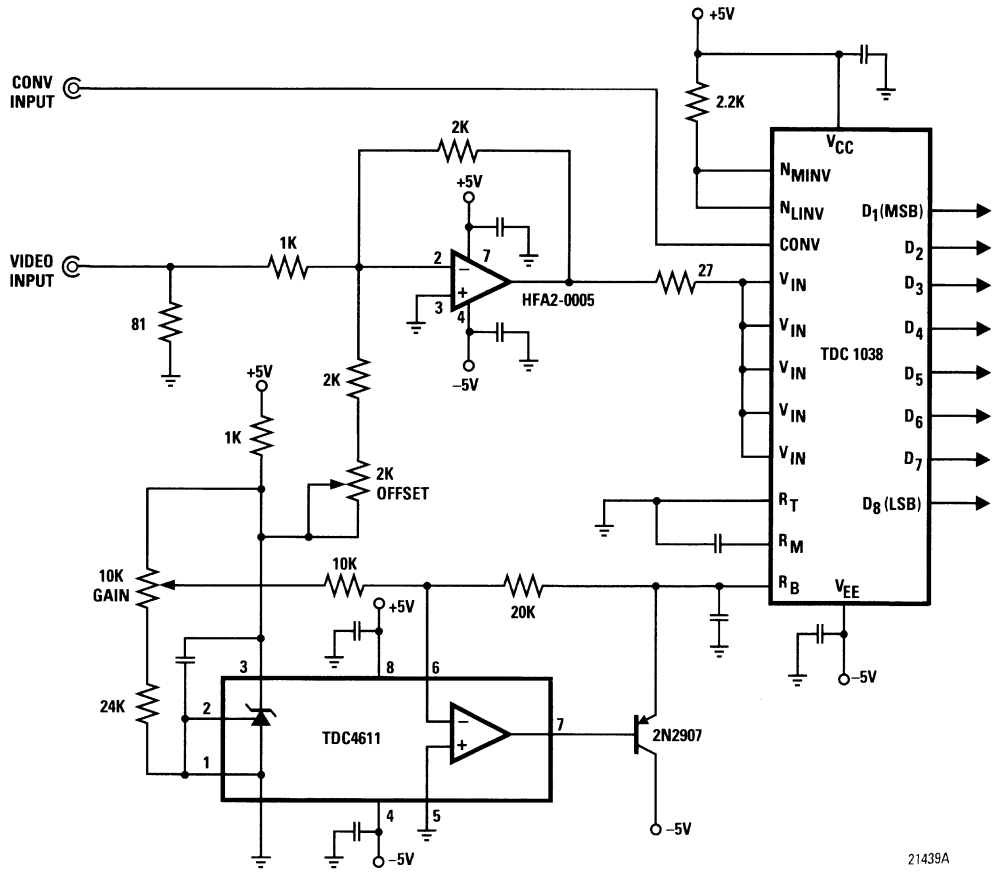
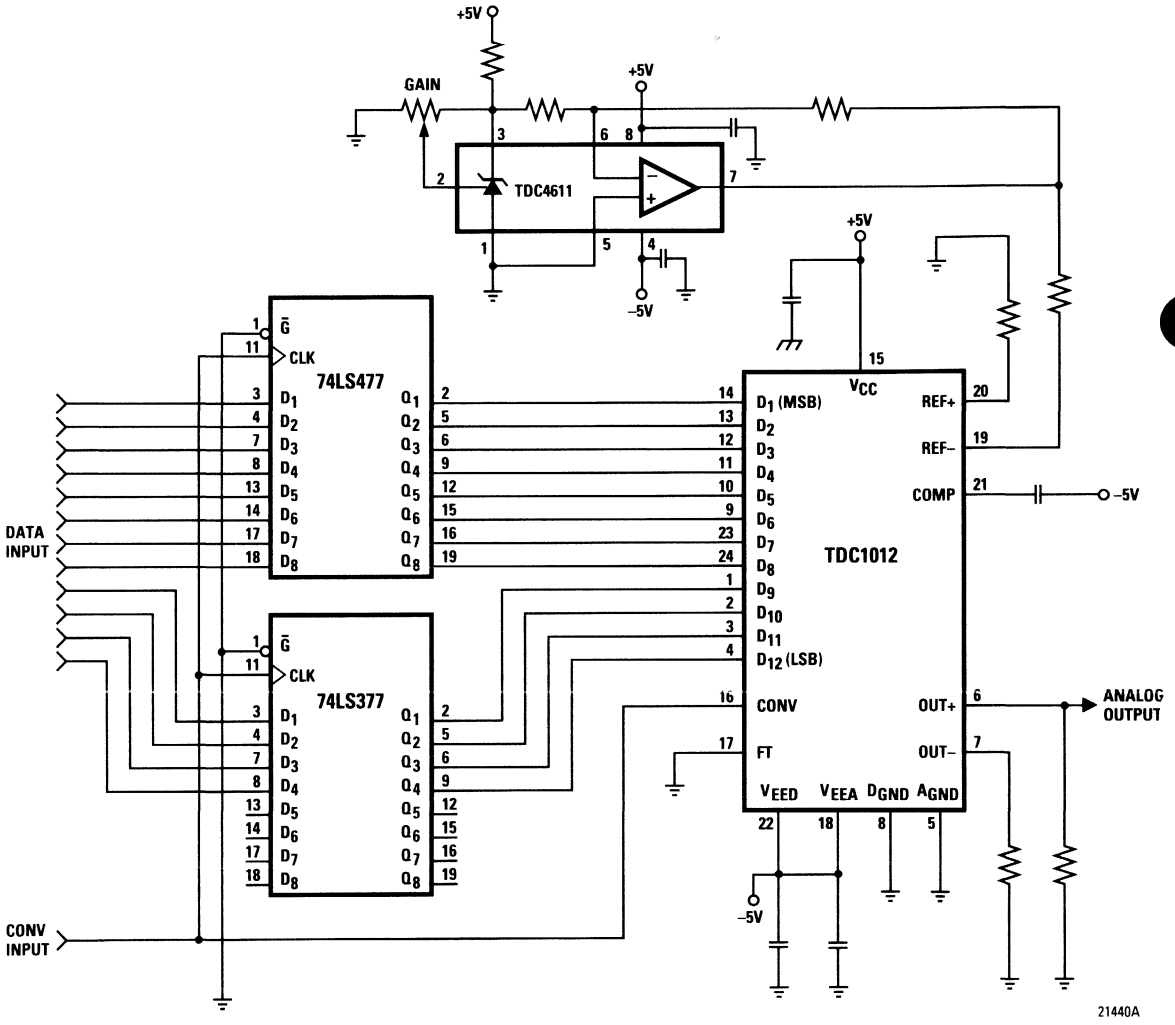


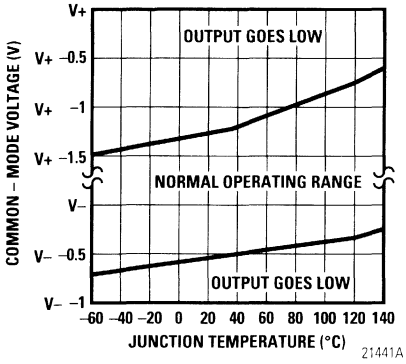
Figure 6. Typical Application of TDC4611 as a Reference for the TDC1012 D/A Converter



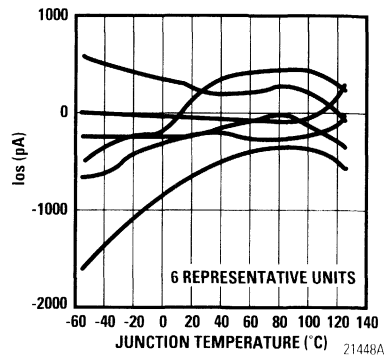
Typical Performance Characteristics (Operational Amplifer)

V+ = 5V, V– = GND = 0V, V_{CM} = V+/2, V_{OUT} = V+/2 T_J = 25°C, unless otherwise noted

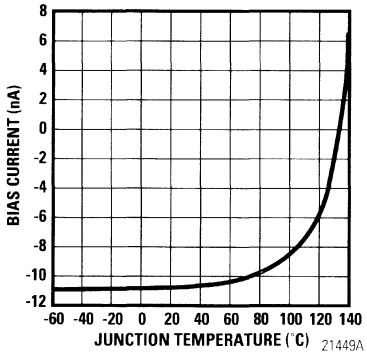
A. Input Common-Mode Voltage Range vs Temperature



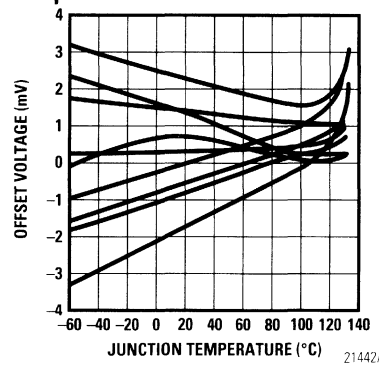
B. Input Offset Current vs Junction Temperature



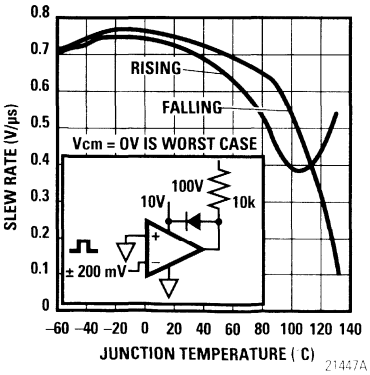
C. Input Bias Current vs Junction Temperature



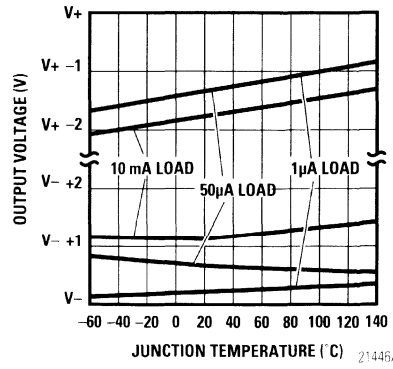
D. V_{OS} vs Junction Temperature on 9 Representative Units



E. Slew Rate vs Temperature and Output Sink Current



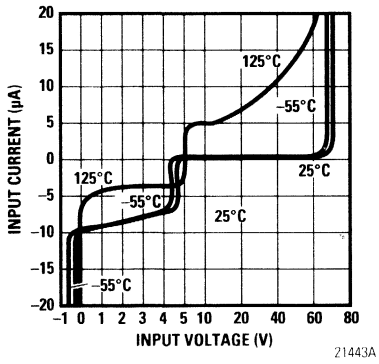
F. Output Voltage Swing vs Temperature and Current



Typical Performance Characteristics (Operational Amplifer)

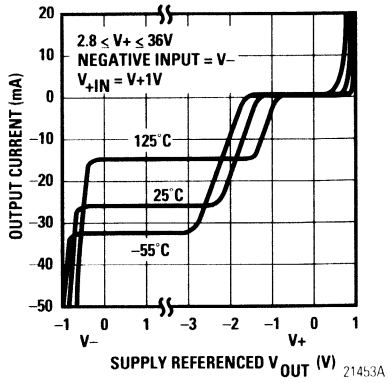
$V+ = 5V$, $V- = GND = 0V$, $V_{CM} = V+/2$, $V_{OUT} = V+/2$ $T_J = 25°C$, unless otherwise noted

G. Input Bias Current vs Common-Mode Voltage



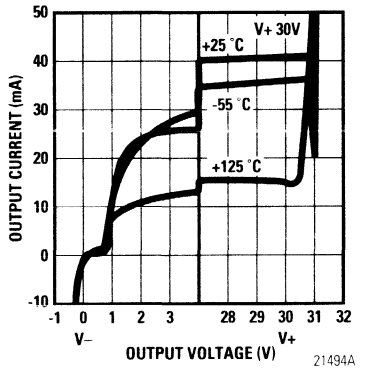
21443A

H. Output Sink Current vs Output Voltage and Temperature



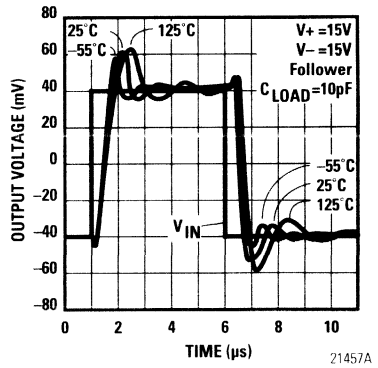
21453A

I. Slew Rate vs Temperature with Common-Mode Voltage below V–



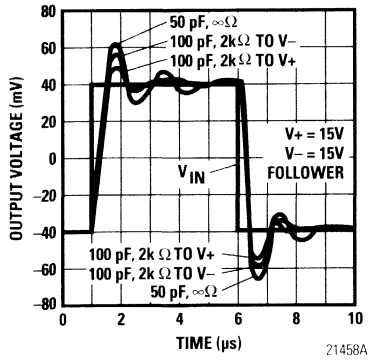
21494A

J. Small-Signal Pulse Response vs Temperature



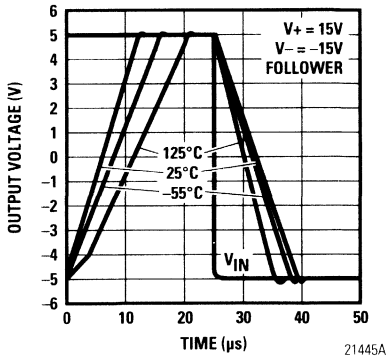
21457A

K. Small-Signal Pulse Response vs Load



21458A

L. Large-Signal Step Response

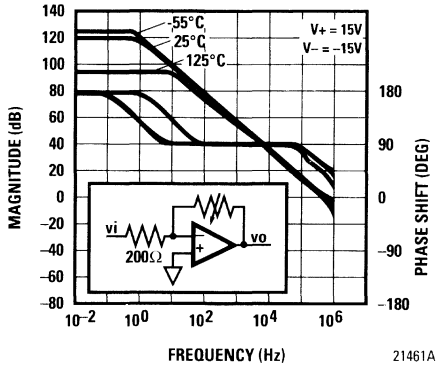


21445A

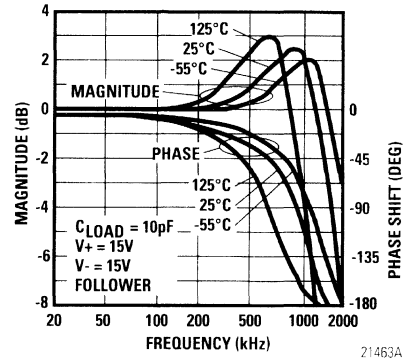
Typical Performance Characteristics (Operational Amplifer)

V+ = 5V, V– = GND = 0V, V_{CM} = V+/2, V_{OUT} = V+/2 T_J = 25°C, unless otherwise noted

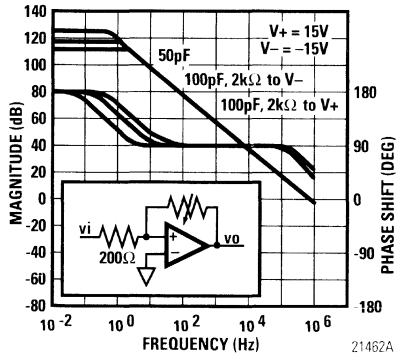
M. Small-Signal Voltage Gain vs Frequency and Temperature



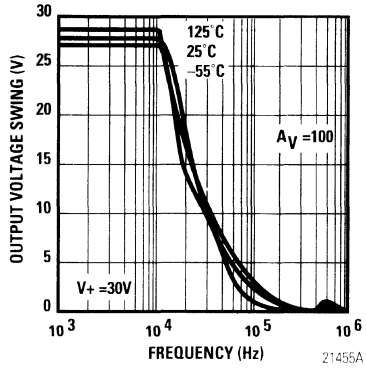
N. Follower Small-Signal Frequency Response



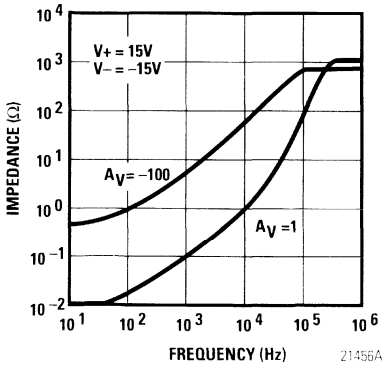
O. Small-Signal Voltage Gain vs Frequency and Load



P. Output Swing, Large-Signal



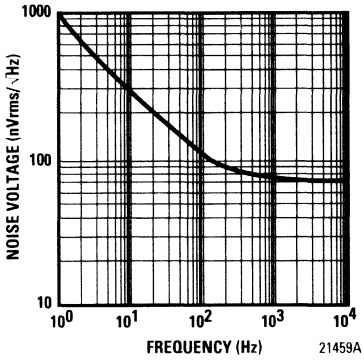
Q. Output Impedance vs Frequency and Gain



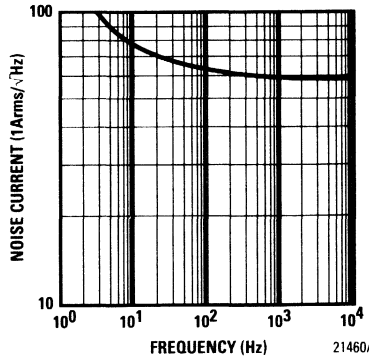
Typical Performance Characteristics (Operational Amplifer)

V+ = 5V, V– = GND = 0V, V_{CM} = V+/2, V_{OUT} = V+/2 T_J = 25°C, unless otherwise noted

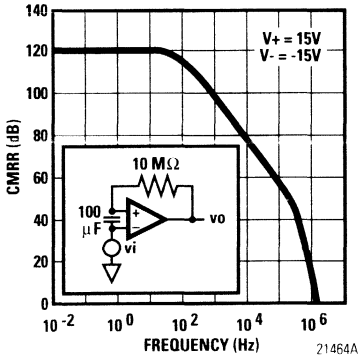
R. Op Amp Voltage Noise vs Frequency



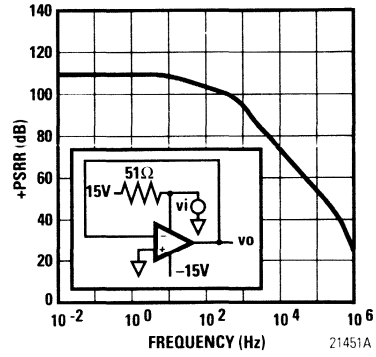
S. Op Amp Current Noise vs Frequency



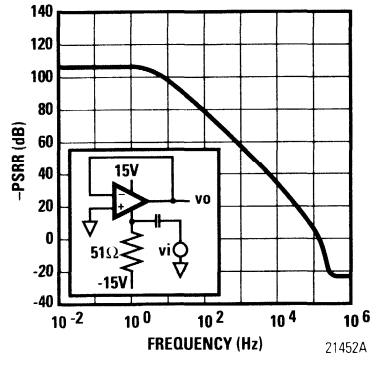
T. Common-Mode Input Voltage Rejection Ratio



U. Positive Power Supply Voltage Rejection Ratio



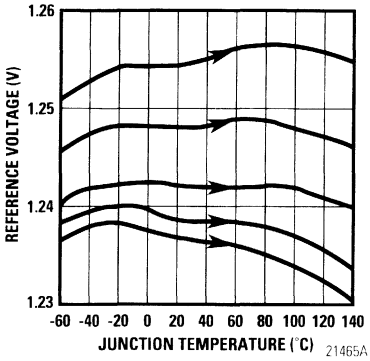
V. Negative Power Supply Voltage Rejection Ratio



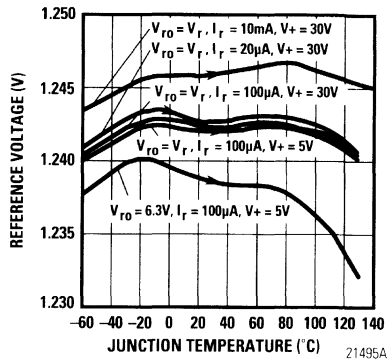
Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V– = 0V, unless otherwise noted

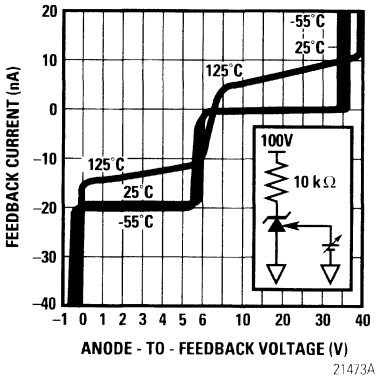
W. Reference Voltage vs Temperature on 5 Representative Units



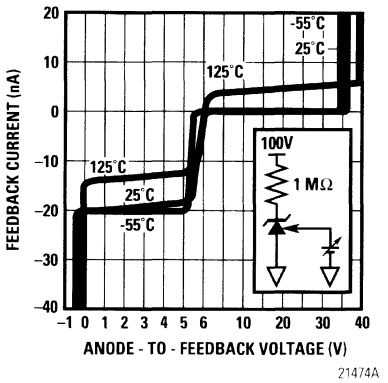
X. Reference Voltage vs Temperature and Bias Point



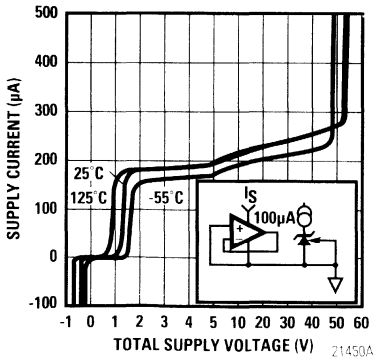
Y. Feedback Current vs Feedback-to-Anode Voltage



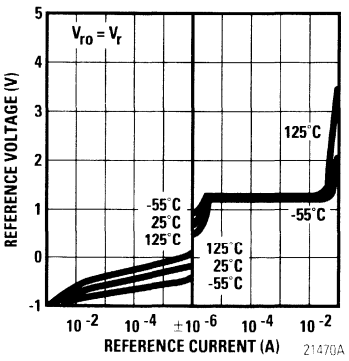
Z. Feedback Current vs Feedback-to-Anode Voltage



AA. Power Supply Current vs Power Supply Voltage



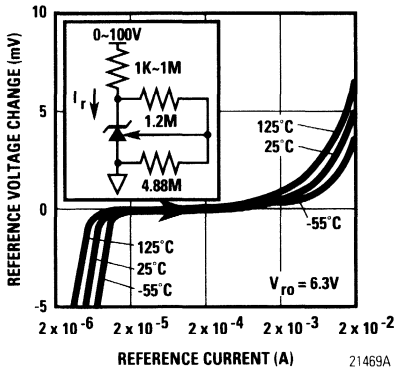
BB. Reference Voltage vs Reference Current



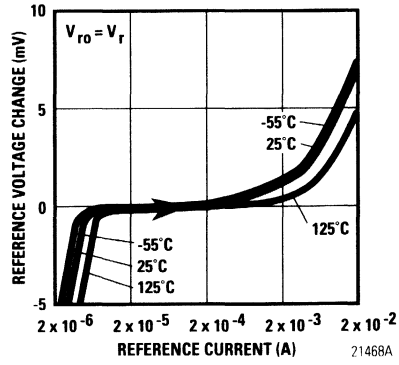
Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V– = 0V, unless otherwise noted

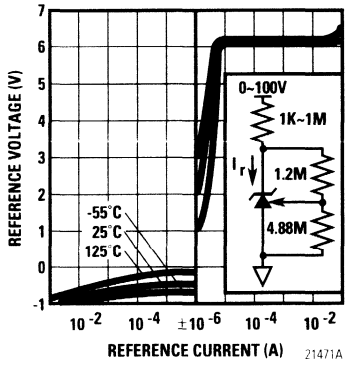
CC. Reference Voltage vs Current and Temperature



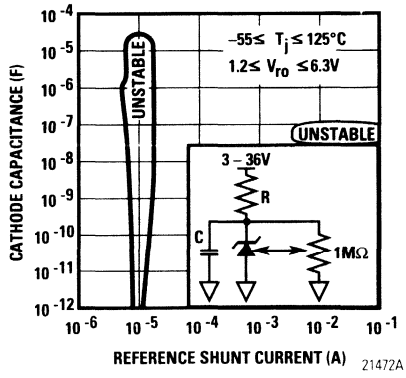
DD. Reference Voltage vs Current and Temperature



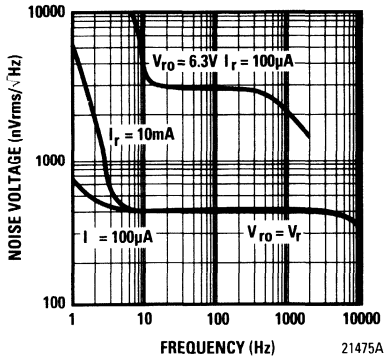
EE. Reference Voltage vs Reference Current



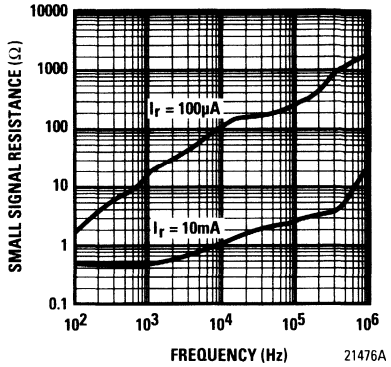
FF. Reference AC Stability Range



GG. Reference Noise Voltage vs Frequency



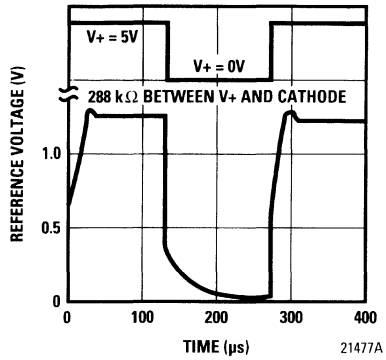
HH. Reference Small-Signal Resistance vs Frequency



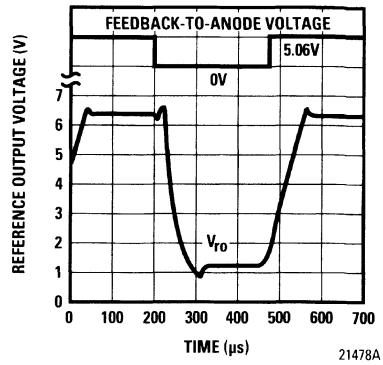
Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V– = 0V, unless otherwise noted

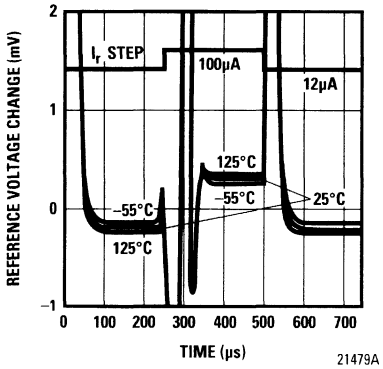
II. Reference Power-Up Time



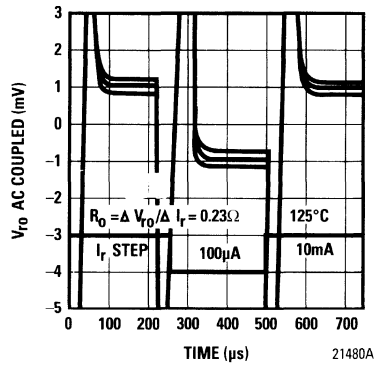
JJ. Reference Voltage with Feedback Voltage Step



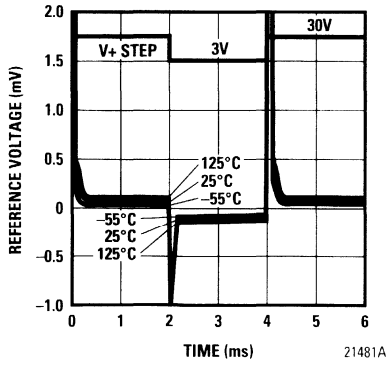
KK. Reference Voltage with 100~12 µA Current Step



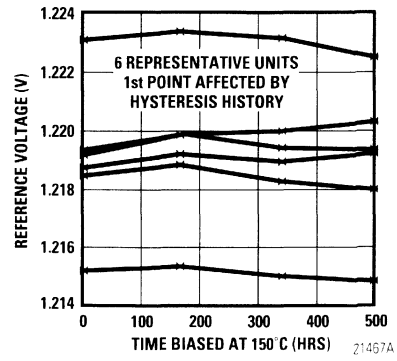
LL. Reference Step Response for 100µA ~ 10mA Current Step



MM. Reference Voltage Change with Supply Voltage Step



NN. Accelerated Reference Voltage Drift vs Time



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC4611B4F	EXT T_A=−55°C to 125°C	Commercial	8 Pin CERDIP	4611B4F
TDC4611NHC	T_A=0°C to 70°C	Commercial	8 Pin Plastic DIP	4611NHC
TDC4611MEC	T_A=0°C to 70°C	Commercial	14 Pin Plastic SOIC	4611MEC

All parameters in this specification are guaranteed by design, sample testing or 100% testing as appropriate. TRW reserves the right to make changes to products and specifications without notice. This information does not convey any license under patent rights of TRW LSI Products Inc., TRW Inc., or others.

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C

TDC4614

Adjustable Voltage Reference with Four Operational Amplifiers

The TDC4614 comprises a precision adjustable voltage reference and four general purpose operational amplifiers on the same monolithic integrated circuit. This combination of circuit functions is ideally suited for complete reference circuits for A/D and D/A converters.

The voltage reference of the TDC4614 uses a band-gap reference source and built-in amplifier to enable the output voltage to be set with one pair of external resistors.

Four separate operational amplifiers are included on the TDC4614 for use with the voltage reference circuit in generating complete voltage reference circuits for A/D and D/A converters where multiple voltage outputs are required. The common-mode input range of the operational amplifiers extend to the negative power supply voltage for additional application flexibility.

The TDC4614 is available in both commercial (0°C to +70°C) and extended (–55°C to +125°C) temperature ranges and in 16-pin CERDIP, plastic DIP, and plastic SOIC packages.

Features

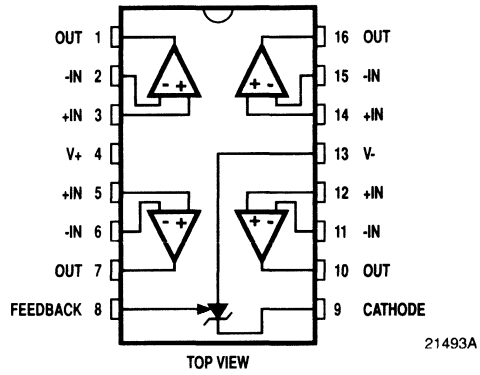
- Low Drift, Adjustable Voltage Reference
- Four Low Offset Voltage Operational Amplifiers
- Wide Common-Mode Input And Power Supply Voltage Range
- Wide Reference Voltage Range and Amplifier Output Voltage Swing
- Low Power Dissipation

Applications

- Complete Voltage References For A/D And D/A Converters
- AC and DC Signal-Conditioning
- Active Filters With Offset Control
- Miniaturized, Reduced Chip Count Circuitry

C

Interface Diagram



16 Pin CERDIP – B9 Package
16 Pin Plastic SOIC – M9 Package
16 Pin Plastic DIP – N9 Package

TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

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Printed in the U.S.A.

Figure 1. Operational Amplifier Simplified Schematic Diagram

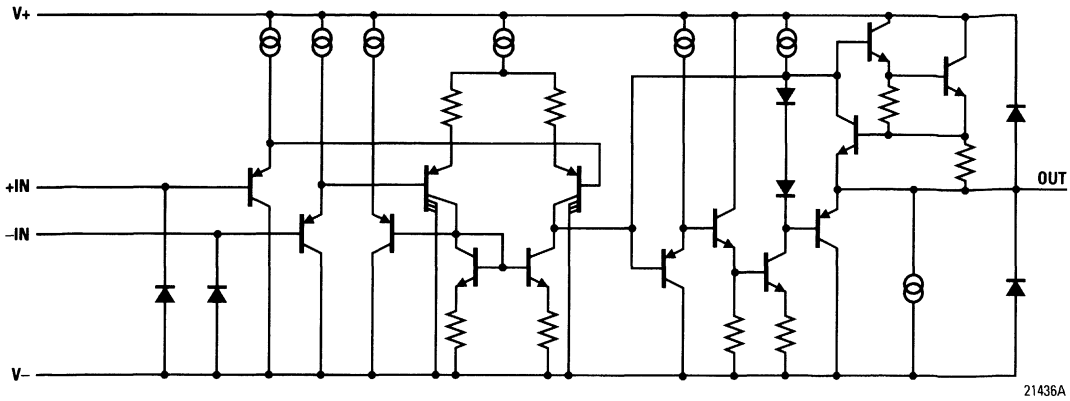


Figure 2. Reference Simplified Schematic Diagram

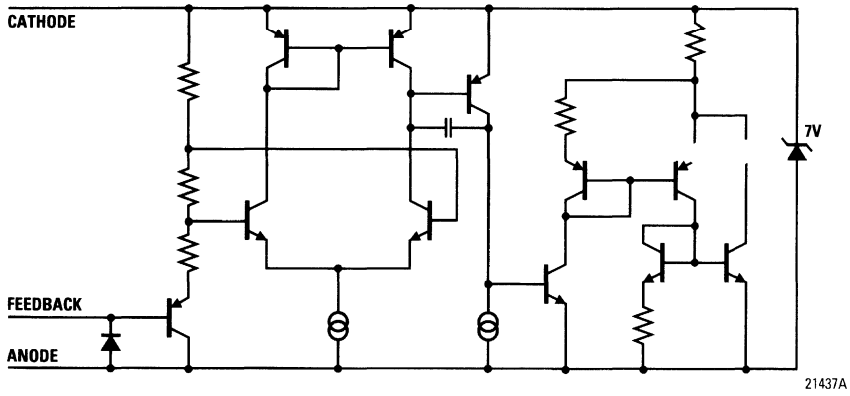
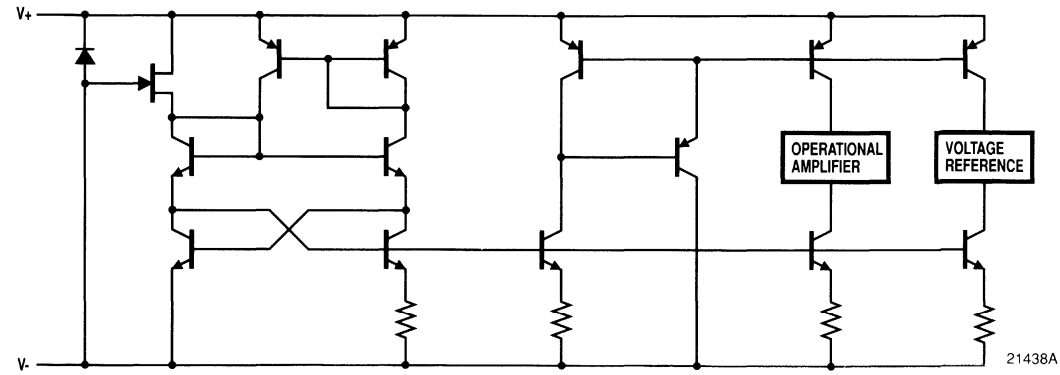


Figure 3. Bias Circuit Simplified Schematic Diagram



Functional Description

General Information

The TDC4614 is made up of four operational amplifiers and an adjustable voltage reference on the same monolithic integrated circuit. The operational amplifiers are general purpose voltage feedback amplifiers ideally suited for DC and low-frequency applications. The voltage reference is a three-terminal band-gap voltage source with its own built-in amplifiers.

Power

The TDC4614 has two power supply input terminals, V+ and V–, and will operate with a wide range of power supply voltages. The TDC4614 will operate with either V+ or V– grounded. The substrate of the TDC4614 is biased at the most negative potential, V–, which is also connected to the ANODE terminal of the voltage reference.

Voltage Reference

The TDC4614 voltage reference employs band-gap shunt-regulator topology that can be modeled as a Zener diode. When current flow in this diode is in the forward direction (from ANODE to CATHODE), it exhibits a normal diode exponential transfer characteristic. Current flowing in the reverse direction generates a constant voltage (CATHODE positive with respect to ANODE). The magnitude of this voltage is set by a pair of external resistors connected between ANODE and CATHODE with a common connection to FEEDBACK. When FEEDBACK is connected directly to ANODE, the voltage between CATHODE and ANODE is its minimum value of approximately 1.2 Volts.

Operational Amplifiers

The four operational amplifiers of the TDC4614 are general purpose voltage- feedback amplifiers with PNP input transistors. The PNP input stage allows a common-mode input range that includes the negative power supply, V–. The inputs are diode-clamped to V–, but not clamped to V+ or to each other, allowing large differential input voltages.

The amplifiers are unity-gain stable with low input bias and power supply currents. All four amplifiers and voltage reference share the same integrated circuit and their only common point is the substrate which is biased at V–. Unused amplifiers should be connected so that both inputs and the output are within their recommended operating conditions (i.e., –IN connected to OUT and +IN connected to FEEDBACK).

The output structure of the TDC4614 amplifier has a deadband voltage of approximately one diode V_{be}. The crossover distortion generated by this deadband can be eliminated by the use of a pull-up or pull-down resistor between the output and V+ or V–. The resistor increases output current and reduces crossover distortion. The value of this resistor should be determined so that the current through it is nominally 1mA. Crossover distortion will be minimized and the amplifier will be frequency-stable driving capacitive loads as large as 200pF.

Package Interconnections

Signal Type	Signal Name	Function	Value	B9, M9, N9 Package Pins
Power	V+	Positive Supply Voltage	+5V Nominal	4
	V–	Negative Supply Voltage	0V Nominal	13
Operational Amplifier 1	+IN	Non-Inverting Operational Amplifier Input	V– to V+ – 1.4V	3
	–IN	Inverting Operational Amplifier Input	V– to V+ – 1.4V	2
	OUT	Operational Amplifier Output	V– +1V to V+ –1.9V	1
Operational Amplifier 2	+IN	Non-Inverting Operational Amplifier Input	V– to V+ – 1.4V	5
	–IN	Inverting Operational Amplifier Input	V– to V+ – 1.4V	6
	OUT	Operational Amplifier Output	V– +1V to V+ –1.9V	7
Operational Amplifier 3	+IN	Non-Inverting Operational Amplifier input	V– to V+ – 1.4V	12
	–IN	Inverting Operational Amplifier Input	V– to V+ - 1.4V	11
	OUT	Operational Amplifier Output	V– +1V to V+ –1.9V	10
Operational Amplifier 4	+IN	Non-Inverting Operational Amplifier Input	V– to V+ – 1.4V	14
	–IN	Inverting Operational Amplifier Input	V– to V+ – 1.4V	15
	OUT	Operational Amplifier Output	V– +1V to V+ –1.9V	16
Reference	Cathode	Reference Cathode	1.2V to 6.3V	9
	Feedback	Reference Control	$V_{CATHODE}$–1.2V	8

Absolute maximum ratings (beyond which the device may be damaged)

Supply Voltage (V+ measured to V–)	–0.3 to 36V
Applied Voltage any pin except CATHODE, measured to V–[1]	–0.3 to 36V
Applied Current, externally forced (any pin)	±20mA
Differential Input Voltage (+IN to –IN)	±36V
Output Short Circuit duration[2]	Indefinite
ESD Tolerance 120pF, 1.5KΩ[3]	±1kV

Notes:
1. The failure is caused not by exessive voltage but rather by excessive current flow. If any pin has a potential less than one diode drop below V– then this allows a parasitic NPN transistor to turn on and conduct current to V–. No damage to the device will occur if this current is limited to the absolute maximum ratings, however the device operation while this parasitic transistor is conducting is undefined and unpredictable.
2. Simultaneous short circuit of Reference and Operational Amplifier with higher power supply voltages may cause the junction temperature to rise above the maximum and thus should not be continuous.
3. Human Body Model

Operating conditions

Parameter	Min	Nom	Max	Unit
V+ Measured to V–	3	5	32	V
Common Mode Input Range (Operational Amplifier)	V–+1		V+–1.9	V
Reference Voltage	1.2		6.3	V
Ambient Temperature	0		70	°C

Electrical characteristics (Operational Amplifier)[1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Unit
V_{OS}	Offset Voltage	4V ≤ V+ ≤ 32V		±7		±5	mV
V_{OS}	Offset Voltage	V+ = 30V, 0V≤V_{CM} ≤28.6V		±7		±5	mV
$V_{OS}TC$	Offset Temperature Coefficient			±30		±25	µV/°C
I_B	Input Bias Current	I_B+IN and I_B–IN		±40		±25	nA
I_{OS}	Input Offset Current	I_{OS} = I_B+IN – I_B–IN		±5		±4	nA
$I_{OS}TC$	I_{OS} Temperature Coefficient	Average value between 25°C and temperature extremes		±4		±4	pA/°C
R_{IN}	(Differential)	T_A = 25°C	1800		1800		MΩ
R_{IN}	(Common-Mode)	T_A = 25°C	3800		3800		MΩ
C_{IN}		Capacitance to ground, Non-Inverting input of follower, T_A = 25°C		6		6	pF
A_{VOL}	Open Loop Voltage Gain	R_L = 10KΩ to GND, V+ = 30V, 5V≤V_{OUT} ≤25V, Open Loop A_{VOL} = $\Delta V_{OUT}/\Delta V_{INDIFF}$	92		92		dB
V_{OH}	Voltage Swing HIGH	R_L = 10KΩ to GND, V+ = 32V	V+ –1.9		V+ –1.8		V
V_{OL}	Voltage Swing LOW	R_L = 10KΩ to V+, V+ = 32V	V– +1.0		V– +1.0		V
I_{OUT+}	Current Sink	V_{OUT} = 1.6V, V_{+IN} = 0V, $V_{–IN}$ = 0.3V	11		8		mA
$I_{OUT–}$	Current Source	V_{OUT} = V+–2.5V, V_{+IN} = 0V $V_{–IN}$ = -0.3V		–13		–13	mA
I_{SC}	Short Circuit Current	V_{OUT} = 0V, V_{+IN} = 3V $V_{–IN}$ = 2V	–50		–46		mA

Note: 1. Unless otherwise specified, these specifications apply for V–=0V, V+=5V, V_{CM}=V+/2, V_{OUT}=V+/2.

Electrical characteristics (Reference)[1]

Parameter		Test Conditions	Temperature				Unit
			Standard		Extended		
			Min	Max	Min	Max	
V_{REF}	Reference Voltage		1.21919	1.2689	1.2390	1.2490	V
$V_{REF}TC$	Temperature Coefficient			20		150	PPM/°C
$V_{REF}LT$	Long Term Stability (Typical)	T_j = 40°C		400		400	PPM/ 1000 HR
$V_{REF}LT$	Long Term Stability	T_j = 150°C		1000		1000	PPM/ 1000 HR
$V_{REF}HS$	Hysteresis[2]			±3.2		±3.2	µV/°C
ΔV/ΔI	V_{REF} Change with Current	I_{REF} 16µA to 100µA I_{REF} 100µA to 10mA		1.1 5.5		1.0 5.0	mV mV
PSS	V_{REF} Change with V+	V_{REF} vs V+ Change for V+ from 5 to V+MAX		86		88	dB
$V_{REF}AS$	V_{REF} Change with Anode Voltage	V+ = V+MAX, V_{ANODE} from GND to V+ – 1V		3.0		5.0	mV
I_{FS}	Feedback Bias Current	$V_{ANODE} \leq V_{FS} \leq 5.06V$		–55		–40	nA
$V_{REF}N$	Noise	10Hz – 10KHz, V_{FS} = 0 Typical Specification		30		30	μV_{RMS}

Notes: 1. Unless otherwise specified, these specifications apply for V– = 0V, V+ = 5V, V_{CM} = V+/2, V_{OUT} = V+/2.

2. Hysteresis is $\Delta V_{RO}/\Delta T_J$ where ΔV_{RO} is the change in V_{RO} caused by a change in T_J after the reference has been "dehysterized" by spiraling the junction temperature in towards 25°C.

System performance characteristics (Operational Amplifier)

Parameter		Test Conditions	Temperature Range					Unit
			Standard			Extended		
			Min	Typ	Max	Min	Max	
GBW	Gain-Bandwidth Product	Closed loop, Gain = –1000, C_L = 30pF, Bandwidth = –3dB Frequency.		.52				MHz
SR	Slew Rate	V+ = 30V[1]	±.45	±.65		±.45		V/µs
N_V	Voltage Noise	100Hz, Input Referred		74				nV/√Hz
N_C	Current Noise	100Hz, Bias Current Noise		58				fA/√Hz
CMRR	Common Mode Rejection Ratio	V+ = 30V, 0V≤V_{CM}≤(V+–1.4V), CMRR = 20log{ΔV+/≤V_{OS}}	75	90		80		dB
PSRR	Power Supply Rejection Ratio	4V≤V+≤30V, V_{CM} = 1/2V+, PSRR = 20log{ΔV+/≤V_{OS}}	70	100		80		dB

Note: 1. Slew rate is measured with the Operational Amplifier in voltage follower mode. For rising slew rate, the input voltage is driven from 5V to 25Vand the output voltage transition is sampled at 10V and 20V. For falling slew rate, the input is driven from 25V to 5V, and the output is sampled at 20V and 10V.

Applications Information

Voltage Reference

The CATHODE input to the TDC4614 may be set anywhere within the range of +1.2 to +6.3 Volts with respect to V– and ANODE. Poor voltage regulation will result when the CATHODE voltage is set to greater than +6.3 Volts. The ***Reference Equivalent Circuit*** shows how external resistors, R_1 and R_2, determine the gain of the built-in amplifier and, therefore, the total voltage (V_{REF}) between ANODE and CATHODE. The 7 Volt Zener diode limits the usable ANODE-to-CATHODE voltage to 6.3 Volts.

A capacitor connected between CATHODE and FEEDBACK will aid noise reduction. The ***Typical Performance Curves*** show values of capacitance and reverse current for optimum results. Keeping the reverse current between 20μA and 3mA ensures the stability of the reference regardless of capacitance.

A ***Typical Interface Circuit*** is shown for using the TDC4614 or TDC4611 (voltage reference with single operational amplifier) with 8-bit flash A/D converters such as the TDC1048 and TDC1038. The PNP transistor in the feedback loop of the TDC4611 is used to sink the reference current of the A/D converter. A ***Typical Interface Circuit*** is also shown for TRW's 12-bit D/A converter, the TDC1012 (TDC1112, TDC1041, and TDC1141, too). The reference voltage applied to the REF– input of the TDC1012 determines the reference current flowing through the resistor on the REF+ input.

Operational Amplifiers

The outputs of the operational amplifiers are very versatile and may be optimized in a number of ways.

Crossover Distortion

In applications where low crossover distortion is required from the operational amplifier, a pull-up or pull-down resistor should be added between the output and V+ or V–. The value of the resistor should be selected to pull an additional 1mA from the amplifier output. This additional class-A current flowing in the TDC4614 output stage will increase power dissipation slightly and minimize crossover distortion.

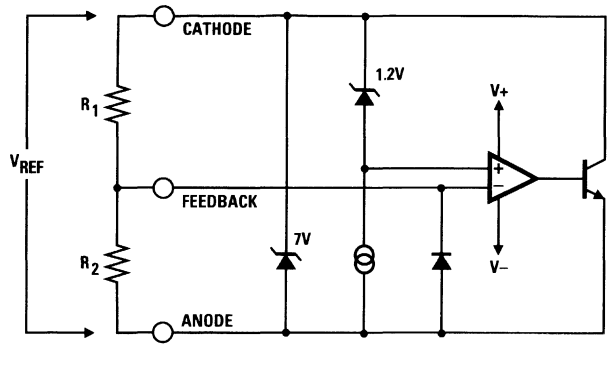
Driving of Capacitive Loads

The output resistance of the amplifier in combination with the capacitive load determines the dominant pole of the amplifier and limits its frequency stability. When driving a capacitance of up to 200pF, pull-up or pull-down resistors used to improve crossover distortion will also ensure frequency stability.

Output Voltage Swing

Unloaded, the TDC4614 amplifier outputs can swing to within 300mV of the negative power supply voltage, V–. A resistor connected between the output and V– will increase the voltage swing, closer to V–. If the output load is referred to V+, the negative-going output swing is increased but bandwidth and slew-rate are reduced.

Figure 4. Reference Equivalent Circuit



$$V_{REF} = 1.2\left(1 + \frac{R_2}{R_1}\right)$$

Figure 5. Typical Application of TDC4614 as Reference for a Flash A/D Converter

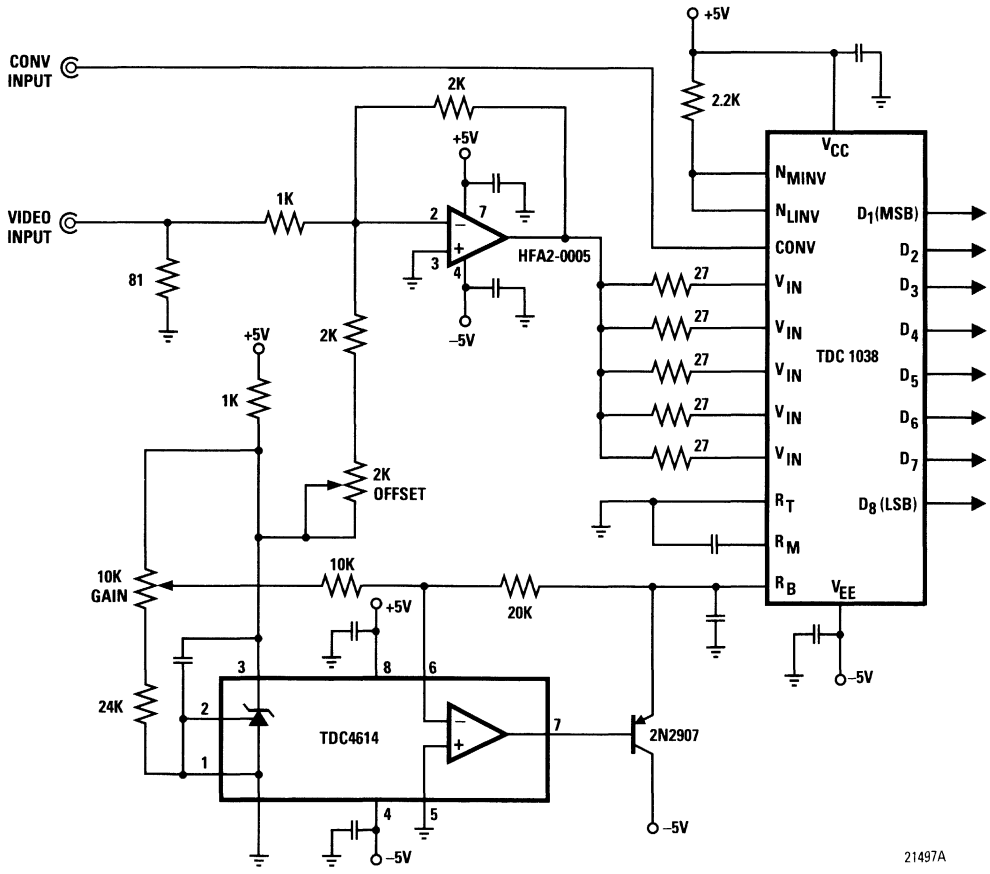
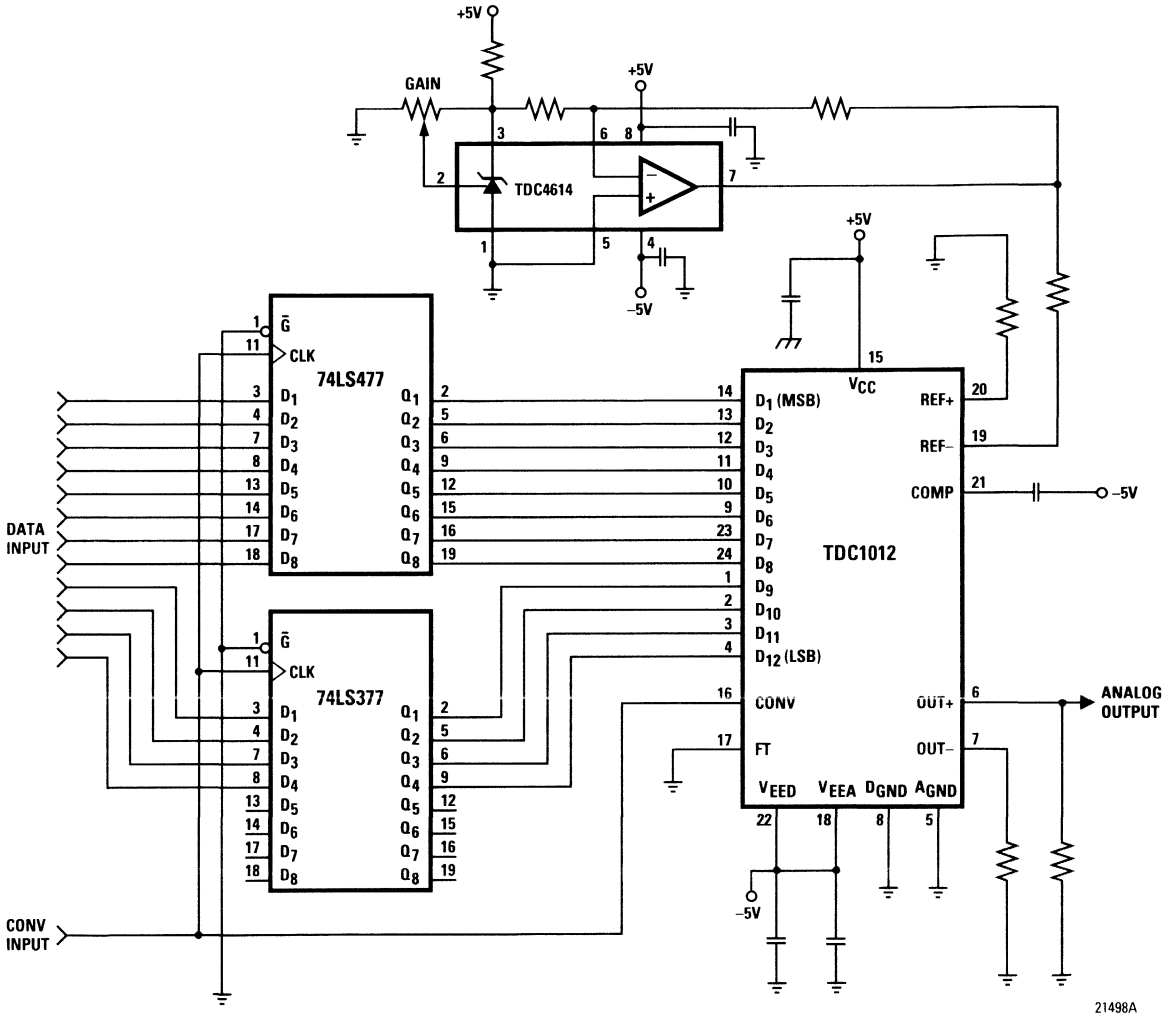
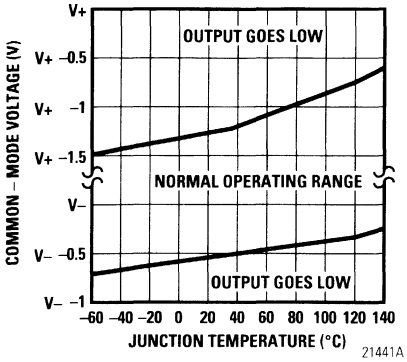


Figure 6. Typical Application of TDC4614 as a Reference for the TDC1012 D/A Converter

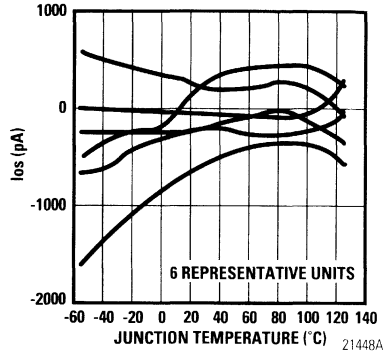


Typical Performance Characteristics (Operational Amplifer)
V+ = 5V, V– = GND = 0V, V_{CM} = V+/2, V_{OUT} = V+/2 T_J = 25°C, unless otherwise noted

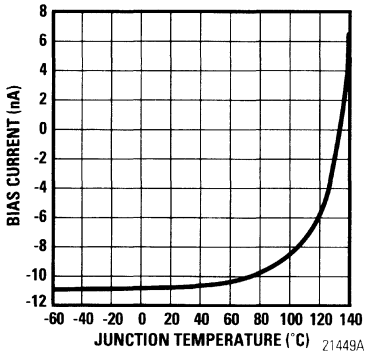
A. Input Common-Mode Voltage Range vs Temperature



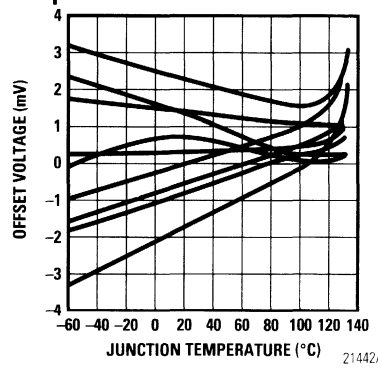
B. Input Offset Current vs Junction Temperature



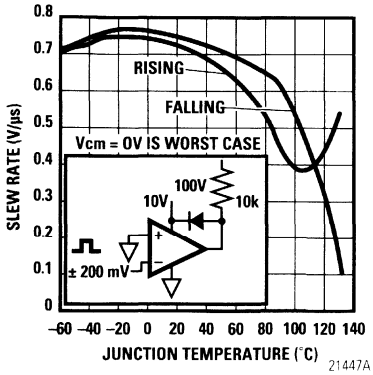
C. Input Bias Current vs Junction Temperature



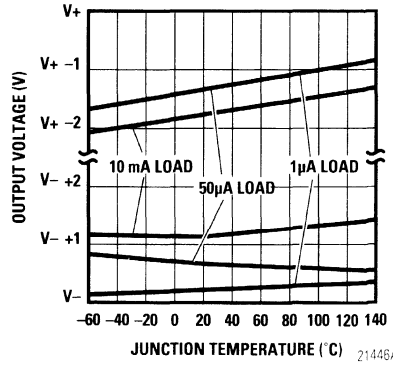
D. V_{OS} vs Junction Temperature on 9 Representative Units



E. Slew Rate vs Temperature and Output Sink Current

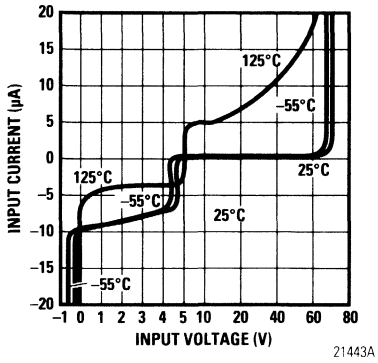


F. Output Voltage Swing vs Temperature and Current

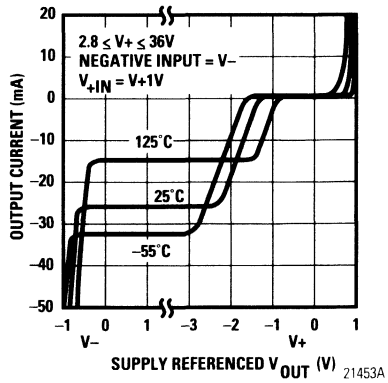


Typical Performance Characteristics (Operational Amplifer)
V+ = 5V, V– = GND = 0V, V_{CM} = V+/2, V_{OUT} = V+/2 T_J = 25°C, unless otherwise noted

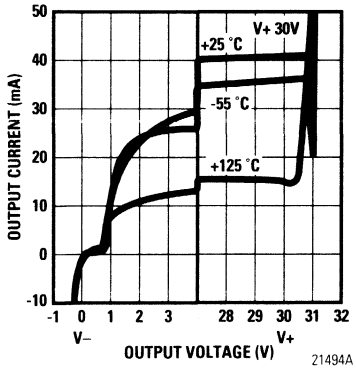
G. Input Bias Current vs Common-Mode Voltage



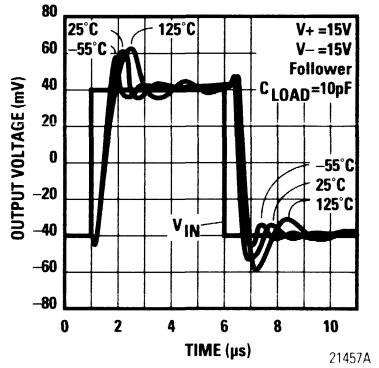
H. Output Sink Current vs Output Voltage and Temperature



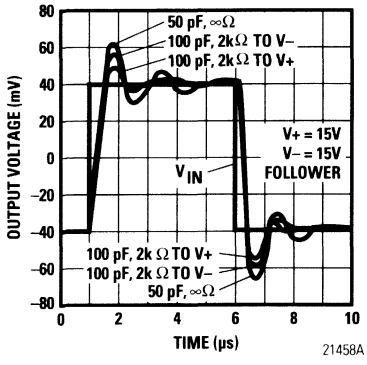
I. Slew Rate vs Temperature with Common-Mode Voltage below V–



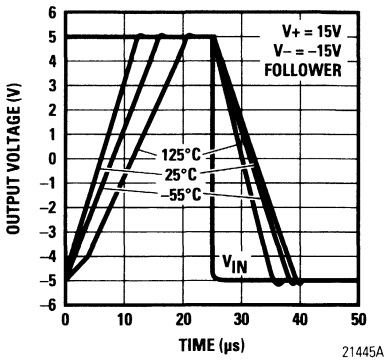
J. Small-Signal Pulse Response vs Temperature



K. Small-Signal Pulse Response vs Load

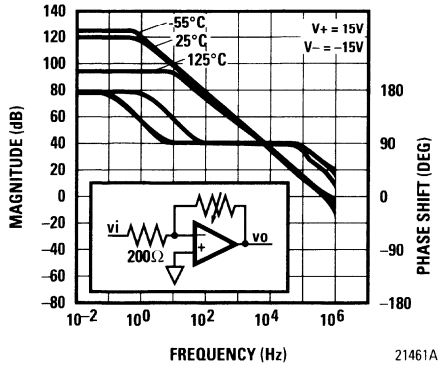


L. Large-Signal Step Response

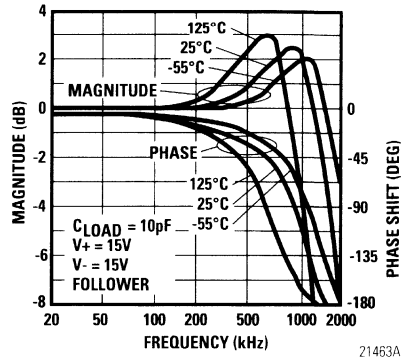


Typical Performance Characteristics (Operational Amplifer)
$V+ = 5V$, $V- = GND = 0V$, $V_{CM} = V+/2$, $V_{OUT} = V+/2$ $T_J = 25°C$, unless otherwise noted

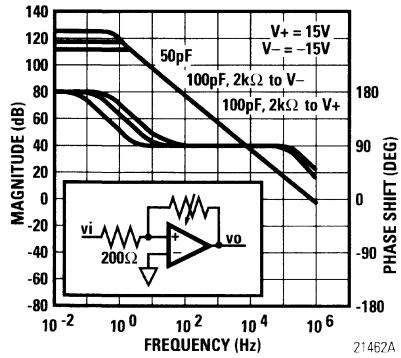
M. Small-Signal Voltage Gain vs Frequency and Temperature



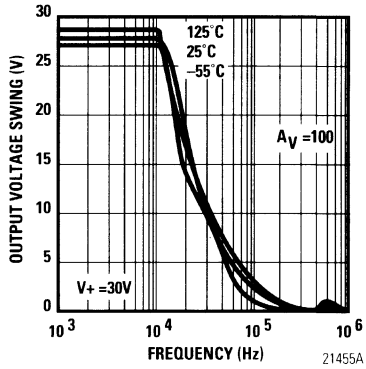
N. Follower Small-Signal Frequency Response



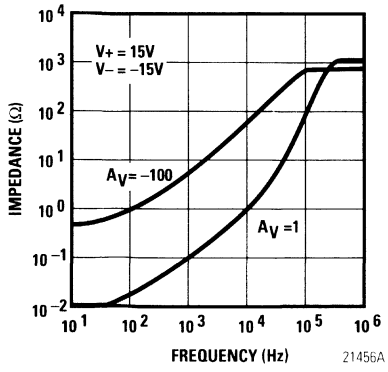
O. Small-Signal Voltage Gain vs Frequency and Load



P. Output Swing, Large-Signal

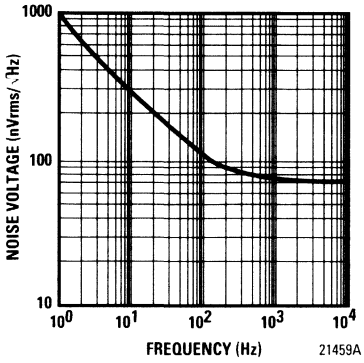


Q. Output Impedance vs Frequency and Gain

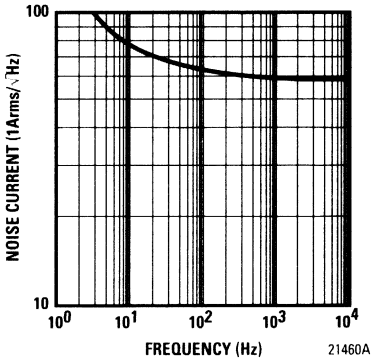


Typical Performance Characteristics (Operational Amplifer)
V+ = 5V, V– = GND = 0V, V_{CM} = V+/2, V_{OUT} = V+/2 T_J = 25°C, unless otherwise noted

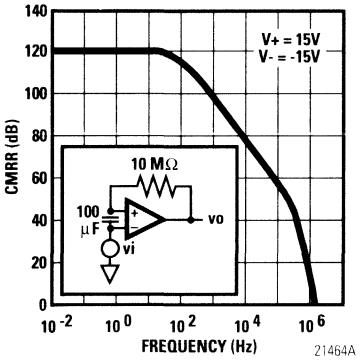
R. Op Amp Voltage Noise vs Frequency



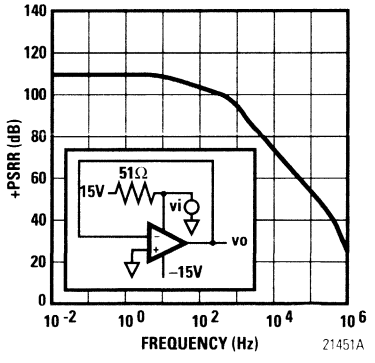
S. Op Amp Current Noise vs Frequency



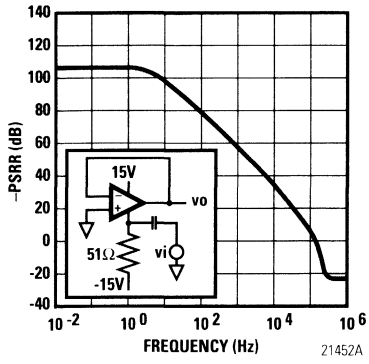
T. Common-Mode Input Voltage Rejection Ratio



U. Positive Power Supply Voltage Rejection Ratio

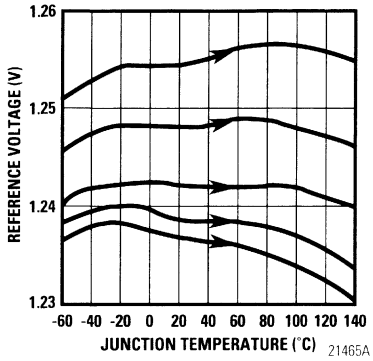


V. Negative Power Supply Voltage Rejection Ratio

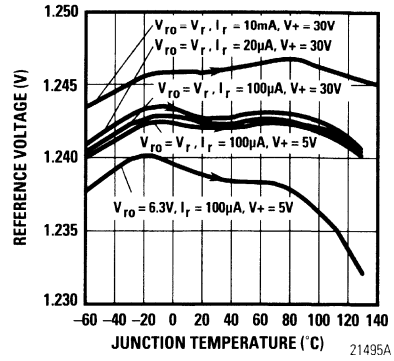


Typical Performance Characteristics (Reference)
T_J = 25°C, FEEDBACK pin shorted to V– = 0V, unless otherwise noted

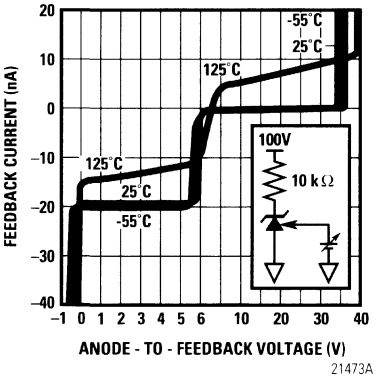
W. Reference Voltage vs Temperature on 5 Representative Units



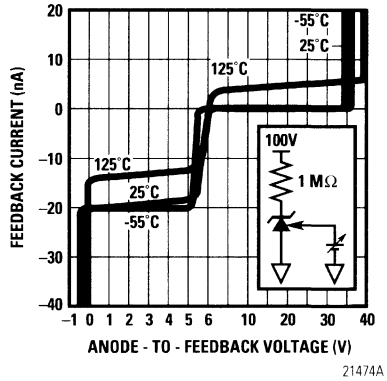
X. Reference Voltage vs Temperature and Bias Point



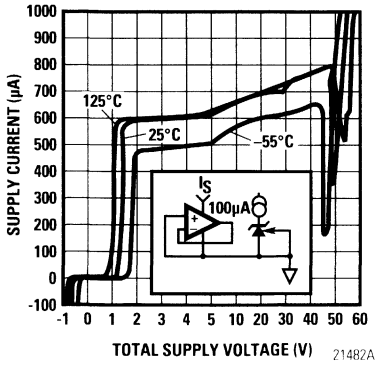
Y. Feedback Current vs Feedback-to-Anode Voltage



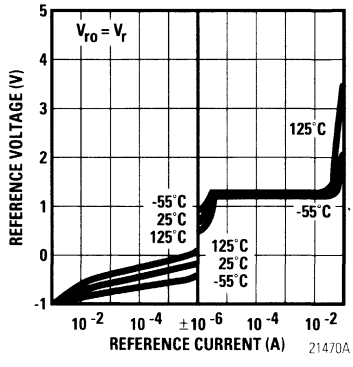
Z. Feedback Current vs Feedback-to-Anode Voltage



AA. Power Supply Current vs Power Supply Voltage

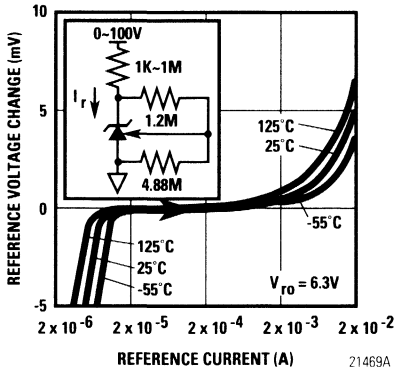


BB. Reference Voltage vs Reference Current

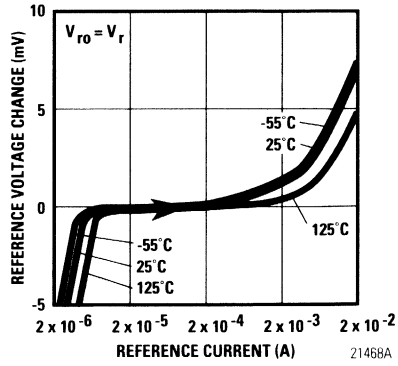


Typical Performance Characteristics (Reference)
T_J = 25°C, FEEDBACK pin shorted to V– = 0V, unless otherwise noted

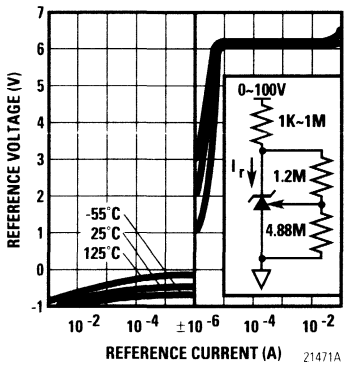
CC. Reference Voltage vs Current and Temperature



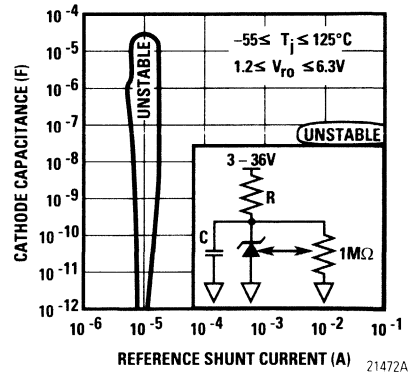
DD. Reference Voltage vs Current and Temperature



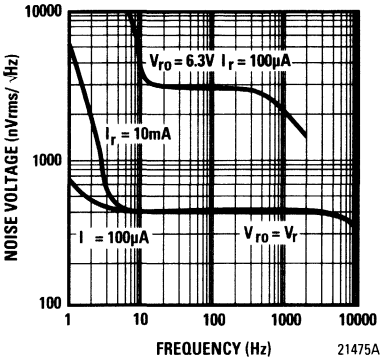
EE. Reference Voltage vs Reference Current



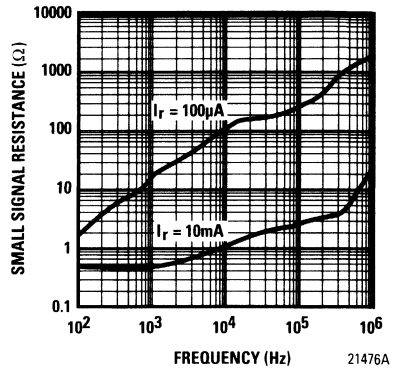
FF. Reference AC Stability Range



GG. Reference Noise Voltage vs Frequency

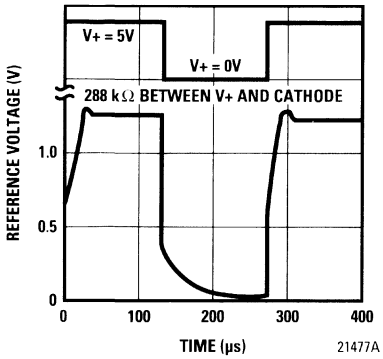


HH. Reference Small-Signal Resistance vs Frequency

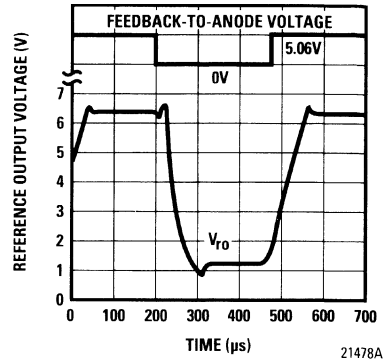


Typical Performance Characteristics (Reference)
T_J = 25°C, FEEDBACK pin shorted to V– = 0V, unless otherwise noted

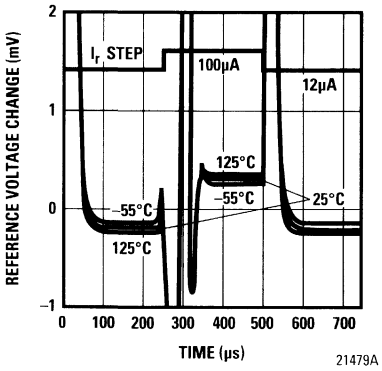
II. Reference Power-Up Time



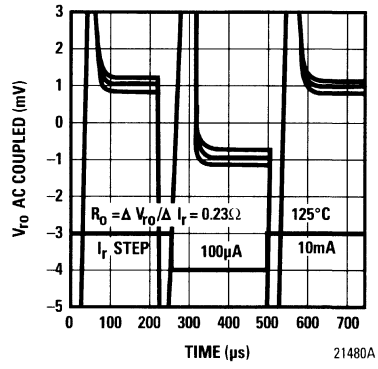
JJ. Reference Voltage with Feedback Voltage Step



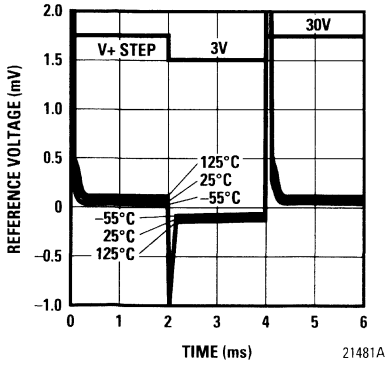
KK. Reference Voltage with 100~12 µA Current Step



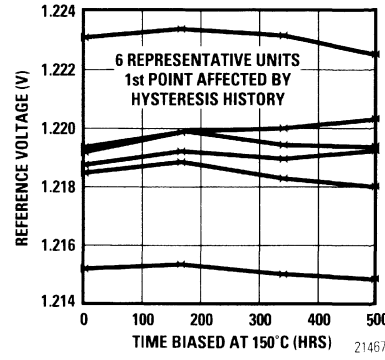
LL. Reference Step Response for 100µA ~ 10mA Current Step



MM. Reference Voltage Change with Supply Voltage Step



NN. Accelerated Reference Voltage Drift vs Time



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC4614B9F	EXT–T_A=–55°C to 125°C	Commercial	16 Pin CERDIP	4614B9F
TDC4614N9C	T_A=0°C to 70°C	Commercial	16 Pin Plastic DIP	4614N9C
TDC4614M9C	T_A=0°C to 70°C	Commercial	16 Pin Plastic SOIC	4614M9C

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C

THC4940

Track and Hold Amplifier

150MHz, Small Signal Bandwidth

The TRW THC4940 is a fast sampling, wide-band track and hold amplifier that offers ultra-fast switching performance plus an unprecedented array of supporting specifications. This combination ensures that the accuracy indicated by the switching specifications is fully realized, even at the highest sampling rates.

The THC4940 contains a high-performance output amplifier capable of driving loads of up to 90pF, which includes the capacitive loads of many flash converters, without the need for an additional buffer. For loads of greater than 90pF, the TRW THC4231 low gain, wide-band op-amp is recommended.

The THC4940 is a welcome addition to A/D conversion systems, especially those employing high-resolution sub-ranging architectures. Its use can improve both signal-to-noise ratio and full-power bandwidth of even the finest flash A/D conversion systems.

The device requires only ±15V power supplies and can accept either ECL or TTL control signals. The THC4940X2B has guaranteed performance over an industrial temperature range of −25°C to +85°C. The THC4940X2A has its performance guaranteed over the −55°C to +125°C case temperature range and is manufactured in facilities certified to MIL-STD-1772. Both versions are available in 24 pin ceramic DIPs.

Features

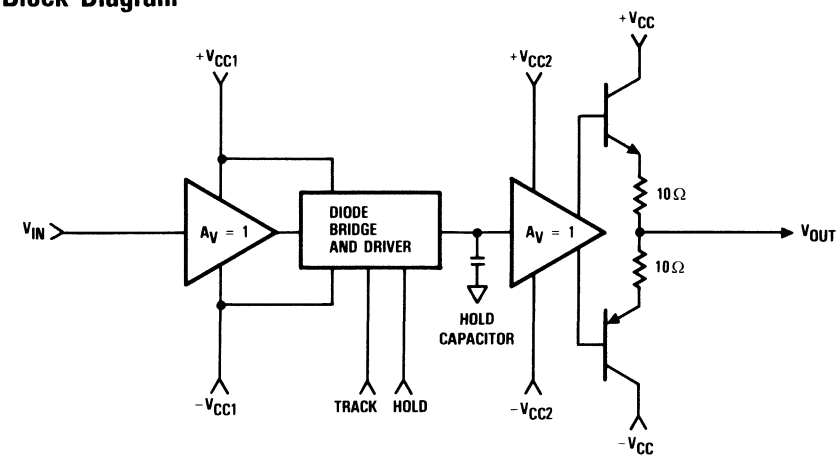
- 10ns Hold-To-Track Acquisition Time
- 12ns Track-To-Hold Settling Time
- 1ps Aperture Jitter
- 150MHz Small Signal Bandwidth
- 74dB Feedthrough Rejection @ 20MHz, V_{IN} = 2Vp-p
- ECL And TTL Compatible Control Signals
- Available In A 24 Pin Ceramic DIP

Applications

- Flash A/D Converter Front End
- High-Resolution, Sub-Ranging A/D Converter System Driving
- Signal De-Glitching For CCD And D/A Systems
- Communications Systems
- Radar And IF Processors

C

Functional Block Diagram

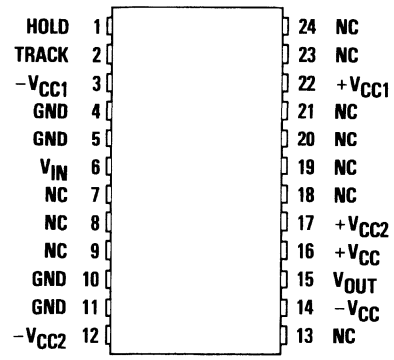


TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

40G05937 Rev. B−11/90
Printed in the U.S.A.

Pin Assignments



24 Pin Ceramic DIP – X2 Package

Functional Description

General Information

The THC4940 consists of an input buffer, diode bridge (which serves as a switch) and driver, hold capacitor and output buffer. In the TRACK mode, the diode bridge is turned on by its driver circuit and conducts the signal from the the input buffer to the output buffer. Since the output impedance of the input buffer is small compared to the impedance of the hold capacitor, the signal passes to the output without loss. This allows the voltage at the hold capacitor to track the input voltage.

When the HOLD command is given, the diode bridge is turned off by the driver circuit which puts the diode bridge into the high-impedance (open) state. This disconnects the input buffer from the hold capacitor and output buffer. In the HOLD mode the voltage seen by the output driver is the DC voltage present on the hold capacitor. Since the input impedance of the output buffer is very high, the loading on the hold capacitor is very small, so the hold capacitor discharges slowly. This maintains the output of the THC4940 at the level of the input when the HOLD command was given.

When the device is returned to the TRACK mode, the diode switch closes, allowing the input buffer to begin charging the hold capacitor to the input voltage which it will continue to track until the device is again switched to the HOLD mode.

Power

The THC4940 operates from three pairs of supply voltages. The supplies for the input buffer, output buffer driver and output transistors are brought out to separate pins so that they may be decoupled to allow high feedthrough rejection. They may all be driven from the same $\pm$15V supply as long as the pins are properly decoupled as shown in the *Typical Interface Circuit*. They may also be driven from supplies of different voltages if desired.

TRACK/HOLD Control

Switching between TRACK and HOLD is controlled by a differential pair input. When the voltage on TRACK (pin 2) is greater than the voltage on HOLD (pin 1), the THC4940 is in TRACK mode. Likewise, the device will be in HOLD mode when the voltage on HOLD (pin 1) is greater than the voltage on TRACK (pin 2). These inputs are compatible with most logic families and specific applications are covered in the *TRACK-HOLD Switching Control* section.

Analog Input

The analog input is buffered, providing a high input impedance of typically 20 kOhms in parallel with 3pF.

Analog Output

The analog output represents either the voltage at the input (TRACK mode), or the voltage at the input when the HOLD command was given (HOLD mode). It is buffered with a 10 Ohm output source impedance (at 1kHz), and can drive loads of up to 90pF with full performance.

No Connects

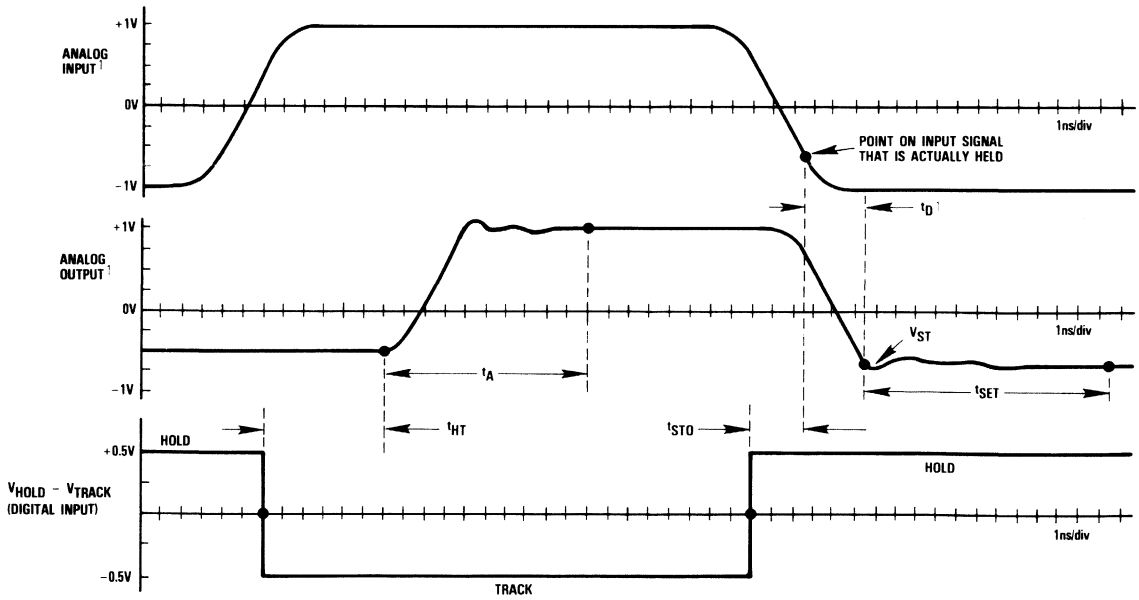
Several pins have no internal connections to the chip. These pins should be left open (disconnected).

Package Interconnections

Signal Type	Signal Name	Function	Value	X2 Package Pins
Power	$+V_{CC}$	Positive Supply Voltage	+15.0V	16
	$+V_{CC1}$	Positive Supply Voltage	+15.0V	22
	$+V_{CC2}$	Positive Supply Voltage	+15.0V	17
	$-V_{CC}$	Negative Supply Voltage	−15.0V	14
	$-V_{CC1}$	Negative Supply Voltage	−15.0V	3
	$-V_{CC2}$	Negative Supply Voltage	−15.0V	12
	GND	Ground	0.0V	4, 5, 10, 11
Controls	TRACK	HOLD/TRACK Control	TTL or ECL	2
	HOLD	HOLD/TRACK Control	TTL or ECL	1
Input	V_{IN}	Analog Input	−2.2 to 2.2V	6
Output	V_{OUT}	Analog Output	−2.2 to 2.2V	15
No Connect	NC	None		7, 8, 9, 13, 18, 19, 20, 21, 23, 24

C

Figure 1. Timing Diagram



Note: 1. There is an analog delay of about 3ns from the analog input to the analog output. (The input amplifier contributes 1ns and the output amplifier contributes 2ns.)

Definitions

Acquisition Time (t_A)

Acquisition Time (HOLD to TRACK) is the time required for the TRACK and HOLD to acquire the input signal (to a specific settling precision) when it switches modes from HOLD to TRACK. It is the time from when the output starts changing to when it has settled to a specified accuracy.

Analog Delay (t_D)

Analog Delay (input to output) is the time required for a signal to travel from the analog input to the analog output. It is typically 3ns for the THC4940.

Aperture Error (E_{AP})

Aperture Error (or aperture uncertainty or jitter) is the sample-to-sample variation in Effective Aperture Delay which is caused by a small amount of noise in the switch control circuitry. Aperture Jitter changes the time at which the device goes into HOLD mode. Aperture Jitter, coupled with the rate of change (slew rate) of the signal at the storage capacitor, causes an error in the held output voltage. (Output voltage error = $\Delta V/\Delta t \bullet \Delta t$, where $\Delta V/\Delta t$ is the slew rate and Δt is the aperture jitter.)

Droop Rate (DR)

Droop Rate is a drift in the held output voltage. It is caused by leakage currents flowing into (or out of) the storage capacitor from the switching circuit and input stage of the output amplifier.

Effective Aperture Delay (t_{STO})

Effective Aperture Delay tells when the input is actually sampled. It is the time from when the HOLD command is given to the point on the input waveform which is held. It does not include analog propagation through the output buffer to the output pin. It takes into account two delays: the input signal transit time through the input amplifier and the time needed for the switch to open after the part is given the HOLD command. Typically, the Effective Aperture Delay is 2.5ns which means the held voltage is that which was at the input pin 2.5ns after the HOLD command was given. (Conceivably, Effective Aperture Delay could be negative if the transit time through the input amplifier were longer than the delay in the switch, though this is not the case here.)

Feedthrough Rejection (FTR)

Feedthrough Rejection (or analog input isolation) is the measure of how well the switch keeps input signals from leaking through to the output in the HOLD mode. It is the ratio of the analog AC signal at the output to the signal at the input while in HOLD mode (switch open). Since the signal that feeds through is due in part to the capacitance of the switch, Feedthrough Rejection worsens with increasing analog input frequency. There are also switching transients which feed through from the digital inputs, however, these quickly settle out and are accounted for in the *Acquisition Time* and *TRACK-to-HOLD Settling Time* specifications.

HOLD-to-TRACK Switch Delay (t_{HT})

HOLD-to-TRACK Switch Delay is the time from when the TRACK input (pin 2) becomes more positive than the voltage on HOLD (pin 1) (the initiation of the TRACK command) to when the output starts to change as it begins to acquire the new signal. Typically it is 6ns for the THC4940.

Pedestal Offset (V_P)

Pedestal Offset (or TRACK-to-HOLD offset) is an output offset voltage found in the HOLD mode. It is caused by a small amount of charge being injected into or out of the storage capacitor when the (diode bridge) switch opens. In practice, this offset is treated the same as an output offset voltage. Unlike most other TRACK and HOLDs, the Pedestal Offset of the THC4940 is virtually unaffected by changes in the analog input voltage.

TRACK-to-HOLD Switching Transient (V_{ST})

TRACK-to-HOLD Switching Transient is the switch-induced transient voltage that appears at the output immediately after the THC4940 switches from TRACK to HOLD.

TRACK-to-HOLD Settling Time (t_{SET})

TRACK-to-HOLD Settling Time is the time required for the TRACK-to-HOLD Switching Transient to settle to within 1mV of its final value.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

(V_{CC}, V_{CC1}, V_{CC2})	+20V
($-V_{CC}$, $-V_{CC1}$, $-V_{CC2}$)	−20V

Input Voltages

V_{IN} (power applied)	±5V
(no power applied)	±3V
TRACK, HOLD (referenced to ground)	±(V_{CC1} − 9V)
(differential with respect to each other)	±3.5V

Output

Current from V_{OUT}	±50mA Continuous

Temperature

Operating, case	−65 to +130°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Reliability

Mean Time Between Failures [2]	1.6 x 10^6 Hours

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. A-grade, Ground Fixed environment @ T_C = 70°C, per MIL-HDBK-217E.

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Operating conditions

Parameter		Temperature Range: Industrial Min	Industrial Typ	Industrial Max	Extended Min	Extended Typ	Extended Max	Units
$+V_{CC}$, $+V_{CC1}$, $+V_{CC2}$	Supply Voltages	+14.25	+15.00	+15.75	+14.25	+15.00	+15.75	V
$-V_{CC}$, $-V_{CC1}$, $-V_{CC2}$	Supply Voltages	−14.25	−15.00	−15.75	−14.25	−15.00	−15.75	V
V_{IN}	Analog Input Voltage	−2.2		2.2	−2.2		2.2	V
V_{ID}	Digital Input Voltage		±(V_{CC1} − 11)			±(V_{CC1} − 11)		V
V_{IDF}	Digital Input Voltage, Differential $\lvert(V_{HOLD} - V_{TRACK})\rvert$	0.3		2.5	0.3		2.5	V
SR_D	Digital Input Slew Rate	20			20			V/μs
T_A	Ambient Temperature	−25		+85				°C
T_C	Case Temperature				−55		+125	°C

DC Electrical characteristics within specified operating conditions ($R_L = 100$ Ohms, $V_{CC} = \pm 15V$)

Parameter		Test Conditions	Temperature Range						Units
			Industrial			Extended			
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset Voltage			20	75		20	75	mV
TC_{VOS}	Offset Voltage, Tempco	End-Point Average		30	140		30	140	μV/°C
I_{IH}	Input Bias Current, Logic HIGH			25	100		25	100	μA
I_{IL}	Input Bias Current, Logic LOW			1	10		1	10	μA
R_{IN}	Analog Input Resistance		15	20		15	20		kOhms
C_{IN}	Analog Input Capacitance			3	4		3	4	pF
I_{IB}	Analog Input Bias Current			30	90		30	90	μA
PSRR	Power Supply Rejection Ratio		36	40		36	40		dB
I_{CC}	Supply Current	Note 1		55	65		55	65	mA
P_D	Power Dissipation	Note 1		1.65	1.95		1.65	1.95	W

Note: 1. $V_{IN} = 0$, TRACK mode, no load.

AC Electrical characteristics within specified operating conditions ($R_L = 100$ Ohms, $V_{CC} = \pm 15V$)

Parameter		Test Conditions	Temperature Range						Units
			Industrial			Extended			
			Min	Typ	Max	Min	Typ	Max	
TRACK Mode									
A_V	Gain	Note 2	0.96	0.98	1.00	0.96	0.98	1.00	V/V
TC_A	Gain Tempco	Note 2		20	30		20	30	ppm/°C
NL_A	Gain Non-Linearity	Note 2		0.02	0.025		0.02	0.025	%
R_{OUT}	Analog Output Resistance	1kHz		10	13		10	13	Ohms
SSBW	Small Signal Bandwidth [1]	−10dBm Input	100	150		100	150		MHz
SR	Slew Rate		390	470		390	470		V/μs
HD2	2nd Harmonic Distortion	Note 3	−47	−57		−47	−57		dBc
HD3	3rd Harmonic Distortion	Note 3	−54	−60		−54	−60		dBc
HOLD Mode									
DR	Droop Rate	$T_A = 25°C$			50			50	μV/μs
		$T_A = -20°C$ to $+85°C$		20	2000				μV/μs
		$T_C = -55°C$ to $+125°C$					20	2000	μV/μs
FTR	Feedthrough Rejection	20MHz, $V_{IN} = 2$Vp-p	70	74		70	74		dB

Notes: 1. −3dB bandwidth.
2. 1kHz, 4Vp-p, no load.
3. 2Vp-p, 20MHz, $R_L = 1$ kOhm.

Switching characteristics within specified operating conditions (R_L = 100 Ohms, V_{CC} = ±15V)

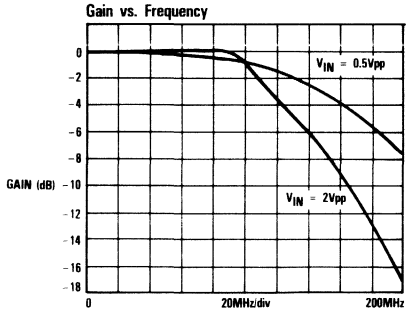
Parameter		Test Conditions	Temperature Range						Units
			Industrial			Extended			
			Min	Typ	Max	Min	Typ	Max	
TRACK-to-HOLD Switching									
t_{SET}	TRACK-to-HOLD Settling Time	To 1mV		12	18		12	18	ns
t_{STO}	Effective Aperture Delay			2.5	3.3		2.5	3.3	ns
E_{AP}	Aperture Error			1.0	1.6		1.0	1.6	ps_{rms}
V_P	Pedestal Offset			2	8		2	8	mV
TC_{VP}	Pedestal Offset, Tempco	End-Point Average		25	60		25	60	µV/°C
PORR	Sensitivity to Supply Voltage				0.5			0.5	mV/V
V_{ST}	Switching Transient	F_S = 2MHz		25	50		25	50	mVp-p
HOLD-to-TRACK Switching									
t_A	Acquisition Time	Note 1		10	15		10	15	ns
		Note 2		16	22		16	22	ns

Notes: 1. To 1.0%, V_{IN} = 2Vp-p, R_L = 1 kOhm
2. To 0.1%, V_{IN} = 2Vp-p, R_L = 1 kOhm

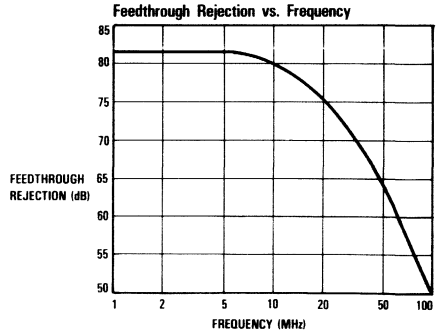
C

Typical Performance Curves (T_A = 25°C, R_L = 100 Ohms, V_{CC} = ±15V)

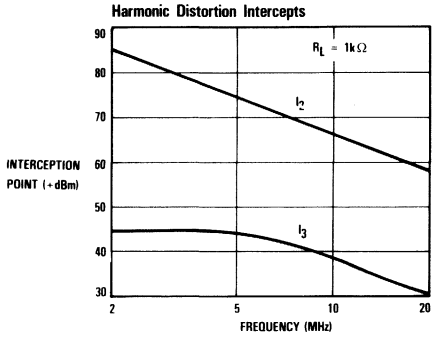
Gain vs. Frequency



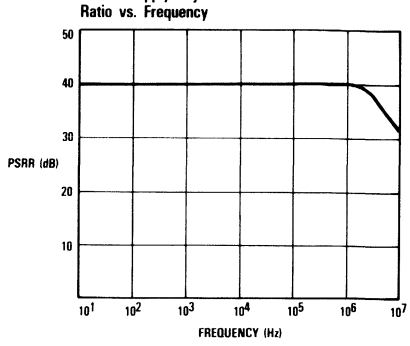
Feedthrough Rejection vs. Frequency



2nd and 3rd Harmonic Distortion Intercepts

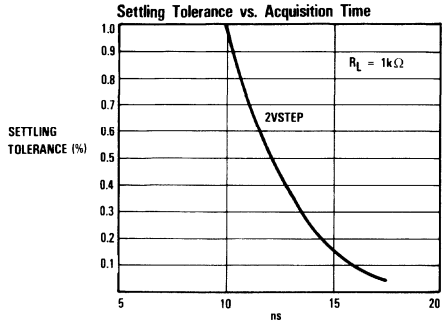


Power Supply Rejection Ratio vs. Frequency

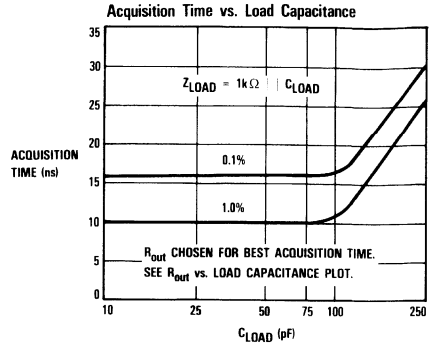


Typical Performance Curves (cont.)

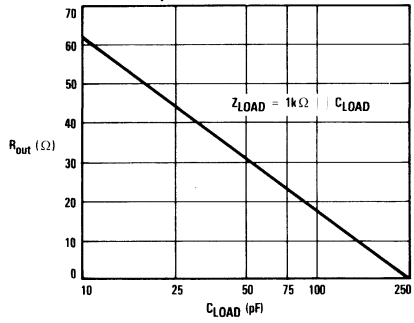
Settling Tolerance vs. Acquisition Time



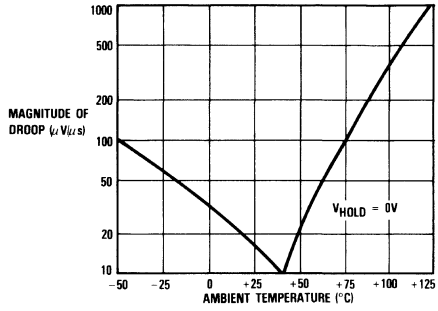
Acquisition Time vs. Load Capacitance



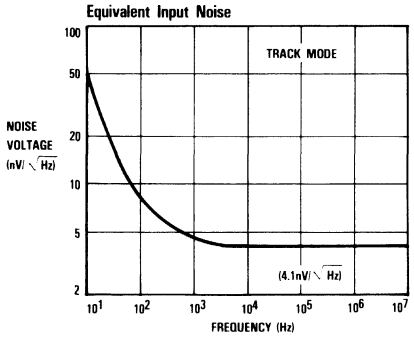
Recommended R_{out} vs. Load Capacitance



Droop Rate Magnitude vs. Temperature



Equivalent Input Noise



Switching Transients and Pedestal

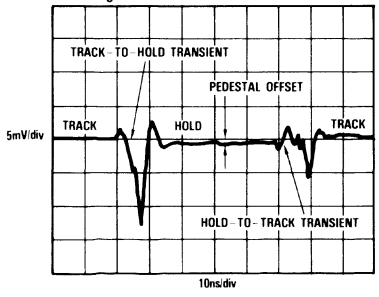
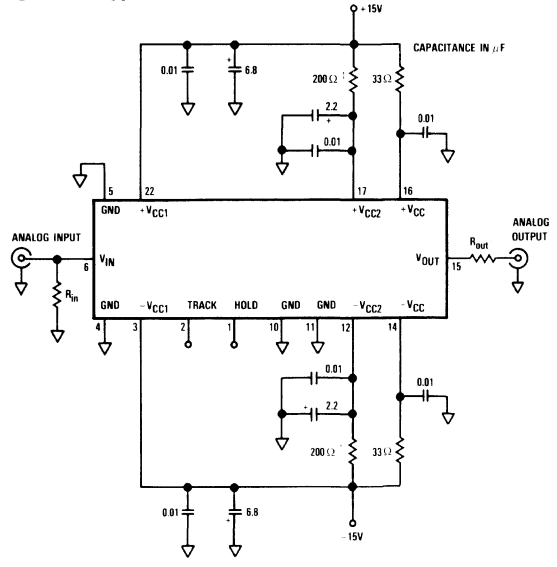


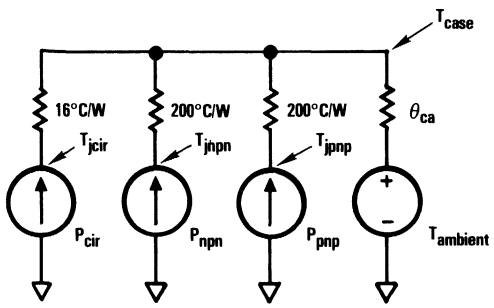
Figure 2. Typical Interface Circuit



Notes: 1. Use 20 or 33Ω when using ±12V supplies.

2. For capacitance loads See the R_{OUT} vs. Load Capacitance curve for the value of R_{OUT}.

Figure 3. Thermal Model



θ_{ca} = 23°C/W in still air without a heat sink. With heat sinking or air flow, θ_{ca} will be lower.

Thermal Model Calculations

$P_{cir} = I_{cc1}[+V_{cc1} - (-V_{cc1})] + I_{cc2}[V_{cc2} - (-V_{cc2})]$

I_{cc1} is the supply current to $\pm V_{cc1}$ (pins 22 and 3).

I_{cc2} is the supply current to $\pm V_{cc2}$ (pins 17 and 12).

Typical values are $\pm V_{cc1} = \pm 15V$, $I_{cc1} = 34mA$, $\pm V_{cc2} = \pm 12V$, $I_{cc2} = 15mA$.

So P_{cir} = (34mA)(30V) + (15mA)(24V) = 1.38W

$P_{XXX} = |\pm V_{cc} - V_{out}| \cdot I_{col}(R_{col} + 10)||I_{col}|$(% duty cycle that XXX is on)

P_{XXX} is the power in either the npn or pnp output transistor.

For $V_{out} > 0$, the power is in the npn and $\pm V_{cc} = +V_{cc}$.

For $V_{out} < 0$, the power is in the pnp and $\pm V_{cc} = -V_{cc}$.

$I_{col} = V_{out}/R_{load}$ or 4mA whichever is greater.

R_{col} is the external resistor between the XXX collector and $\pm V_{cc}$.

Example: $V_{out} = +1V$, 30% duty cycle

$V_{out} = -2V$, 70% duty cycle

$R_{col} = 33\Omega$, $R_{load} = 100\Omega$

$$P_{npn} = \left[15V - 1V - \left(\frac{1V}{100\Omega}\right)\left(33\Omega + 10\Omega\right)\right]\left(\frac{1V}{100\Omega}\right)\left(30\%\right) = 0.041W$$

$$P_{pnp} = \left[-15V - (-2V) - \left(\frac{-2V}{100\Omega}\right)\left(33\Omega + 10\Omega\right)\right]\left(\frac{-2V}{100\Omega}\right)\left(70\%\right) = 0.170W$$

$T_{case} = P_{total}\,\theta_{ca} + T_{ambient} = (P_{cir} + P_{npn} + P_{pnp})\,\theta_{ca} + T_{ambient}$

$T_{cir} = P_{cir}(16°C/W) + T_{case}$

$T_{jnpn} = P_{npn}(200°C/W) + T_{case}$

$T_{jpnp} = P_{pnp}(200°C/W) + T_{case}$

C

Layout Considerations

For optimum performance from any precision high-speed track-and-hold such as the TRW THC4940, a good printed circuit board layout is necessary. First, a ground return path must be provided for signal current loops. One such loop is formed between the signal source and the termination resistor at the analog input of the track-and-hold. Another is formed between the source of the digital sample command and the termination resistors at the digital inputs of the track-and-hold. In the third such loop, current from the power supplies flows through the track-and-hold output amplifier to the load and then through ground return and supply decoupling capacitors to the power supply. Ideally, the input, output, and digital input signals should be transmitted via properly-terminated controlled-impedance transmission lines, such as microstrip or stripline, which work very well on standard printed circuit boards. When a capacitive or high-impedance load makes transmission lines unattractive, be sure to keep the load within an inch or so of the track-and-hold output and provide a wide strip of ground plane for the signal current to return to the decoupling capacitors.

In addition, make certain that the ground return paths mentioned above do not cross over themselves or any other ground return on the printed circuit board. Otherwise these various signals will couple to each other and degrade the precision of the track and hold. For example, to maintain the feedthrough rejection specification, the ground connections of the decoupling capacitors should be kept at least one-quarter inch away from the signal terminations such as the ground side of R_{in}.

The stray reactance of the decoupling capacitors and termination resistors must also be kept low. Surface-mounted multi-layer 0.01μF capacitors are recommended for use right at the power supply pins of the TRW THC4940. Radial lead capacitors may only be used if they are low-loss types with very short leads.

Sockets are not recommended, however some low-profile "bucket"-type sockets work well. Wire wrap methods and boards will severely degrade overall performance and are not recommended.

Input Considerations

The input should be driven from a low impedance source not exceeding 100 Ohms, such as the output of an amplifier or a terminated 50 Ohm transmission line.

TRACK – HOLD Switching Control

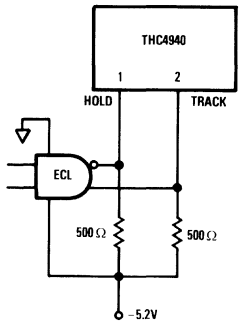
The switch in the THC4940 is controlled by a differential pair input. The device will be in TRACK mode when the voltage on TRACK (pin 2) is greater than the voltage on HOLD (pin 1). Similarly, it will be in HOLD mode when

TRACK – HOLD Switching Control (cont.)

the voltage on HOLD is greater than the voltage on TRACK. The best switching action is realized when the slew rate of the digital input is at least 20V/μs and when the differential signal excursion is no less then 300mV. In addition, it is recommended that the differential voltage on these pins not exceed $\pm$2.5V while the absolute voltage on either pin should not exceed ($|V_{CC1}| - 11V$). This voltage range accommodates most logic families.

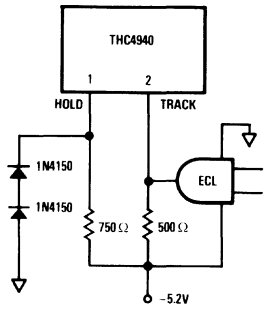
Differential ECL signals may be fed directly to the digital control inputs, each of which represents less than one ECL 10k load. In *Figure 4*, the THC4940 is in TRACK mode when the non-inverting ECL output is HIGH.

Figure 4. Differential ECL Control



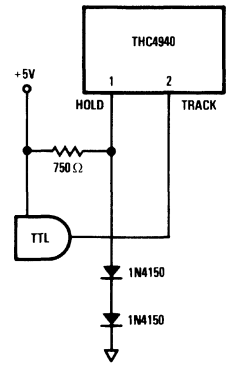
A single-ended ECL signal can be fed directly into one of the digital inputs while the other pin is biased at -1.4V to accommodate ECL voltage levels. In *Figure 5*, the THC4940 is in TRACK mode when the ECL output is HIGH.

Figure 5. Single-Ended ECL Control



For totem-pole-output TTL, a similar connection scheme is used but with a bias voltage of +1.4V. The digital input represents about 5 LS TTL loads at a HIGH level. In *Figure 6*, the THC4940 is in TRACK mode when the TTL output is HIGH.

Figure 6. TTL Control



Driving Capacitive Loads

In order to maintain performance while driving capacitive loads, a small-value resistor should be placed between the THC4940 and the load. The optimum value of resistance should be selected from the plot of *R_{out} vs. Load Capacitance*. For this combination, acquisition time is shown on the *Acquisition Time vs. Load Capacitance* plot. (If the load capacitance is variable, as it is with some flash A/D converters, the average typical capacitance should be used.)

Lower Power Operation

The power dissipation in the output stage transistors may be decreased slightly by reducing the output stage supply voltages ($+V_{CC}$, $-V_{CC}$) to as low as $\pm$5V. This only minimally affects performance while substantially reducing output transistor junction temperatures. See *Figure 3* for further details.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
THC4940X2B	IND–T_A = –25°C to 85°C	Industrial	24 Pin Ceramic DIP	4940X2B
THC4940X2A	EXT–T_C = –55°C to 125°C	High Reliability	24 Pin Ceramic DIP	4940X2A

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C

Signal Synthesis

Direct Digital Frequency Synthesis (DDFS) offers signal flexibility and stability that is unattainable with analog techniques. DDFS is the process whereby the digital samples representing a desired analog signal are computed. These samples are then fed to a D/A converter for the construction of the analog signal. The TMC2340 produces data representing baseband signals up to 12.5MHz (higher with aliasing or multiplexing techniques) with a 0.006Hz frequency resolution and can change frequencies cleanly in 25ns. It produces a pair of 16-bit quadrature outputs.

The synthesizer can produce Frequency Modulation (FM) or Phase Modulation (PM) simultaneously with Amplitude Modulation (AM). It is carefully designed to drive the TDC1012 signal synthesis D/A converter, to create the lowest-distortion digital synthesizer subsystem available today.

Signal Synthesis

Product	Clock Rate [1] (MHz)	Frequency Resolution (Hz)	SFDR (dB)	Output	Package		Grade [2]	Notes	Page
Digital Frequency Synthesizers									
TMC2340-1	25	0.006	106	Dual 16-Bit	H5	120 Pin PPGA	C	AM, FM, PM Inputs.	D3
					L5	132 Lead CERQUAD	V	Quadrature Outputs.	
	20	0.006	106	Dual 16-Bit	H5	120 Pin PPGA	C		
					L5	132 Lead CERQUAD	V		

Product	Resolution Bits	Differential Linearity Error [1] (± %)	Conv Rate [1] (Msps)	Rise Time [1] (ns)	Package		Grade [2]	Notes	Page
Associated D/A Converters									
TDC1041-1	10	0.048	20	4	R3	28 Lead PLCC	C	Low Cost 10-Bit Video D/A	B75
	10	0.096	20	4	R3	28 Lead PLCC	C	TTL Interface.	
TDC1141-1	10	0.048	50	4	R3	28 Lead PLCC	C	Low Cost 10-Bit Video D/A	B105
	10	0.096	50	4	R3	28 Lead PLCC	C	ECL Interface.	
TDC1012-3	12	0.012	20	4	J7, N7	24 Pin DIP	C	Signal Synthesis D/A.	B23
					R3	28 Lead PLCC	C	70dBc SFDR. Very Low Glitch.	
-2	12	0.024	20	4	J7, N7	24 Pin DIP	C, V, SMD	Drives 25Ω Directly.	
					R3	28 Lead PLCC	C	TTL Interface.	
-1	12	0.048	20	4	J7, N7	24 Pin DIP	C, V, SMD		
					R3	28 Lead PLCC	C		
	12	0.048	20	4	J7, N7	24 Pin DIP	C, V, SMD		
					R3	28 Lead PLCC	C		
TDC1112-3	12	0.012	50	4	J7, N7	24 Pin DIP	C	Signal Synthesis D/A.	B87
					R3	28 Lead PLCC	C	70dBc SFDR. Very Low Glitch.	
-2	12	0.024	50	4	J7, N7	24 Pin DIP	C, V	Drives 25Ω Directly.	
					R3	28 Lead PLCC	C	ECL Interface.	
-1	12	0.048	50	4	J7, N7	24 Pin DIP	C, V		
					R3	28 Lead PLCC	C		
	12	0.048	50	4	J7, N7	24 Pin DIP	C, V		
					R3	28 Lead PLCC	C		

Notes: 1. Guaranteed. See product specifications for test conditions.

2. A = High Reliability, $T_C = -55°C$ to $125°C$.
B = Industrial, $T_C = -25°C$ to $85°C$.
C = Commercial, $T_A = 0°C$ to $70°C$.
V = MIL-STD-883 Compliant, $T_C = -55°C$ to $125°C$.
SMD = Available per Standardized Military Drawing, $T_C = -55°C$ to $125°C$.

TMC2340

Digital Synthesizer
Dual 16-Bit, 25MOPS

The TMC2340 performs waveform synthesis, modulation, and demodulation. When presented with a TTL clock signal and user-selected 15-bit amplitude and 32-bit phase increment values, the TMC2340 automatically generates quadrature-matched pairs of 16-bit sine and cosine waves in DAC-compatible 16-bit offset binary format. If desired, these waveforms are easily phase or frequency-modulated on-chip, and the amplitude input facilitates gain adjustment or amplitude modulation. Digital output frequencies are restricted only by the Nyquist limit of clock rate/2, with frequency resolution of 0.006Hz at the guaranteed maximum 25MHz clock rate.

A new data word pair is available at the output every clock cycle. All input and output data ports are registered, with a user-configurable phase accumulator structure and input clock enables to simplify interfacing. The phase data range over a full 2π radians. All signals are TTL compatible.

Fabricated in TRW's OMICRON-C™ one-micron CMOS process, the TMC2340 operates at the 25MHz maximum clock rate over the full commercial temperature (0 to 70°C) and supply (4.75V to 5.25V) voltage ranges, and is available in a low-cost 120 pin plastic pin grid array. The MIL-STD-883 version, the TMC2340L5V, is housed in a ceramic chip crarier and is specified over the full extended (−55°C to 125°C) case temperature range.

Features

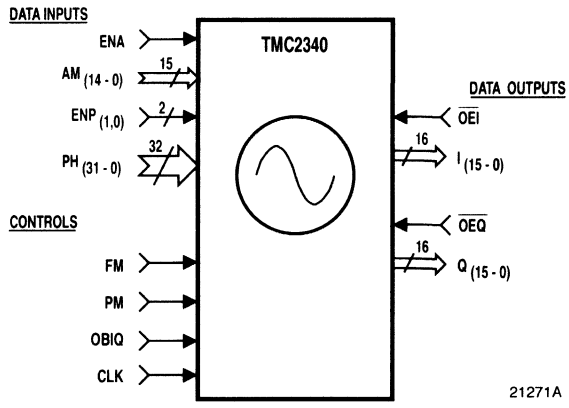
- User-Configurable Phase Accumulator For Waveform Synthesis, Frequency Modulation Or Phase Modulation
- Amplitude Input For Gain Adjustment And Amplitude Modulation
- Guaranteed 25Msps Pipelined Data Throughput Rate
- 15-Bit Magnitude, 32-Bit Phase Data Input Precision
- 16-Bit Offset Binary Or 15-Bit Unsigned Magnitude Output Data Format
- Input Register Clock Enables Simplify Interfacing
- Low Power Consumption CMOS Process
- Single +5V Power Supply
- Available In A 120 Pin Plastic Pin Grid Array Package
- Compliant With MIL-STD-883B In A 132 Leaded CERQUAD

D

Applications

- Digital Waveform Synthesis, Including Quadrature Functions
- Digital Modulation And Demodulation

TMC2340 Logic Symbol



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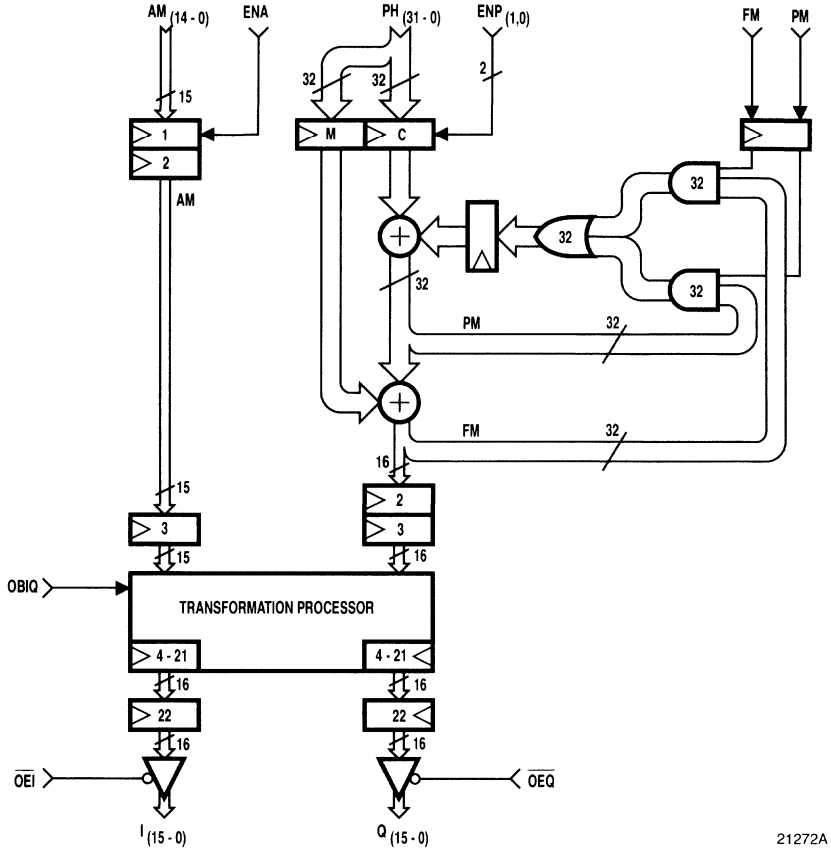
Printed in the U.S.A.

Functional Block Diagram



Functional Description

General Information

The TMC2340 converts Polar (Phase and Magnitude) data into Rectangular (Cartesian) format. The first transformed result is available at the outputs 22 clock cycles after startup, with new output data available every 40ns. All input and output data ports are registered, with input clock enables to simplify system bus connections.

The input ports accept 15-bit amplitude and 32-bit phase data, and the output ports produce 16-bit Rectangular data words in either 16-bit offset binary or 15-bit unsigned magnitude format. The 32-bit phase accumulator handles high-accuracy (0.006Hz at the maximum clock rate) phase increment values with minimal accumulation error. The flexible input phase accumulator structure supports frequency or phase modulation, as determined by the input register clock enable $ENYP_{1,0}$ and accumulator controls FM and PM. The 16 MSBs (Most Significant Bits) of phase data are used in the transformation itself.

Signal Definitions

Power

V_{DD}, GND — The TMC2340 operates from a single +5V supply. All power and ground pins must be connected.

Clock

CLK — The TMC2340 operates from a single clock. All enabled registers are strobed on the rising edge of CLK, which is the reference for all timing specifications.

Inputs/Outputs

AM_{14-0} — AM_{14-0} is the registered peak amplitude 15-bit input data port. AM_{14} is the MSB.

PH_{31-0} — PH_{31-0} is the registered Phase angle increment 32-bit input data port. The input phase accumulators are fed through this port in conjunction with the input enable select $ENP_{1,\ 0}$. PH_{31} is the MSB.

I_{15-0} — I_{15-0} is the registered X-coordinate 16-bit output data port. This output is forced into the high-impedance state when $\overline{OEI}$ = HIGH. I_0 is the LSB. I_{15} will be "stuck at" logic HIGH if OBIQ = 0.

Q_{15-0} — Q_{15-0} is the registered Cartesian Y-coordinate 16-bit output data port. This output is forced to the high-impedance state when $\overline{OEQ}$ = HIGH. Q_0 is the LSB. Q_{15} will remain at logic HIGH if OBIQ = 0.

Controls

ENA — Data presented to the input port AM are latched into the input registers on the current clock when ENA is HIGH. When ENA is LOW, the data stored in the register remains unchanged.

$ENP_{1,\ 0}$ — The value presented to the PH input port is latched into the phase accumulator input registers on the current clock, as determined by the control inputs $ENP_{1,\ 0}$, as shown below:

$ENP_{1,0}$	Instruction
00	No registers enabled, current data held
01	M register input enabled, C data held
10	C register input enabled, M data held
11	M register set to 0, C register input enabled

where C is the Carrier register and M is the Modulation register, and 0 = LOW, 1 = HIGH. See the *Functional Block Diagram*.

FM, PM — The user determines the internal phase Accumulator structure implemented on the next clock by setting the accumulator control word FM, PM, as shown below:

FM, PM	Instruction
00	No accumulation performed
01	PM accumulator path enabled
10	FM accumulator path enabled
11	(Nonsensical) logical OR of PM and FM

where 0 = LOW, 1 = HIGH. See the *Functional Block Diagram*.

The accumulator will roll over correctly when full-scale is exceeded, allowing the user to perform continuous phase accumulation through 2π radians, or 360 degrees.

OBIQ — The format select control sets the numeric format of the Rectangular data: offset binary format when HIGH, and unsigned when LOW. This is a static input. See the *Timing Diagram*.

$\overline{OEI}$, $\overline{OEQ}$ — Data in the output registers are available at the outputs of the device when the respective asynchronous Output Enables are LOW. When $\overline{OEX}$ or $\overline{OEY}$ is HIGH, the respective output port is in the high-impedance state.

D

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins	L5 Package Pins
Power	V_{DD}	Supply Voltage	C3, E3, H3, L4, L6, L8, L11, F11, E11, C11, C8, C6	1, 9, 21, 37, 45, 53, 67, 87, 91, 99, 112, 120
	GND	Ground	D3, E2, E1, F2, G3, K3, L3, L7, K11, J11, G11, F12, E12, D11, C10, C9, B7, C7, C5, C4	5, 11, 12, 14, 17, 29, 33, 49, 75, 83, 86, 89, 95, 104, 108, 115, 116, 124, 129
Clock	CLK	System Clock	F3	13
Inputs	AM_{14-0}	Radius Data	F13, G13, G12, H13, H12, H11, J13, J12, K13, K12, L13, L12, M13, M12, N13	85, 84, 82, 81, 80, 79, 78, 77, 76, 74, 73, 71, 69, 68, 66
	PH_{31-0}	Phase Data	L10, N12, N11, M10, L9, N10, M9, N9, M8, N8, N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, N2, M2, N1, L2, M1, L1, K2, J3, K1, J2, J1	61, 60, 59, 58, 57, 56, 55, 54, 52, 51, 50, 48, 47, 46, 44, 43, 42, 41, 40, 39, 38, 36, 34, 31, 30, 28, 27, 26, 25, 24, 23, 22
Outputs	I_{15-0}	I Data	D13, D12, C13, B13, C12, A13, B12, A12, B11, A11, B10, A10, B9, A9, B8, A8	90, 92, 93, 94, 96, 97, 100, 102, 105, 106, 107, 109, 110, 111, 113, 114
	Q_{15-0}	Q Data	A7, A6, B6, A5, B5, A4, B4, A3, A2, B3, A1, B2, B1, C2, C1, D2	117, 118, 119, 121, 122, 123, 125, 126, 127, 130, 132, 3, 4, 6, 7, 8
Controls	ENR	Radius In Enable	M11	63
	$ENP_{1,0}$	Phase In Enable	G1, G2	18, 16
	FM, PM	Modulation	H2, H1	29, 19
	OBIQ	Cartesian Data Format	F1	15
	$\overline{OEI}$	I Out Enable	E13	88
	$\overline{OEQ}$	Q Out Enable	D1	10
No Connect	NC	No Connect Pins	–	2, 32, 35, 62, 64, 65, 72, 98, 101, 103, 128, 131
		Index Pin	D4	–

Static Control Input

OBIQ determines the numeric format of the output data: offset binary if HIGH and unsigned magnitude if LOW. This control acts with 2-cycle latency on the chip's 22-cycle data path and is normally hardwired to a system-specific state. exclusive OR of PH_{31} and PH_{30} as a sign bit to the corresponding I_{14-0}.

Table 1. Data Input/Output Formats – Integer Format

Port	OBIQ	Bit # 31	30	29	. . .	16	15	14	. . .	0	Format
AM	X							2^{14}	. . .	2^{0}.	U
PH	X	$\pm 2^{0}$	2^{-1}	2^{-2}	. . .	2^{-15}	2^{-16}	2^{-17}	. . .	2^{-31} ($\times\pi$)	T/U
I	0							2^{14}	. . .	2^{0}.	U
I	1						2^{15}	2^{14}	. . .	2^{0}.	B
Q	0							2^{14}	. . .	2^{0}.	U
Q	1						2^{15}	2^{14}	. . .	2^{0}.	B

Notes:

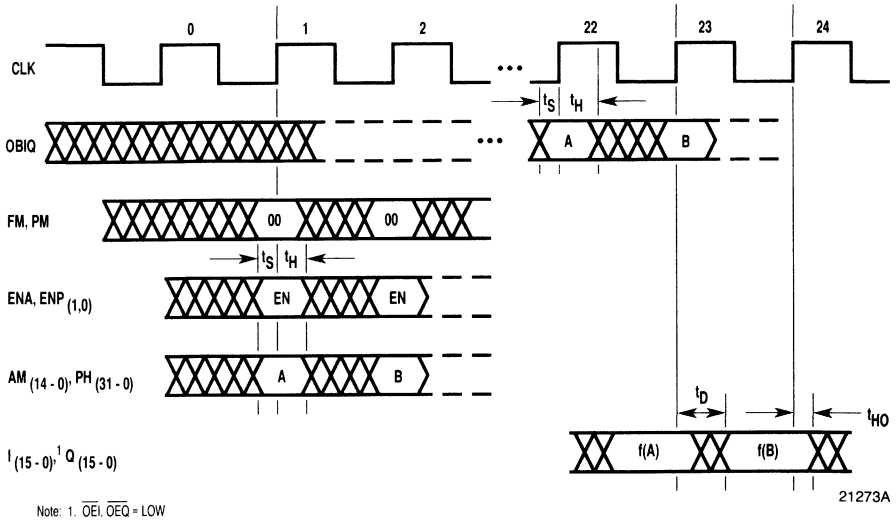
1. $\pm 2^{0}$ denotes two's complement sign or highest magnitude bit - since phase angles are modulo 2π and phase accumulator is modulo 2^{32}, this bit may be regarded as $\pm\pi$.
2. All phase angles are in terms of π radians, hence notation "$\times\pi$."
3. A sign-and-magnitude "Q" output is obtained by appending the input bit PH_{31} as a sign bit to the corresponding (i.e., delayed 22 cycles) $Q_{14:0}$.
4. A sign-and-magnitude "I" output is obtained by appending the exclusive OR of PH_{31} as a sign bit to the corresponding $I_{14:0}$.
5. When OBIQ = 0, outputs I_{15} and Q_{15} become "do not connects" and will stay logic HIGH. (They may be wired to V_{DD}, left open, or connected to any logic input without damage to the part or excessive power consumption.)
6. Formats:

T/U = Two's Complement/Unsigned Magnitude 32 Bits
U = Unsigned Magnitude 15 Bits
B = Offset Binary 16 Bits

AM, I, Q			PH	
HEX	U	B	T	U
FFFF		32767	$-\pi \cdot 2^{-15}$	$\pi(2-2^{-15})$
– –	– –	– –		
8001		1	$-\pi(1-2^{-15})$	$\pi(1+2^{-15})$
8000		0	$-\pi$	π
7FFF	32767	–1	$\pi(1-2^{-15})$	$\pi(1-2^{-15})$
– –	– –	– –		
0001	1	–32767	$\pi \cdot 2^{-15}$	$\pi \cdot 2^{-15}$
0000	0	–32768	0	0

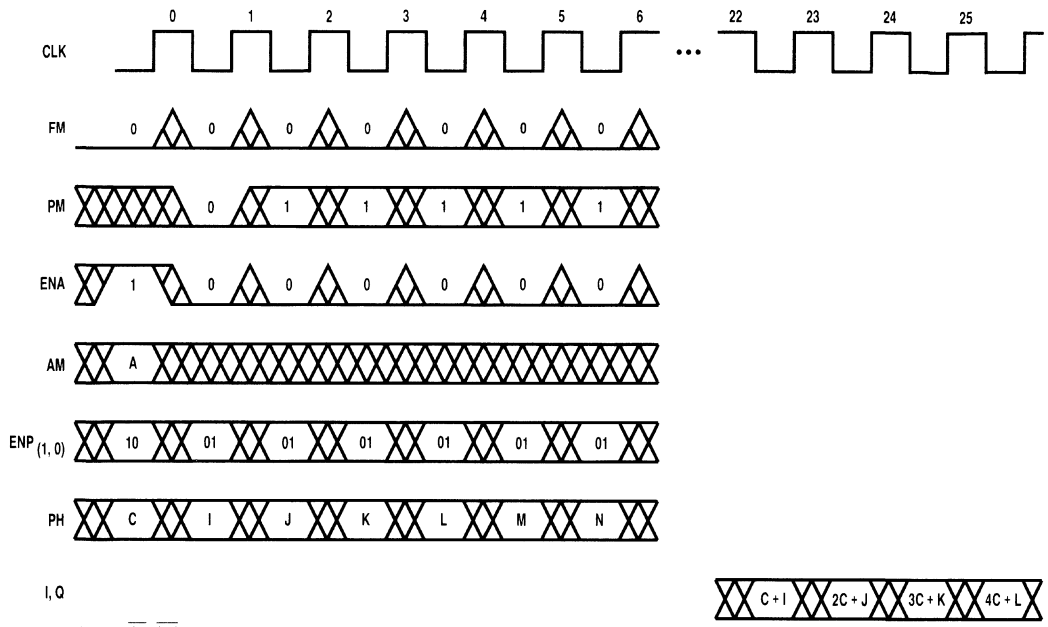
"Hex" column contains the 16 MSBs of the 32-bit phase input (16 LSBs are 0), the 15 bits of the amplitude input or the 16 bits of the offset binary output.

Figure 1. Timing Diagram, Operating Conditions



Note: 1. $\overline{OEI}$, $\overline{OEQ}$ = LOW

Figure 2. Timing Diagram, Phase Modulation



Notes: 1. $\overline{OEI}$, $\overline{OEQ}$ = LOW.
2. Carrier C and peak amplitude A loaded on CLK 0.
3. Modulation values I, J, K, L, . . . loaded on CLK 1, CLK 2, etc.
4. Output corresponding to modulation loaded at CLK i emerged t_{DO} after CLK i + 21.
5. To modulate amplitude, vary AM with ENA = 1.

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Figure 3. Equivalent Input Circuit

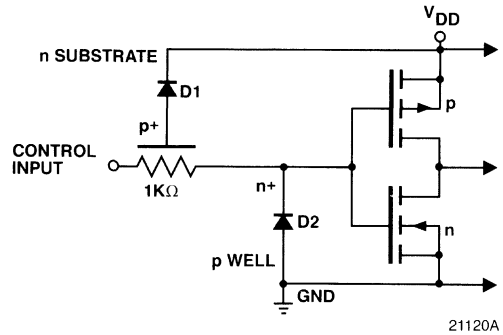

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Figure 4. Equivalent Output Circuit

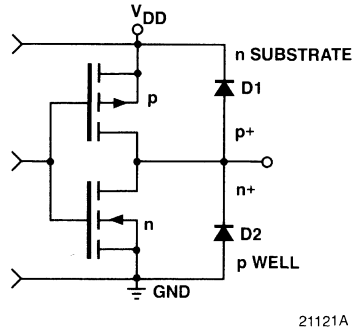

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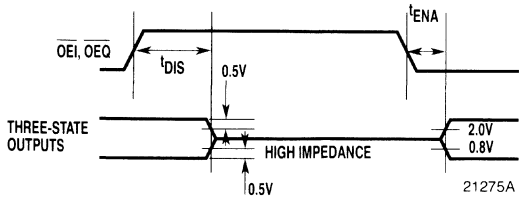
Figure 5. Transition Levels for Three-State Measurements



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Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD} + 0.5)V

Output Voltage

Applied voltage ..... −0.5 to (V_{DD} + 0.5)V [2]

Forced current ..... −6.0 to 6.0mA [3,4]

Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −60 to +130°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

D

Operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
V_{DD}	Supply Voltage		4.75	5.25	4.5	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8		0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0		2.0		V
I_{OL}	Output Current, Logic LOW			8.0		8.0	mA
I_{OH}	Output Current, Logic HIGH			−4.0		−4.0	mA
t_{CY}	Cycle Time	V_{DD} = Min	50			55	ns
		TMC2340-1	40			45	ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD} = Min	10			11	ns
		TMC2340-1	8			8	ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD} = Min	8			8	ns
		TMC2340-1	6			6	ns
t_S	Input Setup Time		12			13	ns
		TMC2340-1	10			11	ns
t_H	Input Hold Time		1			2	ns
		TMC2340-1	1			2	ns
T_A	Ambient Temperature, Still Air		0	70			°C
T_C	Case Temperature				−55	125	°C

Electrical characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		10		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz $\overline{OEI}$ and $\overline{OEQ}$ = V_{DD}		160		160	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		−10		−10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		−40		−40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.	−20	−100	−20	−100	μA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but specified operation is guaranteed.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		22		25	ns
		TMC2340-1		20		23	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF		4		4	ns
		TMC2340-1		4		4	ns
t_{ENA}	Output Enable Delay	V_{DD} = Min, C_{LOAD} = 40pF		13		17	ns
		TMC2340-1		12		15	ns
t_{DIS}	Output Disable Delay	V_{DD} = Min, C_{LOAD} = 40pF		14		14	ns
		TMC2340-1		13		13	ns

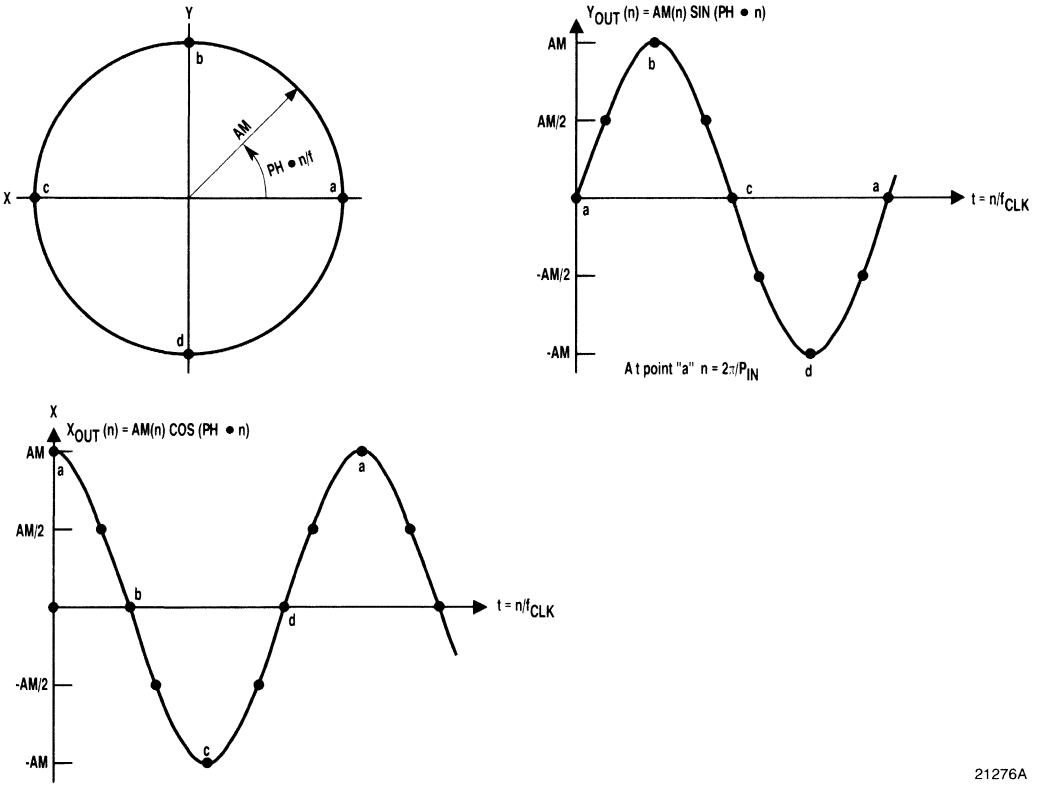
Phase/Amplitude to Sine/Cosine Conversion Geometry

Polar-To-Rectangular Conversion Geometry

The TMC2340 performs a coordinate-space transformation according to the familiar trigonometic relationships shown in *Figure 6*.

With constant amplitude and phase increment values and either FM or PM HIGH, the TMC2340 will output a series of complex number pairs representing the horizontal and vertical projections of a vector rotating about the origin, i.e., a cosine wave and a sine wave.

Figure 6. Input to Output Relationship for Sinusoid Generation



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Digital Waveform Synthesis

Waveform Generation and Modulation

Utilizing the internal phase accumlators in a TMC2340, users can easily generate high-accuracy digital quadrature sinusoidal waveforms with minimal support. The 32-bit data path ensures negligible cumulative error in most applications, and the accuracy of the transform is limited only by the truncation of the result to 16 bits prior to the Transform Processor and the ± 1 LSB maximum error of the transform algorithm. Amplitude Modulation is of course performed simply by varying the amplitude input. Either Frequency (phase angle shifted by the cumulative sum of the modulation input) or Phase (phase angle shifted by the instantaneous modulation input) Modulation can be realized by configuring the TMC2340 as shown in *Figures 7 and 8*.

In *Figure 7*, the output valid during clock rising edge $m+22$ is:

$$I_{m+22} = AM_m \cos(PH_m + mPC)$$
$$Q_{m+22} = AM_m \sin(PH_m + mPC)$$

where PH_m and AM_m are the chip inputs at rising edge m, PC is the (constant) carrier phase increment, $PM_1 = 0$, $PM_{2,...m} = 1$, and $FM_{1-m} = 0$.

Expressed in terms of time instead of clock cycles,

$$I_{(m+22)/f_{clk}} = AM_{m/f_{clk}} \cos(PH_{m/f_{clk}})$$

where f_{clk} is the frequency of the square wave applied to CLK.

Figure 7. Performing Phase Modulation

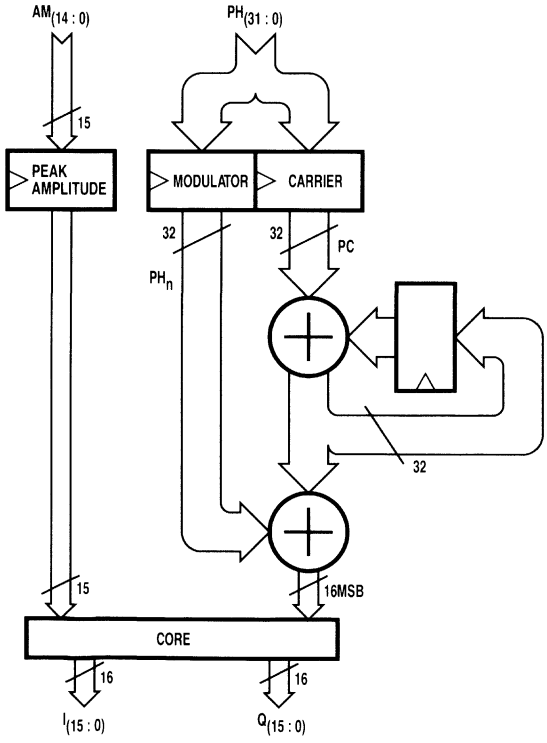

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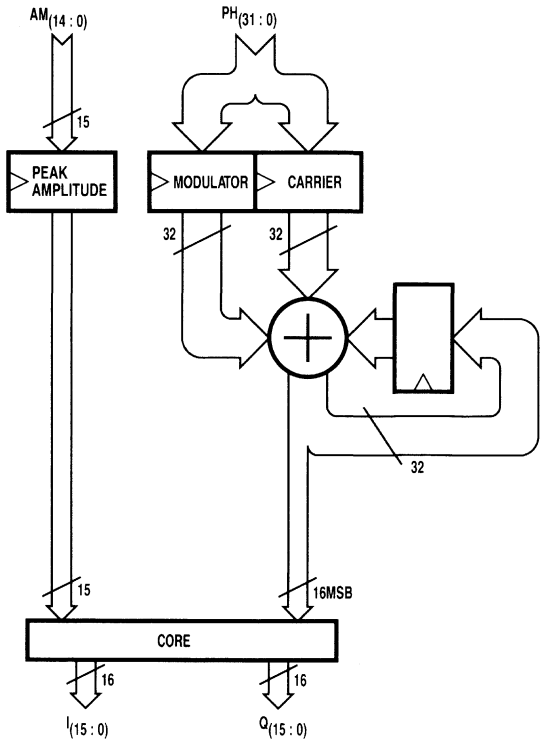
Figure 8. Performing Frequency Modulation



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In *Figure 8*, the output valid during clock rising edge n+22 is:

$$I_{m+22} = AM_m \cos\left(\sum_{m=1}^{n} PH_m + nPC\right)$$

$$Q_{n+22} = AM_m \sin\left(\sum_{m=1}^{n} PH_m + nPC\right)$$

where PH_m and AM_m are the chip inputs at rising edge AM, PC is the (constant) carrier phase increment, $FM_1 = 0$, $FM_{2...n} = 1$, and $PM = 0$.

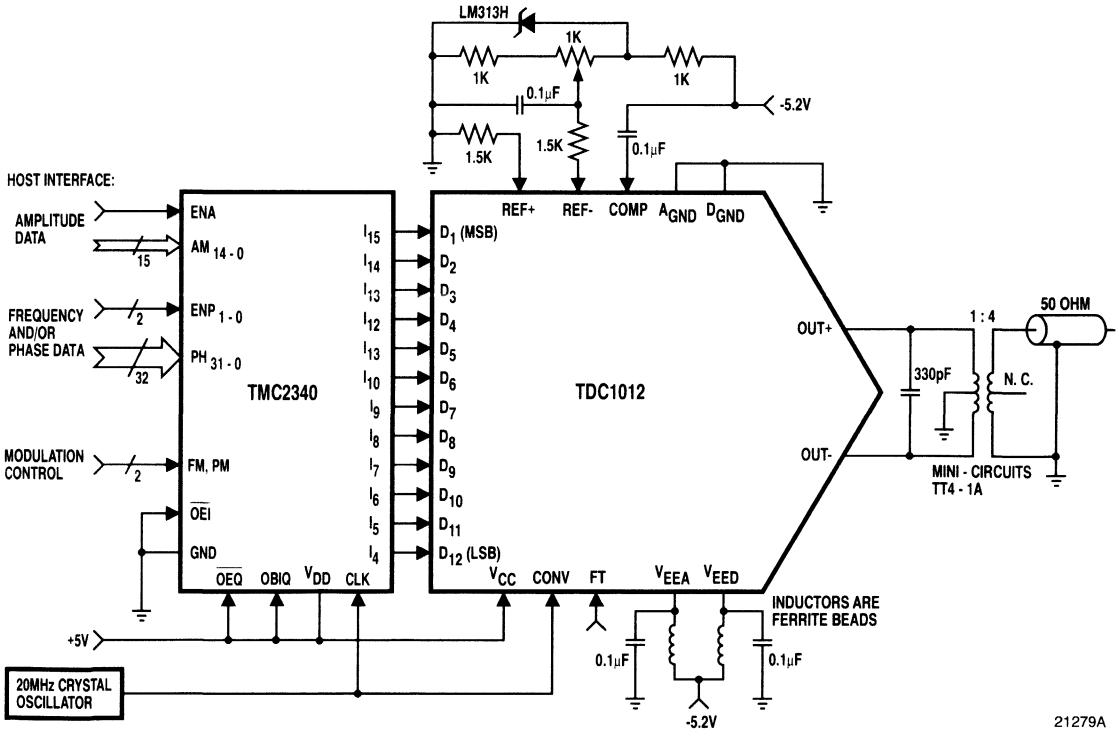
Expressed in terms of time instead of clock cycles,

$$I_{(n+22)/fclk} = AM_{m/fclk} \cos\left(\sum_{m-1}^{n} PH_{m/fclk} + PC \bullet m/fclk\right)$$

Digital Synthesizer with TDC1012 D/A Converter

Connection of the TMC2340 to the TDC1012 D/A converter is straightforward. As shown in *Figure 9*, the TDC1012 data lines are connected to either the I or Q outputs. Both outputs may be used, with two TDC1012's for quadrature synthesis.

Figure 9. Frequency Synthesizer



Note: To use two TDC1012's in quadrature, connect second TDC1012 to Q_{15} (MSB) to Q_4 and ground $\overline{OEQ}$.

Control of the TMC2340

The TMC2340 needs to be initialized to tell it what frequency and amplitude sinusoid to generate. To initialize amplitude, apply the desired full-scale amplitude to the AM input port of the TMC2340 (AM_{14} through AM_0) and pull ENA HIGH for one clock cycle. This will load the amplitude. If ENA is held HIGH, then the amplitude will follow the inputs on the AM port. If the user assumes an implied binary point before the MSB of the AM port, the input range will be 0 to just under 1, and the outputs will fall between 0 and 2, with binary points after I_{15} and Q_{15}.

To set the frequency, the C register must be loaded with a value which is the phase increment per clock cycle. If the binary point is considered to be just left of the MSB (input range is 0 to almost 1) then the output frequency is the TMC2340 clock frequency multiplied by the number loaded into C. Since C is 32 bits wide, with a 20MHz clock, one LSB represents a frequency increment of 0.005Hz.

To load the C register, set $ENYP_1 = 1$ and $ENYP_0 = 0$; the data presented at the PH port will be loaded on the next clock rising edge.

At this point the TMC2340 has been initialized and can be put into one of three modes depending upon the states of FM and PM:

Mode 0 FM = 0, PM = 0
In this mode the chip is in standby. The unchanging output corresponds to AM cos(PM) on the I outputs with PM being the phase increment.

Mode 1 FM = 1, PM = 0
Frequency Modulation Mode. The chip generates an output signal of peak amplitude AM and frequency determined by accumulating the sum of the phase increment values in the C and M registers (more about the M register in a later section).

Mode 2 FM = 0, PM = 1
Phase Modulation Mode. The TMC2340 generates a sinusoid of the frequency represented in the C register and the peak amplitude in the AM register. On each clock cycle, the phase of the signal is offset by the value in the M register.

Modulation

The output of the TMC2340 can be phase (Mode 2) or frequency (Mode 1) modulated. An unmodulated sinusoid results if the contents of registers C and M are held constant. Its frequency is set by C (Mode 2) or C + M (Mode 1). Since the state of the M register is not defined at power up, the M register should be loaded or cleared to begin operation.

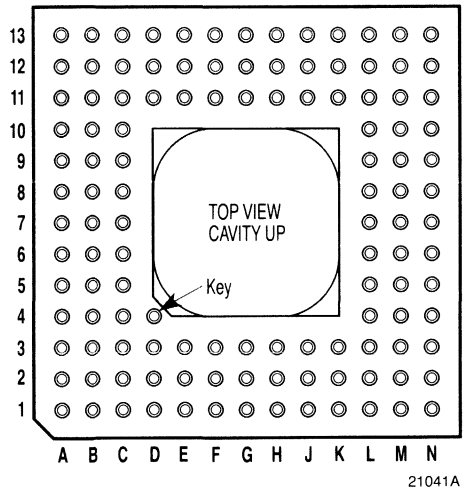
If the signal is to be frequency modulated then the modulation signal is loaded into the M register. The format for the frequency is the same as that for the C register. If $ENYP_{1,0} = 0, 1$ then the data that is presented at the PH port is automatically loaded on each clock rising edge.

For phase modulation, the phase deviation is loaded into the M register (same manner as for frequency modulation). The units of the phase offset are cycles and full-scale is just under one output cycle per TMC2340 clock cycle. The MSB represents a phase of 180°, and the LSB a phase of about 8×10^{-8} degrees (eight one-hundred-millionths of a degree), or $\pi/2^{31}$ radians.

To synchronize two TMC2340s, first load them with their respective data in mode 0, then switch them simultaneously to either Mode 1 or Mode 2.

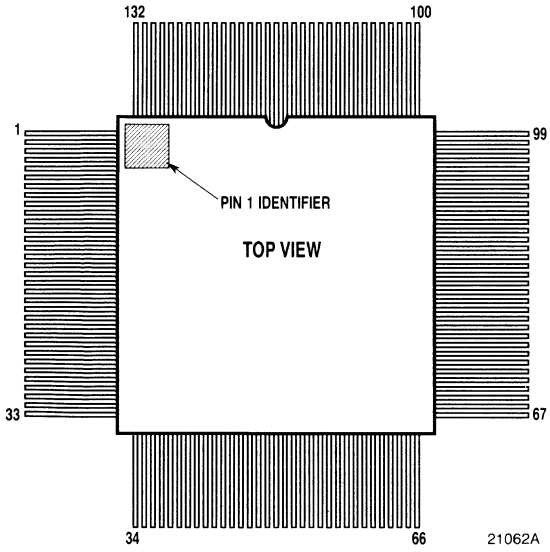
Pin Assignments – 120 Pin Plastic Pin Grid Array, H5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	Q_5	B3	Q_6	C5	GND	E1	GND	G11	GND	K1	PH_2	L10	PH_{31}	M12	AM_1
A2	Q_7	B4	Q_9	C6	V_{DD}	E2	GND	G12	AM_{12}	K2	PH_4	L11	V_{DD}	M13	AM_2
A3	Q_8	B5	Q_{11}	C7	GND	E3	V_{DD}	G13	AM_{13}	K3	GND	L12	AM_3	N1	PH_8
A4	Q_{10}	B6	Q_{13}	C8	V_{DD}	E11	V_{DD}	H1	PM	K11	GND	L13	AM_4	N2	PH_{10}
A5	Q_{12}	B7	GND	C9	GND	E12	GND	H2	FM	K12	AM_5	M1	PH_6	N3	PH_{12}
A6	Q_{14}	B8	I_1	C10	GND	E13	$\overline{OEI}$	H3	V_{DD}	K13	AM_6	M2	PH_9	N4	PH_{15}
A7	Q_{15}	B9	I_3	C11	V_{DD}	F1	OBIQ	H11	AM_9	L1	PH_5	M3	PH_{11}	N5	PH_{17}
A8	I_0	B10	I_5	C12	I_{11}	F2	GND	H12	AM_{10}	L2	PH_7	M4	PH_{13}	N6	PH_{19}
A9	I_2	B11	I_7	C13	I_{13}	F3	CLK	H13	AM_{11}	L3	GND	M5	PH_{16}	N7	PH_{21}
A10	I_4	B12	I_9	D1	$\overline{OEQ}$	F11	V_{DD}	J1	PH_0	L4	V_{DD}	M6	PH_{18}	N8	PH_{22}
A11	I_6	B13	I_{12}	D2	Q_0	F12	GND	J2	PH_1	L5	PH_{14}	M7	PH_{20}	N9	PH_{24}
A12	I_8	C1	Q_1	D3	GND	F13	AM_{14}	J3	PH_3	L6	V_{DD}	M8	PH_{23}	N10	PH_{26}
A13	I_{10}	C2	Q_2	D11	GND	G1	ENP_1	J11	GND	L7	GND	M9	PH_{25}	N11	PH_{29}
B1	Q_3	C3	V_{DD}	D12	I_{14}	G2	ENP_0	J12	AM_7	L8	V_{DD}	M10	PH_{28}	N12	PH_{30}
B2	Q_4	C4	GND	D13	I_{15}	G3	GND	J13	AM_8	L9	PH_{27}	M11	ENA	N13	AM_0



Pin Assignments – 132 Leaded CERQUAD, L5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{DD}	23	PH_1	45	V_{DD}	67	V_{DD}	89	GND	111	I_2
2	NC	24	PH_2	46	PH_{18}	68	AM1	90	I_{15}	112	VDD
3	Q_4	25	PH_3	47	PH_{19}	69	AM2	91	V_{DD}	113	I_1
4	Q_3	26	PH_4	48	PH_{20}	70	GND	92	I_{14}	114	I_0
5	GND	27	PH_5	49	GND	71	AM_3	93	I_{13}	115	GND
6	Q_2	28	PH_6	50	PH_{21}	72	NC	94	I_{12}	116	V_{SS}
7	Q_1	29	GND	51	PH_{22}	73	AM_4	95	GND	117	Q_{15}
8	Q_0	30	PH_7	52	PH_{23}	74	AM_5	96	I_{11}	118	Q_{14}
9	V_{DD}	31	PH_8	53	V_{DD}	75	GND	97	I_{10}	119	Q_{13}
10	$\overline{OEQ}$	32	NC	54	PH_{24}	76	AM_6	98	NC	120	V_{DD}
11	GND	33	GND	55	PH_{25}	77	AM_7	99	V_{DD}	121	Q_{12}
12	GND	34	PH_9	56	PH_{26}	78	AM_8	100	I_9	122	Q_{11}
13	CLK	35	NC	57	PH_{27}	79	AM_9	101	NC	123	Q_{10}
14	GND	36	PH_{10}	58	PH_{28}	80	AM_{10}	102	I_8	124	GND
15	TCXY	37	V_{DD}	59	PH_{29}	81	AM_{11}	103	NC	125	Q_9
16	ENP_0	38	PH_{11}	60	PH_{30}	82	AM_{12}	104	GND	126	Q_8
17	GND	39	PH_{12}	61	PH_{31}	83	GND	105	I_7	127	Q_7
18	ENP_1	40	PH_{13}	62	NC	84	AM_{13}	106	I_6	128	NC
19	FM_0	41	PH_{14}	63	ENA	85	AM_{14}	107	I_5	129	GND
20	PM_1	42	PH_{15}	64	NC	86	GND	108	GND	130	Q_6
21	V_{DD}	43	PH_{16}	65	NC	87	V_{DD}	109	I_4	131	NC
22	PH_0	44	PH_{17}	66	AM_0	88	$\overline{OERX}$	110	I_3	132	Q_5



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2340H5C1	STD – T_A = 0°C to 70°C	Commercial	120 Pin Plastic Pin Grid Array	2340H5C1
TMC2340H5C	STD – T_A = 0°C to 70°C	Commercial	120 Pin Plastic Pin Grid Array	2340H5C
TMC2340L5V1	EXT – T_C = – 55°C to 125°C	MIL-STD-883B	132 Leaded CERQUAD	2340L5V1
TMC2340L5V	EXT – T_C = – 55°C to 125°C	MIL-STD-883B	132 Leaded CERQUAD	2340L5V

Imaging Products

TRW has provided image processing components to the television brocasting industry since the mid 1970s; many of the products in this databook have applications in this area.

Specifically designed for image processing are the Image Resampling Sequencers (TMC2301, TMC2302). These address generators are given an image manipulation transfer function representing a shift, rotate, warp, or zoom. They product sets of memory pixel addresses that translate to the desired pixel in the output image. High-speed processing elements such as the TMC2249 Mixer and TMC2250 Matrix Multiplier accept these input pixels and compute the values of the output pixels.

The TMC2272 Colorspace Converter is a completely programmable device that can convert between any two color image representations (working in conjunction with the TMC2330 Coordinate Transformer when dealing with HSI-type representations).

The TMC2330 itself is tailored to convert between vector and rectangular coordinate systems – as is necessary to put a radar or ultrasound image on a raster scan display. It is used in general vector image processing, as well as reconstructing CAT and NMR images.

The TMC2311 Fast Cosine Transform is the fundamental element in the major appproaches to image compression. TRW will shortly introduce companion devices that implement standard compression algorithms.

Other products include a Half-Band Filter, Image Convolver, Digital Mixer, and Image Filters, all designed to process images efficiently in real-time.

Imaging Products

TRW

Product	Description	Size	Clock Rate [1] (MHz)	Power [1] (Watts)		Package	Grades [2]	Notes	Page
TMC1028	Digital FIR Filter	4 x 4 x 8	10	3.7	J4	48 Pin DIP	C, A	Cascadeable.	H3
TMC2242-1	Half-Band Digital Filter	12/16-Bit	40	0.5	R2	44 Lead PLCC	C	2:1 Interpolate or Decimate.	H15
-			30	0.5	R2	44 Lead PLCC	C	Low-Pass (−6dB@0.25FS)	
TMC2243	Video Filter	10 x 10 x 3	20	0.5	G8	69 Pin PGA	C, V	Cascadeable.	H29
					H8	69 Pin PPGA	C		
TMC2246-1	Image Filter	10 x 11 Bit	40	0.5	H5	121 Pin PPGA	C	Four-Pixel Interpolator.	H43
					L5	132 Lead CERQUAD	V		
-			30	0.5	H5	121 Pin PPGA	C		
					L5	132 Lead CERQUAD	V		
TMC2249-1	Digital Mixer	12 x 12 x 2	30	0.5	H5	121 Pin PPGA	C	Cascadeable.	H55
-					L5	132 Lead CERQUAD	V	Programmable Delays.	
			25	0.5	H5	121 Pin PPGA	C		
					L5	132 Lead CERQUAD	V		
TMC2250-2	Matrix Multiplier	12 x 10 x 9	40	1.2	H5	121 Pin PPGA	C	2D Convolution 3 x 3, 2 x 4.	H69
-1			36	1.2	H5	121 Pin PPGA	C	1D Convolution, 9 Taps.	
					G1	121 Pin PGA	V	3 x 3 Matrix x 3 x 1 Vector.	
-			30	1.2	H5	121 Pin PPGA	C		
					G1	121 Pin PGA	V		
TMC2255-1	2D Convolver	5 x 5 x 8 Bit	12.5	0.6	R1	68 Lead PLCC	C	3 x 3, Symmetric 5 x 5	H89
-			10	0.6	R1	68 Lead PLCC	C	2D Convolver.	
TMC2272-2	Color Space Converter	3 x 12 Bit	40	1.2	H5	121 Pin PPGA	C	3 x 3 Matrix x 3 x 1 Vector.	E3
-1			36	1.2	H5	121 Pin PPGA	C		
-			30	1.2	H5	121 Pin PPGA	C		
TMC2301-2	Image Resampling Sequencer	4K x 4K Pixels	20	0.5	G8	68 Pin Grid Array	C	Second Order.	E39
					R1	68 Lead PPGA	C	2-Dimension.	
-1			18	0.4	G8	68 Pin Grid Array	C, V SMD		
					R1	68 Lead PPGA	C		
					L1	68 Leaded CC	V		
-			15	0.4	G8	68 Pin Grid Array	C, V SMD		
					R1	68 Lead PPGA	C		
					R1	68 Leaded CC	V		
TMC2302-1	Image Manipulation Sequencer	65K x 65K Pixels	40	0.4	H5	121 Pin PPGA	C	Third Order.	E41
			30	0.4	H5	121 Pin PPGA	C	3-Dimension.	
TMC2311-2	Fast Cosine Transform	12-Bit	17.8	0.7	R1	68 Lead PLCC	C	Data Compression Processor.	F47
-1			14.5	0.7	R1	68 Lead PLCC	C	Meets CCITT Specifications.	
-			17.8	0.7	R1	68 Lead PLCC	C	8 x 8, 2-Dimension.	
TMC2330-1	Coordinate Transformer	16 x 16 Bit	25	0.7	H5	121 Pin PPGA	C	Cartesian ↔ Polar Conversion.	F65
					L5	132 Lead CERQUAD	V		
-			20	0.7	H5	121 Pin PPGA	C		
					L5	132 Lead CERQUAD	V		

Notes: 1. Guaranteed. See product specifications for test conditions.

2. A = High Reliability, $T_C = -55°C$ to $125°C$.
C = Commercial, $T_A = 0°C$ to $70°C$.
V = MIL-STD-883 Compliant, $T_C = -55°C$ to $125°C$.
SMD = Available per Standardized Military Drawing, $T_C = -55°C$ to $125°C$.

Digital Colorspace Converter/Corrector
36 Bit Color (12 Bits x 3 Components) 40MHz

A 40MHz, three-channel, 36 bit (three 12-bit components) colorspace converter and color corrector, the TMC2272 uses 9 parallel multipliers to process high-resolution imagery in real time.

The TMC2272 also operates at any slower clock rate and with any smaller data path width, allowing it to handle all broadcast and consumer camera, frame-grabber, encoder/decoder, recorder and monitor applications as well as most electronic imaging applications.

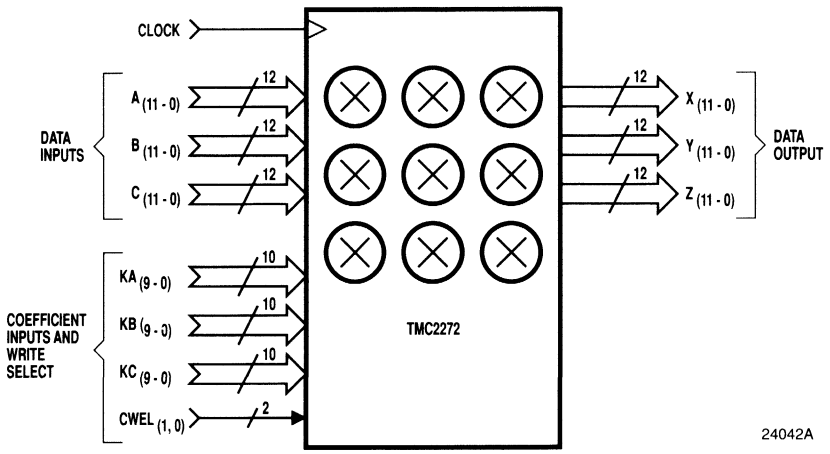
The TMC2272's processing ability allows colorspaces to be optimized for every input or output device; camera, monitor, transmission or storage medium in real time, regardless of the signal format required by each stage in a system. For instance, a frame buffer may be operated in any desired colorspace in an otherwise RGB system with the use of two TMC2272s for translation to and from the desired frame-buffer colorspace.

A complete set of three 12-bit samples is processed on every clock cycle, with a five-cycle pipeline latency. Full 23-bit (for each of three components) internal precision is provided with 10-bit user-defined coefficients. The coefficients may be varied dynamically, with three new coefficients loaded every clock cycle. (The full set of nine can be replaced in three clock cycles.) Rounding to 12 bits per component is performed only at the final output. This allows full accuracy with correct rounding and overflow headroom for applications that require less than 12-bit per component. All inputs and outputs are registered on the rising edges of the clock.

The TMC2272 is fabricated in TRW's OMICRON-C™ 1μ CMOS process and has fully guaranteed performance over the full commercial temperature range of 0 to 70°C, and all other operational conditions specified in the ***Operating conditions*** table. The TMC2272 is available in a 121-pin plastic pin-grid array (PPGA) package in three speed grades.

E

Logic Symbol



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40G06753 Rev. A – 8/90
Printed in the U.S.A.

Features

- 40MHz (25ns) Pipelined Throughput
- 3 Simultaneous 12-Bit Input And Output Channels (64 Giga [2^{36}] Colors)
- Two's Complement Inputs And Outputs
- Overflow Headroom Available In Lower Resolution
- 10-Bit User-Defined Coefficients
- TTL-Compatible Input And Output Signals
- Full Precision Internal Calculation
- Output Rounding
- On-Board Coefficient Memory
- OMICRON-C™ 1μ CMOS process

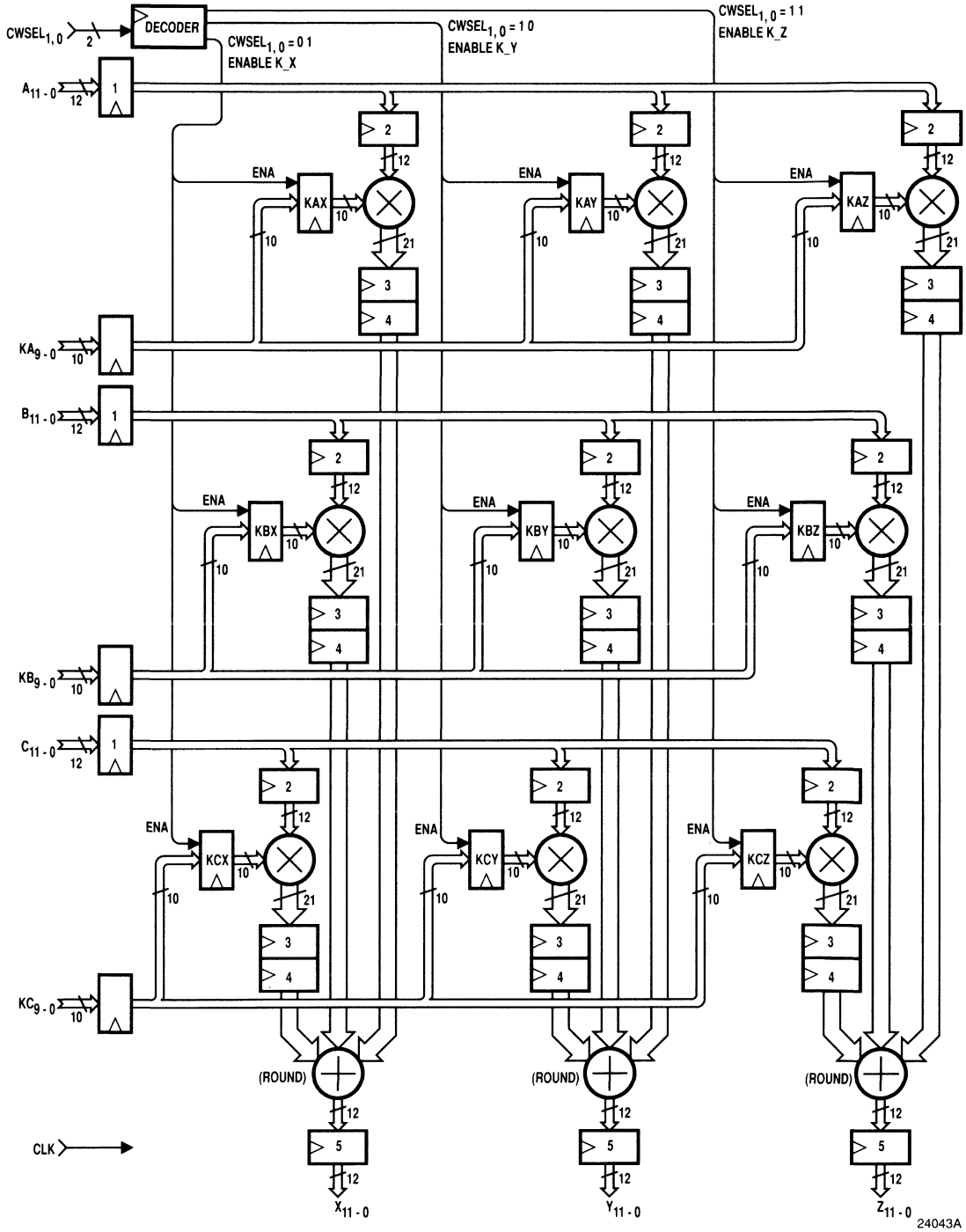
Applications

- Translation Between Component Color Standards (RGB, YIQ, YUV, etc.)
- Broadcast Composite Color Encoding And Decoding (All Standards)
- Broadcast Composite Color Standards Conversion And Transcoding
- Camera Tube And Monitor Phosphor Colorimetry Correction
- White Balancing And Color-Temperature Conversion
- Image Capture, Processing and Storage
- Color Matching Between Systems, Cameras And Monitors
- Three-Dimensional Perspective Translation

Associated Products

- TDC1058 A/D Converter
- TDC1049 A/D Converter
- TMC2242 Interpolator/Decimator
- TMC2330 Rectangular/Polar Converter
- TDC1012 D/A Converter
- TMC0171 D/A Converter

Figure 1. Functional Block Diagram



Functional Description

General Information

The TMC2272 is a nine-multiplier array with the internal bus structure and summing adders needed to implement a 3 x 3 matrix multiplier (triple dot product). With a 40MHz guaranteed maximum clock rate, this device offers video and imaging system designers a single-chip solution to numerous common image and signal-processing problems.

The three data input ports (A_{11-0}, B_{11-0}, C_{11-0}) accept 12-bit two's complement integer data, which is also the format for the output ports (X_{11-0}, Y_{11-0}, and Z_{11-0}). Other format and path width options are discussed in the numeric format and overflow section. The coefficient input ports (KA, KB, KC) are always 10-bit two's complement fractional. ***Table 2*** details the bit weighting.

Full precision is maintained throughout the TMC2272. Each output is accurately rounded to 12-bits from the 23-bits entering the final adder.

Signal Definitions

A(n), B(n), C(n) — Indicates the data word presented to that input port during the specified clock rising edge (n). Applies to input ports A_{11-0}, B_{11-0}, and C_{11-0}.

KAX(n) thru KCZ(n) — Indicates coefficient value stored in the specified one of the nine onboard coefficient registers KAX through KCZ, input during or before the specified clock rising edge (n).

X(n), Y(n), Z(n) — Indicates data available at that output port t_{DO} after the specified clock rising edge (n). Applies to output ports X_{11-0}, Y_{11-0}, and Z_{11-0}.

The TMC2272 utilizes six input and output ports to realize a "triple dot product," in which each output is the sum of all three input words in multiplied by the appropriate stored coefficients. The three corresponding sums of products are available at the outputs five clock cycles after the input data are latched, and three new data words rounded to 12-bits are then available every clock cycle. See the *Applications Discussion* regarding encoded video standard conversion matrices.

$$X(5) = A(1)KAX(1) + B(1)KBX(1) + C(1)KCX(1)$$
$$Y(5) = A(1)KAY(1) + B(1)KBY(1) + C(1)KCY(1)$$
$$Z(5) = A(1)KAZ(1) + B(1)KBZ(1) + C(1)KCZ(1)$$

Pin Definitions

Power

V_{DD}, GND — The TMC2272 operates from a single +5V supply. All pins must be connected.

Control

$CWSEL_{1-0}$ — This input selects which three of the 9 coefficient registers, if any, will be updated on the next clock cycle from the KA_{9-0}, KB_{9-0} and KC_{9-0} inputs. See ***Table 4*** and the *Functional Block Diagram*.

Clock

CLK — The TMC2272 operates from a single system clock input. All timing specifications are referenced to the rising edge of clock.

Data and Coefficient Inputs

A_{11-0}, B_{11-0}, C_{11-0} — These are the three 12-bit wide data input ports.

KA_{9-0}, KB_{9-0}, KC_{9-0} — These are the 10-bit wide coefficient input ports. The value at each of these three inputs will update one coefficient register as selected by the coefficient write select ($CWSEL_{1-0}$) on the next clock. See ***Table 1*** and the *Functional Block Diagram*.

Outputs

X_{11-0}, Y_{11-0}, Z_{11-0} — These are the data outputs. Data are available at the 12-bit registered Output Ports X, Y, and Z t_{DO} after every clock rising edge.

Table 1. Coefficient Loading

		$CWSEL_{1,0}$			
		00	01	10	11
Input	KA_{9-0}	Hold All	Load KAX	Load KAY	Load KAZ
Input	KB_{9-0}	Hold All	Load KBX	Load KBY	Load KBZ
Input	KC_{9-0}	Hold All	Load KCX	Load KCY	Load KCZ

Package Interconnections

Signal Type	Signal Name	Function	H5 Package
Power	V_{DD}	Supply Voltage	F3, H3, L7, C8, C4
	GND	Ground	E3, G3, J3, L4, L6, H11, C7, C5, A4, B5
Clock	CLK	System Clock	D11
Controls	$CWSEL_{1,0}$	Coefficient Write Select	J12, J13
Inputs	A_{11-0}	Data Input A	E11, D13, E12, E13, F11, F12, F13, G13, G11, G12, H13, H12
	B_{11-0}	Data Input B	B10, A11, B11, C10, A12, B12, C11, A13, C12, B13, C13, D12
	C_{11-0}	Data Input C	A5, C6, B6, A6, A7, B7, A8, B8, A9, B9, A10, C9
	KA_{9-0}	Coefficient Input KAX, KAY, or KAZ (See Pin Definitions and Table 1)	K13, J11, K12, L13, L12, K11, M13, M12, L11, N13
	KB_{9-0}	Coefficient Input KBX, KBY, or KBZ (See Pin Definitions and Table 1)	M11, L10, N12, N11, M10, L9, N10, M9, N9, L8
	KC_{9-0}	Coefficient Input KCX, KCY, or KCZ (See Pin Definitions and Table 1)	M8, N8, N7, M7, N6, M6, N5, M5, N4, L5
Outputs	X_{11-0}	Output X	B4, A3, A2, B3, A1, C3, B2, B1, D3, C2, C1, D2
	Y_{11-0}	Output Y	D1, E2, E1, F2, F1, G2, G1, H1, K1, J2, J1, H2
	Z_{11-0}	Output Z	M4, N3, M3, N2, M2, L3 N1, L2, K3, M1, L1, K2

Figure 2. Impulse Response

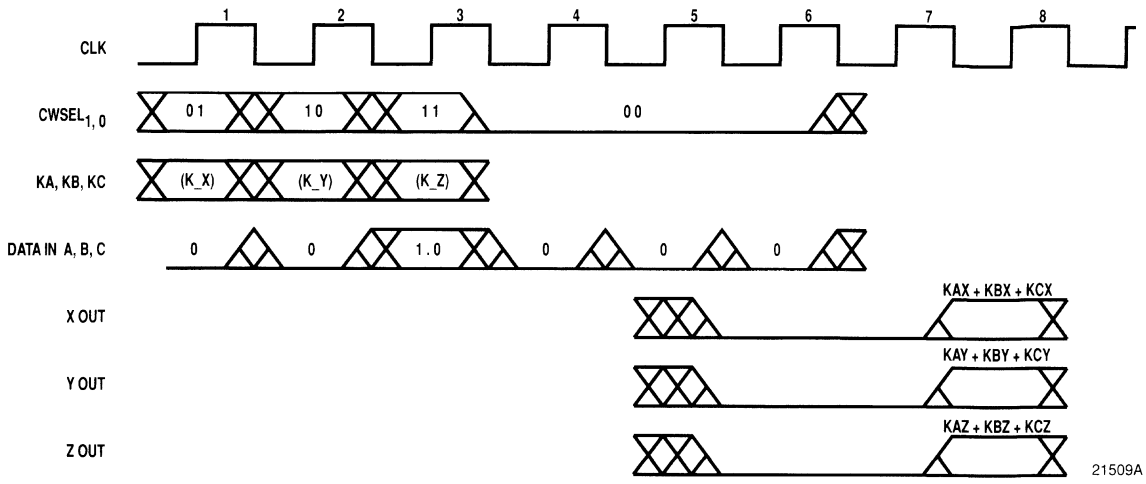
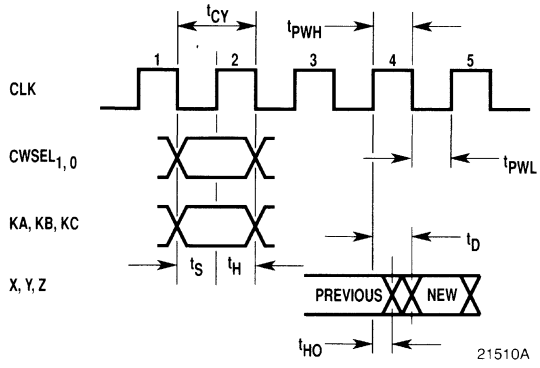


Figure 3. Input/Output Timing Diagram



Numeric Format and Overflow

Table 2 shows the binary weightings of the input and output ports of the TMC2272. Although the internal sums of products could grow to 23-bits, the outputs X, Y, and Z are rounded to yield 12-bit integer words. Thus the output format is identical to the input data format. Bit weighting is easily adjusted by applying the same scaling correction factor to both input and output data words.

As shown in *Table 2*, the TMC2272's matched input and output data formats accommodate 0dB (unity) gain. Therefore the user must be aware of input conditions that could lead to numeric overflow. Maximum input data and coefficient word sizes must be taken into account with the specific translation performed to ensure that no overflow occurs.

Use with Fewer Than 12 Bits

The TMC2272 can be configured to provide several format and overflow options when used in systems with fewer than 12-bits of resolution. An 8-bit system will be used as an example, however these concepts apply to any other word width.

The most apparent mode of operation is to left justify the incoming data and to ground the unused input LSBs. However, the outputs will still be rounded to the least significant bit of the TMC2272, having little if any effect on the top 8 bits actually used. Because the TMC2272 carries out all calculations to full precision, the preferred mode of operation is to right justify and sign extend the data as shown in ***Figure 4***. Since all the LSBs are used, the desired output will be rounded correctly, and overflow will be accommodated by bits 7 through 10.

The TMC2272 may also be used in unsigned binary 8-bit systems as shown in ***Figure 5***. Bits 11 through 8 will handle overflow.

In all applications, a digital zero (ground) should be connected to all unused inputs.

E

Table 2. Bit Weightings for Input and Output Data Words

Bit Weights	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}
INPUTS																						
All Modes Data A, B, C	$-I_{11}$	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	.									
Coefficients KA, KB, KC												$-K_9$	.	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0
Internal Sum	X_{20}	X_{19}	X_{18}	X_{17}	X_{16}	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	.	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
OUTPUTS																						
X, Y, Z	$-O_{11}$	O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	.									

Note: A minus sign indicates a two's complement sign bit.

Figure 4. Two's Complement 8-Bit Application

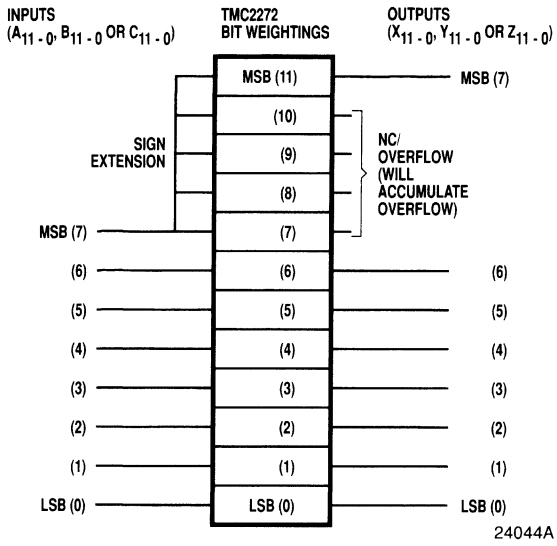
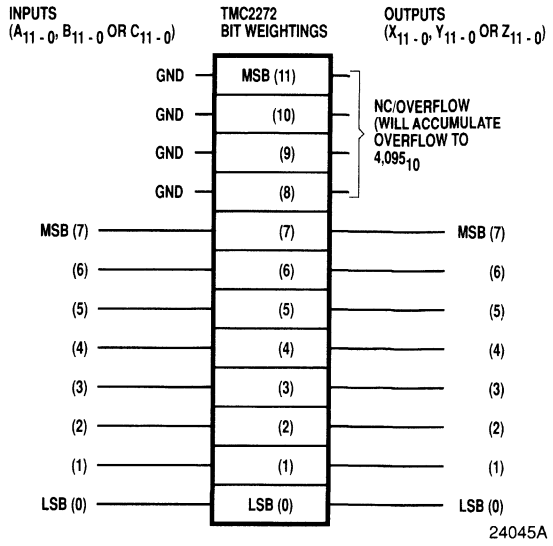


Figure 5. Binary 8-Bit Application



Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltage	–0.5 to +7.0V
Input Voltage	–0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage	–0.5 to (V_{DD} + 0.5)V[2]
Forced current	–6.0 to 6.0mA[3,4]
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating case	–60 to +130°C
junction	175°C
Lead soldering (10 seconds)	300°C
Storage	–65 to 150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range Standard Min	Nom	Max	Units
V_{DD}	Supply Voltage	4.75	5.0	5.25	V
V_{IL}	Input Voltage,Logic LOW			0.8	V
V_{IH}	Input Voltage,Logic HIGH	2.0			V
I_{OL}	Output Current,Logic LOW			4.0	mA
I_{OH}	Output Current,Logic HIGH			–2.0	mA
t_{CY}	Cycle Time				
	TMC2272	33			ns
	TMC2272-1	27.7			ns
	TMC2272-2	25			ns
t_{PWL}	Clock Pulse Width,LOW				
	TMC2272	15			ns
	TMC2272-1	12			ns
	TMC2272-2	10			ns
t_{PWH}	Clock Pulse Width,HIGH	10			ns
t_S	Input Setup Time				
	TMC2272	8			ns
	TMC2272-1	7			ns
	TMC2272-2	6			ns
t_H	Input Hold Time				
	TMC2272	3			ns
	TMC2272-1	3			ns
	TMC2272-2	2			ns
T_A	Ambient Temperature, Still Air	0		70	°C

E

Electrical characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD}=Max, V_{IN}=0V		12	mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, f=20MHz		160	mA
I_{IL}	Input Current,Logic LOW[2]	V_{DD}=Max, V_{IN}=0V		–10	uA
IIH	Input Current,Logic HIGH[2]	V_{DD}=Max, V_{IN}=V_{DD}		10	uA
I_{OIL}	Input Current,Logic LOW[3]	V_{DD}=Max, V_{IN}=0V		–40	uA
I_{OIH}	Input Current,Logic HIGH[3]	V_{DD}=Max, V_{IN}=V_{DD}		40	uA
V_{OL}	Output Voltage,Logic LOW	V_{DD}=Min, I_{OL}=4mA		0.4	V
V_{OH}	Output Voltage,Logic HIGH	V_{DD}=Min, I_{OH}=-2mA	2.4		V
I_{OS}	Short-Circuit Output Current	V_{DD}=Max, Output HIGH, One Pin to Ground, One Second Duration Max.	–20	–80	mA
C_I	Input Capacitance	T_A=25°C, f=1MHz		10	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		10	pF

Notes:
1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Except pins X_{11-0}, Y_{11-0}
3. Pins X_{11-0}, Y_{11-8} only.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
t_D	Output Delay	V_{DD}=Min, C_{LOAD}=25pF			
	TMC2272			18	ns
	TMC2272-1			17	ns
	TMC2272-2			16	ns
t_{HO}	Output Hold Time	V_{DD}=Max, C_{LOAD}=25pF			
	TMC2272		4		ns
	TMC2272-1		3		ns
	TMC2272-2		3		ns

Figure 6. Equivalent Input Circuit

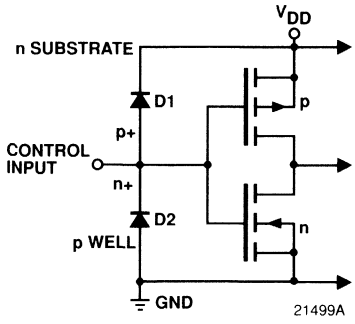
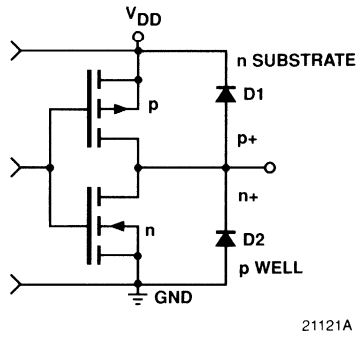


Figure 7. Equivalent Output Circuit



Applications Discussion

The TMC2272 can convert between any two three-coordinate colorspaces with the selection of the proper coefficients. Sets of coefficients for some popular colorspace conversions are presented below.

By concatenating coefficient matrices of single transformations, the user can program the TMC2272 to perform compound transforms efficiently. For example, given an RGB input, correction of the relative values of R and B, for color temperature, conversion to YIQ, modification of contrast by changing Y, and conversion back to RGB can be performed as quickly and easily as any simple transformation. To calculate the final set of coefficients from the coefficients of the individual transformations, the procedure in ***Figure 8*** (concatenation) is used. If more than two matrices are to be combined, the result from the concatenation of the first two matrices is concatenated with the third. If more matrices must be incorporated in the final function, the last step is repeated.

Figure 8. Concatenation

$$\begin{vmatrix} A & B & C \\ D & E & F \\ G & H & I \end{vmatrix} \begin{vmatrix} J & K & L \\ M & N & O \\ P & Q & R \end{vmatrix} = \begin{vmatrix} AJ+BM+CP & AK+BN+CQ & AL+BO+CR \\ DJ+EM+FP & DK+EN+FQ & DL+EO+FR \\ GJ+HM+IP & GK+HN+IQ & GL+HO+IR \end{vmatrix}$$

24046A

Converting Video Data from RGB to YIQ or YUV

The TMC2272 simplifies the task of converting encoded color video data between the RGB (color component) format and the YIQ (quadrature encoded chrominance) or YUV (color difference) format. Beginning with RGB component data, the standard relationships, with 8-bit quantization, are:

$$Y = (77R + 150G + 29B)/256 \quad \text{and} \quad Y = (77R + 150G + 29B)/256$$
$$I = (153R - 71G - 82B)/256 + 128 \qquad U = (131R - 110G - 21B)/256 + 128$$
$$Q = (54R - 134G + 80B)/256 + 128 \qquad V = (-44R - 87G + 131B)/256 + 128$$

In digital systems, I and Q or U and V are sometimes renormalized to:

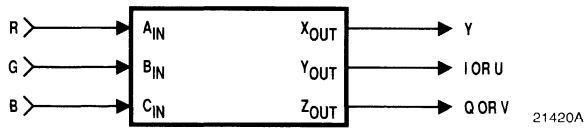
$$I = (128R - 59G - 69B)/256$$
$$Q = (52R - 128G + 76B)/256$$
$$U = (128R - 107G - 21B)/256$$
$$V = (-43R - 85G + 128B)/256$$

With each coefficient expressed as a fraction of 256, these numbers are easily converted to binary for loading into the coefficient storage of the TMC2272. The half-scale (80hex) offsets included in the chrominance and color-difference terms can easily be added to the appropriate sums after the matrix multiplication, if desired. ***Table 3*** contains the 10-bit two's complement coefficients to be loaded into the TMC2272 to perform the desired conversion from RGB format. Once these factors are in place the user can continuously convert encoded data at real-time video rates, with three new encoded outputs available on every clock cycle.

Table 3. Colorspace Conversion Coefficients[1,2]

Conversion	KAX	KAY	KAZ	KBX	KBY	KBZ	KCX	KCY	KCZ
RGB to YIQ	04D	099	036	096	3B9	37A	01D	3AE	050
RGB to YIQ[3]	04D	080	034	096	3C5	380	01D	3BB	04C
RGB to YUV	04D	083	3D4	096	392	3A9	01D	3EB	083
RGB to YUV[3]	04D	080	3D5	096	395	3AB	01D	3EB	080

Notes:
1. All entries are given in 10-bit two's complement hexadecimal such that all entries beginning in "2" or "3" are negative.
2. This table assumes the following bus assignments:



3. Second and fourth rows are renormalized such that largest coefficient = .5 (080_{hex}).

Converting Video Data from YIQ or YUV to RGB

With a different set of coefficients, the TMC2272 can perform the inverse conversions, whose governing equations are:

$$R = (256Y + 243I + 159Q)/256 \quad \text{and} \quad R = (256Y + 0U + 292V)/256$$
$$G = (256Y - 72I - 164Q)/256 \qquad G = (256Y - 101U - 149V)/256$$
$$B = (256Y - 284I + 443Q)/256 \qquad B = (256Y + 520U + 0V)/256$$

Since the first YUV → RGB equation set includes the coefficient "520," which won't fit into a 10-bit two's complement integer format, we must either divide all coefficients by 2, degrading precision by one bit, or by 520/511. In ***Table 4***, the 520/511 correction factor was selected.

The values corresponding to digital normalization (see RGB to YIQ discussion) are:

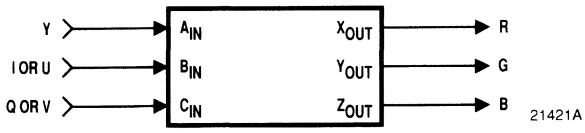
$$R = 256Y + 292I + 167Q)/256 \quad \text{and} \quad R = (256Y + 0U + 359V)/256$$
$$G = (256Y - 86I - 172Q)/256 \qquad G = (256Y - 88U - 183V)/256$$
$$B = (256I - 341I + 456Q)/256 \qquad B = (256Y + 453U + 0V)/256$$

E

Table 4. Colorspace Conversion Coefficients[1,2]

Conversion	KAX	KAY	KAZ	KBX	KBY	KBZ	KCX	KCY	KCZ
YIQ to RGB	100	100	100	0F3	3B8	3E4	09F	35C	1BB
YIQ to RGB[3]	100	100	100	124	3AA	2AB	0A7	354	101
YUV to RGB	0FC	0FC	0FC	000	39D	1FF	11F	36E	000
YUV to RGB[3]	100	100	100	000	3A8	125	167	349	000

Notes:
1. All entries are given in 10-bit two's complement hex, such that all entries beginning in "2" or "3" are negative.
2. This table assumes the following bus assignments:



3. Second and fourth rows are renormalized such that largest coefficient = .5 (080_{hex}).

HSV (HSI) Format Conversions

HSV (or HSI) refers to Hue (color) Saturation (vividness) and Value (intensity or brightness), quantities which are directly related to the human perception of light and color. The V (or I) levels are simply the Y (or luminance) levels. Hue and Saturation are derived from the R-Y and B-Y color difference values of a signal.

HSV Calculations:

Value (V) = Intensity (I) = Y

Hue (H) = Arctan (B-Y/R-Y)

Saturation (S) = $\sqrt{(R\text{-}Y)^2 + (B\text{-}Y)^2}$

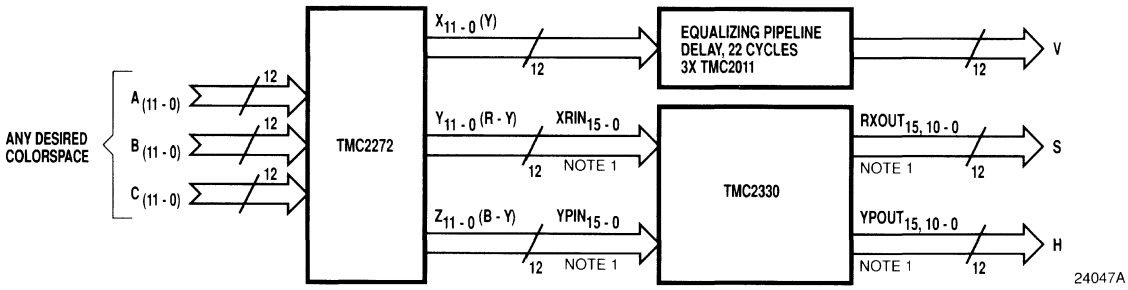
R-Y = S * cos(H)

B-Y = S * sin(H)

One may use two 64Kx8 ROM look-up-tables to calculate Hue and Saturation from R-Y and B-Y in an 8-bit system. However, the finite size of this LUT may limit performance, especially if the TMC2272's full precision is used. The TMC2330, developed to translate between rectangular and polar coordinates, can perform the trigonometric transformations to 16 bit precision at 25MHz. These calculations are the the same as required in HSV calculations. A 4 Giga-byte x 32 bit LUT can achieve the same accuracy and precision as the TMC2330, if it is programmed correctly.

To convert between Y, R-Y, B-Y and HSV, the the TMC2272 isn't needed at all; simply use the TMC2330. To convert between HSV and any other format, use the TMC2330 to translate between HSV and Y, R-Y, B-Y, and use the TMC2272 to translate between Y, R-Y, B-Y and the other format. See *Figures 9* and *10*.

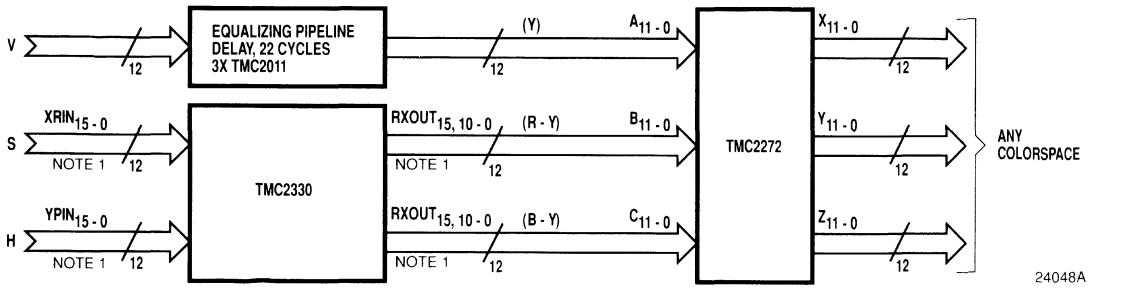
Figure 9. Conversion to HSV



Notes: 1. Connect TMC2272 MSBs (Bits 11) to TMC 2330 MSBs (Bits 15) and also to TMC2330 Bits 14-11. Connect TMC2272 LSBs (Bits 10-0) to TMC2330 LSBs (Bits 10-0). TMC2330 output bits 14-11 are overflow.

2. TMC2272 $Y_{11\text{-}0}$ outputs should not be confused with the designation "Y" used to signify the intensity components. The assignment of components to TMC2272 inputs and outputs may be altered through the selection of appropriate coefficients.

Figure 10. Conversion from HSV



Notes: 1. Connect input MSBs (Bits 11) to TMC2330 MSBs (Bits 15) and also to TMC2330 Bits 14-11. Connect input LSBs (Bits 10-0) to TMC2330 LSBs (Bits 10-0).

2. TMC2272 $Y_{11\text{-}0}$ outputs should not be confused with the designation 'Y' used for an intensity component. Component assignment depends on the coefficients used.

Input Interpolation/Output Decimation and Filtering

In some applications the two color-difference signals (R-Y/B-Y or Cr/Cb, for example,) are transmitted at one-half the rate of the luminance (Y) signal. These two color-difference signals are often multiplexed to one signal which is at the same sample rate as the luminance signal. In many applications, if the color difference signals are already band-limited, it is satisfactory to use the same color difference sample for each two luminance samples. Little improvement is obtained with a simple averaging ([A+B]/2) interpolation filter. If the color difference signal is not band-limited, either of these two methods may yield unsatisfactory results due to aliasing. In this case, a TRW TMC2242 digital low-pass ("half-band") interpolating filter will correctly band-limit each color difference signal as it is interpolated. See *Figure 11*.

The same methods are used to decimate the color difference outputs. Simple decimation by removing every other sample of color information may yield unsatisfactory results due to aliasing. This is a problem because the color difference signals have now been transformed with the higher-bandwidth luminance signals and therefore have higher bandwidths than they had before the transform. The best performance is obtained by using a precise low-pass ("half-band") decimation filter such as the TRW TDC2242 to remove aliasing components. See *Figure 12*.

The TDC2242 is a bi-directional, selectable rate filter/interpolator/decimator.

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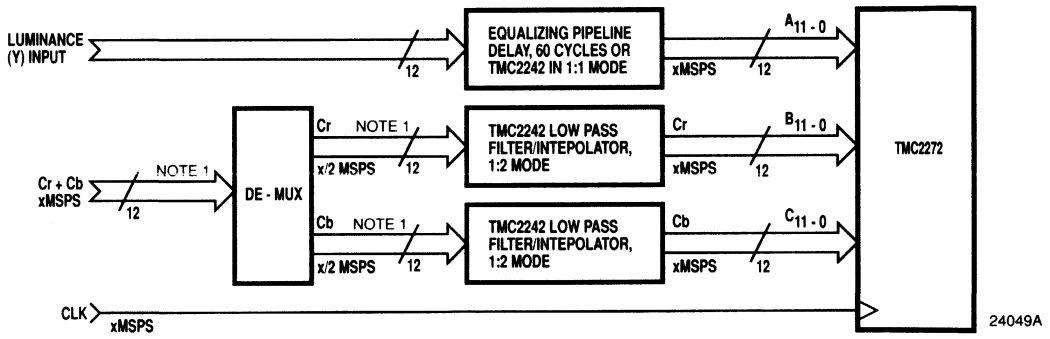
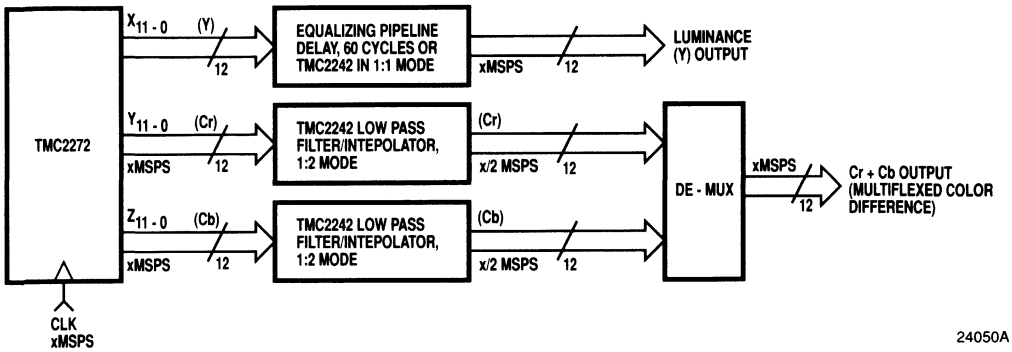
Figure 11. Input Interpolation and Filtering



Notes: 1. Width of input paths will vary with source.
2. See TMC2242 Datasheet for further information.

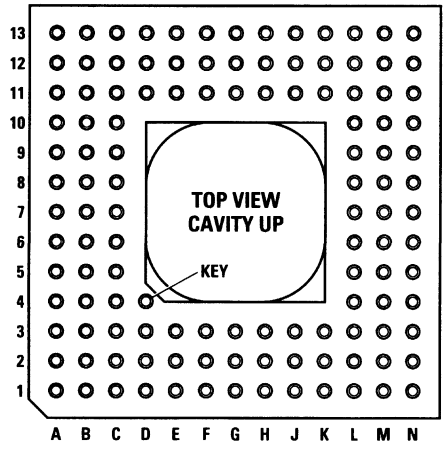
Figure 12. Output Decimation and Filtering



Pin Assignments – 121-Pin Plastic Pin Grid Array H5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	X7	B5	GND	C9	C_0	F1	Y_7	H13	A_1	L5	KC_0	M9	KB_2
A2	X_9	B6	C_9	C10	B_8	F2	Y_8	J1	Y_1	L6	GND	M10	KB_5
A3	X_{10}	B7	C_6	C11	B_5	F3	V_{DD}	J2	Y_2	L7	V_{DD}	M11	KB_9
A4	GND	B8	C_4	C12	B_3	F11	A_7	J3	GND	L8	KB_0	M12	KA_2
A5	C_{11}	B9	C_2	C13	B_1	F12	A_6	J11	KA_8	L9	KB_4	M13	KA_3
A6	C_8	B10	B_{11}	D1	Y_{11}	F13	A_5	J12	$CWSEL_1$	L10	KB_8	N1	Z_5
A7	C_7	B11	B_9	D2	X_0	G1	Y_5	J13	$CWSEL_0$	L11	KA_1	N2	Z_8
A8	C_5	B12	B_6	D3	X_3	G2	Y_6	K1	Y_3	L12	KA_5	N3	Z_{10}
A9	C_3	B13	B_2	D11	CLK	G3	GND	K2	Z_0	L13	KA_6	N4	KC_1
A10	C_1	C1	X_1	D12	B_0	G11	A_3	K3	Z_3	M1	Z_2	N5	KC_3
A11	B_10	C2	X_2	D13	A_{10}	G12	A_2	K11	KA_4	M2	Z_7	N6	KC_5
A12	B_7	C3	X_6	E1	Y_9	G13	A_4	K12	KA_7	M3	Z_9	N7	KC_7
A13	B_4	C4	V_{DD}	E2	Y_{10}	H1	Y_4	K13	KA_9	M4	Z_{11}	N8	KC_8
B1	X_4	C5	GND	E3	GND	H2	Y_0	L1	Z_1	M5	KC_2	N9	KB_1
B2	X_5	C6	C_{10}	E11	A_{11}	H3	V_{DD}	L2	Z_4	M6	KC_4	N10	KB_3
B3	X_8	C7	GND	E12	A_9	H11	GND	L3	Z_6	M7	KC_6	N11	KB_6
B4	X_{11}	C8	V_{DD}	E13	A_8	H12	A_0	L4	GND	M8	KC_9	N12	KB_7
												N13	KA_0

Note: Pin D4 has no electrical connection. It is a mechanical orientation pin.



Ordering Information

Product Number	Speed MHz	Temperature Range	Screening	Package	Package Marking
TMC2272H5C	30	STD-TA = 0°C to 70°C	Commercial	121 Pin Plastic PGA	2272H5C
TMC2272H5C-1	36	STD-TA = 0°C to 70°C	Commercial	121 Pin Plastic PGA	2272H5C-1
TMC2272H5C-2	40	STD-T_A = 0°C to 70°C	Commercial	121 Pin Plastic PGA	2272H5C-2

All parameters in this specification are guaranteed by design, characterization, sample testing ot 100% testing, as appropriate.
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TMC2301

CMOS Image Resampling Sequencer

15, 18MHz

The TMC2301 is a VLSI circuit which supports image resampling, rotation, rescaling, and filtering by generating input bit plane, interpolation coefficient lookup table, and output bit plane memory addresses along with external multiplier – accumulator control signals. The TMC2301 can process data fields of up to 4096 x 4096 multibit words at a clock rate of up to 18MHz. An IRS – based system can nearest – neighbor resample a 512 x 512 image in 15 milliseconds, translating, zooming, rotating, or warping it, depending on the transform parameter set loaded. A complete bilinear interpolation of the same image can be completed in 60 milliseconds. Image resampling speed is independent of the angle of rotation, degree of warp, or amount of zoom specified.

A high performance, TMC2301 – based system can execute bilinear and cubic convolution algorithms that rotate images accurately and in real time. Keystone or other perspective correction, image plane distortion, and numerous other second order polynomial transformations can be programmed and executed under direct user control. Direct access to the interpolation coefficient lookup table allows dynamic modification of the algorithm.

Following an initialization with the transform parameters and control bits defining the operation to be executed, the IRS assumes control of the input and output data fields and executes unattended. Data word size is user selectable. All inputs except INTER and all outputs are registered on the rising edge of clock. All outputs are three – state controlled except ACC, CZERO, END, and DONE.

Fabricated in TRW's OMICRON – C™ one micron CMOS process, the TMC2301 operates at clock rates of up to 18MHz over the full commercial (0 to 70°C) temperature and 15MHz over the extended (–55 to +125°C) temperature and supply voltage ranges. All signals are TTL compatible.

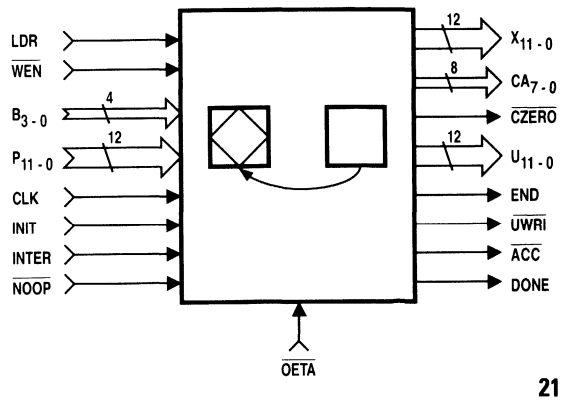
Features

- Rotation, Warping, Panning, Zooming, And Compression Of Images In Real Time
- 18MHz Clock Rate
- 4096 x 4096 Image Field Addressing Capability
- User – Selectable Nearest – Neighbor, Bilinear Interpolation, And Cubic Convolution Resampling Algorithms
- Static Convolutional Filtering Of Up To 16 x 16 Pixel Windows
- Single – Pass Or Two – Pass Convolution Operations
- Low Power – Consumption CMOS Process
- Single 5V Power Supply
- Available In A 68 Pin Grid Array And Low – Cost Plastic Leaded Chip Carrier (J – Bend)

Applications

- Video Special – Effects Generators
- Image Recognition Systems, Robotics
- Artificial Intelligence
- High – Precision Image Registration (LANDSAT Processing)
- High – Speed Data Encoding/Decoding
- General Purpose Image Processing
- Image Data Compression

Logic Symbol



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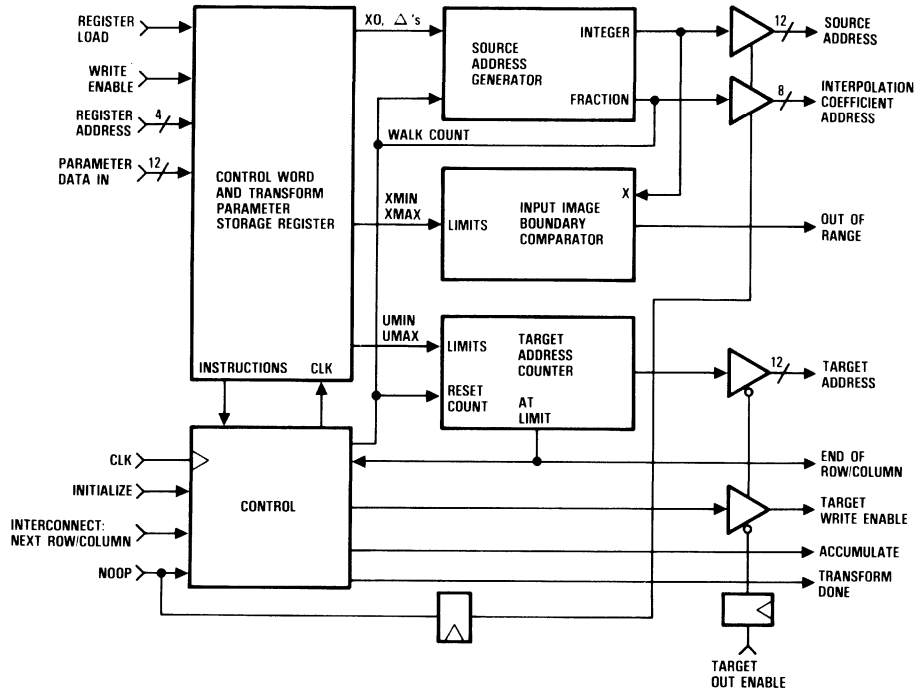
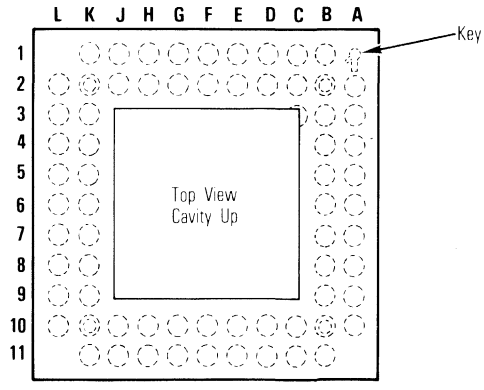
Functional Block Diagram

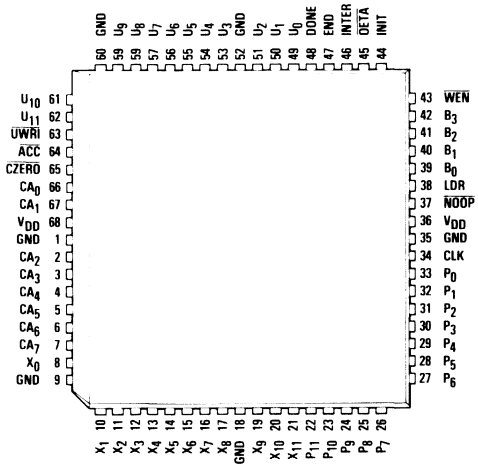


Pin Assignments – 68 Pin Grid Array, G8 or H8 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B2	INIT	K2	U_{10}	K10	X_1	B10	P_6
B1	$\overline{OETA}$	L2	U_{11}	K11	X_2	A10	P_5
C2	INTER	K3	$\overline{UWRI}$	J10	X_3	B9	P_4
C1	END	L3	$\overline{ACC}$	J11	X_4	A9	P_3
D2	DONE	K4	$\overline{CZERO}$	H10	X_5	B8	P_2
D1	U_0	L4	CA_0	H11	X_6	A8	P_1
E2	U_1	K5	CA_1	G10	X_7	B7	P_0
E1	U_2	L5	V_{DD}	G11	X_8	A7	CLK
F2	GND	K6	GND	F10	GND	B6	GND
F1	U_3	L6	CA_2	F11	X_9	A6	V_{DD}
G2	U_4	K7	CA_3	E10	X_{10}	B5	$\overline{NOOP}$
G1	U_5	L7	CA_4	E11	X_{11}	A5	LDR
H2	U_6	K8	CA_5	D10	P_{11}	B4	B_0
H1	U_7	L8	CA_6	D11	P_{10}	A4	B_1
J2	U_8	K9	CA_7	C10	P_9	B3	B_2
J1	U_9	L9	X_0	C11	P_8	A3	B_3
K1	GND	L10	GND	B11	P_7	A2	$\overline{WEN}$



Pin Assignments



68 Leaded (J Bend) Plastic Chip Carrier – L1 or R1 Package

Functional Description

General Information

The IRS is a versatile self–sequencing address generator designed primarily to filter a two–dimensional image or to remap and resample it from one set of Cartesian coordinates (x, y) into a new, transformed set (u, v). Most applications use two identical devices in tandem, one generating the row coordinates (X and U), the other generating the column coordinates (Y and V). The algorithm performed by the TMC2301 consists of two steps: a coordinate system transformation, followed by pixel interpolation. Interpolation is necessary when the transformed pixel positions (U, V) do not coincide with the original pixel positions (X, Y). The new pixel intensity values are obtained by interpolating the original pixels in the neighborhood of the transformed pixel positions. See Figure 1.

The IRS executes a general second order coordinate transformation of the form:

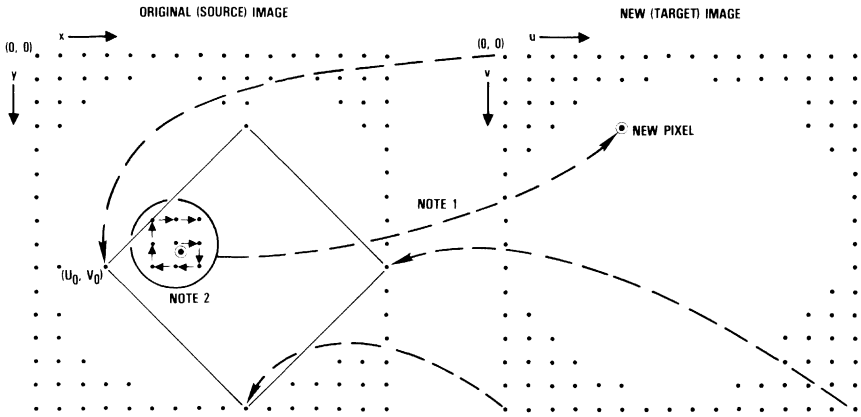
$$X(u, v) = Au^2 + Bu + Cuv + Dv^2 + Ev + F$$
$$Y(u, v) = Gu^2 + Hu + Kuv + Lv^2 + Mv + N$$

where A through N are user–defined parameters. It steps sequentially through the pixels of a user–defined rectangle in the new set of coordinates, computing the "old" address (X, Y) corresponding to each "new" location (U, V).

The TMC2301 uses the external multiplier–accumulator, connected to the system clock, to calculate the interpolated pixel value by summing the products of the original pixel values stored in the source buffer RAM and the appropriate weights from the polynomial transform lookup table. The new interpolated image value is then stored in the corresponding (U, V) memory location. Finally, the new image address is incremented by one pixel in the "U" direction or reset to the start of the next line (with "V" incremented), proceeding line–by–line through the entire destination image.

The TMC2301 can support any nearest neighbor, bilinear, or cubic resampling, according to the user's requirements. The bilinear and cubic kernels require a coefficient lookup table and multiplier–accumulator. Both one–pass and two–pass algorithms are supported. Sophisticated "walkaround" algorithms implementing static filters are also easily realized, utilizing convolutional kernels of up to 16 x 16 pixels. Both one and two–pass algorithms are supported. For each output point in a typical static single–pass filter, the IRS will generate a series of addresses, "walking" around that point in two dimensions. At the end of each walk, it will advance one pixel along the output scan line, then begin the walk for the next pixel.

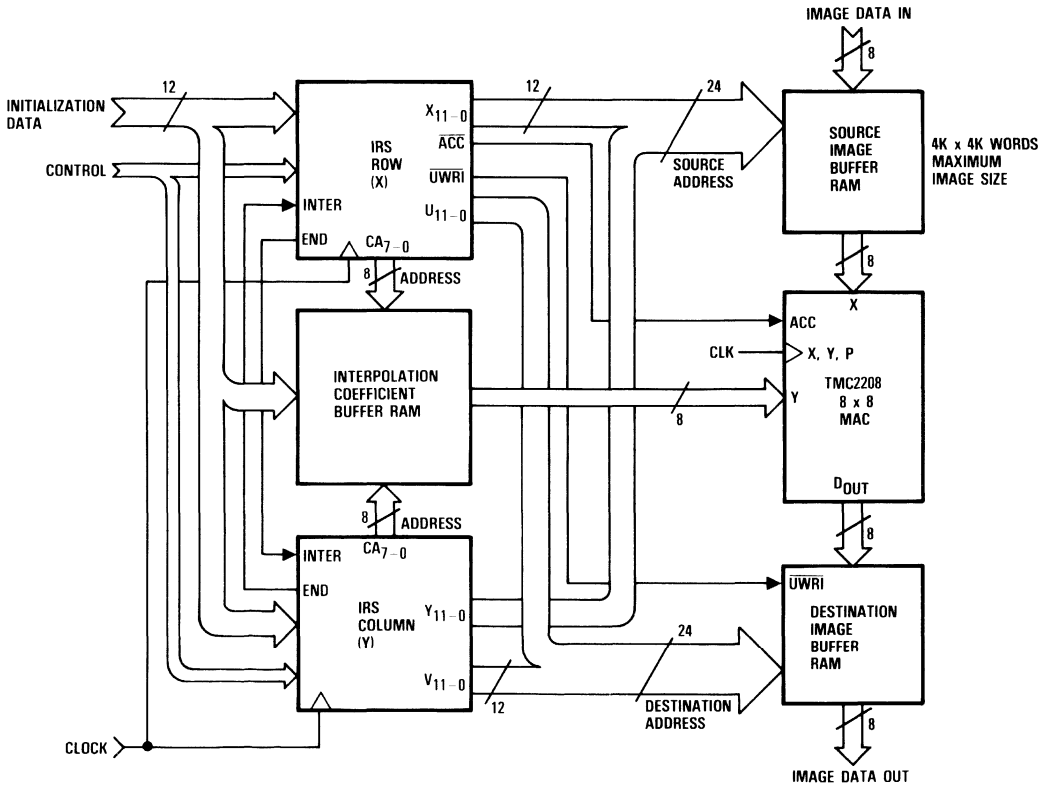
Figure 1. Image Resampling Geometry Showing Image Rotation and Expansion



Notes:
1. Coordinate transformation U, V pixel mapped into X, Y coordinates.
2. Pixel interpolation walk new U, V pixel intensity calculated from surrounding X, Y pixel neighborhood.

A basic TMC2301-based system is shown in Figure 2. In this typical system, two Image Resampling Sequencers process the image. The only other external parts needed are a multiplier-accumulator, external interpolation coefficient lookup table RAM, and the user-specified Source and Destination Image Memory.

Figure 2. Basic 2-D Image Convolver Using TMC2301 Image Resampling Sequencer Utilizing Typical 8-Bit Data Path



Signal Definitions

Power

V_{DD}, GND — The TMC2301 operates from a single +5V supply. All pins must be connected.

Clock

CLK — The TMC2301 has a single clock input. The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

P_{11-0} — The coordinate transformation parameters are loaded through the registered 12-bit P input port. P_{11} is the Most Significant Bit.

B_{3-0} — The write addresses for the individual coordinate transform parameters are presented at the registered 4-bit B input port. B_3 is the Most Significant Bit.

Outputs

X_{11-0} — The current X (or Y) source pixel address of the image being resampled is indicated by the registered 12-bit X_{11-0} output bus. This output is forced to the high impedance state when $\overline{NOOP}$ is LOW. X_{11} is the Most Significant Bit.

CA_{7-0} — The current interpolation kernel coefficient lookup table address is indicated by the registered 8-bit CA_{7-0} output bus. This output is forced to the high impedance state when $\overline{NOOP}$ is LOW. CA_7 is the Most Significant Bit.

U_{11-0} — The U (or V) target address of the image being generated is indicated by the registered 12-bit U_{11-0} output bus. This output is forced to the high impedance state when $\overline{OETA}$ is HIGH. U_{11} is the Most Significant Bit.

Controls

INIT — The control logic is cleared and initialized for the start of a new image transformation when the registered INIT input is HIGH for a minimum of two clock cycles. Normal operation begins after INIT goes LOW.

$\overline{WEN}$ — The registered Write Enable input allows the transformation parameters to be written into the preload register indicated by the address at the B input port when LOW. See Figure 4.

LDR — The data held in all transformation parameter preload registers is latched into the storage registers when the registered input LDR is HIGH. When LDR is LOW, the parameters remain unchanged. See Figure 4.

$\overline{ACC}$ — The accumulation register of the external multiplier-accumulator is initialized by the registered $\overline{ACC}$ output. $\overline{ACC}$ goes LOW for one cycle at the start of each interpolation "walk," effectively clearing the storage register by loading in only the new first product. See Figure 9.

$\overline{UWRI}$ — After the end of each interpolation "walk," the Target Memory (U or V) Write Enable goes LOW for one clock cycle. See Figure 9. This registered output is forced to the high impedance state when $\overline{OETA}$ is HIGH.

INTER — In the common two-device system configuration, the Interconnect inputs are connected to the END flag outputs. The END flag from the row (X) sequencer thus indicates an "end of line" to the column (Y) device, while the column sequencer in turn sends a "bottom of frame" signal to the row device, forcing a reset of the address counter.

$\overline{NOOP}$ — The Clock is overridden when the registered input $\overline{NOOP}$ is LOW, holding all address generators in their current state. Also, the output buffers for the address busses X_{11-0} and CA_{7-0} are forced to the high impedance state. This allows the user access to all external memory. When $\overline{NOOP}$ goes HIGH, normal operation resumes on the next clock cycle.

$\overline{OETA}$ — The target memory outputs $\overline{UWRI}$ and address bus U_{11-0} are in the high-impedance state when the registered Output Enable input is HIGH. When $\overline{OETA}$ is LOW, they are enabled on the next clock cycle.

Flags

$\overline{CZERO}$ — The registered $\overline{CZERO}$ flag of a horizontal dimension TMC2301 goes HIGH if $X < 0$, $XMIN \leq X \leq XMAX$, or $X \geq 4096$ (1000 hex). It goes LOW if $0 \leq X < XMIN$ or $XMAX < X < 4096$. The logical AND of the $\overline{CZERO}$ flags of a two-dimensional pair of TMC2301s will go LOW when the source address falls outside a rectangle with vertices (XMIN, YMIN), (XMAX, YMIN), (XMIN, YMAX), and (XMAX, YMAX), denoting an invalid address. The external data path can be wired to substitute a selected background value whenever this AND = 0.

END — The registered END flag goes HIGH during the last pixel of the last walk in a row in the case of the row chip, and the last pixel of the last walk in a column in the column chip, in the two-device architecture. This output is used as the end-of-line and end-of-frame indicator in conjunction with the INTER inputs of both TMC2301s.

DONE — In the standard two-device system, a row sequencer DONE flag HIGH after the last walk at the end of the last row of an image (during $\overline{UWRI}$ LOW) indicates the end of the transform. This registered output is usually ignored on the column device. See the Transformation Control Parameters, AUTOINIT.

Package Interconnections

Signal Type	Signal Name	Function	G8, H8 Package Pins	L1, R1 Package Pins
Power	V_{DD}	Supply Voltage	L5, A6	36, 68
	GND	Ground	F2, K1, K6, L10, F10, B6	1, 9, 18, 35, 52, 60
Clock	CLK	System Clock	A7	34
Inputs	P_{11-0}	Parameter Register Data	D10, D11, C10, C11, B11, B10, A10, B9, A9, B8, A8, B7	22, 23, 24, 25, 26, 27 28, 29, 30, 31, 32, 33
	B_{3-0}	Parameter Register Address	A3, B3, A4, B4	42, 41, 40, 39
Outputs	X_{11-0}	Source Address	E11, E10, F11, G11, G10, H11 H10, J11, J10, K11, K10, L9	21, 20, 19, 17, 16, 15, 14, 13, 12, 11, 10, 8
	CA_{7-0}	Coefficient Address	K9, L8, K8, L7, K7, L6, K5, L4	7, 6, 5, 4, 3, 2, 67, 66
	U_{11-0}	Target Address	L2, K2, J1, J2, H1, H2, G1, G2, F1, E1, E2, D1	62, 61, 59, 58, 57, 56, 55, 54, 53, 51, 50, 49
Controls	INIT	Initialize	B2	44
	$\overline{NOOP}$	No Operation	B5	37
	$\overline{WEN}$	Parameter Write Enable	A2	43
	LDR	Lead Parameter Data Registers	A5	38
	$\overline{ACC}$	Accumulate	L3	64
	$\overline{OETA}$	Target Memory Output Enable	B1	45
	$\overline{UWRI}$	Target Memory Write Enable	K3	63
	INTER	Interconnect	C2	46
Flags	$\overline{CZERO}$	Coefficient Zero	K4	65
	END	End of Row/Page	C1	47
	DONE	End of Transform	D2	48

Transformation Control Parameters

The TMC2301 is a self-sequencing device which requires no cycle-to-cycle intervention from the host system. To program the device, the user loads the 16 operating parameters, which define the transformation to be performed, which sections of the original and resampled image spaces are to be utilized, and various control words. Filtering operations are further defined by the values the user loads into the external coefficient memory. The transform parameters are described below. See also Tables 1 through 3.

XMIN, XMAX, YMIN, YMAX — These four parameters outline the "source" rectangular region of the original image. Whenever the IRS pair generates an (X, Y) address within this boundary the $\overline{CZERO}$ flags will denote a valid memory read. In the most common case, XMIN < XMAX, YMIN < YMAX, 000h < X < FFFh <, and 000h < Y < FFFh. In this case, addresses out-of-bounds cause one or both $\overline{CZEROs}$ to go LOW. Refer to Application Note TP-38 for further information on other boundary violation cases. Each parameter is expressed in 12-bit unsigned binary integer notation. See Figure 12.

UMIN, UMAX, VMIN, VMAX — These four parameters outline the "target" region of the (u, v) plane, into which the resampled image will be written. The IRS will generate, line by line, a scan that fills only this portion of the plane, permitting the user to assemble a mosaic of multiple rectangular subimages. Care must be taken to ensure that UMAX > UMIN and VMAX > VMIN. Each parameter is expressed in 12-bit unsigned binary integer notation. See Figure 12.

(X_0, Y_0) — These are the coordinates of the first pixel to be read from the original image. In many applications, this point will be one of the four corners of the original image to be resampled. The pixels near (X_0, Y_0) in the original image will be used to compute the upper left pixel of the transformed image. In non-inverting, non-reversing applications (X_0, Y_0) will be the upper left corner of the original subimage. Each coordinate is expressed in 13-bit integer plus 5-bit fraction, two's complement notation.

dX/dU_0 — Is the initial horizontal partial first derivative indicating the displacement along the X axis which corresponds to each one-pixel movement along the U axis. Usually, $0 < dX/dU_0 < 1$ corresponds to magnification, whereas $dX/dU_0 > 1$ represents reduction and $dX/dU_0 < 0$ denotes reflection about a vertical axis. The first derivatives are expressed in 8-bit integer, 12-bit fraction two's complement notation.

dX/dV_0 — Is the initial horizontal-vertical partial first derivative. It indicates the displacement along the X axis corresponding to each one-pixel movement along the V axis. The coefficients dX/dV_0 and dY/dU_0 define image rotation and shear.

dY/dU_0 — Is the initial vertical-horizontal partial first derivative. It indicates the displacement along the Y axis corresponding to each one-pixel movement along the U axis.

dY/dV_0 — Is the initial vertical partial first derivative. It indicates the displacement along the Y axis corresponding to each one-pixel step along the V axis. Since dX/dU_0 and dY/dV_0 are separate parameters, vertical magnification and reflection need not match their horizontal counterparts.

NOTE: For each incremental move along the U axis, the starting point of the new "walk around spiral" is indexed to the ENDING point of the previous walk around spiral, rather than to its center. Therefore, the terms dX/dU_0 and dY/dU_0 must be adjusted accordingly. Since each new line is referenced back to the previous line's initial spiral starting point, no similar dX/dV_0 or dY/dV_0 correction is needed.

d^2X/dU^2 — Is the second order horizontal derivative. It indicates the rate of change of the horizontal-horizontal first derivative with each step along a line in the output image space. All six second-order derivatives are 4-bit integer, 20-bit fractional two's complement parameters.

d^2X/dV^2 Is the second order horizontal-vertical-vertical derivative. It indicates the rate of change of the horizontal-vertical first derivative with each step down a column in the output image space.

d^2Y/dU^2 Is the second order vertical-horizontal-horizontal derivative. It indicates the rate of change of the the vertical-horizontal first derivative with each step along a line of the output image space.

d^2Y/dV^2 Is the second order vertical derivative. It indicates the rate of change of the vertical-vertical first derivative with each step down a column of the output image space.

$d^2X/dUdV$ Is the mixed second order derivative indicating the rate of change of the first order horizontal derivative as one proceeds downwards through the output image space. This is also the rate of change of the first order horizontal-vertical derivative during horizontal sweeps in the output image space.

$d^2Y/dUdV$ Is the mixed second order derivative indicating the rate of change of the first order vertical derivative as one moves horizontally across the output space, or, equivalently, the rate of change of the first order vertical-horizontal derivative as one moves vertically in the output image space.

Row/Column Select Sets the mode to either Row (0) or Column (1) operation.

Mode This 2-bit control word defines three unique instructions:

Code	Instruction
00, 01	single-pass operation
10	pass 1 of two-pass operation
11	pass 2 of two-pass operation

In single-pass operation, the device walks through the entire (k + 1) x (k + 1) kernel for each output pixel, where k is the value written into the Kernel section (see below) of the parameter register. Two-pass operation, which requires a dimensionally separable kernel, is executed first for a (k + 1) element kernel in one direction, then for a (k + 1) element kernel in the other direction. For kernel sizes exceeding 2 x 2, the two-pass algorithm is obviously beneficial, requiring 2n samples per output point instead of n x n. In this case, the intermediate image data stored in the destination image memory following the first pass is used as the source image data on the second pass. The user may design his system to switch source and destination memory bank addresses in place, or could utilize a second TMC2301 pair in a pipelined architecture. This would require a third image buffer for the final destination image. Both devices of a system pair are usually set to the same mode.

Kernel The effective kernel width (height) exceeds this 4-bit unsigned number by 1, thereby providing kernels of 1 x 1 to 16 x 16 source pixels per output, for either resampling or filtering. Simple static filters can be implemented with kernels of up to 16 x 16 pixels (Kernel = 15), while resampling interpolation kernels are limited to 4 x 4 pixels (Kernel = 3), due to the four bits of fractional X (or Y) address generated by the TMC2301. See the Applications Discussion, below. Again, both devices in a pair are generally initialized with equal Kernel values.

Field of View (FOV) As the device walks through its kernel coefficients, each corresponding step in (x, y) space is normally one pixel length or height; this is a field of view of 1. However, the user can subsample the original space before filtering or resampling, by applying the coefficient kernel over a view field of up to 7 units. At a field of view of F, the pixels selected for each kernel operation are F pixels apart. This is useful in oversampled pictures, whose intensity changes only slowly from pixel to pixel.

Autoload (ALR) When set to 1 (HIGH), the LDR control is automatically asserted when INIT is strobed, loading the coefficient set currently stored in the preload registers.

Autoinit (AIN) At the end of an image, if the AIN bit is 1 (HIGH) the DONE flag goes HIGH for one clock cycle and a new transform begins. If 0 (LOW), $\overline{\text{UWRI}}$ and the DONE flag remain HIGH during the sequence until the user strobes the INIT control to begin a new image transformation.

Pipe (PIPE) — Adjusts the timing of the target memory write controls, to compensate for buffered source image RAM. If the PIPE bit is 1 (HIGH), outputs $\overline{ACC}$ and $\overline{UWRI}$ will be delayed one clock cycle relative to the generation of the target address (U or V). See Figure 9.

Test Mode (TM) — This mode is available for user inspection of the coefficient data. The source image and coefficient addresses are calculated by an internal 28-bit accumulator. When TM is 1 (HIGH), the sign bit, normally discarded, and the lower 11 bits of internal data are substituted for the upper 12 bits appearing at the source address port (X) during a standard transform cycle. This allows user verification of algorithm mathematics during debug. Since the TM bit is registered and cannot be changed during a single clock cycle, two distinct clock cycles are required to access both the MSW and LSW of the internal accumulator. See Figure 3.

Figure 3. Test Mode Data Routing

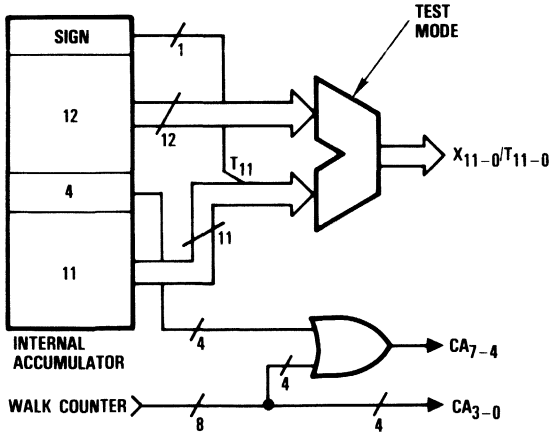


Table 1. Parameter Registers – Row Sequencer

Address	Name	Description
0000	XMIN	Left side of Source Window
0001	XMAX	Right side of Source Window
0010	X_0 (LSW)	Source starting point – X coordinate
0011	X_0 (MSW)	Source starting point – X coordinate
0011	Controls	Mode Select Bits
0100	dX/dU_0 (LSW)	Row/Row first differential
0101	dX/dU_0 (MSW)	Row/Row first differential
0101	TM, FOV	Test Mode, Field of View
0110	dX/dV_0 (LSW)	Row/Column first differential
0111	dX/dV_0 (MSW)	Row/Column first differential
0111	Kernel	Resampling/Filtering Kernel
1000	$d^2X/dUdV$ (LSW)	Mixed second differential
1001	$d^2X/dUdV$ (MSW)	Mixed second differential
1010	d^2X/dU^2 (LSW)	Row second differential
1011	d^2X/dU^2 (MSW)	Row second differential
1100	d^2X/dV^2 (LSW)	Row/Column second differential
1101	d^2X/dV^2 (MSW)	Row/Column second differential
1110	UMIN	Left edge of Final Image
1111	UMAX	Right edge of Final Image

Table 2. Parameter Registers – Column Sequencer

Address	Name	Description
0000	YMIN	Top of Source Window
0001	YMAX	Bottom of Source Window
0010	Y_0 (LSW)	Source starting point – Y coordinate
0011	Y_0 (MSW)	Source starting point – Y coordinate
0011	Controls	Mode Select Bits
0100	dY/dU_0 (LSW)	Column/Row first differential
0101	dY/dU_0 (MSW)	Column/Row first differential
0101	TM, FOV	Test Mode, Field of View
0110	dY/dV_0 (LSW)	Column/Column first differential
0111	dY/dV_0 (MSW)	Column/Column first differential
0111	Kernel	Resampling/Filtering Kernel Size
1000	$d^2Y/dUdV$ (LSW)	Mixed second differential
1001	$d^2Y/dUdV$ (MSW)	Mixed second differential
1010	d^2Y/dU^2 (LSW)	Column/Row second differential
1011	d^2Y/dU^2 (MSW)	Column/Row second differential
1100	d^2Y/dV^2 (LSW)	Column second differential
1101	d^2Y/dV^2 (MSW)	Column second differential
1110	VMIN	Top edge of Final Image
1111	VMAX	Bottom edge of Final Image

Table 3. Parameter Registers Binary Format (Row Or Column Sequencer)

Addr	Format												Limits	
	MSB											LSB	Dec	Hex
0000*	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
0001*	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
0010	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	$4096-2^{-5}$	0FFF.F8
0011							-2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	-4096	F000.00
0011 (Control)	ALR	AIN	PIPE	R/C	M_1	M_0								
0100	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	$128-2^{-12}$	007F.FFF
0101					-2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	-128	FF80.000
0101* (TM, FOV)	TM	2^{2}	2^{1}	2^{0}										
0110	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	$128-2^{-12}$	007F.FFF
0111					-2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	-128	FF80.000
0111* (Kernel)	2^{3}	2^{2}	2^{1}	2^{0}										
1000	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	$8-2^{-20}$	0007.FFFFF
1001	-2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	-8	FFF8.00000
1010	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	$8-2^{-20}$	0007.FFFFF
1011	-2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	-8	FFF8.00000
1100	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	$8-2^{-20}$	0007.FFFFF
1101	-2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	-8	FFF8.00000
1110*	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
1111*	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000

* unsigned binary notation

A "−" indicates MSB is sign bit

Operation of the Transformation Parameter Registers

Numerous applications require the ability to update the coordinate transformation parameters "on the fly." Because the parameters are double-buffered, the user can load any or all of them into the preload registers without upsetting the operation in progress. Then LDR (load data registers) will update all transform parameters to the new values simultaneously. This feature is particularly valuable for "pin cushion" and "fish eye" transformations, or polar-to-rectangular conversions, which cannot be performed with constant second derivatives. The Autoload function updates the preload registers at the beginning of a new image automatically. See the Transformation Control Parameters section. Note also that data can be loaded in to the registers while $\overline{\text{NOOP}}$ is active (LOW).

Figure 4. Operation of LDR Control for Parameter Update

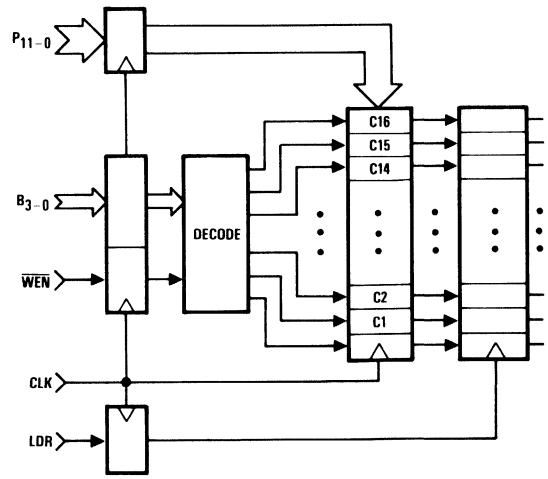
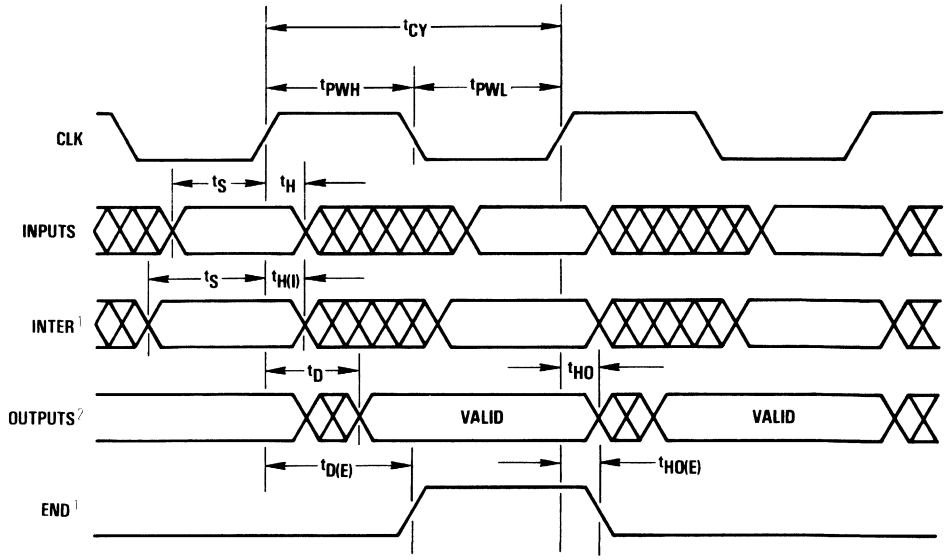


Figure 5. Timing Diagram



Notes:

1. t_S and $t_{D(E)}$ are guaranteed to allow full speed operation in the standard two-device architecture. See text.
2. All outputs except END. See text.

Figure 6. Equivalent Input Circuit

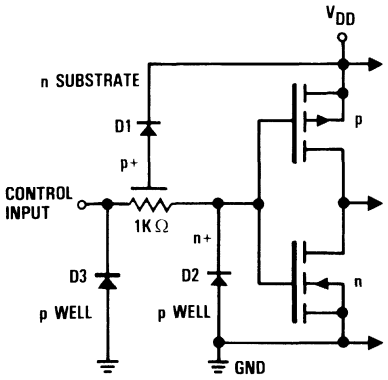


Figure 7. Equivalent Output Circuit

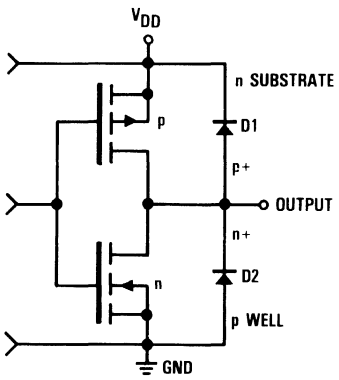
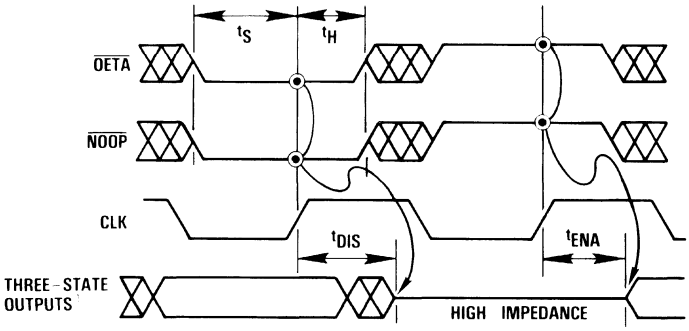


Figure 8. Transition Level for Three-State Measurement



Note:
1. All outputs except $\overline{ZERO}$, $\overline{ACC}$, END and DONE.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} +0.5)V
Output	
Applied voltage [2]	−0.5 to (V_{DD} +0.5)V
Forced current [3,4]	−1.0 to +6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Extended Min	Extended Nom	Extended Max	Units
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			8.0			8.0	mA
I_{OH}	Output Current, Logic HIGH			-4.0			-4.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				-55		125	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		5		5	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 15MHz		75		75	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	-10	+10	-75	+75	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Min, V_{IN} = V_{DD}	-10	+10	-75	+75	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Min, V_{IN} = 0V	-40	+ 40	-40	+ 40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Min, V_{IN} = V_{DD}	-40	+ 40	-40	+ 40	μA
I_{OS}	Short-Circuit Output Current [2]	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		-100		-100	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Notes:

1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Guaranteed but not tested.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard −1 Min	Standard −1 Max	Standard Min	Standard Max	Extended Min	Extended Max	Units
t_{CY}	Cycle Time	V_{DD} = Min	55		66		66		ns
t_{PWL}	Clock Pulse Width LOW	V_{DD} = Min	25		30		30		ns
t_{PWH}	Clock Pulse Width HIGH	V_{DD} = Min	25		30		30		ns
t_S	Input Setup Time[1]		18		20		20		ns
t_H	Input Hold Time		2		2		2		ns
$t_{H(I)}$	Input Hold Time, INTER		10		10		10		ns
t_D	Output Delay[2]	V_{DD} = Min, C_{LOAD} = 40pF		27		35		35	ns
$t_{D(E)}$	Output Delay, END[1]	V_{DD} = Min, C_{LOAD} = 10pF		37		45		45	ns
t_{HO}	Output Hold Time[2]	V_{DD} = Max, C_{LOAD} = 40pF	5		5		5		ns
$t_{HO(E)}$	Output Hold Time, END	V_{DD} = Max, C_{LOAD} = 10pF	10		10		10		ns
t_{DIS}	Three-State Disable Delay	V_{DD} = Min, C_{LOAD} = 40pF		18		20		20	ns
t_{ENA}	Three-State Enable Delay	V_{DD} = Min, C_{LOAD} = 40pF	27		35		35		ns

Notes:
1. $t_S + t_{D(E)} = t_{CY}$ max.
2. Excluding output pin END.

Applications Discussion

Basic Operation

Each TMC2301 pair contains address controllers which execute patterns much like the following FORTRAN 3-level nested DO loop:

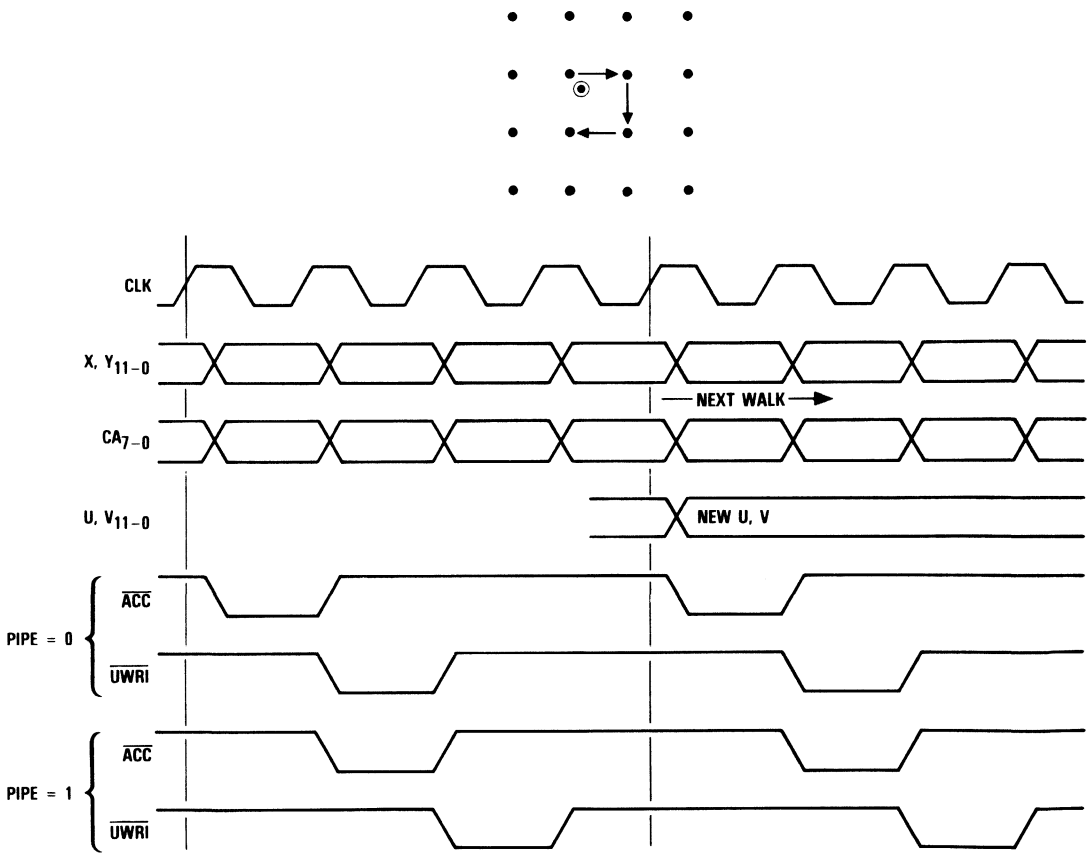
1. The inner loop is a clockwise outgoing spiral "walk" through the N-element coefficient kernel.
2. The middle loop is a left-to-right "scan" along each row of the output image space.
3. Finally, the outer loop is a top-to-bottom "scan" down each column of the output image space.

A typical one-pass image transformation proceeds as follows:

1. The device pair outputs the addresses (X_0, Y_0), which is the first point in the source image, and (CAX, CAY), the interpolation lookup table address for the first pixel in the kernel. The output $\overline{ACC}$ goes LOW, causing the external accumulator to load the first product without summation, clearing the accumulator.
2. For the next N cycles, the IRS walks through an outward clockwise spiral in (x, y) space, accumulating pixel-interpolation coefficient products. The spiral sequence is depicted in Figure 9.
3. After the completion of the first spiral walk, the IRS outputs the target address of the first pixel, (UMIN, VMIN) and the control $\overline{UWRI}$, along with the initial (X, Y) values of the next spiral walk. $\overline{ACC}$ and $\overline{UWRI}$ can be delayed by one clock cycle by setting the control bit PIPE to 1 (HIGH), simplifying the task of interfacing the TMC2301 to buffered source image memory.
4. After the last cycle of the next spiral, $\overline{UWRI}$ again goes LOW for one clock, and the target address outputs are updated, pointing to the location of the pixel calculation just completed, (UMIN + 1, VMIN).

5. The third spiral walk begins with $\overline{ACC}$ going LOW, and ends with (UMIN + 2, VMIN) output and $\overline{UWRI}$ going LOW.
6. he procedure continues until (UMAX + 1, VMIN) is reached, at which point the device resets to U (position within row) and increments V (number of row). Thus, the next (U, V) set after (UMAX + 1, VMIN) will be (UMIN, VMIN + 1), followed by (UMIN + 1, VMIN + 1), etc.
7. Upon completion of the walk corresponding to (UMAX + 1, VMAX + 1), the TMC2301 will generate a DONE flag with the final UWRI, and begin a new sequence.

Figure 9. Timing Diagram and Pixel Map Showing Outward Clockwise Spiral Walk Generated by TMC2301 (2 x 2 Kernel Shown)



Notes:
1. Assumes that $\overline{OETA}$ is LOW and $\overline{NOOP}$ is HIGH.
2. Timing Parameters are not shown on this diagram.

On any given clock cycle, the actual (X, Y) and (U, V) outputs of the IRS are given by the following equations:

$$x = X_0 + dX/dU_0 * m + dX/dV_0 * n + d^2X/dUdV * m * n + d^2X/dU^2 * (m^2 - m)/2 + d^2X/dV^2 * (n^2 - n)/2^0 + FOV * CAX(w) + FOV * m * CAX(Ker)$$

$$y = Y_0 + dY/dU_0 * m + dX/dV_0 * n + d^2Y/dUdV * m * n + d^2Y/dU^2 * (m^2 - m)/2 + d^2Y/dV^2 * (n^2 - n)/2^0 + FOV * CAY(w) + FOV * m * CAY(Ker)$$

$$u = UMIN + m$$

$$v = VMIN + n$$

where FOV is the 4-bit field of view parameter, normally set to 1 so that the spiral walk proceeds in single-pixel steps. Setting FOV to 4 would expand the spiral walk, allowing the user to trade two bits of image size for two bits of additional interpixel positioning resolution. CAX(w) and CAY(w) are the current value of the coefficient address outputs, and CAX(KER) and CAY(KER) are the terminal values of each pixel walk. The CA(KER) terms arise because the IRS computes each new walk's starting point from the previous spiral walk's end point, rather than its starting point.

Interpolation Coefficient Lookup Table Addressing

The external coefficient lookup table RAM stores the interpolation values used to calculate the value of the new pixel. These values are selected by the user, allowing maximum filtering flexibility. In simple filtering applications, all 8 bits of coefficient address are available to access up to 256 interpolation coefficients, for kernels of 16 x 16 pixels. This address is generated by the internal walk counter of the TMC2301. In most applications, the same Kernel parameter value is selected in both IRS devices; thus, the Coefficent Address outputs CA_{7-0} for the X and Y devices are identical, and the user needs only one of the 8-bit buses for memory access.

Applications executing a coordinate transformation, however, will almost always generate non-integer source pixel addresses; that is, the U (or V) locations will not map to the X (or Y) addresses exactly, and fractional address components are generated. The user then must account for this spatial offset in both dimensions by storing the appropriate corrected interpolation kernel values in the lookup table. The 8-bit address bus is broken up into two parts: the fractional portion (upper 4 bits), and the walk counter (lower 4 bits). Thus, in resampling applications, the maximum kernel size is 4 x 4 pixels, or 16 locations. As in the filtering example, assuming that the user has selected the same kernel size for both IRS devices, the 4 bits of least-significant address generated by both devices will be identical, and redundant. The four most significant address bits, however, will reflect the current fractional offsets of the resampled pixel from the nearest X (Y) location, to a spatial resolution of 4 bits, in the X (or Y) directions. Utilization of the 12 bits (total) of lookup table address is left to the user, to be arranged as desired for memory access. See Figure 3.

Application Examples

One of the more common applications for the TMC2301 is simple static filtering. In this case the source and target memories locations are identical and no coordinate transformation is performed. The (X, Y) and (U, V) outputs listed in Table 4 show the address sequencing generated by the TMC2301 to execute the walk of a 5 x 5 pixel interpolation kernel. The normalized coefficients shown implement a first-order Butterworth Low Pass Filter with cutoff radius of $1/\sqrt{2}$. Note that the (U, V) output address is updated following the completion of the walk for that location.

Figure 10. Pixel Map Showing Walk Sequence for 5 x 5 Static Filter

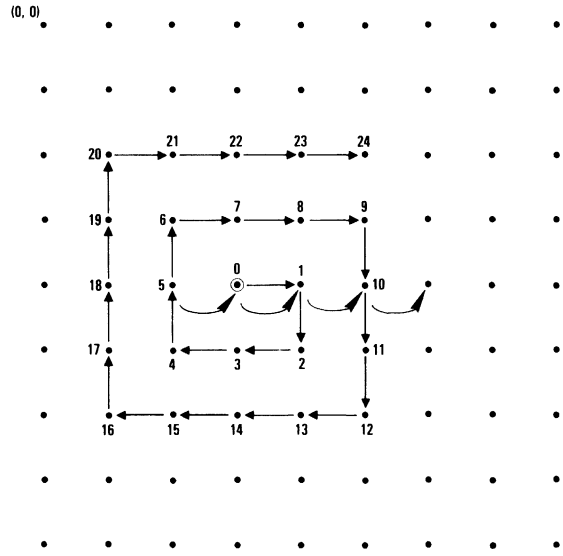


Table 4. IRS Outputs for Static Filter Illustrated in Figure 10

Cycle	X	Y	Index (CA)	Coefficient	U	V
1	3	4	0	0.2176	2	4
2	4	4	1	0.0725	2	4
3	4	5	2	0.0435	2	4
4	3	5	3	0.0725	2	4
5	2	5	4	0.0435	2	4
6	2	4	5	0.0725	2	4
7	2	3	6	0.0435	2	4
8	3	3	7	0.0725	2	4
9	4	3	8	0.0435	2	4
10	5	3	9	0.0198	2	4
11	5	4	10	0.0272	2	4
12	5	5	11	0.0198	2	4
13	5	6	12	0.0128	2	4
14	4	6	13	0.0198	2	4
15	3	6	14	0.0272	2	4
16	2	6	15	0.0198	2	4
17	1	6	16	0.0128	2	4
18	1	5	17	0.0198	2	4
19	1	4	18	0.0272	2	4
20	1	3	19	0.0198	2	4
21	1	2	20	0.0128	2	4
22	2	2	21	0.0198	2	4
23	3	2	22	0.0272	2	4
24	4	2	23	0.0198	2	4
25	5	2	24	0.0128	2	4
26	4	4	0	0.2175	3	4

Figure 11 illustrates the sequence for a bilinear resampling of a 63° rotation. The starting point is translated +1 in the Y-direction. A common rotation matrix might be:

$dX/dU_0 = \cos(a) = .6$ $\quad dY/dU_0 = \sin(a) = .8$

$dX/dV_0 = -\sin(a) = -.8$ $\quad dY/dV_0 = \cos(a) = .6$

However, we have included a linear compression factor of 5:1, and must accommodate the fact that each time u is incremented, the start of the new walk is referenced to the END of the previous walk. Given these corrections, the rotation matrix becomes:

$dX/dU_0 = 5\cos(a) = 3$ $\quad dY/dU_0 = 5\sin(a) - FOV = 3$

$dX/dV_0 = -5\sin(a) = -4$ $\quad dY/dV_0 = 5\cos(a) = 3$

Kernel = 1

Figure 11. Pixel Map Showing Parameters for 63° Rotation and 5:1 Compression Listed in Table 5

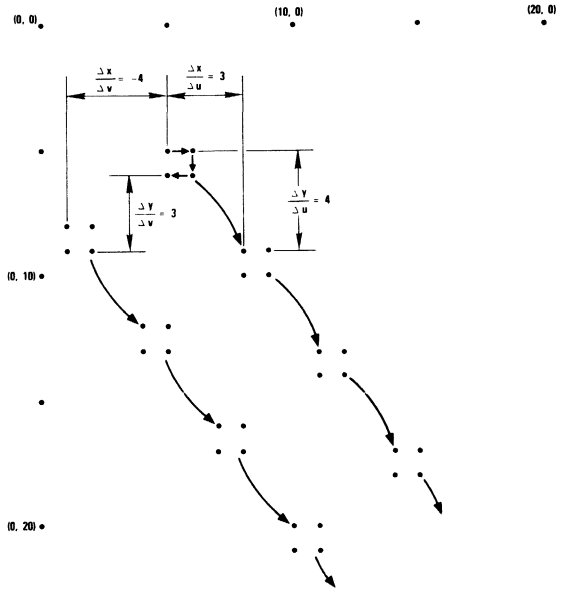
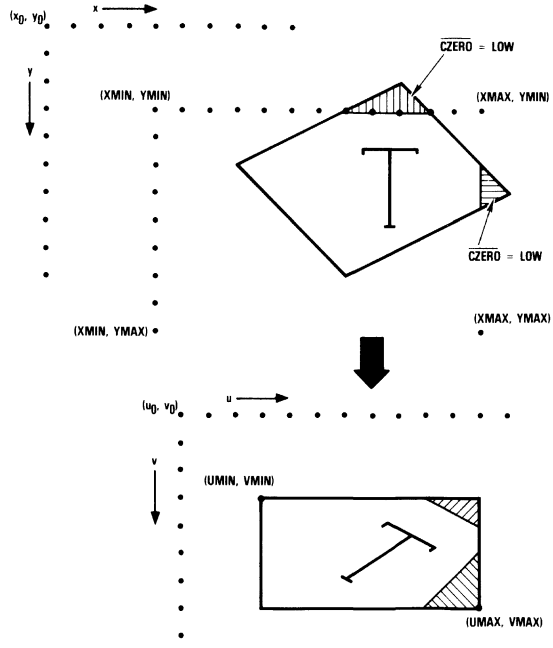


Table 5. IRS Outputs for Operation Illustrated in Figure 11

Cycle	X	Y	Index	U	V
1	5	5	0	4	5
2	6	5	1	4	5
3	6	6	2	4	5
4	5	6	3	4	5
5	8	9	0	5	5
6	9	9	1	5	5
7	9	10	2	5	5
8	8	10	3	5	5
9	11	13	0	6	5
10	12	13	1	6	5
11	12	14	2	6	5
12	11	14	3	6	5
13	14	17	0	7	5
14	15	17	1	7	5
15	15	18	2	7	5
16	14	18	3	7	5
17	1	8	0	8	5
18	2	8	1	8	5
19	2	9	2	8	5
20	1	9	3	8	5
21	4	12	0	5	6
22	5	12	1	5	6
23	5	13	2	5	6
24	4	13	3	5	6
25	7	16	0	6	6
26	8	16	1	6	6
27	8	17	2	6	6
28	7	17	3	6	6
29	10	20	0	7	6
30	11	20	1	7	6
31	11	21	2	7	6
32	10	21	3	7	6
33	0	15	0	8	6

Figure 12 may help clarify the relationships among (X_0, Y_0), (XMIN, YMIN), (XMAX, YMAX), (UMIN, VMIN), and (UMAX, VMAX). With positive first derivatives, (X_0, Y_0) and (UMIN, VMIN) represent the upper left corners of the original image and the new destination field, respectively. The lower right corner of the transformed image is located at (UMAX + 1, VMAX + 1); the location of the corresponding corner of the original image depends on the values of the derivatives. Not to be confused with (X_0, Y_0), the points (XMIN, YMIN) and (XMAX, YMAX) define the "usable" rectangular portion of the original image; points (X, Y) lying outside this region are ignored in most resampling and filtering applications. This feature permits one to construct a mosaic of several abutting subimages in the (x, y) plane, without danger of edge effect interference between adjacent subimages. Note in the figure that the upper left and lower left corners of the original image lie outside the admissible region; in practice, the values fetched at these locations will not be included in the convolutional sums.

Figure 12. Pixel Maps Demonstrating Source and Destination Image Boundaries and Image Clipping (Note Shaded Area)



Note: Assume 000h < X < FFFh
000h < Y < FFFh

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2301G8C2	STD – T_A = 0°C to 70°C	Commercial	68 Pin Grid Array	2301G8C2
TMC2301G8V	EXT – T_C = – 55°C to 125°C	MIL-STD-883	68 Pin Grid Array	2301G8V
TMC2301G8V1	EXT – T_C = – 55°C to 125°C	MIL-STD-883	68 Pin Grid Array	2301G8V1
TMC2301H8C	STD – T_A = 0°C to 70°C	Commercial	68 Pin Grid Array	2301H8C
TMC2301H8C1	STD – T_A = 0°C to 70°C	Commercial	68 Pin Grid Array	2301H8C1
TMC2301L1V	EXT – T_C = – 55°C to 125°C	MIL-STD-883	68 Leaded Hermetic Ceramic Chip Carrier	2301L1V
TMC2301L1V1	EXT – T_C = – 55°C to 125°C	MIL-STD-883	68 Leaded Hermetic Ceramic Chip Carrier	2301L1V1
TMC2301R1C	STD – T_A = 0°C to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	2301R1C
TMC2301R1C1	STD – T_A = 0°C to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	2301R1C1
TMC2301R1C2	STD – T_A = 0°C to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	2301R1C2

TMC2302

Image Manipulation Sequencer
40MHz

The TMC2302 is a high-speed self-sequencing VLSI circuit address generator which supports image resampling, rotation, rescaling, warping, and filtering. It generates input bit plane, interpolation coefficient lookup table, and output bit plane memory addresses along with pixel interpolator control signals.

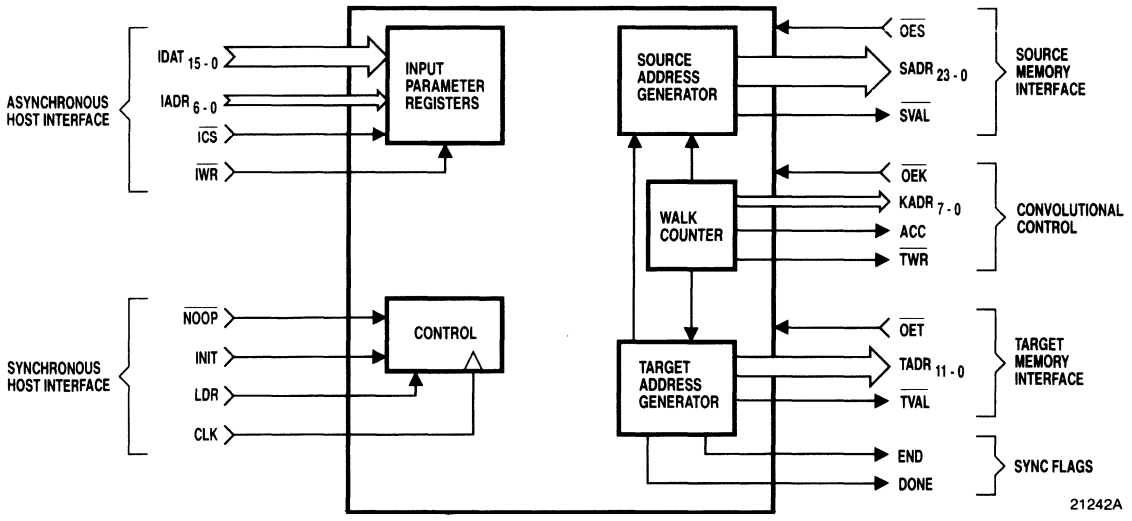
Similar in architecture to the TRW TMC2301 Image Resampling Sequencer, the TMC2302 features numerous enhancements. In addition to an increase in the maximum clock rate to 40MHz, the device offers three-dimensional address generation and implements two-dimensional image transformation polynomials of up to third order.

The TMC2302 can process image data fields with up to 24 bits of binary resolution (2^{24} pixels) per dimension, with 0 to 16-bit subpixel resolution.

A system based on two TMC2302s can nearest-neighbor resample a two-dimensional 512 x 512 pixel image in 6.5 milliseconds, translating, rotating, or warping it, depending on the user-selected transformation parameters. A complete bilinear interpolation of the same image can be completed in 26 milliseconds, while a nearest-neighbor resampling of a 3D image 128 pixels on a side takes only 53 milliseconds with three TMC2302s. Image resampling speed is independent of angle of rotation, degree of warp, or amount of zoom specified.

E

Simplified Block Diagram



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FAX: (619) 455-6314

40G06360 Rev. B–11/90
Printed in the U.S.A.

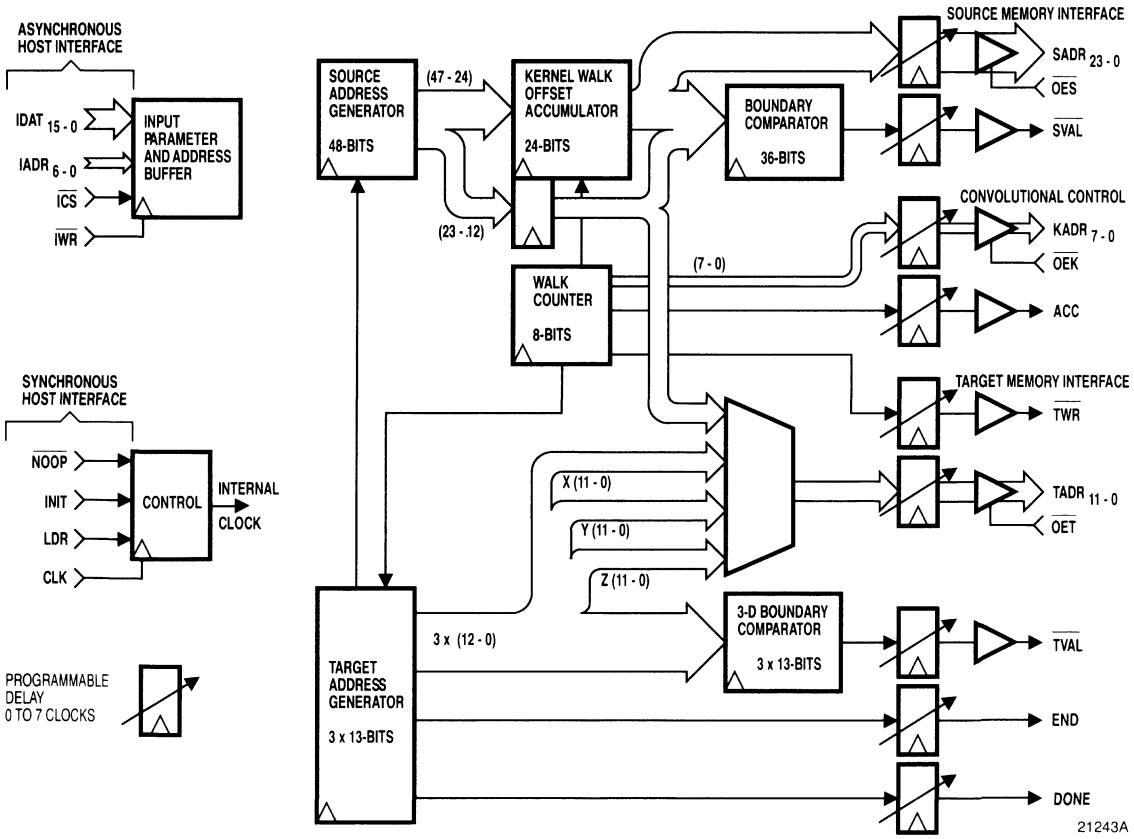
Features

- Asynchronous Loading Of Control Parameters
- Rapid (25ns Per Pixel) Rotation, Warping, Panning, And Scaling Of Images
- Three-Dimensional Image Addressing Capability
- General Third-Order Polynomial Transformations In Two Dimensions Implemented On-Chip; Three-Dimensional Transformation Of Up To Order 1.5 Also Supported
- Flexible, User-Configurable Pixel Datapath Timing Structure
- Static Convolutional Filtering Of Up To 16 x 16 Pixel (One-Pass), 256 x 256 Pixel (Two-Pass) Or 256 x 256 x 256 Pixel (Three-Pass) Windows
- User-Selectable Source Image Subpixel Resolution of 2^{-8} to 2^{-16}
- 24-Bit (Optional 36-Bit) Positioning Precision Within The Source Image Space, 48-Bit Internal Precision
- Low Power One-Micron OMICRON-C™ CMOS Process
- Available In A 120 Pin Plastic Pin Grid Array

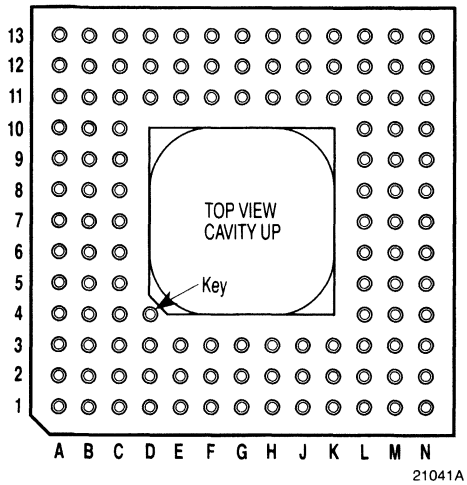
Applications

- High-Performance Video Special-Effects Generators
- Guidance Systems
- Image Recognition, Robotics
- High-Precision Image Registration (LANDSAT Processing)

Functional Block Diagram



Pin Assignments – 120 Pin Plastic Pin Grid Array, H5 Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
C3	V_{DD}	G3	V_{DD}	L3	$\overline{NC}$	L7	V_{DD}	L11	V_{DD}	G11	GND	C11	GND	C7	$IADR_5$
B2	$SADR_{15}$	G1	$SADR_6$	M2	$\overline{OEK}$	N7	$TADR_1$	M12	GND	G13	$IDAT_0$	B12	$IDAT_8$	A7	$IADR_6$
B1	$SADR_{14}$	H1	$SADR_5$	N2	$KADR_7$	N8	$TADR_2$	M13	$\overline{TVAL}$	F13	$IDAT_1$	A12	$IDAT_9$	A6	$\overline{OES}$
D3	GND	H2	$SADR_4$	L4	V_{DD}	M8	$TADR_3$	K11	V_{DD}	F12	GND	C10	$IDAT_{10}$	B6	$SADR_{23}$
C2	V_{DD}	H3	GND	M3	$KADR_6$	L8	$TADR_4$	L12	GND	F11	V_{DD}	B11	$IDAT_{11}$	C6	$SADR_{22}$
C1	$SADR_{13}$	J1	$SADR_3$	N3	$KADR_5$	N9	$TADR_5$	L13	$\overline{NOOP}$	E13	$IDAT_2$	A11	$IDAT_{12}$	A5	$SADR_{21}$
D2	$SADR_{12}$	J2	$SADR_2$	M4	$KADR_4$	M9	$TADR_6$	K12	INIT	E12	$IDAT_3$	B10	$IDAT_{13}$	B5	$SADR_{20}$
E3	GND	K1	$SADR_1$	L5	GND	N10	$TADR_7$	J11	V_{DD}	D13	$IDAT_4$	C9	$IDAT_{14}$	A4	V_{DD}
D1	$SADR_{11}$	J3	V_{DD}	N4	$KADR_3$	L9	$TADR_8$	K13	GND	E11	GND	A10	$IDAT_{15}$	C5	$SADR_{19}$
E2	$SADR_{10}$	K2	$\overline{SADR_0}$	M5	$KADR_2$	M10	$TADR_9$	J12	CLK	D12	$IDAT_5$	B9	$\overline{ICS}$	B4	$SADR_{18}$
E1	$SADR_9$	L1	$\overline{SVAL}$	N5	$KADR_1$	N11	$TADR_{10}$	J13	$\overline{IWR}$	C13	$IDAT_6$	A9	$IADR_0$	A3	$SADR_{17}$
F3	V_{DD}	M1	ACC	L6	$KADR_0$	N12	$TADR_{11}$	H11	GND	B13	$IDAT_7$	C8	$IADR_1$	A2	$SADR_{16}$
F2	$SADR_8$	K3	GND	M6	$\overline{OET}$	L10	DONE	H12	V_{DD}	D11	V_{DD}	B8	$IADR_2$	C4	GND
F1	$SADR_7$	L2	V_{DD}	N6	$\overline{TWR}$	M11	GND	H13	SYNC	C12	GND	A8	$IADR_3$	B3	V_{DD}
G2	GND	N1	GND	M7	$TADR_0$	N13	ENDD	G12	V_{DD}	A13	V_{DD}	B7	$IADR_4$	A1	GND

Functional Description

General Information

The TMC2302 is a versatile, high-performance address generator which can control, under user direction, filtering or remapping of two or three-dimensional images by resampling them from one set of Cartesian coordinates (x, y, z) into a new, transformed set (u, v, w). Most applications utilize two identical devices for two-dimensional, or three devices for three-dimensional, image processing. The host CPU initializes the system by loading the input image buffer RAM with the source image pixel data and the TMC2302s with the image transformation and system configuration control parameters. These parameters are loaded by a separate, asynchronous input clock. The IMS-based system then executes the entire transformation as programmed, generating a DONE flag upon completion of the transform. The user can program the chip to repeat the transform continuously or to halt at the end.

General Information (cont.)

The IMSs continuously compute the target bit plane (u, v) or bit space addresses (u, v, w) in typical line-by-line, raster-scan serial sequence. For each output pixel address, they compute the corresponding remapped source image coordinates, each of whose upper 24 bits become the source bit plane addresses (x, y). An additional lower twelve bits are available through the target address port in the optional extended address mode. Source image addresses may be generated at up to 40MHz, with the corresponding target image addresses then appearing at up to (40/k)MHz, where "k" is the size of the interpolation kernel implemented. In the two-device system, one TMC2302 computes the horizontal coordinates x and u while the other generates the y and v (vertical) addresses. In a three-dimensional system, one additional device would provide the z and w (depth or time) coordinates.

To support a wide range of image transformations, the "row" or x/u device implements a 16-term polynomial of the form:

$$x = a + bu + cu^2 + du^3 + ev + fvu + gvu^2 + hvu^3 + iv^2 + jv^2u + kv^2u^2 + lv^2u^3 + mv^3 + nv^3u + ov^3u^2 + pv^3u^3$$

where a through p are the user-defined image transformation parameters. The TMC2302 steps sequentially through the pixels within a user-defined rectangle in the target image space, computing the "old" source image address (x, y, z) corresponding to each "new" target image pixel (u, v, w). User-programmable flags are available to indicate when the source and target image addresses have fallen outside of a defined rectangular area, simplifying the generation of complex images or image windows.

In the three-dimensional mode, the x/u transformation equation is:

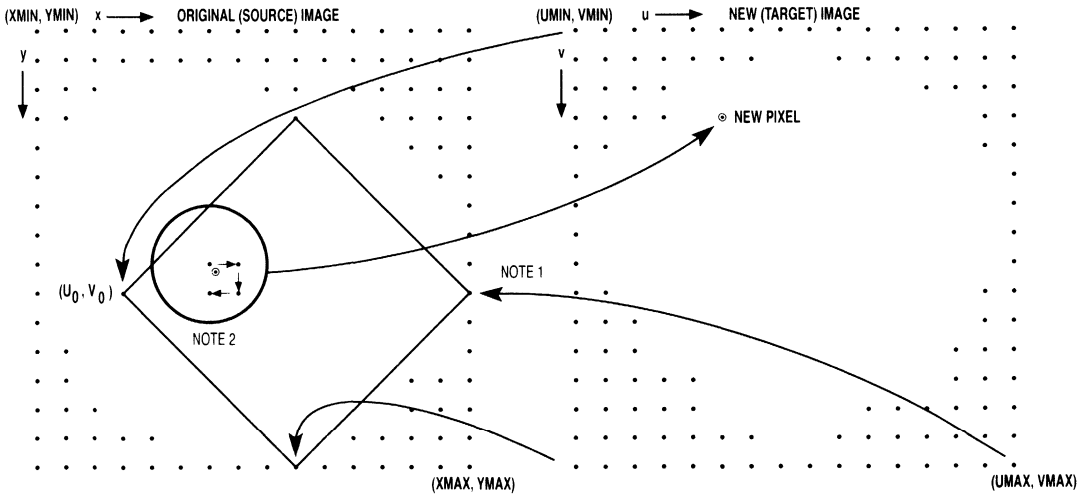
$$x = a + bu + ev + kw + fuv + ivw + luw + juvw$$

See "The Image Transformation Polynomial" section of the *Applications Discussion* .

The TMC2302 utilizes an external multiplier-accumulator or interpolator, connected to the system clock, to calculate the interpolated pixel value for each color. The products of the original source image pixel values surrounding the remapped pixel location (interpolation kernel) and the appropriate weights stored in the coefficient lookup table are summed. The resulting new interpolated image pixel value is then stored in the corresponding (U, V, W) memory location in the target image memory buffer. Next, the target image address is incremented by one in the "u" direction until UMAX is reached (end of line), when U is reset to UMIN, and the V counter is incremented to give the first pixel location in the next line. The process is repeated, proceeding line-by-line through the image, until VMAX is reached. In the case of three-dimensional images, the IMS system also steps through each page in the image, incrementing in the "w" direction with the completion of each image plane until WMAX is reached, and the transformation is complete.

The Image Manipulation Sequencer can support any nearest-neighbor, bilinear interpolation, or cubic convolution resampling, according to the user's requirements. Interpolation kernels of more than one pixel require an external interpolation coefficient lookup table and multiplier-accumulator. One, two, and three-pass algorithms are supported. For each output point in a typical two-dimensional single-pass static image filter, the TMC2302 implements a spiralling pixel resampling algorithm, "walking" around the resampling neighborhood in two dimensions and generating the appropriate coefficient table addresses to sum up the interpolated pixel value in the external pixel interpolator. At the end of each walk, the TMC2302 will advance one pixel along the output scan line and then execute the walk for that next pixel. When performing multiple-pass interpolation, the TMC2302 system proceeds along only one dimension per pass, which requires dimensionally separable, preferably orthogonal, coefficients.

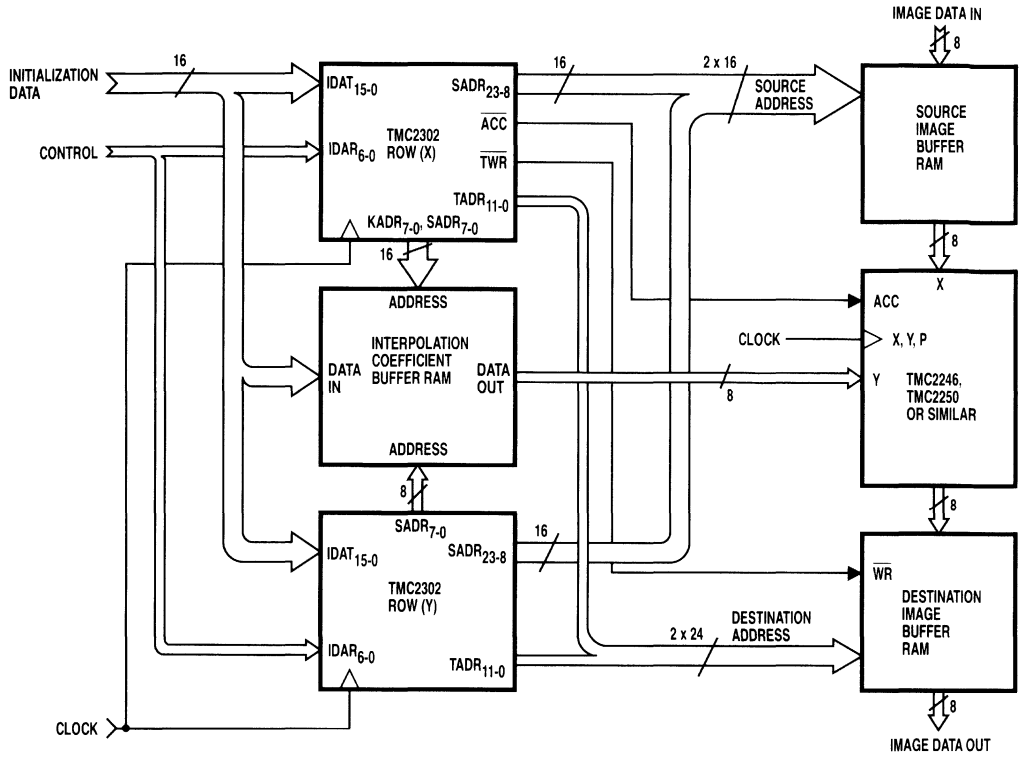
Figure 1. Image Resampling Geometry Showing Two-Dimensional Image Rotation and Expansion



NOTES: 1. Coordinate transformation U, V pixel mapped into X, Y coordinates. 2. Bilinear pixel interpolation walk. New U, V pixel intensity calculated from surrounding X, Y pixel neighborhood 21244A

A basic, two-dimensional TMC2302-based system is shown in *Figure 2*. In this typical arrangement, two Image Manipulation Sequencers process the image. The only other components needed beyond the source and target image buffer memories are a multiplier-accumulator or pixel interpolator such as the TRW TMC2246 Image Mixer or TMC2250 Matrix Multiplier, and the Interpolation Coefficient Lookup Table RAM or ROM.

Figure 2. Basic Two-Dimensional Image Convolver Using TMC2302 IMS with Typical 8-Bit Data Path



21245A

Signal Definitions

Power

V_{DD}, GND — The TMC2302 operates from a single +5V supply. All pins must be connected.

Clock

CLK — The pixel clock of the TMC2302 strobes all internal registers except the control parameter preload registers. All timing specifications except those are referenced to the rising edge of CLK.

$\overline{IWR}$ — The internal image transformation and configuration control parameter registers are double buffered to simplify interfacing with system controllers. Depending on the state of the chip select $\overline{ICS}$, control words input to $IDAT_{15-0}$ and the corresponding input parameter register addresses presented to $IADR_{6-0}$ are strobed into the outer preload registers on the rising edge of the Input parameter Write clock $\overline{IWR}$. See *Figure 3*.

Inputs

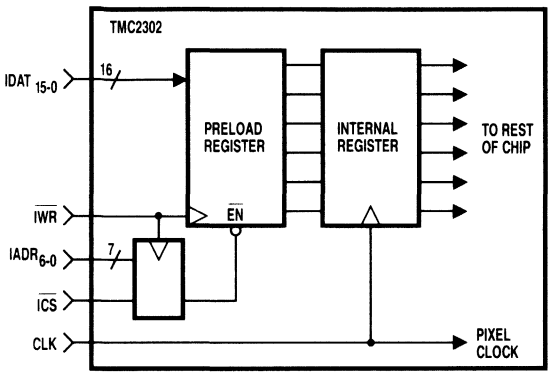
$IADR_{6-0}$ — The input parameter preload register currently indicated by the Input parameter register Address $IADR_{6-0}$ is loaded with the data presented to input port IDAT on the rising edge of $\overline{IWR}$, as demonstrated in *Figure 3*.

$IDAT_{15-0}$ — Configuration and transformation parameter Input Data is presented, along with the appropriate input register address word $IADR_{6-0}$, to the parameter Input Data port

Inputs (cont.)

IDAT$_{15-0}$ (cont.) IDAT$_{15-0}$ and is latched into the preload registers on the next rising edge of $\overline{IWR}$. Preload register updates are disabled by the chip select control $\overline{ICS}$. See ***Figure 3***.

Figure 3. Image Transformation and Configuration Control Parameters Register Structure



Outputs

SADR$_{23-0}$ The 24-bit address of one dimension (X, Y, Z) of the source image pixel value currently being resampled is output through the Source Address port SADR$_{23-0}$. This port can be forced to the high-impedance state by the enable control $\overline{OES}$.

KADR$_{7-0}$ The integer address steps for each dimension of the spiral interpolation walk performed by the TMC2302, as determined by the transform parameter KERNEL, are generated by the internal walk counter and output at the Coefficient Address output port KADR$_{7-0}$. This port can be forced to the high-impedance state by the enable control $\overline{OEK}$.

TADR$_{11-0}$ The 12-bit address of one dimension (U, V, W) of the target image pixel value just resampled is output through the Target Address Port TADR$_{11-0}$. This port is forced into the high-impedance state by the enable control $\overline{OET}$. TADR$_{11-0}$ can be delayed up to seven clock cycles after the nominal sequence shown in ***Table 1*** by utilization of the pipeline delay parameter PIPTAD. For systems requiring greater spatial resolution in the source image than that offered by the SADR$_{23-0}$ alone, the Target Address Port can be reconfigured to output 12 additional LSBs of the source address by placing the device into the Extended mode, in which case the pipeline delay parameter must be set to 0 to maintain alignment with the current source address port output. See the ***Device Configuration and Control Parameters*** section.

Controls

$\overline{ICS}$ The input parameter preload register write clock $\overline{IWR}$, and thus the preloading of all configuration and transformation parameters, is disabled on the next clock when the registered Input parameter Chip Select input is HIGH. When $\overline{ICS}$ returns LOW, they are enabled on the next clock. See ***Figure 3***.

INIT The TMC2302 control logic is cleared and initialized for the start of a new image transformation, and the internal working registers are updated with the contents of the current control parameter preload registers when the registered control input INIT is HIGH. The image transformation then commences with the first source image pixel address nine clocks later.

SYNC The user can select between continuous or one-frame operation with the registered input control SYNC. Assuming that INIT remains LOW and $\overline{NOOP}$ remains HIGH, if SYNC remains HIGH at the end of a transform the TMC2302 will begin the next image transformation without interruption. This assumes either that the user is not changing the parameter set, or that a new set of parameters has already been loaded into the preload registers midframe, prior to the beginning of the last line in the transform.

Controls (cont.)

SYNC (cont.) If SYNC is LOW during the last clock cycle of a transform, the device will complete the image, having loaded the new transform parameter set during the first clock of the final line of the transform, and halt in the state set on the first clock cycle of the next transform. These outputs are held until SYNC is again brought HIGH, and operation resumes on the next clock. See ***Figure 5***.

ACC The external pixel interpolator or multiplier-accumulator is initialized for a new accumulation of products by the registered Accumulator Control output ACC. On the first cycle of each interpolation walk, this output goes LOW for one cycle, effectively clearing the register by loading in only the first new resampled pixel value. When performing nearest-neighbor resampling, this control will remain LOW throughout the entire transform. This output can be delayed up to seven clock cycles after the nominal sequence shown in ***Table 1*** by the pipeline delay parameter PIPACC. See the ***Device Configuration and Control Parameters*** section.

$\overline{TWR}$ On the last cycle of each interpolation walk, the Target Write Enable goes LOW for one clock cycle, returning HIGH for all but the last cycle of the next walk. When performing nearest-neighbor resampling, this control will remain LOW throughout the entire transform. This output can be forced to the high-impedance state by the enable control $\overline{OET}$, and can be delayed up to seven clock cycles after the nominal sequence shown in ***Table 1*** by the pipeline delay parameter PIPTWR. See the ***Device Configuration and Control Parameters*** section.

$\overline{NOOP}$ Assuming that INIT remains LOW, the internal system clock of the TMC2302 will be disabled on the next clock, halting the current transform, when the registered control input $\overline{NOOP}$ goes LOW. When $\overline{NOOP}$ returns HIGH, normal operation resumes on the next clock. This control does not affect the loading of the configuration and transformation parameter preload registers.

$\overline{OES}$ The source address port $SADR_{23-0}$ is enabled when the asynchronous output enable $\overline{OES}$ is LOW. When $\overline{OES}$ is HIGH, the port is in the high-impedance state.

$\overline{OEK}$ The interpolation coefficient address port $KADR_{7-0}$ is enabled when the asynchronous output enable $\overline{OEK}$ is LOW. When $\overline{OEK}$ is HIGH, the port is in the high-impedance state.

$\overline{OET}$ The target address port $TADR_{11-0}$ and target write enable $\overline{TWR}$ are enabled when the asynchronous Target Output Enable $\overline{OET}$ is LOW. When $\overline{OET}$ is HIGH, these outputs are in the high-impedance state. This control functions in both the normal and extended addressing modes.

Flags

$\overline{SVAL}$ When the current source image address component output is within the working space defined by the parameters XMIN and XMAX (or YMIN, YMAX for the column (Y/V) device or ZMIN, ZMAX for the page (Z/W) device), the Source Address Valid flag $\overline{SVAL}$ for that device is LOW. This flag will go HIGH on the clock in which the corresponding component address falls outside the defined region. In a typical system, the $\overline{SVAL}$ outputs of all IMS devices are OR'ed together to generate a global boundary violation flag. The user might then insert zeroes into the pixel interpolator to ignore that portion of the image outside the defined space, or insert a background color or image. This output can be delayed up to seven clock cycles after the nominal sequence shown in ***Table 1*** by the pipeline delay parameter PIPSVA. See the ***Device Configuration and Control Parameters*** section.

Flags (cont.)

$\overline{\text{TVAL}}$ When the current target image addresses are within the working space defined by the parameters UMINI and UMAXI, and VMINI and VMAXI (and WMINI and WMAXI for systems processing three-dimensional images), the Target Address Valid flag $\overline{\text{TVAL}}$ for that device is LOW. This flag will go HIGH on the clock in which the current target address outputs fall outside the defined region. Since each TMC2302 device is programmed with distinct MINI/MAXI parameters and generates a separate $\overline{\text{TVAL}}$ flag, the user may define separate two or three-dimensional target space windows for each device. $\overline{\text{TVAL}}$ can be delayed up to seven clock cycles after the nominal sequence shown in ***Table 1*** by the pipeline delay parameter PIPTVA. See the ***Device Configuration and Control Parameters*** section.

ENDD During the last pixel interpolation walk of a row (X/U device), the last row in a page (Y/V device), or the last page in a three-dimensional transform (Z/W device), the flag ENDD goes HIGH for the entire walk, indicating End of the transform in that dimension. It remains LOW otherwise. This output can be delayed up to seven clock cycles after the nominal sequence shown in ***Table 1*** by the pipeline delay parameter PIPEND. See the ***Device Configuration and Control Parameters*** section.

DONE On the last clock cycle of the current image transform, the DONE flags on all TMC2302s go HIGH for one clock cycle. On the next clock cycle, all devices output the first addresses and control signals for the next image transform. If SYNC is LOW, the IMS system halts. If SYNC is HIGH, operation continues without interruption. See "SYNC," in the ***Controls*** section. This flag can be delayed up to seven clock cycles after the nominal sequence shown in ***Table 1*** by the pipeline delay parameter PIPDON. Also see "PFLS," in the ***Device Configuration and Control Parameters*** section.

E

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins
Power	V_{DD}	Supply Voltage	C3, C2, F3, G3, J3, L2, L4, L7, L11, K11, J11, H12, G12, F11, D11, A13, A4, B3
	GND	Ground	D3, E3, G2, H3, K3, N1, L5, M11, M12, L12, K13, H11, G11, F12, E11, C12, C11, C4, A1
Clocks	CLK	System Clock	J12
	$\overline{IWR}$	Input Parameter Write Clock	J13
Inputs	$IDAT_{15-0}$	Input Parameter Data	A10, C9, B10, A11, B11, C10, A12, B12, B13, C13, D12, D13, E12, E13, F13, G13
	$IADR_{6-0}$	Input Parameter Address	A7, C7, B7, A8, B8, C8, A9
Outputs	$SADR_{23-0}$	Source Address	B6, C6, A5, B5, C5, B4, A3, A2, B2, B1, C1, D2, D1, E2, E1, F2, F1, G1, H1, H2, J1, J2, K1, K2
	$KADR_{7-0}$	Coefficient Address	N2, M3, N3, M4, N4, M5, N5, L6
	$TADR_{11-0}$	Target Address	N12, N11, M10, L9, N10, M9, N9, L8, M8, N8, N7, M7
Controls	INIT	Initialize	K12
	SYNC	Run/Halt	H13
	$\overline{ICS}$	Input Parameter Chip Select	B9
	ACC	Accumulate	M1
	$\overline{TWR}$	Target Memory Write Enable	N6
	$\overline{NOOP}$	No Operation	L13
	$\overline{OES}$	Source Address Output Enable	A6
	$\overline{OEK}$	Coefficient Address Output Enable	M2
	$\overline{OET}$	Target Address Output Enable	M6
Flags	$\overline{SVAL}$	Source Address Valid	L1
	$\overline{TVAL}$	Target Address Valid	M13
	ENDD	End of Dimension	N13
	DONE	Done	L10
No Connects	NC	No Connect	L3
		Index Pin	D4

Table 1. Nominal Output Signal Timing

$SADR_{23-0}$ [1]	ACC	$TADR_{11-0}$	$\overline{TWR}$	END	DONE
$X_{I-1,J,0}$	0	$U_{L-1,M}$	1	0	0
$X_{I-1,J,1}$	1	$U_{L-1,M}$	1	0	0
$X_{I-1,J,2}$	1	$U_{L-1,M}$	1	0	0
•					
•					
•					
$X_{I-1,J,K}$	1	$U_{L-1,M}$	0	1	0
$X_{I,J,0}$	0	$U_{L,M}$	1	1	0
$X_{I,J,1}$	1	$U_{L,M}$	1	1	0
$X_{I,J,2}$	1	$U_{L,M}$	1	1	0
•					
•					
•					
$X_{I,J,K}$	1	$U_{L,M}$	0	1	1

Note: 1. $KADR_{7-0}$ timing identical.

The nominal sequence of address and control signals of a two-dimensional, single-pass-programmed TMC2302 system, with all PIPE parameters set to 0, is shown in *Table 1*. Here, the values of the last two new target image pixels $U_{L-1,M}$ and $U_{L,M}$ are being calculated, and the beginning and end of the interpolation walks of length K which sample source image pixels in the neighborhod of locations ($X_{I-1,J}$, $X_{I,J}$) can be seen. Utilizing the arrival of the source image address ($SADR_{31-0}$) as a reference point, the other signals shown can be delayed up to seven clock cycles from the nominal timing shown here, allowing the user to configure these outputs to match the timing latencies of his pixel data path structure. Considerable speed and timing variations in image buffer memory, data register, and pixel interpolator structure can thus be accomodated, with minimal corresponding support hardware. Also see "PFLS," in the *Device Configuration and Control Parameters* section.

Transformation Coefficient and Configuration and Control Parameters

The TMC2302 is intended to act as a co-processor, requiring only that the user program the device to perform the image transformation desired by loading in the appropriate device configuration and transformation control parameters discussed in this section. The user then issues an "Init" command, allowing his system to run unattended until the completion of the image when a "Done" flag is generated to inform the host system.

The capabilities and flexibility of the TMC2302 Image Manipulation Sequencer are apparent when reviewing the following tables which define the transformation coefficient and configuration and control parameters. These tables are broken up into two separate groups. The first parameters discussed are the control words which select the dimension calculated, the functional configuration of each device, the working space in which they will operate, the size of the interpolation kernel desired, and the timing of the various address and control signals involved in handling the pixel data pipeline. The second parameters are the polynomial transform coefficients used in performing image manipulation. The TMC2302 utilizes three levels of internal 48-bit accumulators to calculate these values by forward difference accumulation, generating no significant cumulative spatial error for most applications. The user must be aware that all internal parameter and coefficient registers must be set by the user, including resetting after powerup any unused control words or coefficients.

A major difference between the TMC2302 and the TMC2301 is that elimination of the device interconnects. Instead, the user programs all X, U, V, and W boundaries into all TMC2302 devices. The system's progress through the image is monitored by each device independently and in parallel.

Transformation Coefficient and Configuration and Control Parameters (cont.)

The boundary values are usually identical in all devices in order to maintain synchronous operation.

As mentioned above, the TMC2302 also features user-programmable image data pipeline configuration controls. All output signals except the source and coefficient address outputs can be individually delayed by the user up to seven clocks after the nominal system timing illustrated in *Table 1*. This allows the user to software-configure the TMC2302s in his system to match his pixel interpolator, image buffer, and interpolation coefficient RAM structure timing.

The user can also program the device to continue into the next image for a set number of clock cycles after the Done flag has appeared. First, this "flushes" the final resampled pixel data word through the interpolation pipeline, all the way to the target image RAM. Also, valid pixel data will then appear on the first clock of the next transform independent of the length of the pixel pipeline, incurring no lost clock cycles.

Device Configuration and Control Parameters

UMIN, VMIN, WMIN — The memory addresses of the target image boundaries corresponding to the top, left side, and front page of the new image being generated are defined in all devices of the user's system by the parameters UMIN, VMIN, and WMIN, respectively. At the beginning of the transformation, the initial source image coordinate (X_0, Y_0, Z_0) will be mapped to this coordinate set. The numeric format assumed is 12-bit unsigned binary integer.

UMAX, VMAX, WMAX — The memory addresses of the target image boundaries corresponding to the bottom, right side, and last page of the image being generated are defined in all devices by the parameters UMAX, VMAX, and WMAX, respectively. These values should be greater than the UMIN/VMIN/WMIN values defined above. Numeric format assumed is unsigned 12-bit binary integer.

Note: The parameter UMAX must exceed UMIN so as to ensure that a minimum of 5 system clock cycles in two-dimensional operation, or 15 clock cycles in three-dimensional operation, pass between the periods in which these two target address values are generated. Thus in 2D nearest neighbor operation UMAX must be 5 greater than UMIN. In 2D bilinear interpolation mode (4-pixel two-dimensional kernel), the distance must be two pixels in the target image (actually enforcing a spacing of 8 system clocks).

UMINI, VMINI, WMINI — The target image addresses corresponding to those of the top, left side, and front page of the 2 or 3 dimensional region indicated by the valid target address flag $\overline{\text{TVAL}}$ are UMINI, VMINI, and WMINI, respectively. Thus, to define a valid region beginning at "m," the MINI parameter value is "m." These parameters are assumed to be in 12-bit unsigned binary integer format.

UMAXI, VMAXI, WMAXI — The target image addresses one more than those of the right side, bottom and back page of the region indicated by the valid target address flag $\overline{\text{TVAL}}$ are UMAXI, VMAXI, and WMAXI, respectively. Thus, to define a valid region ending at "n," the MAXI parameter value is "n+1". These parameters are assumed to be in 12-bit unsigned integer format.

XMIN, XMAX — The source image boundaries are defined for each device by the parameters XMIN and XMAX, in the case of the row device. The column device then contains YMIN and YMAX, and the page device (in systems performing three-dimensional operations) ZMIN and ZMAX. The value of XMAX should be greater than XMIN if the boundary violation flag $\overline{\text{SVAL}}$ is to operate correctly. These values are assumed to be in 32-bit unsigned binary integer format.

PFLS — The user can set the number of clock cycles that the TMC2302 continues in to the next image following the DONE flag, allowing his system to Flush all control and data pipeline paths and halt after a maximum of seven cycles. The numeric format assumed is three-bit unsigned binary integer.

Device Configuration and Control Parameters (cont.)

PTAD, PDON, PEND, PTVA, PSVA, PTWR, PACC — As mentioned above, the control signals and target image pixel addresses generated by the TMC2302 can be delayed up to seven clock cycles after the nominal timing shown in *Table 1* by setting the appropriate Pipeline delay word. The numeric format assumed for all delay words is three-bit unsigned binary integer.

XTND — When the user sets the control bit XTND to 1, the TMC2302 operates in an extended-resolution source address bus configuration. Assuming that the user has his own raster scan generator available elsewhere to manage the flow of output pixels from the TMC2302 system, the target address output bus $TADR_{11-0}$ is reconfigured internally into an extension of the source address bus, as $SADR_{11-0}$. The original source address bus $SADR_{23-0}$ is then $SADR_{35-12}$, providing 36 bits of spatial resolution in the source address space. An XTND of 0 puts the device in the standard 24-bit source, 12-bit target address configuration.

E3D — Setting this control bit to 0 indicates a two-dimensional image transform is to be performed. When the E3D is set to 1, a three-dimensional image is assumed, using three TMC2302 devices.

DIM — The user sets each TMC2302 to operate in a specific dimension as follows:

$DIM_{1,0}$	Dimension
00	X/U (Row) Device
01	Y/V (Column) Device
10	Z/W (Page) Device
11	No Operation

MODE — In systems performing the standard two-dimensional spiral interpolation walk, MODE is set to 11, indicating single-pass operation. When performing multiple-pass resampling, the user must set this two-bit control word pass-by-pass in all IMSs, to implement each pass direction. For instance, setting MODE to 00 causes the TMC2302 system to increment only in the X-direction, holding the Y (and Z) addresses constant until the end of that pixel walk. On the next pass through the image, the user sets MODE = 01, with the kernel increment in Y only. In 3D, the IMS system then proceeds again through the (U, V) target image space, walking kernels only along the Z direction.

$MODE_{1,0}$	Resampling Performed
00	X-Pass
01	Y-Pass
10	Z-Pass
11	Two-Dimension Spiral Walk

KERNEL — This parameter determines the size of the interpolation walk performed. To implement a convolutional sum of K+1 pixels, the parameter KERNEL is set to K, up to a maximum of 255. In single-pass operation, this value must be identical in all devices, giving a square interpolation kernel. In multiple-pass operation, however, non-square kernels may be implemented, with different K values in each dimension. Or, the user could utilize a banded memory architecture in two-pass mode to access an entire row or column of a kernel in one clock, completing the entire sum in a single pass through the other dimension of the kernel. Numeric format is 8-bit unsigned integer.

FOV — The user determines the size of each step in an interpolation walk, in terms of the number of source image pixels, by setting the Field Of View control. The binary weighting of the image transformation parameters and source address must be taken into account when determining this value. See *Table 6* and the *Applications Discussion* section. The numeric format assumed is unsigned 16-bit integer.

Table 2. Control Parameter Registers Binary Format (Row, Column or Page Device)

Name	Addr Hex	MSB															LSB	Limits Dec	Limits Hex
UMIN	30					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
UMAX	31					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
UMINI	32					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
UMAXI	33					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
VMIN	34					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
VMAX	35					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
VMINI	36					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
VMAXI	37					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
WMIN	38					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
WMAX	39					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
WMINI	3A					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
WMAXI	3B					2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	4095 0	FFF 000
XMINL	3C	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	0	00000000
XMINM	3D	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	$2^{32}-1$	FFFFFFFF
XMAXL	3E	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	0	00000000
XMAXM	3F	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	$2^{32}-1$	FFFFFFFF
PFLS	40		2^{2}	2^{1}	2^{0}													7 0	7 0
PTAD	40					2^{2}	2^{1}	2^{0}										7 0	7 0
PDON	40								2^{2}	2^{1}	2^{0}							7 0	7 0
PEND	40											2^{2}	2^{1}	2^{0}				7 0	7 0
PTVA	40														2^{2}	2^{1}	2^{0}	7 0	7 0
PSVA	41		2^{2}	2^{1}	2^{0}													7 0	7 0
PTWR	41					2^{2}	2^{1}	2^{0}										7 0	7 0

Note: Table 1 continues on the following page.

Table 2. Control Parameter Registers Binary Format (cont.)

Name	Addr Hex	MSB							Format								LSB	Limits Dec	Hex
PACC	41								2^2	2^1	2^0							7 0	7 0
XTND	41											XTND							
E3D	41												E3D						
DIM	41													DIM_1	DIM_0				
MODE	41															$MODE_1$	$MODE_0$		
KERNEL	42									2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	255 0	FF 00
FOV	43	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	$2^{16}-1$ 0	FFFF 0000

Transformation Parameter Registers

The Transformation Parameter Word storage register addresses for the X/U device are listed in ***Table 3***, along with the differential terms for each polynomial coefficient for both two and three-dimensional transforms. The polynomial terms for the other IMS device(s) are found by replacing every "X" in the table with a Y (or Z). A TMC2302-based system can perform image manipulations of up to third order in two dimensions, and three-dimensional transforms of up to order 1.5 ("first-and-a-half order"). Also, see "The Image Transformation Polynomial", in the *Applications Discussion* section.

The notation used to define each polynomial coefficient term in ***Table 3*** is easily interpreted. Each differential is of course defined by a differential in X, followed by the corresponding dependent U, V, or W terms. Thus,

DXUV is equivalent to $d^2X/dUdV$

and

DXUUUV to d^4X/dU^3dV.

Table 3. Transformation Polynomial Coefficient Register Addresses

Name	Parameter		Coefficient Word Addresses (hex)		
	2D Term	3D Term	MSW	CSW	LSW
A	X_0	X_0	00	01	02
B	DXU	DXU	03	04	05
C	DXUU		06	07	08
D	DXUUU		09	0A	0B
E	DXV	DXV	0C	0D	0E
F	DXUV	DXUV	0F	10	11
G	DXUUV	X_0	12	13	14
H	DXUUUV	DXU	15	16	17
I	DXVV	DXVW	18	19	1A
J	DXUVV	DXUVW	1B	1C	1D
K	DXUUVV	DXW	1E	1F	20
L	DXUUUVV	DXUW	21	22	23
M	DXVVV		24	25	26
N	DXUVVV		27	28	29
O	DXUUVVV		2A	2B	2C
P	DXUUUVVV		2D	2E	2F

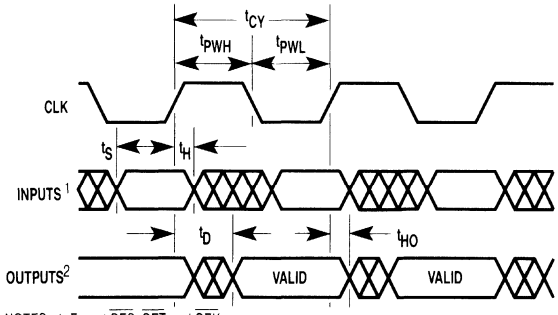
Note: The X_0 and DXU terms must each be loaded into two different registers when performing 3D transforms. Table 3 shows the binary weighting of all of the Transformation Parameter words, which are 48-bit signed fractional binary.

Table 4. Integer Binary Weighting of Transformation Parameters

	Format																Limits	
	MSB															LSB	Dec	Hex
MSW	-2^{47}	2^{46}	2^{45}	2^{44}	2^{43}	2^{42}	2^{41}	2^{40}	2^{39}	2^{38}	2^{37}	2^{36}	2^{35}	2^{34}	2^{33}	2^{32}	$2^{48}-1$	FFFFFFFFFFFF
CSW	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}		
LSW	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	0	000000000000

Note: A minus sign indicates a sign bit.

Figure 4a. Timing Diagram, Pixel Clock, Control, and Outputs



NOTES: 1. Except $\overline{OES}$, $\overline{OET}$, and $\overline{OEK}$.
2. Assumes $\overline{OES}$, $\overline{OET}$, and $\overline{OEK}$ = LOW. All pipeline latency parameters set to 0.

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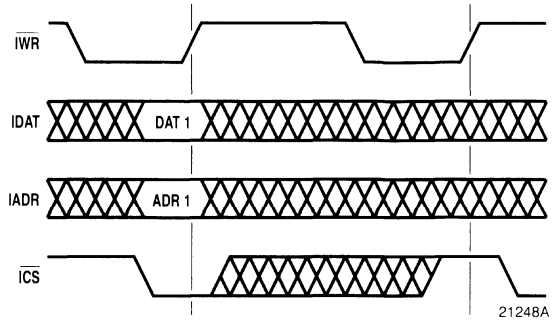
Figure 4b. Timing Diagram, Preload Parameters



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Value "DAT 1" is loaded into address "ADR 1" on the first rising edge of $\overline{IWR}$, since $\overline{ICS}$ = 0.

Nothing happens on the second rising edge of $\overline{IWR}$, when $\overline{ICS}$ = 1.

Figure 5. Equivalent Input Circuit

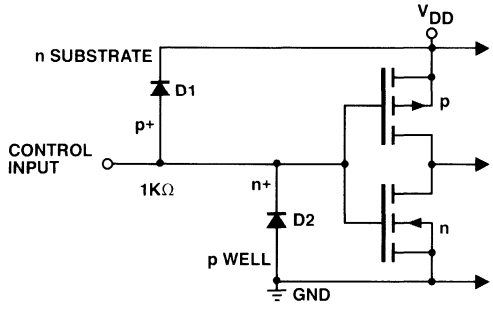

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Figure 6. Equivalent Output Circuit

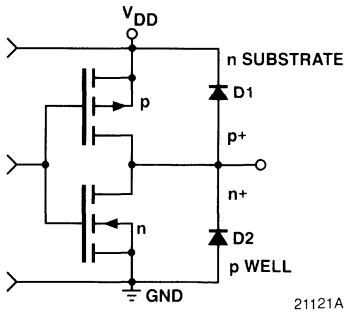

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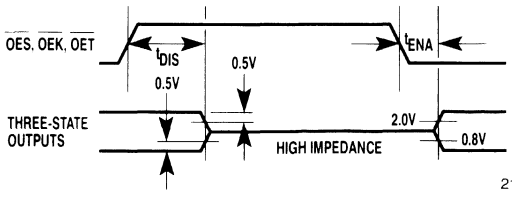
Figure 7. Threshold Levels for Three-State Measurements



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Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD} + 0.5)V

Output

Applied voltage [2] ..... −0.5 to (V_{DD} + 0.5)V

Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −60 to +130°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.

Operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Nom	Standard Max	−1 Min	−1 Nom	−1 Max	Units
V_{DD}	Supply Voltage		4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IL}	Input Voltage, Logic LOW				0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0			2.0			V
I_{OL}	Output Current, Logic LOW				8.0			8.0	mA
I_{OH}	Output Current, Logic HIGH				−4.0			−4.0	mA
t_{CY}	Cycle Time	V_{DD} = Min	33			25			ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD} = Min	15			12.5			ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD} = Min	15			10			ns
t_S	Input Setup Time		10			8			ns
t_H	Input Hold Time		2			2			ns
T_A	Ambient Temperature, Still Air		0		70	0		70	°C

Electrical characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	−1 Min	−1 Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		10		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz, $\overline{OES} = \overline{OEK} = \overline{OET}$ = 5V		70		70	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	−10		−10		μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V	−40		−40		μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.	−20	−70	−20	−70	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	−1 Min	−1 Max	Units
t_{DO}	Output Delay	V_{DD} = Min, C_{LOAD} = 25pF		15		12	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 25pF	4		4		ns
t_{ENA}	Three-State Output Enable Delay [1]	V_{DD} = Min, C_{LOAD} = 25pF		12		12	ns
t_{DIS}	Three-State Output Disable Delay [1]	V_{DD} = Min, C_{LOAD} = 25pF		15		15	ns

Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Applications Discussion

The Image Transformation Polynomial

On any given clock cycle, when performing a two-dimensional geometric transformation the addresses output by the row (X/U) TMC2302 are generated by forward difference accumulation according to the following third-order polynomial:

$$x(u,v) = a + bu + cu^2 + du^3 + ev + fvu + gvu^2 + hvu^3 + iv^2 + jv^2u + kv^2u^2 + lv^2u^3 + mv^3 + nv^3u + ov^3u^2 + pv^3u^3 + FOV \cdot CAX(ca) + FOV \cdot u \cdot CAX(Ker)$$

The polynomial utilized for three-dimensional transforms is:

$$x(u,v,w) = a + bu + ev + kw + fuv + ivw + luw + juvw + FOV \cdot CAX(ca) + FOV \cdot u \cdot CAX(Ker),$$

where $UMIN \leq u \leq UMAX$, $VMIN \leq v \leq VMAX$, $WMIN \leq w \leq WMAX$, and the polynomials for the column or page devices are obtained by replacing the x by a y or z, as appropriate.

The Image Transformation Polynomial (cont.)

FOV is the 16-bit field-of-view parameter, normally set so that the spiral walk proceeds in single-pixel steps. FOV can be increased to expand the step size and thus the spiral walk, subsampling the image. See *Table 2* and *Table 6*. Also, CAX(ca) is the current value of the coefficient address, and CAX(Ker) is the terminal value of each pixel walk in that dimension. See the *Interpolation Coefficient Lookup Table Addressing*. The CAX(Ker) term arises because the IRS computes each new walk's starting point from the previous spiral walk's end point, rather than its starting point.

We can reform the two-dimensional polynomial as:

$$x(u,v) = (a + ev + iv^2 + mv^3) + (b + fv + jv^2 + nv^3)u + (c + gv + kv^2 + ov^3)u^2 + (d + hv + lv^2 + pv^3)u^3,$$

and retain the simpler three-dimensional form:

$$x(u,v,w) = a + bu + ev + kw + fuv + ivw + luw + juvw$$

and define each of the polynomial coefficients in arithmetic terms, as shown in *Table 5*.

Table 5. Transformation Polynomial Coefficients

	Parameter			
	Two-Dimensional		Three-Dimensional	
Name	Term	Coefficient	Term	Coefficient
A	X_0	a	X_0	a
B	DXU	b+c+d	DXU	b
C	DXUU	2c+6d	—	0
D	DXUUU	6d	—	0
E	DXV	e+i+m	DXV	e
F	DXUV	f+g+h+j+k+l+n+o+p	DXUV	f
G	DXUUV	2(g+k+o)+6(h+l+p)	X_0	a
H	DXUUUV	6(h+l+p)	DXU	b
I	DXVV	2i+6m	DXVW	i
J	DXUVV	2(j+k+l)+6(n+o+p)	DXUVW	j
K	DXUUVV	4k+12l+12o+36p	DXW	k
L	DXUUUVV	12l+36p	DXUW	l
M	DXVVV	6m	—	0
N	DXUVVV	6(n+o+p)	—	0
O	DXUUVVV	12o+36p	—	0
P	DXUUUVVV	36p	—	0

Understanding The Polynomial Coefficients An Overview

As the formulae indicate, the source address is a polynomial function of the two (or three) dimensions of the target address. Each of the 16 terms of the equation is of the form:

$$\frac{d^{m+n+p}x}{du^m\,dv^n\,dw^p},$$

and may be treated approximately as a mixed partial difference of order m, n, and p.

The simplest term, X_0, is a zeroeth (non-) function of the target addresses; it specifies the source address point corresponding to the upper left point in the target space.

The next-simplest terms, dX/dU and dY/dV, govern the relative scales of the source and target images, i.e., how large a step in source space corresponds to a unit step in the corresponding direction in the target space. As long as the cross-terms, dX/dV and dY/dU, are zero, this is a straight scale operation, without rotation or shear.

Understanding the Polynomial Coefficients (cont.)

The first-order cross terms, dX/dV and dY/dU, generate source space displacements perpendicular to unit displacements in the target space, thereby causing shearing of the image. In conjunction with the parallel source terms described above, they govern rotation, shear, and scaling of the image.

Although the actions of the higher-order terms become progressively difficult to describe, all terms behave essentially as partial differences of various orders, and a little thought and common sense will generally lead the user to the proper conclusions. For example, the term dXUU (using the notation of *Table 3*) is a horizontal scale factor which increases as one progresses across each row, causing a quadratic horizontal warp. In fact, all terms of the form dmX/dUm or dnY/dVn cause only stretching of the image, never rotation.

Interpolation Coefficient Lookup Table Addressing

The external coefficient lookup table RAM stores the interpolation coefficient values used to calculate the value of the new pixel. These values are selected by the user, allowing maximum filtering flexibility. In simple filtering applications, the source and target pixel addresses map one-to-one, and only one interpolation coefficient set is required. These integer addresses are generated for each dimension by the internal walk counters of each TMC2302.

However, applications performing a coordinate transformation will almost always generate non-integer source pixel addresses; that is, the U (or V) locations will not map to the X (or Y) addresses exactly, and fractional source address components are generated. The user must then expand the interpolation coefficient lookup table to include spatially-corrected values, as determined by the subpixel resolution of the system.

The TMC2301 Image Resampling Sequencer allows the user to trade subpixel resolution against interpolation step size by obtaining the interpolation coefficient addresses directly from the fractional part of the source address. The TMC2302 gives the user 16 different interpolation bit weighting positions. The complete Interpolation Coefficient Address for that dimension then consists of both the 8-bit interpolation walk address $KADR_{7-0}$, weighted to match the source address binary point by the parameter FOV, and the fractional portion of the source pixel address $SADR_{23-0}$, to the desired subpixel resolution. See *Table 6*.

Internal and External Data Formats

The source address value output by the TMC2302 is a 24-bit two's complement number, with binary point assignable by the user anywhere in the 16 lower bits. The Extended mode appends 12 additional fractional bits for greater output precision. All internal computations include these 24 plus 12 bits, plus an additional 12 lower bits, for 48-bit precision. See *Table 6*.

Internally, each TMC2302's source address (X, Y, or Z) generator computes a 48-bit address through a mode-specific accumulation of the sixteen 48-bit user-specified resampling parameters. The 24 most significant bits of the final accumulation emerge via the source address port, whereas the "extend" mode makes the 12 next-most-significant bits available at the target address port. The 12 least significant bits are truncated internally.

Source Address Bit Weighting and Setting the Binary Point

When performing nearest-neighbor resampling, the user may arbitrarily trade source image size against subpixel resolution merely by adhering to a single binary point position for all resampling parameters. For example, if the binary point follows the 16 most significant bits in each resampling parameter, then it will appear following the source address' 16 most significant bits, leaving 8 (20 in extended mode) bits of subpixel resolution.

In any filtering or resampling operation performing an interpolation walk, the user should set the Field of View (FOV) parameter according to the desired binary point position determined above, as follows. To provide 2^{24} integral pixel positions per dimension, with no subpixel resolution, set FOV = 0001 (hex). For 2^{23} positions with 1-bit (0.5) subpixel resolution, FOV = 0010 (hex). Similarly, for 2^{9} positions and 15-bit subpixel resolution, FOV = 8000 (hex). As shown in *Table 6*, using the parameter FOV the user effectively "shifts" the bit weight of the coefficient address word $KADR_{7-0}$ to match the established location of his source address binary point. In each case, the EXTEND mode provides 12 additional bits of subpixel resolution but eliminates the separate target or raster address, which must then be generated elsewhere in the user's system.

Table 6. Relative Bit Weighting – Source Address

Word \ Weight	2^{47}	$2^{46} \ldots 2^{40}$	2^{39}	2^{32}	$2^{31} \ldots 2^{25}$	2^{24}	$2^{23} \ldots 2^{16}$	$2^{15} \ldots 2^{12} \ldots 2^{8}$	$2^{7} \ldots 2^{0}$
Transform Parameters	−47	46							0
Internal Source Address Generator	−47	46							0
Source Address Output $SADR_{23-0}$	−23	22 ... 16	15	8	7 ... 1	0			
Extended Mode Only $TADR_{11-0}$							11 ... 4	3 ... 0	
$KADR_{7-0}$									
FOV = 0001					$2^{7} \ldots \ldots 2^{0}$				
FOV = 0002				2^{7}	$2^{6} \ldots 2^{0}$				
•									
•									
•									
FOV = 8000		$2^{7} \ldots 2^{1}$	2^{0}						

Note: A minus sign indicates a sign bit.

E

Utilization of the Image Boundary Flags $\overline{SVAL}$ and $\overline{TVAL}$

As mentioned above, the TMC2302 provides two programmable valid address, or boundary flags. The source valid flag $\overline{SVAL}$ is asserted when the current source image address output for that device's source image dimension is within the space defined by the configuration parameters XMIN and XMAX, or YMIN and YMAX, or ZMIN and ZMAX, as appropriate. Also, the target valid flag $\overline{TVAL}$ is available to indicate when the current target image address values fall within the space defined by the configuration parameters UMINI, UMAXI, VMINI, VMAXI, and also WMINI and WMAXI in three-dimensional systems. Note that all of these parameters are each programmed into each individual TMC2302. Thus, the user could define two (or three) different working spaces, one indicated by each IMS device.

Figure 8 may help clarify the relationships among (X_0, Y_0, Z_0), (UMIN, VMIN, WMIN), and (UMAX, VMAX, WMAX), for the two-dimensional case. With positive first derivatives, (X_0, Y_0) and (UMIN, VMIN) represent the upper left corners of the original image and the new destination field, respectively. The lower right corner of the new transformed image is located at (UMAX, VMAX); the location of the corresponding corner of the original image depends on the values of the derivatives.

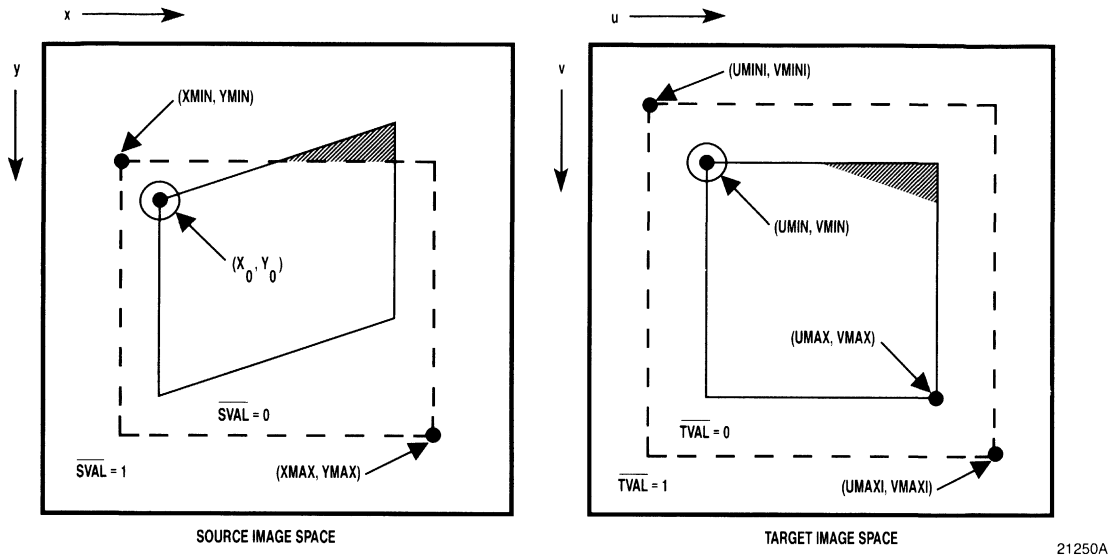
Not to be confused with (X_0, Y_0), the points (XMIN, YMIN) and (XMAX, YMAX) define the "usable" rectangular portion of the original image which is indicated by the valid address flag $\overline{SVAL}$; points (X, Y) lying outside this region are ignored in most resampling and filtering applications. Specifically, the point (X_0, Y_0) is the location from which the TMC2302 system begins the image resampling sequence. Every step beyond that point in the source image space is defined by the address generators implementing the image transformation polynomials.

The valid source address flag feature permits one to construct a mosaic of several abutting subimages in the (X, Y) plane, without danger of edge effect interference between adjacent subimages. Note in the figure that the upper right corner of the resampled source image lies outside the admissible region; in practice, the values fetched at these locations will not be included in the convolutional sums. One might, for instance, program these boundary values to alert the system that an edge is being approached and to modify the interpolation coefficients appropriately, or simply to ignore pixel values outside the defined space.

Utilization of the Image Boundary Flags $\overline{SVAL}$ and $\overline{TVAL}$ (cont.)

The flag $\overline{TVAL}$ however is utilized somewhat differently. Working in unison with the target address working space defined by UMIN/UMAX, etc, the target address valid flag could be programmed to delineate image areas other than the immediate working space, and the flag of each TMC2302 to indicate unique regions anywhere within the target image. With this flexibility, the user can generate windows, composite multiple images, or simply switch to a background image or border color.

Figure 8. Pixel Maps Demonstrating Source and Destination Image Boundaries, Violation Flags, and Image Clipping (Note Shaded Areas)



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2302H5C [1]	STD – T_A = 0°C to 70°C	Commercial, 30MHz	120 Pin Plastic PGA	2302H5C
TMC2302H5C1 [1]	STD – T_A = 0°C to 70°C	Commercial, 40MHz	120 Pin Plastic PGA	2302H5C1

Note: 1. Consult factory for availability.

Transform Products

Transform products perform complex conversions from one signal space to another. The high level of integration in TRW products yields very efficient, cost-effective implementations of the basic signal processing functions.

The Fast Fourier Transform is a basic tool in time/frequency domain processing. The TMC2310 executes a 1K point 16-bit FFT in 514μs (16 points in 4μs).

The Fast Cosine Transform is the key functional element in image compression. The TMC2311 operates on 12-bit data at a 15 MegaPixel/s rate.

The TMC2330 is tailored to convert data in polar coordinate space to rectangular space, or vice-versa, at rates of 25 million operations per second.

Transform Products

Product	Description	Size	Clock Rate [1] (MHz)	Power [1] (Watts)	Package		Grades [2]	Notes	Page
TMC2310-1	Fast Fourier Transform	16-Bit	20	0.75	G5	89 Pin PGA	V	1024 Point Complex FFT in	F3
					L4, L6	100 Lead LCC	V	514μs with 19-Bit Internal	
-			20	0.75	H7	89 Pin PPGA	C	Precision and Block	
			15	0.75	G5	89 Pin PGA	V	Floating-Point Rescaling.	
					L4, L6	100 Lead LCC	V		
TMC2311-2	Fast Cosine Transform	12-Bit	17.8	0.7	R1	68 Lead PLCC	C	Data Compression Processor.	F47
-1			14.5	0.7	R1	68 Lead PLCC	C	Meets CCITT Specifications.	
-			17.8	0.7	R1	68 Lead PLCC	C	8 x 8, 2-Dimension.	
TMC2330-1	Coordinate Transformer	16 x 16 Bit	25	0.7	H5	121 Pin PPGA	C	Cartesian ↔ Polar Converter.	F65
					L5	132 Lead CERQUAD	V		
-			20	0.7	H5	121 Pin PPGA	C		
					L5	132 Lead CERQUAD	V		

Notes: 1. Guaranteed. See product specifications for test conditions.

2. C = Commercial, $T_A = 0°C$ to $70°C$.
V = MIL-STD-883 Compliant, $T_C = -55°C$ to $125°C$

TMC2310

FFT Processor
16/19-Bit, 20MHz

The TMC2310 is an advanced integrated circuit which is capable of executing complex Fast Fourier Transforms (FFT), forward or inverse, of up to 1024 points, with or without data windowing. The device operates with either unconditional or conditional overflow block floating-point, rescaling. Adaptive and static Finite Impulse Response filtering, real and complex multiplication or multiply-accumulation, and magnitude squared operations are also supported. Sinusoidal coefficients ("Roots of Unity") for Fourier Transforms are provided in a Coefficient Look-Up Table in on-chip ROM. At the maximum clock rate of 20MHz, the device will execute radix-2 butterflies in 100ns, and 1024-point complex transforms (5120 butterflies) in 514μSec.

The TMC2310 provides the arithmetic, control, coefficient memory and address generation logic for a variety of signal processing and vector algorithms. External memory is used for storage of complex data and window or filter coefficients. Each data port is bidirectional and the device can be used with one or two banks of memory for either in-place or bank switched memory configurations allowing the user to overlap I/O operations with arithmetic execution. All functions utilize the same basic system architecture, ensuring maximum flexibility.

The control structure has been designed to simplify its use as a high-speed arithmetic accelerator. The device is programmed by initializing two internal configuration registers to set device parameters such as function, transform length, data addressing modes, single or bank switching memory architecture, and other options. Once initialized, the device generates data addresses and control for external memory, transfers data, executes the algorithm, and provides a DONE flag to indicate completion.

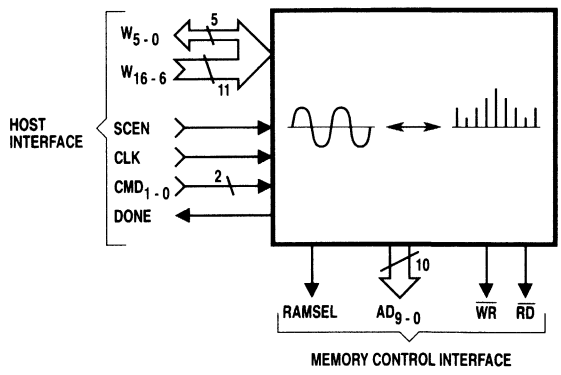
Built with TRW's one-micron, OMICRON-C™ CMOS process, the TMC2310 is available in 89 pin plastic and 88 pin ceramic pin grid arrays and a 100 leaded ceramic chip carrier.

Features

- Stand Alone Execution Of Forward Or Inverse Complex Fast Fourier Transforms, Adaptive And Non-Adaptive FIR Filtering, Multiplication Or Multiplication-Accumulation (Real Or Complex) Magnitude Squared
- Fast 100ns Per Butterfly Yields A 2MHz To 4MHz Sampling Rate In Single-Device Systems (16-Point FFT In 4μSec, 1024-Point In 514μSec)
- Pipelined Addressing Mode And Internal Data Storage To Reduce Memory Bandwidth
- Multiple-Transform Array Mode To Increase Throughput
- On-Chip ROM Coefficient Look-Up Table For FFT Coefficients ("Twiddle Factors")
- 16-Bit Fixed-Point Data Format With 19-Bit Intermediate And Final Results For Improved Precision
- Conditional Overflow Rescaling Or Manual Scaling (Block Floating-Point) For High Signal-To-Noise Performance
- Scaler (Block Exponent) Output
- User Programmable Window Functions
- Complete On-Chip Address Generation And Control For Off-Chip Data And Window/(FIR) Coefficient Memory

F

Logic Symbol



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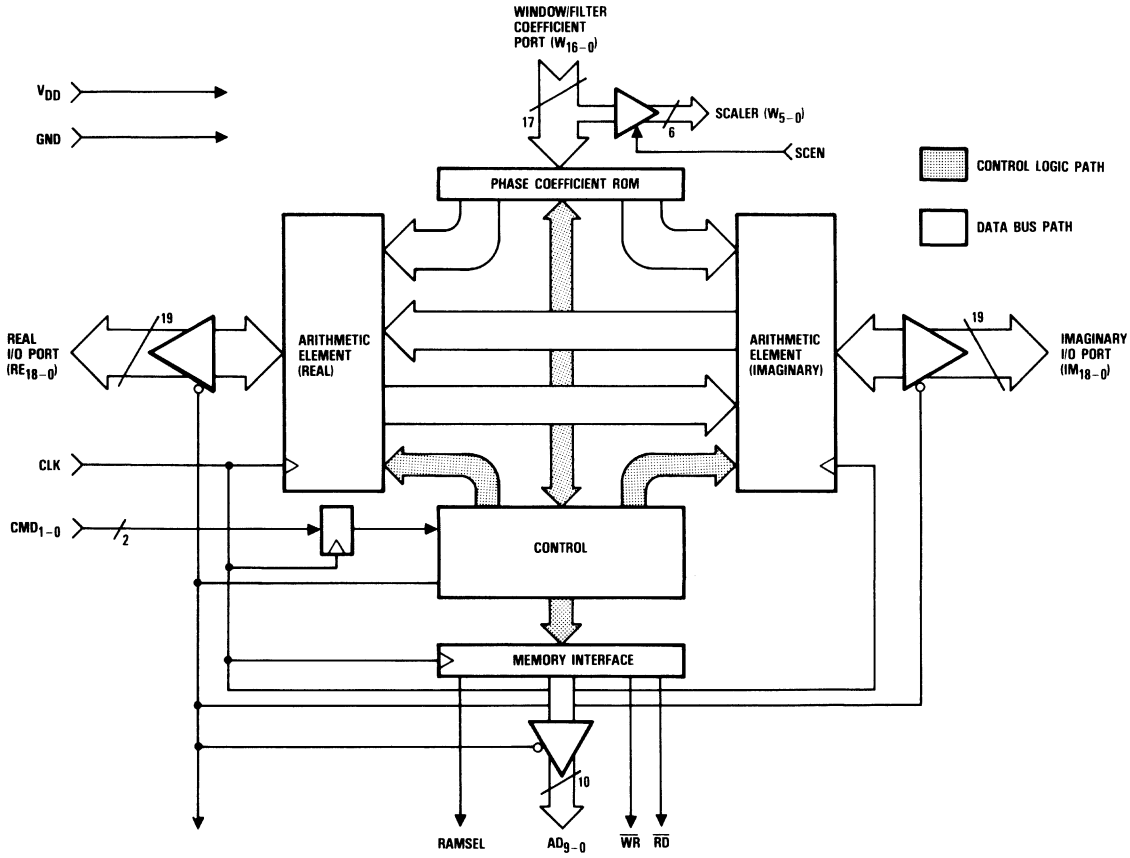
Applications

- Radar
- Sonar
- Digital Communications
- High – Speed Modems
- Image Processing, Graphics
- Test Instrumentation
- Medical Electronics
- Spectral Decomposition/Analysis
- Frequency – Multiplex Demodulation
- Adaptive Filtering And Equalization
- Pulse And Image Compression
- Frequency And Time Domain Digital Filtering
- High – Speed Complex Multiplication

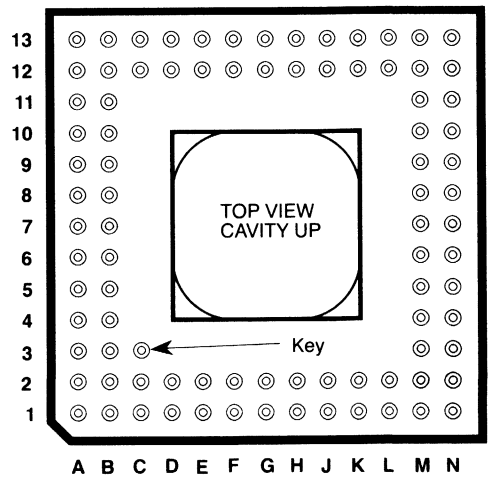
Functional Block Diagram



Pin Assignments — 88 Pin Ceramic (G5) or 89 Pin Plastic (H7) Pin Grid Array

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B1	GND	N2	GND	M13	GND	A12	RE_0
C2	CMD_0	M3	IM_{18}	L12	SCEN	B11	RE_1
C1	CMD_1	N3	IM_{17}	L13	W_0	A11	RE_2
D2	DONE	M4	IM_{16}	K12	W_1	B10	RE_3
D1	RAMSEL	N4	IM_{15}	K13	W_2	A10	GND
E2	RD	M5	IM_{14}	J12	W_3	B9	RE_4
E1	WR	N5	IM_{13}	J13	W_4	A9	RE_5
F2	CLK	M6	IM_{12}	H12	W_5	B8	RE_6
F1	AD_0	N6	IM_{11}	H13	W_6	A8	RE_7
G1	GND	N7	IM_{10}	G13	W_7	A7	RE_8
G2	GND	M7	GND	G12	GND	B7	GND
H1	V_{DD}	N8	V_{DD}	F13	V_{DD}	A6	V_{DD}
H2	V_{DD}	M8	IM_9	F12	W_8	B6	RE_9
J1	AD_1	N9	IM_8	E13	W_9	A5	RE_{10}
J2	AD_2	M9	IM_7	E12	W_{10}	B5	RE_{11}
K1	AD_3	N10	IM_6	D13	W_{11}	A4	RE_{12}
K2	AD_4	M10	IM_5	D12	W_{12}	B4	RE_{13}
L1	AD_5	N11	IM_4	C13	W_{13}	A3	RE_{14}
L2	AD_6	M11	IM_3	C12	W_{14}	B3	RE_{15}
M1	AD_7	N12	IM_2	B13	W_{15}	A2	RE_{16}
N1	AD_8	N13	IM_1	A13	W_{16}	A1	RE_{17}
M2	AD_9	M12	IM_0	B12	GND	B2	RE_{18}

C3 Index Pin (H7 packge only)



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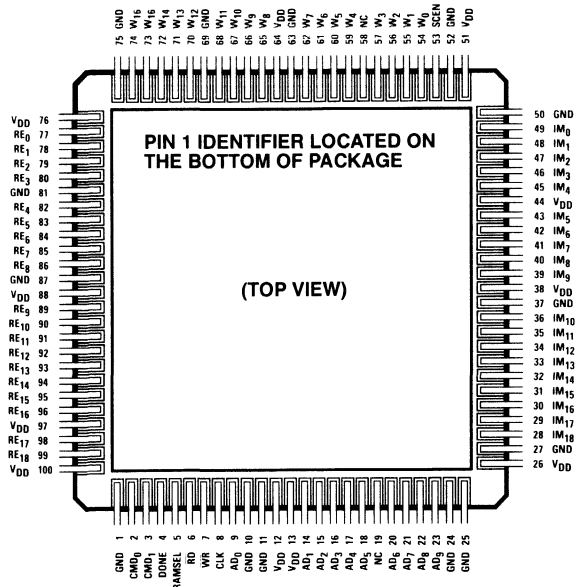
Pin Assignments

100 Leaded Ceramic Chip Carrier, L4 Package



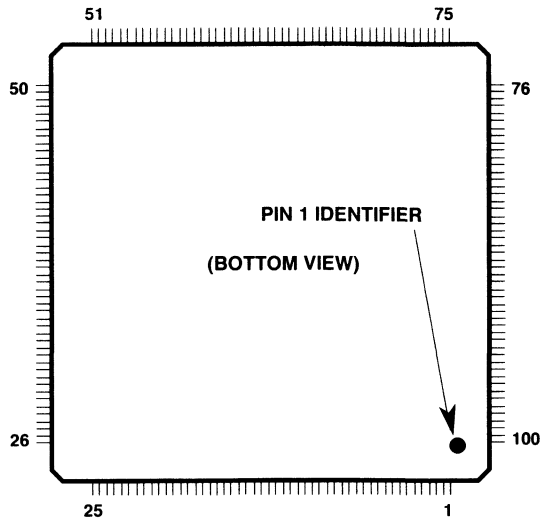


Figure 1. Basic TMC2310 System

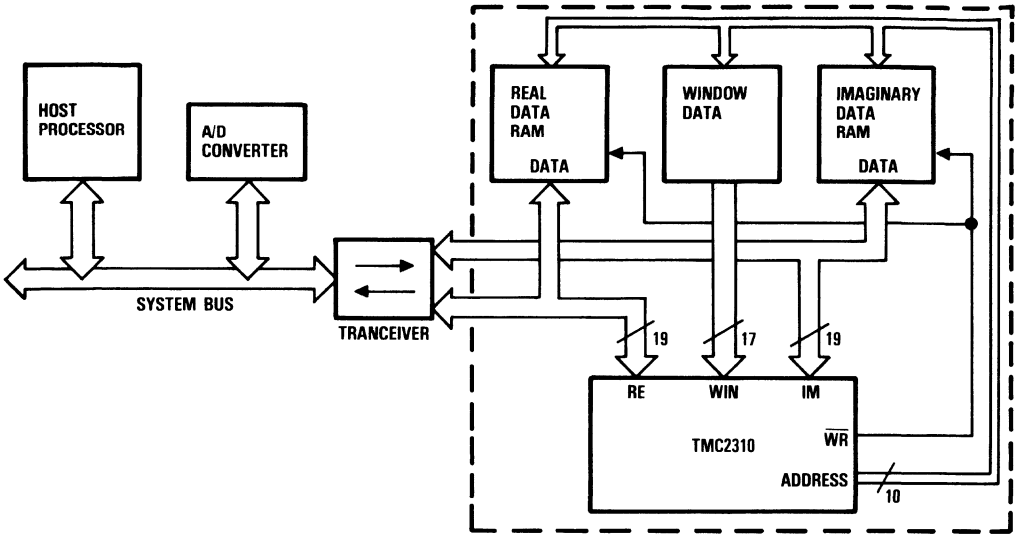
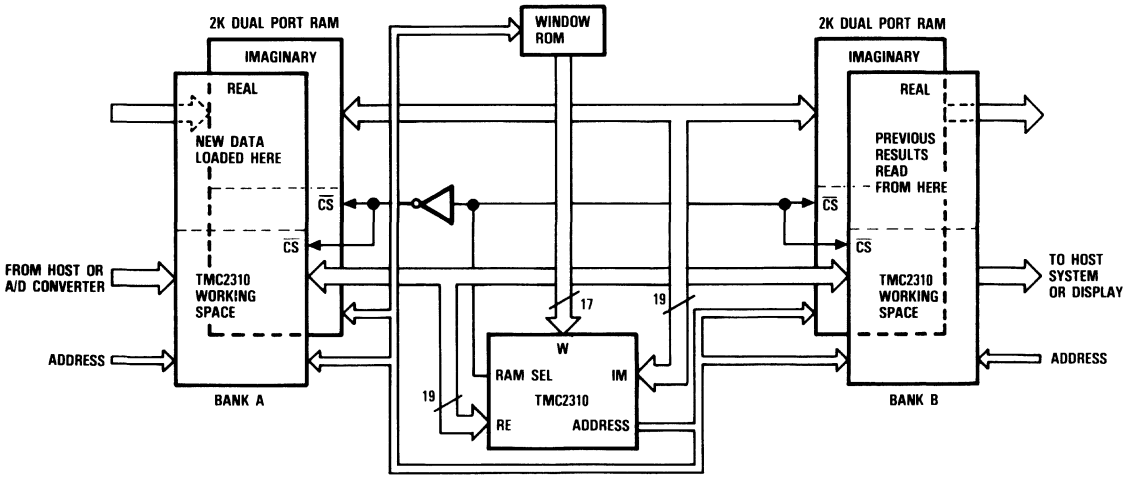


Figure 2. TMC2310 with Dual – Port Memory



Functional Description

General Information

The TMC2310 performs radix – 2, Decimation In Time (DIT) Fast Fourier Transforms. It accepts 16 – bit input data and maintains 19 – bit intermediate results, with either automatic pass – by – pass or unconditional data rescaling (block floating – point). The 19 – bit (RE, IM) data buses will accommodate up to three bits of word growth per data pass. Incoming data is rescaled to 16 – bit, two's complement fractions on subsequent passes based on the maximum overflow detected during the previous pass (auto scale) or under user control (manual scale). To reduce memory bandwidth require – ments (number of passes), the device performs radix – 2 butterflies in sets of four (radix – 4 addressing). A "pass" is defined as one arithmetic operation performed on the entire data array. Therefore, a butterfly operation is considered to be one data pass. Fourier Transforms require multiple data passes with external memory used for storage of intermediate and final results. All other (non – FFT) operations are completed in one pass.

As shown in Figures 1 and 2, a system can be con – figured with either single or multi – port RAM, a window coefficient RAM/ROM, and very little additional hardware (see Applications Section). Multi – port memory simplifies the system interface, while use of a banked memory architecture (Figure 2) allows I/O operations to be overlapped with data processing, maximizing system performance. The internal sequencing and control logic allows the device to operate with minimal support from the host system. External control consists of the pro – gramming of two internal configuration registers and a START, LOAD or RESET command. System performance is limited by either the maximum system clock rate or the memory access time. The architecture and sequencing of the TMC2310 are designed to minimize the number of wasted clock cycles between passes, ensuring that each butterfly can be executed in two clock cycles.

The TMC2310 also supports the use of window functions for Fourier transforms. In order to perform windowing the user need only provide a set of coefficients in external ROM or RAM and program the device accordingly. Window functions are applied to (multiplied by) the input data during the first data pass. Typical configurations utilize a 1K x 17 (x16 for positive coefficients) block of RAM or ROM on the dedicated window memory bus. For additional information regarding window functions consult reference [1].

The TMC2310 also performs in – place, memory based Finite Impulse Response (FIR) filtering. This function utilizes the external window port memory for storage of filter coefficients. Fixed coefficient and adaptive FIR filters can be implemented with 16 to 1024 coefficients (taps). Time domain filtering is accomplished with a memory based shift register technique in which the accumulated sum of products is determined (convolution of filter coefficients with stored data samples). Adaptive filtering allows real – time updates to filter coefficients by a dynamic update value.

Real and Complex vector arithmetic functions include multiplication, multiply – accumulation, and magnitude squared ($I^2 + Q^2$). By combining functions a variety of signal processing algorithms can be performed including frequency domain filtering, signal analysis and signal synthesis.

A multiple – transform array mode offers multiple equal – length transform capability. Any number of equal – length transforms may be selected up to a maximum of 1024 points. For example, the user may execute 16 contiguous 64 – point transforms, reducing the computation overhead associated with starting and executing single transforms. The window coefficients may be identical or unique to each transform. Scaling is performed on all points of all transforms equally, based on the maximum overflow of the previous data pass or by the user specified value.

At the end of the transform, the user may read the 19 – bit data output and the 6 – bit scaling factor ("block exponent") generated by the internal shift/rescale circuitry. The 4 – bit "Total Scaler" value indicates the number of shifts performed on the data (block exponent) while the remaining 2 bits indicate the overflow encountered during the final data pass. Nineteen bits are used for intermediate results in order to minimize roundoff error during transforms. Provisions have been made, however, to allow the use of 16 – bit wide memory systems. This can reduce memory component count but may increase roundoff error (arithmetic noise).

The TMC2310 consists of five major sections: two arithmetic elements, external memory interface, control logic and coefficient ROM.

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Arithmetic Elements (AEs)

Each AE consists of an array multiplier, adders/accumulators and data storage. The AEs interface to external data and window memory, as well as internal coefficient ROM. Communication between AEs allow the device to perform complex arithmetic operations. In order to minimize arithmetic error, each AE retains maximum precision until the output stage where data is rounded to 19 bits (Real and Imaginary). The bidirectional data buses transfer data between the AE and external memory. 19-bit input values are shifted at the input to the multiplier array. This shift is either automatic (FFT auto scale modes) or user controlled (manual scale). On the first pass, when the upper three bits contain significant data, the user must right shift the input data using manual scaling, otherwise truncation of the Most Significant Bits (MSBs) will occur.

External Memory Interface

The TMC2310 provides all the necessary addressing and control for external memory. Read and write addresses are provided as well as control outputs for write strobes, read enables and a source/destination RAM select for multiple memory bank systems. The single, 10-bit address output is multiplexed for read and write operations. The sequence is determined by the selected function as well as other user specified options.

The sequence may be specified as bit-reversed or sequential for FFT/IFFT operations. The selected sequence has no effect on execution time, however, it does affect the ordering of input data and whether additional memory is required (scratch pad). The device supports a special "pipelined" addressing mode for all operations. Under normal addressing, the address and controls are output during the same clock period as the data. In the pipelined mode, address and controls are output one clock cycle prior to the data, providing added flexibility in the host system interface as well as reducing memory speed requirements (See Timing and Applications).

Coefficient ROM

An internal ROM is included as a coefficient look-up table to the AEs. The ROM supplies the sinusoidal coefficients ("Roots of Unity") required for forward and inverse FFTs. The ROM is accessed under internal control and outputs data to the arithmetic elements during FFT passes (Sine and Cosine values). The ROM contains coefficients to support transforms of up to 1K (1024) data points.

Control

The control section configures the data paths and provides internal sequencing. The device operation is defined by two internal configuration registers. Once the function has been "STARTed", the device performs all sequencing and activates the DONE flag upon completion.

Signal Definitions

Power

V_{DD}, GND — The TMC2310 operates from a single +5V supply. All power and ground lines must be connected.

Clock

CLK — The TMC2310 operates from a single system clock. All internal and external operations are referenced to the rising edge of CLK.

Data Buses

RE_{18-0} — RE-Bus is a bidirectional data bus for "Real" data. This bus is time multiplexed for reads and writes. When the device is Idle, this bus is in the high-impedance state. RE_0 is the Least Significant Bit (LSB). RE_{15-3} is also used to load the internal configuration registers. Data placed on the bus is clocked into a configuration register during a LOAD command. Registers may also be programmed by storing configuration data in address 0 of the Real data memory. A LOAD command causes a read operation with the address bus set to address 0.

IM_{18-0} — IM-Bus is a bidirectional data bus for "Imaginary" data. This bus is time multiplexed for reads and writes. When the device is idle, this bus is in the high-impedance state. IM_0 is the LSB.

W_{16-0} — The W-Bus is used to input the 17-bit window and FIR Filter coefficients. W_{5-0} is also used as an output to access the block exponent and last pass overflow.

Data Buses (cont.)

W_{16-0} (cont.) The scaler exponent (W_{3-0}) indicates the number of shifts performed on the data for multiple pass transforms while W_{5-4} indicates the overflow (in bits) that occurred during the previous pass. W_{5-4} indicates how many, if any, of the three MSBs (RE_{18-16}, IM_{18-16}) of the final results contain significant data (i.e. bits which are not an extension of the sign).

Control Inputs

CMD_{1-0} The registered CoMmanD input is used to RESET the device, LOAD configuration registers, and START an operation. Commands are issued by placing a valid command on the input for one (or more) clock cycle(s) then returning to the CONT command. The input should normally remain in the inactive (CONT) state. The operation of each command is as follows:

CMD_{1-0}	Command	Operation
00	RESET	If RESET is held for at least 4 clock cycles, the DONE flag, $\overline{WR}$, RAMSEL are set HIGH. The Address bus (AD_{9-0}), data buses RE_{18-0}, IM_{18-0} and W_{16-0} are set to high-impedance state, and the $\overline{RD}$ output is LOW. A RESET command held for only one cycle does not reset the chip, but causes the last pass scaler (W_{5-4}) to be added to the current scaler exponent (W_{3-0}). RESET held for more than one cycle will clear the scaler exponent field (W_{5-0}).
01	LOAD	AD_{9-0} is activated and a read is performed with the address set to zero. If LOAD is followed by a CONT then the device will be put into a RESET state.
10	START	START causes the device to begin an operation. The START command must be valid for at least one clock cycle, but not longer than 4 clock cycles. After two start-up cycles, the DONE flag is set LOW and the data and address buses become active. Upon completion of the operation, $\overline{WR}$, and DONE are HIGH, $\overline{RD}$ is LOW, AD_{9-0}, RE_{18-0} and IM_{18-0} are in high-impedance, and execution suspended until the next command. The state of the RAMSEL pin is dependent on the mode determined in Configuration Register 2. The START command clears the current contents of the scaler exponent (W_{3-0}).
11	CONT	CONTinue is the inactive state for the command input. It has no internal effect. After a command has been issued, the CMD input should be set to this state. Following a START, the CMD input must be set to CONT for the operation to complete properly. If the previous command was a RESET or LOAD then the device remains in RESET.

SCEN The SCaler output ENable is used to read the block exponent and last pass overflow. When SCEN is HIGH, the six LSBs of the W-Bus are enabled and consist of the data block (scaler) exponent (W_{3-0}) and the last pass overflow (W_{5-4}). When SCEN is LOW, the W-Bus is in high-impedance and acts as an input. At the end of an operation, the scaler exponent will show the total number of right-shifts performed on the data array (both from manual and auto scaling), and the last pass scaler (W_{5-4}) will give the overflow occurring during the last pass through the data.

Control Outputs

AD_{9-0} The 10-bit ADdress output provides memory addressing for the data and window memories. The device supports sequential and bit-reversed addressing for FFTs, FIR data shift addressing, and multiple transform addressing for both read and write operations. Under normal conditions, the memory address is output on the same clock cycle as the read or write operation. Selecting pipelined addressing causes the address, $\overline{RD}$ and RAMSEL to appear one clock cycle prior to the read/write data.

$\overline{WR}$ WRite is an active LOW pulse used to strobe data into the external data memory.

Control Outputs (cont.)

$\overline{WR}$ (cont.) The address and control outputs are guaranteed to be valid before $\overline{WR}$ is LOW and after $\overline{WR}$ goes HIGH.

$\overline{RD}$ ReaD can be used to control the output enables of external memory. It indicates the direction of the RE and IM data buses. When LOW, the TMC2310 is performing a read (input) operation, and a HIGH indicates a write (outputs enabled) operation. When the DONE output flag is HIGH, $\overline{RD}$ is set LOW.

RAMSEL The RAM SELect output is used to bank select external memory and to identify the location of the initial and final results. Its operation is determined by setting a 2-bit parameter in Configuration Register 2. It can be used to select between physically separate memories or as an additional address line in paged memory systems. Detailed operation of RAMSEL is given in *Tables 3, 4, 5* and *6*.

DONE The DONE flag goes LOW after an operation is "STARTed" and remains LOW until it is complete. One cycle after DONE goes HIGH, the device is idle and final results are available in external memory. DONE= HIGH also indicates that the chip's data (RE and IM) and address (AD_{9-0}) bus drivers are in the high-impedance state, $\overline{WR}$ is inactive (HIGH), and $\overline{RD}$ is LOW. DONE can be used as a host interrupt as well as a control line to allow host system access to data memory and results.

Package Interconnections

Signal Type	Signal Name	Function	G5, H7 Package Pins	L4 Package Pins
Power	V_{DD}	Supply Voltage	H1, H2, N8, F13, A6	12, 13, 26, 38, 44, 51, 64, 76, 88, 97, 100
	GND	Ground	B1, G1, G2, N2, M7, M13, G12, B12, A10, B7	1, 10, 11, 24, 25, 27, 37, 50, 52, 63, 69, 75, 81, 87
Clock	CLK	System Clock	F2	8
Data	RE_{18-0}	Data Bus (Real)	B2, A1, A2, B3, A3, B4, A4, B5, A5, B6, A7, A8, B8, A9, B9, B10, A11, B11, A12	99, 98, 96, 95, 94, 93, 92, 91, 90, 89, 86, 85, 84, 83, 82, 80, 79, 78, 77
	IM_{18-0}	Data Bus (Imaginary)	M3, N3, M4, N4, M5, N5, M6, N6, N7, M8, N9, M9, N10, M10, N11, M11, N12, N13, M12	28, 29, 30, 31, 32, 33, 34, 35, 36, 39, 40, 41, 42, 43, 45, 46, 47, 48, 49
	W_{16-0}	Window/Coefficient Bus	A13, B13, C12, C13, D12, D13, E12, E13, F12, G13, H13, H12, J13, J12, K13, K12, L13	74, 73, 72, 71, 70, 68, 67, 66, 65, 62, 61, 60, 59, 57, 56, 55, 54
Controls	CMD_{1-0}	Command Inputs	C1, C2	3, 2
	SCEN	Scaler Exponent Enable	L12	53
	AD_{9-0}	Address Bus Output	M2, N1, M1, L2, L1, K2, K1, J2 J1, F1	23, 22, 21, 20, 18, 17, 16, 15, 14, 9
	RAMSEL	Source/Target RAM Select	D1	5
	$\overline{RD}$	External Memory Enable	E2	6
	$\overline{WR}$	Write Strobe Output	E1	7
Flags	DONE	Function Complete Flag	D2	4
No Connect	NC	No Connect Pins	-	19, 58
	-	Index Pin	C3	

Device Operation

Upon power-up of the device, the user should immediately issue a RESET command (CMD_{1-0} = 00), forcing the device into a "DONE" state. A RESET must be performed prior to any attempt to initialize internal configuration registers. Following the RESET, the DONE flag is HIGH and the address and data (RE, IM and W) buses are set to high-impedance.

Prior to performing any operation, the user must initialize and configure the device by programming two internal configuration registers (CR1, CR2). There are two methods of initializing the registers. Data may be stored in external memory, address location "0" or it may be placed directly on the RE-Bus (RE_{15-3}). A LOAD command (CMD_{1-0} = 01) causes a read on the RE-Bus with AD_{9-0} = 0. Data read from memory (or directly from the bus) is stored into the configuration register selected by bit 15 of the data word. A minimum of two load commands are required to input the two words, CR1 and CR2.

The configuration registers define the function to be performed as well as other operating parameters. Once programmed, device operation is controlled by the two-bit command control (CMD_{1-0}). Commands are used to begin or suspend operations, and to load configuration registers. Operations may be repeated (under the same conditions) without reloading the configuration registers by issuing additional START commands. If the RESET command has been applied after the configuration registers have been loaded, however, it may be necessary to reload Configuration Register 2. RESET will clear bits 3, 4 and 5 of CR2 and the internal SCaler ENable (SCEN) register.

Once the input data has been stored in external memory (beginning at address 0) and the configuration registers initialized, device operation begins following a START command. After the START command has been initiated, the command input must be set to CONT (CMD_{1-0} = 11) within 4 clock cycles for proper operation. During execution, the device takes control of the local data memory bus, enables the address output bus and generates external memory control. The DONE flag will be set HIGH to indicate that the TMC2310 has completed its operation and final results are available in memory.

All intermediate and final results are stored in external memory in 19-bit, two's complement format. Upon completion of the operation, the SCaler ENable input (SCEN) can be used to read the last pass overflow and the scaler exponent. The last pass overflow (W_{5-4}) indicates the word growth that occurred during execution of single pass operations or, during the final butterfly pass of a transform. The 4-bit scaler exponent (W_{3-0}) indicates the number of right-shifts performed on the data array during a multiple pass transform (common data exponent). At the end of an operation, the host system must read the scaler exponent prior to a RESET command. Failure to do so will result in an incorrect scaler exponent value. A RESET command applied for one clock cycle will allow the last pass overflow to be added to the current value of the scaler exponent. RESET held for more than one clock cycle will clear the scaler exponent field (W_{5-0}). Immediately after a START command, the scaler exponent will be initialized.

Configuration Register 1 (CR1)

Configuration Register 1 defines the operation, transform length, FFT addressing sequence, and scaling modes.

Function Codes

Table 1 indicates the input and output values for each function. The RE and IM buses are multiplexed for reads and writes while the W-Bus is used for input only. W-Bus(1) and W-Bus(2) indicate the input for first and second cycle read on the W-Bus, respectively. To input two words, the read address for both W-Bus operands is available during the first (read) cycle. It may be necessary for the user to register the address or data externally for proper synchronization (see Applications section).

In general, single pass operations (MPY, MAC, MAGSQ) read data from memory and output results to the same address, overwriting the original input data. If the input data are to be saved, use of the RAMSEL allows results be output to a separate result memory or directly to the host system. All data should be stored in external memory begining at address 0. The TMC2310 begins all operations at address 0.

Table 1 includes operations designated as "2-Re" (2 Real), "R/I" (Real/Imaginary), and "Cmplx" (Complex). The distinction is as follows:

2-Re — These operations involve only a single data word from the W-Bus. The data word

Function Codes (continued)

input in the W – Bus is applied to the data input on both the RE and IM data buses.

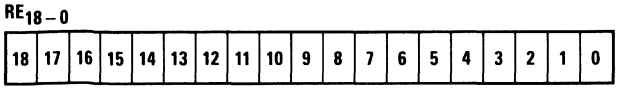
R/I — These operations involve two values input from the W – Bus with the first W – Bus operand applied to the RE data and the second applied to the IM data. No cross terms are evaluated.

Cmplx — These operations involve two W – Bus operands, interpreted as a complex data value. The function involves a complex operation including cross terms.

Table 1. Function Codes vs. Bus Function

Code	Function	Inputs				Outputs	
		RE – Bus	IM – Bus	W – Bus(1)	W – Bus(2)	RE – Bus	IM – Bus
0000	IFFT No – Window	R	I	–	–	Complex IFFT Results	
0001	MPY – ACC 2 – Re	R	I	W	–	Σ RW	Σ IW
0010	MPY – ACC R/I	R	I	W_1	W_2	Σ RW_1	Σ IW_2
0011	MPY – ACC Cmplx	R	I	W_R	W_I	Σ $RW_R - IW_I$	Σ $IW_R + \Sigma$ RW_I
0100	MAGSQ	R	I	–	–	$[R^2 + I^2]/2$	$[R^2 + I^2]/2$
0101	MPY 2 – Re	R	I	W	–	RW	IW
0110	MPY R/I	R	I	W_1	W_2	RW_1	IW_2
0111	MPY Cmplx	R	I	W_R	W_I	$RW_R - IW_I$	$IW_R + RW_I$
1000	FFT No – Window	R	I	–	–	Complex FFT Results	
1001	FIR 2 – Re	R_m	I_m	W_n	–	Σ R_mW_n	Σ I_mW_n
1010	FIR R/I	R_m	I_m	W_{1n}	W_{2n}	Σ R_mW_{1n}	Σ I_mW_{2n}
1011	FIR Adaptive	R_m	C_n	σ	–	Σ R_mC_n	$C_n(1 - \sigma)$
1100	FFT Re – Window	R	I	W	–	Complex FFT Results	
1101	IFFT Re – Window	R	I	W	–	Complex IFFT Results	
1110	Cmplx MPY + FFT	R	I	W_R	W_I	Complex FFT Results	
1111	Cmplx MPY + IFFT	R	I	W_R	W_I	Complex IFFT Results	

Configuration Register 1 (CR1) Format



Not Used (Don't Care)

Manual Scale Factor
- 00 Shift 0 Bits
- 01 Shift 1 Bit
- 10 Shift 2 Bits
- 11 Shift 3 Bits

Scaling Mode
- 0 Auto Scale (Manual On First Pass)
- 1 Manual Scale (All Passes)

FFT Addressing Sequence
- 00 No Bit – Reverse (In – Place FFT)
- 01 Bit – Reverse On First Pass Read
- 10 Bit – Reverse On Last Pass Write
- 11 Bit – Reverse On First Pass Read And Last Pass Write

Single Transform Length
- 000 Undefined
- 001 16 Points
- 010 32 Points
- 011 64 Points
- 100 128 Points
- 101 256 Points
- 110 512 Points
- 111 1024 Points

Function Code
- 0000 IFFT No Window
- 0001 Multiply – Accumulate 2 Real Inputs
- 0010 Multiply – Accumulate RE/IM Inputs
- 0011 Multiply – Accumulate Complex Input
- 0100 Magnitude Squared
- 0101 Multiply 2 Real Inputs
- 0110 Multiply RE/IM Inputs
- 0111 Multiply Complex
- 1000 FFT No Window
- 1001 FIR Filter, 2 Real Inputs
- 1010 FIR Filter, Dual RE/IM Inputs
- 1011 FIR Adaptive
- 1100 FFT Real Window
- 1101 IFFT Real Window
- 1110 Complex Multiply + FFT
- 1111 Complex Multiply + IFFT

Configuration Register Select Bit
- 0 Configuration Register 1 (CR1)

Not Used (Don't Care)

F

CR1[14:11]

0000 IFFT No Windowing. A complex Inverse Fast Fourier Transform is performed on data stored in external memory. No windowing is performed (rectangular window) during the IFFT and the W–Bus is unused. The memory addressing sequence and the transform length are determined by other parameters. The N–point inverse FFT is defined by:

$$h(n) = \sum_{k=0}^{N-1} H(k)e^{+j2\pi nk/N}$$

0001 Multiply–Accumulate Two Real Inputs. Both the RE and IM data are multiplied by the data word input on the W–Bus. Results are accumulated and written back to external memory. The output to memory is the sum of all previous multiplications. (e.g. Address 20_{10} = sum of first 21 products (0–20), Address 49_{10} = sum of first 50 products, etc.)

0010 Multiply–Accumulate Real/Imaginary. The RE data input is multiplied by the first word input on the W–Bus. The IM input is multiplied by the second word input on the W–Bus. The output to memory is the accumulation of all previous multiplications.

$$RE_{out}(N) = \sum_{K=0}^{N} RE_{in}(k)W_1(k)$$

$$IM_{out}(N) = \sum_{K=0}^{N} IM_{in}(k)W_2(k)$$

0011 Multiply–Accumulate Complex. Complex multiplication is performed on each (RE, IM) and (W_R, W_I) pair. The output to memory is the accumulation of all previous complex multiplications. Input of a complex operand on the W–Bus is done on two consecutive clock cycles.

$$RE_{out}(N) = \sum_{K=0}^{N} [RE_{in}(k)W_R(k) - IM_{in}(k)W_I(k)]$$

$$IM_{out}(N) = \sum_{K=0}^{N} [IM_{in}(k)W_R(k) + RE_{in}(k)W_I(k)]$$

($W_R = W_1$, $W_I = W_2$)

0100 Magnitude Squared. The RE and IM data are squared separately. The squares are summed, halved and output to both the RE and IM data memories.

$$RE_{out}(n) = IM_{out}(n) = [RE_{in}^2(n) + IM_{in}^2(n)]/2$$

0101 Multiply 2–Real. The RE and IM data are multiplied by the single data word input on the W–Bus during the read cycle. Results are output to the corresponding memory address.

$$RE_{out}(n) = RE_{in}(n)W_1(n)$$
$$IM_{out}(n) = IM_{in}(n)W_1(n)$$

0110 Multiply Real/Imaginary. The RE data value is multiplied by the data input on the first W–Bus cycle. The IM input is multiplied by the data input on the second W–Bus cycle. The result output to memory is:

$$RE_{out}(n) = RE_{in}(n)W_1(n)$$
$$IM_{out}(n) = IM_{in}(n)W_2(n)$$

0111 Multiply Complex. A complex multiplication is performed on the data input on the RE, IM and W–Bus inputs. The complex output to memory is:

$$(RE + jIM)(W_R + jW_I) =$$
$$RE_{out}(n) = [RE_{in}(n)W_R(n)] - [IM(n)_{in}W_I(n)]$$
$$IM_{out}(n) = [IM_{in}(n)W_R(n)] + [RE(n)_{in}W_I(n)]$$

1000 FFT No Windowing. A complex Fast Fourier Transform is performed on data stored in external memory. No windowing is performed (rectangular window) during the FFT and the W–Bus is unused. The memory addressing sequence and the transform length are determined by other parameters. The forward FFT is defined by:

$$H(k) = \sum_{n=0}^{N-1} h(n)e^{-j2\sigma nk/N}$$

CR1[14:11] (continued)

1001 FIR 2 – Real. Finite Impulse Response filtering is done by performing a RAM based multiplication – accumulation on data and coefficients stored in external memory. Multiplication with accumulation is performed between filter coefficients input on the W – Bus and the RE and IM data. The RE and IM data are shifted down one location in memory with the final accumulated result written into location N – 1. Two separate data sets may be convolved simultaneously, using the RE and IM data and one filter coefficient data set. (See Applications section for more detailed descriptions of FIR operation.) The output is:

$$RE(i)_{out} = RE(i+1)_{in},\ RE(N-1)_{out} = \sum_{n=0}^{N-1} RE(n)W_1(n)$$

$$IM(i)_{out} = IM(i+1)_{in},\ IM(N-1)_{out} = \sum_{n=0}^{N-1} IM(n)W_1(n)$$

1010 FIR Real/Imaginary. Finite Impulse Response filtering is done by performing a RAM based multiplication – accumulation on data and coefficients stored in external memory. Multiplication with accumulation is performed between filter coefficients input on the W – Bus, and the RE and IM data. The RE and IM data are shifted down one location in memory with the final accumulated result written into location N – 1. When the next input sample is loaded into address N – 1 the operation may be re – STARTed to form the next sum. Two sets of coefficients are used, both input through the W – Bus, one for RE data and a second for IM data. (See Applications section for more detailed description of FIR Operation.) The data outputs are:

$$RE(i)_{out} = RE(i+1)_{in},\ RE(N-1)_{out} = \sum_{n=0}^{N-1} RE(n)W_1(n)$$

$$IM(i)_{out} = IM(i+1)_{in},\ IM(N-1)_{out} = \sum_{n=0}^{N-1} IM(n)W_2(n)$$

1011 FIR Adaptive. Adaptive FIR filtering allows concurrent updates to filter coefficients by the value specified on the W – Bus. The RE – Bus is used for input data and the IM – Bus used for filter coefficients. The W – Bus determines the coefficient update value (σ). The data on the RE – Bus is multiplied, accumulated and shifted down one address in memory. The final convolution result is output to address N – 1. The next input sample is stored in address N – 1, and the operation re – STARTed to form the next sum. The filter coefficients, input on the IM – Bus, are modified and stored back to their original address locations as follows:

$IM(i)_{out} = IM(i)_{in}(1 - \sigma(i))$ or,
New Coefficient = [Old Coefficient] • [1 – update value]

Update values are input on the W – Bus for each coefficient (during the read cycle). The data output is:

$$RE(i)_{out} = RE(i+1)_{in},\ RE(N-1) = \sum_{k=0}^{N-1} RE(k)IM(k)$$

1100 FFT Real Window. An FFT is performed on complex data in external memory. During the first FFT pass, the RE and IM data are multiplied by the window coefficients input through the W – Bus. The real data window is applied to both the RE and IM data. The forward FFT with real windowing is defined by:

$$H(k) = \sum_{n=0}^{N-1} h(n)w(n)e^{-j2\pi nk/N}$$

1101 IFFT Real Window. An Inverse FFT is performed on the complex data in external memory. During the first IFFT pass, the RE and IM data are multiplied by the window coefficients input through the W – Bus. The real data window is applied to both the RE and IM data. The inverse FFT with real windowing is defined by:

$$h(n) = \sum_{k=0}^{N-1} H(k)w(k)e^{+j2\pi nk/N}$$

F

1110 Complex Multiplication + FFT. Prior to performing the FFT, a complex multiplication is performed between the RE and IM data and complex data stored in external memory input through the W–Bus. This operation requires one additional pass, compared to the FFT with Real Window, to complete the complex multiplication.

1111 Complex Multiplication + IFFT. Prior to performing the inverse FFT, a complex multiplication is performed between the RE and IM data and complex data stored in external memory and input through the W–Bus. This operation requires one additional pass, compared to the IFFT with Real Window, to perform the complex multiplication.

Single Transform Length CR1[10:8]

000 Undefined
001 16 data points (Recommended for Non–FFT/IFFT Operations)
010 32 data points
011 64 data points
100 128 data points
101 256 data points
110 512 data points
111 1024 data points

This field defines the number of data points for a single transform. To reduce computational overhead, multiple transforms can be performed concurrently up to the 1024–point limit. This field sets the number of points for a single transform while the number of concurrent transforms is determined by Configuration Register 2 (CR2[14:8]). The total number of data points for any operation is obtained by multiplying the single transform length by the "number of transforms" in CR2:

(Transform Length)•(No. of Transforms)=Total number of data points

For all non–transform operations, use of transform length = 16 is recommended. This provides the maximum flexibility in selecting the size of the data set, allowing any number of points which is a multiple of 16 (see Table 2).

FFT Addressing Sequence CR1[7:6]

00 No Bit–reverse (In–Place, Sequential Addressing) (Use for Non–FFT Operations)
01 Bit–reverse address during first pass read
10 Bit–reverse address during last pass write
11 Bit–reverse address during first pass read and last pass write

Several types of address sequences are available for transforms. Data scrambling is required when performing the FFT/IFFT. If the data is scrambled in memory prior to the start of the transform, then it can be done "in–place", thereby reducing the external memory requirements (see Applications). If data is stored in sequence, the TMC2310 must perform scrambling during the first pass of the transform (CR1[7:6] = 01 or 11). The scrambling amounts to a bit–wise reversing of the memory address. When performing the "bit–reversed" addressing, the user must provide additional memory for intermediate storage to avoid overwriting unused input data. The user must also store the window function in either bit–reversed or sequential order to match the ordering to the input data. (See Applications section.)

Bit–reversing the memory address during the last data pass write (CR1[7:6] = 10 or 11) may be useful if the data will undergo additional FFT processing. The final results are placed in scrambled order in preparation for the next operation.

Scaling Modes CR1[5]

0 Auto Scaling
1 Manual Scaling (Use for All Non–FFT Operations)

This field determines the input data shifting. For multiple pass transforms using auto scaling, the input data is shifted by the number of bits set by the manual scale factor (CR1[4:3]) for the first pass or by the Last Pass Overflow scaler (W_{5-4}) determined from the last pass of the previous operation (CR2[3]). Subsequent passes shift the data based on the overflow of the previous pass. During each pass of the FFT, the maximum overflow (0–3 bits) is monitored as results are output to external memory. The overflow value is used as a shift count for incoming data on the next pass. The number of shifts performed during all passes (including the first pass) and the overflow from the final data pass are available on the W–Bus using the SCaler ENable control (SCEN).

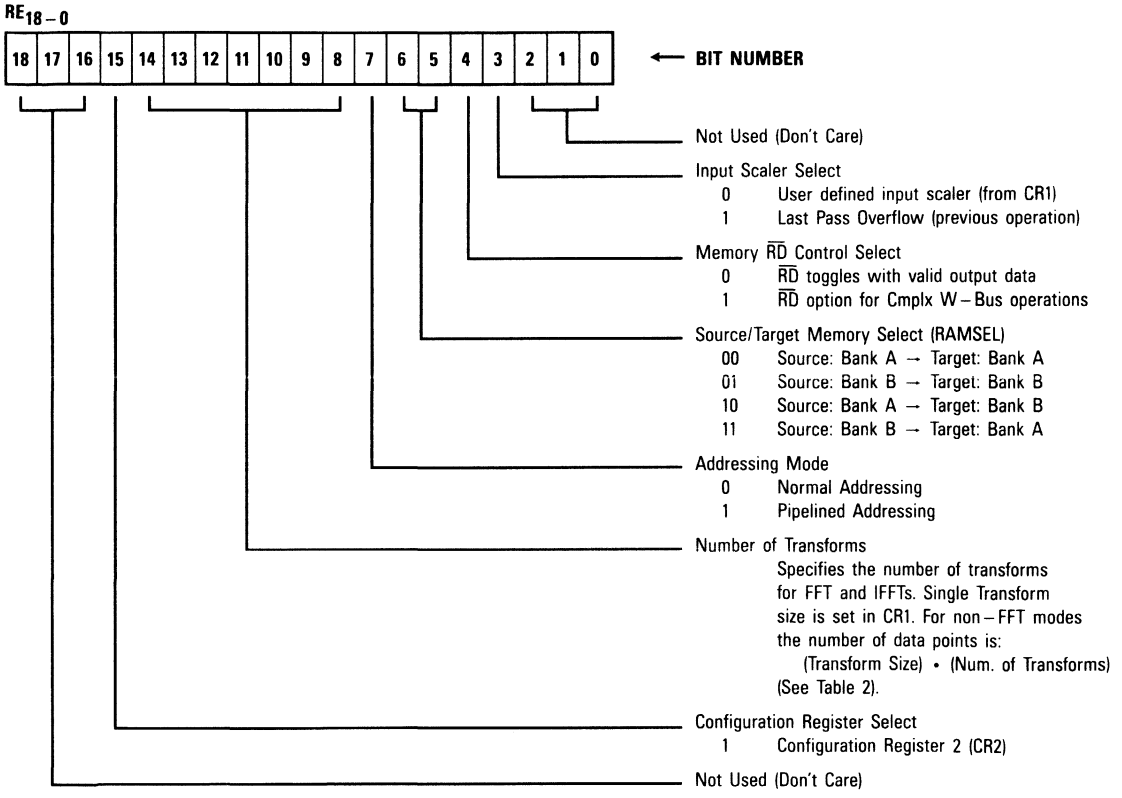
Use of manual scaling disables the overflow detection circuitry and shifts input data on every pass. The shift amount for each pass is determined by the manual scale factor set in CR1[4:3].

Manual Scale Factor CR1[4:3]

00 Shift by 0 bits
01 Shift by 1 bit
10 Shift by 2 bits
11 Shift by 3 bits

This field specifies the number of shifts performed on the input data. In auto scaling, it defines the shift performed on the first data pass only. For manual scaling, the data is shifted by this value on each pass. If the Input Scaler Select (CR2[3]) is activated to use the Last Pass Overflow scaler then the Manual Scale Factor will be overridden during the first data pass in either the Auto or Manual Scaling modes. Also, the initial or first pass shift factor specified for either Auto or Manual Scaling will not be included in the Data Block (Scaler) exponent, W[3:0]. The user must be cautious when performing manual scaling in order to avoid arithmetic errors due to incorrect scaling. (See Applications section.)

Configuration Register 2 (CR2) Format



F

Configuration Register 2 (CR2)

Configuration Register 2 is used to define the operation of the RAMSEL and $\overline{RD}$ signals, the addressing modes and the total number of data points for each operation.

Number of Transforms CR2[14:8]

0000000	Undefined
bbbbbbb	Number of 16 – point transforms
bbbbbb0	Number of 32 – point transforms
bbbbb00	Number of 64 – point transforms
bbbb000	Number of 128 – point transforms
bbb0000	Number of 256 – point transforms
bb00000	Number of 512 – point transforms
1000000	Single 1024 – point transform

This parameter is used in conjunction with the single transform length set in CR1. The total number of points is determined by multiplying the transform length by the number of transforms. The possible combinations of transform length and number of transform/data points are specified in Table 2.

Table 2. Possible Combinations of Transform Length and Number of Transforms

Trans. Length CR1[10:8]	Num. Transforms CR2[14:8]	Number of FFT Transforms	Number of Taps or Data Words
xxx	0000000	Undefined for all transform sizes	
000	xxxxxxx	Undefined for all transform sizes	
001 16 – Point	0000001	1 Transform	16 Taps/Words
	0000010	2 Transforms	32 Taps/Words
	0000011	3 Transforms	48 Taps/Words
	•	•	•
	•	•	•
	1000000	64 Transforms	1024 Taps/Words
010 32 – Point	0000010	1 Transform	32 Taps/Words
	0000100	2 Transforms	64 Taps/Words
	0000110	3 Transforms	96 Taps/Words
	•	•	•
	•	•	•
	1000000	32 Transforms	1024 Taps/Words
011 64 – Point	0000100	1 Transform	64 Taps/Words
	0001000	2 Transforms	128 Taps/Words
	0001100	3 Transforms	192 Taps/Words
	•	•	•
	•	•	•
	1000000	16 Transforms	1024 Taps/Words
100 128 – Point	0001000	1 Transform	128 Taps/Words
	0010000	2 Transforms	256 Taps/Words
	0011000	3 Transforms	384 Taps/Words
	•	•	•
	•	•	•
	1000000	8 Transforms	1024 Taps/Words
101 256 – Point	0010000	1 Transform	256 Taps/Words
	0100000	2 Transforms	512 Taps/Words
	0110000	3 Transforms	768 Taps/Words
	1000000	4 Transforms	1024 Taps/Words
110 512 – Point	0100000	1 Transform	512 Taps/Words
	1000000	2 Transforms	1024 Taps/Words
111 1024 – Point	1000000	1 Transform	1024 Taps/Words

Addressing Mode CR2[7]

0 Normal Addressing
1 Pipelined Addressing

This field selects the addressing mode for external memory access. In normal addressing, the memory address, $\overline{RD}$, RAMSEL and the read/write data are output on the same clock cycle. In pipelined addressing, the address, $\overline{RD}$, and RAMSEL outputs appear one clock cycle prior to the data. This enables the system to setup one cycle in advance by externally registering the address and controls. In both modes, the $\overline{WR}$ strobe is synchronized with the data and is guaranteed to meet data setup and hold times. Pipelined addressing is supported for all device operations. (See Applications section.)

Source/Target Memory Select CR2[6:5]

00 Source: Bank A (RAMSEL = HIGH)
Target: Bank A (RAMSEL = HIGH)

01 Source: Bank B (RAMSEL = LOW)
Target: Bank B (RAMSEL = LOW)

10 Source: Bank A (RAMSEL = HIGH)
Target: Bank B (RAMSEL = LOW)

11 Source: Bank B (RAMSEL = LOW)
Target: Bank A (RAMSEL = HIGH)

This field allows the user to select the locations of the initial data inputs and the final data results in multiple memory bank systems. Use of banked memory systems allow I/O operations to be overlapped with arithmetic processing. RAMSEL allows the device to select between the two banks of memory (RAMSEL = HIGH indicating Bank A and RAMSEL = LOW indicating memory Bank B). It may also be used as an additional address line in paged memory systems.

Transform operations require multiple data passes. The state of RAMSEL for each pass is based on the FFT addressing sequence (CR1[7:6]), the pass number and the Source/Target Memory select. Passes involving bit-reversed addressing require that RAMSEL toggle between reading and writing to prevent overwriting unused data. The TMC2310 identifies passes involving bit-reversed addressing and sets RAMSEL accordingly. During a bit-reverse pass, the TMC2310 either reads data with RAMSEL = HIGH and outputs with RAMSEL = LOW, or, reads with RAMSEL = LOW and outputs with RAMSEL = HIGH. Systems utilizing bit-reversed addressing must use RAMSEL for memory control to obtain proper results.

The operation of RAMSEL for transform operations is defined in tables 3, 4, 5 and 6. The state of RAMSEL is shown for each pass. The table indicates the logic level of RAMSEL for input and output during each pass. All single pass (non-FFT) operations (except FIR) allow the source and target data locations to be specified with this two-bit control parameter.

For FIR filter operations, RAMSEL has been designed to differentiate device outputs between shifted data samples and the accumulated convolutional sum output at the end of each pass. When CR2[6:5] is set to "00" or "10" RAMSEL remains HIGH (Bank A) for all reads and writes (data shifting in memory) except during the last write. The last write of an FIR pass is the convolutional sum, which is output with RAMSEL = LOW. When CR2[6:5] is set to "01" or "11" RAMSEL remains LOW (Bank B) for all reads and writes except during the last output cycle when the sum result is written to memory with RAMSEL = HIGH.

Upon power-up RESET, RAMSEL will be in a HIGH state. Once CR2 has been loaded into the device, RAMSEL will reflect the Source/Target Memory Selection specified in CR2[6:5]. After the operation has been completed and the DONE flag has returned to a HIGH state, RAMSEL will return to the "Source" state designated in CR2[6:5] unless a RESET has been applied. RESET will clear CR2[5] and force RAMSEL HIGH.

Application of the RESET command will clear CR2[5] and force RAMSEL = HIGH. CR2 must be loaded into the device to activate this option.

Memory $\overline{RD}$ Control Select CR2[4]

0 $\overline{RD}$ toggles to denote valid output results
1 $\overline{RD}$ option for Complex W-Bus operations

During all device operations, $\overline{RD}$ indicates the direction of the RE and IM data buses. When LOW, the TMC2310 is performing a read (input) operation, and a HIGH indicates a write (outputs enabled) operation. When the device performs operations requiring complex inputs to the W-Bus, real and imaginary inputs are time multiplexed on successive cycles. W_R inputs appear with the RE and IM data inputs ($\overline{RD}$ = LOW) while the W_I inputs appear

on the following cycle, when the device is outputting results ($\overline{RD}$ = HIGH). Due to the latency in the architecture of the device, however, results will not appear for at least seven cycles from the corresponding inputs. Under normal operations (CR2[4] = 0) the $\overline{RD}$ signal will not be activated until the first valid result appears, afterwhich $\overline{RD}$ will toggle on successive cycles. For operations that require complex W–Bus inputs CR2[4] can be set HIGH to allow the $\overline{RD}$ signal to toggle upon application of the START command. This will enable the W_R and W_I inputs to be synchronized with the FALLING and RISING edge of the $\overline{RD}$ signal, respectively. For modes that do not involve complex inputs to the W–Bus the $\overline{RD}$ Control Select should be set LOW.

Application of the RESET command will clear CR2[4], therefore, CR2 must be loaded into the device to activate this option.

Input Scaler Select (First Pass Only) CR2[3]

0 First Pass Input Scaler defined in CR1[4:3]
1 Last Pass Overflow from previous operation used as Scaler Input

Under normal operations the input data scale factor must be specified for the first pass of any operation using the Manual Scale Factor CR1[4:3]. For some applications it may be necessary to perform additional signal processing functions on the existing data set. When activated (CR2[3] = 1), this option allows the Last Pass Overflow scaler from the previous operation to be used as the input scaler for the next operation. This feature eliminates the user from extracting the $W_{5:4}$ field from the W–Bus and will be useful to post process the data after a particular application. For example, the user may want to rescale the 19–bit data to 16 bits following an FFT operation. By activating this feature, the Last Pass Overflow scaler (from the FFT) will be used to rescale the data as it is input to the device for a multiplication by 1.0 (0.9999...). Additional operations that will benefit from this feature are MAGSQ or a filter multiplication following the FFT.

Application of the RESET command will clear CR2[3] and the scaler exponent field (W_{5-0}). CR2 must be loaded into the device to activate this option.

Tables 3, 4, 5 and 6 show the operation of RAMSEL for multiple pass transforms. The state of RAMSEL is shown for read and write operations during each data pass.

For example:

16–point FFT (Real or No Window)

Source = Bank A; Target = Bank A (CR2[6:5] = 00)
Bit–reverse addressing on first pass read (CR1[7:6] = 01)

Pass 0: Input data with RAMSEL = H (HIGH)
Output data with RAMSEL = L (LOW)
(Data moved from Bank A to Bank B)

Pass 1: Input data with RAMSEL = LOW
Output data with RAMSEL = HIGH
(Data moved from Bank B back to Bank A)

16–point Complex Multiply + FFT

Source = Bank B; Target = Bank B (CR2[6:5] = 01)
Bit–reverse addressing on first pass read (CR1[7:6] = 01)

Pass W: Input data with RAMSEL = L (LOW)
Output data with RAMSEL = L (LOW)
(Data remains in Bank B)

Pass 0: Input data with RAMSEL = L (LOW)
Output data with RAMSEL = H (HIGH)
(Data moved from Bank B to Bank A)

Pass 1: Input data with RAMSEL = HIGH
Output data with RAMSEL = LOW
(Data moved from Bank A back to Bank B)

The tables are valid for single and multiple transforms, however, RAMSEL operation is determined by the single transform size only.

Table 3a. RAMSEL Operation for Source = Bank A (RAMSEL=HIGH); Target = Bank A (RAMSEL=HIGH) Operation: FFT/IFFT Real or No Windowing

Source/Target CR2[6:5]	Addressing Seq. CR1[7:6]	Single Transform Size	Pass 0 [1] Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
00	00	16	H/H	H/H			
		32	H/H	H/H	H/H		
		64	H/H	H/H	H/H		
		128	H/H	H/H	H/H	H/H	
		256	H/H	H/H	H/H	H/H	
		512	H/H	H/H	H/H	H/H	H/H
		1024	H/H	H/H	H/H	H/H	H/H
	01, 10 or 11	16	H/L	L/H			
		32	H/L	L/L	L/H		
		64	H/L	L/L	L/H		
		128	H/L	L/L	L/L	L/H	
		256	H/L	L/L	L/L	L/H	
		512	H/L	L/L	L/L	L/L	L/H
		1024	H/L	L/L	L/L	L/L	L/H

Note: 1. H = HIGH
L = LOW

Table 3b. RAMSEL Operation for Source = Bank A (RAMSEL=HIGH); Target = Bank A (RAMSEL=HIGH) Operation: Complex Multiply + FFT/IFFT

Source/ Target CR2[6:5]	Addressing Sequence CR1[7:6]	Single Transform Size	Pass W [1,2] Read/Write	Pass 0 Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
00	00	16	H/H	H/H	H/H			
		32	H/H	H/H	H/H	H/H		
		64	H/H	H/H	H/H	H/H		
		128	H/H	H/H	H/H	H/H	H/H	
		256	H/H	H/H	H/H	H/H	H/H	
		512	H/H	H/H	H/H	H/H	H/H	H/H
		1024	H/H	H/H	H/H	H/H	H/H	H/H
	01, 10 or 11	16	H/H	H/L	L/H			
		32	H/H	H/L	L/L	L/H		
		64	H/H	H/L	L/L	L/H		
		128	H/H	H/L	L/L	L/L	L/H	
		256	H/H	H/L	L/L	L/L	L/H	
		512	H/H	H/L	L/L	L/L	L/L	L/H
		1024	H/H	H/L	L/L	L/L	L/L	L/H

Notes: 1. H = HIGH
L = LOW
2. Pass "W" is the complex multiplication pass for FFT/IFFTs that perform complex multiplication prior to the transform.

Table 4a. RAMSEL Operation for Source = Bank B (RAMSEL=LOW); Target = Bank B (RAMSEL=LOW) Operation: FFT/IFFT Real or No Windowing

Source/Target CR2[6:5]	Addressing Seq. CR1[7:6]	Single Transform Size	Pass 0 [1] Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
01	00	16	L/L	L/L			
		32	L/L	L/L	L/L		
		64	L/L	L/L	L/L		
		128	L/L	L/L	L/L	L/L	
		256	L/L	L/L	L/L	L/L	
		512	L/L	L/L	L/L	L/L	L/L
		1024	L/L	L/L	L/L	L/L	L/L
	01, 10 or 11	16	L/H	H/L			
		32	L/H	H/H	H/L		
		64	L/H	H/H	H/L		
		128	L/H	H/H	H/H	H/L	
		256	L/H	H/H	H/H	H/L	
		512	L/H	H/H	H/H	H/H	H/L
		1024	L/H	H/H	H/H	H/H	H/L

Note: 1. H = HIGH
L = LOW

Table 4b. RAMSEL Operation for Source = Bank B (RAMSEL=LOW); Target = Bank B (RAMSEL=LOW) Operation: Complex Multiply + FFT/IFFT

Source/ Target CR2[6:5]	Addressing Sequence CR1[7:6]	Single Transform Size	Pass W [1,2] Read/Write	Pass 0 Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
01	00	16	L/L	L/L	L/L			
		32	L/L	L/L	L/L	L/L		
		64	L/L	L/L	L/L	L/L		
		128	L/L	L/L	L/L	L/L	L/L	
		256	L/L	L/L	L/L	L/L	L/L	
		512	L/L	L/L	L/L	L/L	L/L	L/L
		1024	L/L	L/L	L/L	L/L	L/L	L/L
	01, 10 or 11	16	L/L	L/H	H/L			
		32	L/L	L/H	H/H	H/L		
		64	L/L	L/H	H/H	H/L		
		128	L/L	L/H	H/H	H/H	H/L	
		256	L/L	L/H	H/H	H/H	H/L	
		512	L/L	L/H	H/H	H/H	H/H	H/L
		1024	L/L	L/H	H/H	H/H	H/H	H/L

Notes: 1. H = HIGH
L = LOW
2. Pass "W" is the complex multiplication pass for FFT/IFFTs that perform complex multiplication prior to the transform.

Table 5a. RAMSEL Operation Source = Bank A; Target = Bank B
Operation: FFT/IFFT Real or No Windowing

Source/Target CR2[6:5]	Addressing Seq. CR1[7:6]	Single Transform Size	Pass 0 [1] Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
10	00, 01	16	H/L	L/L			
		32	H/L	L/L	L/L		
		64	H/L	L/L	L/L		
		128	H/L	L/L	L/L	L/L	
		256	H/L	L/L	L/L	L/L	
		512	H/L	L/L	L/L	L/L	L/L
		1024	H/L	L/L	L/L	L/L	L/L
	10	16	H/H	H/L			
		32	H/H	H/H	H/L		
		64	H/H	H/H	H/L		
		128	H/H	H/H	H/H	H/L	
		256	H/H	H/H	H/H	H/L	
		512	H/H	H/H	H/H	H/H	H/L
		1024	H/H	H/H	H/H	H/H	H/L
	11	16	Not Allowed				
		32	H/L	L/H	H/L		
		64	H/L	L/H	H/L		
		128	H/L	L/H	H/H	H/L	
		256	H/L	L/H	H/H	H/L	
		512	H/L	L/H	H/H	H/H	H/L
		1024	H/L	L/H	H/H	H/H	H/L

Note: 1. H = HIGH
L = LOW

F

Table 5b. RAMSEL Operation Source = Bank A; Target = Bank B Operation: Complex Multiply + FFT/IFFT

Source/ Target CR2[6:5]	Addressing Sequence CR1[7:6]	Single Transform Size	Pass W [1,2] Read/Write	Pass 0 Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
10	00	16	H/L	L/L	L/L			
		32	H/L	L/L	L/L	L/L		
		64	H/L	L/L	L/L	L/L		
		128	H/L	L/L	L/L	L/L	L/L	
		256	H/L	L/L	L/L	L/L	L/L	
		512	H/L	L/L	L/L	L/L	L/L	L/L
		1024	H/L	L/L	L/L	L/L	L/L	L/L
	01	16	H/H	H/L	L/L			
		32	H/H	H/L	L/L	L/L		
		64	H/H	H/L	L/L	L/L		
		128	H/H	H/L	L/L	L/L	L/L	
		256	H/H	H/L	L/L	L/L	L/L	
		512	H/H	H/L	L/L	L/L	L/L	L/L
		1024	H/H	H/L	L/L	L/L	L/L	L/L
	10	16	H/H	H/H	H/L			
		32	H/H	H/H	H/H	H/L		
		64	H/H	H/H	H/H	H/L		
		128	H/H	H/H	H/H	H/H	H/L	
		256	H/H	H/H	H/H	H/H	H/L	
		512	H/H	H/H	H/H	H/H	H/H	H/L
		1024	H/H	H/H	H/H	H/H	H/H	H/L
	11	16	Not Allowed					
		32	H/H	H/L	L/H	H/L		
		64	H/H	H/L	L/H	H/L		
		128	H/H	H/L	L/H	H/H	H/L	
		256	H/H	H/L	L/H	H/H	H/L	
		512	H/H	H/L	L/H	H/H	H/H	H/L
		1024	H/H	H/L	L/H	H/H	H/H	H/L

Notes:
1. H = HIGH
   L = LOW
2. Pass "W" is the complex multiplication pass for FFT/IFFTs that perform complex multiplication prior to the transform.

Table 6a. RAMSEL Operation Source = Bank B; Target = Bank A
Operation: FFT/IFFT Real or No Windowing

Source/Target CR2[6:5]	Addressing Seq. CR1[7:6]	Single Transform Size	Pass 0 [1] Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
11	00, 01	16	L/H	H/H			
		32	L/H	H/H	H/H		
		64	L/H	H/H	H/H		
		128	L/H	H/H	H/H	H/H	
		256	L/H	H/H	H/H	H/H	
		512	L/H	H/H	H/H	H/H	H/H
		1024	L/H	H/H	H/H	H/H	H/H
	10	16	L/L	L/H			
		32	L/L	L/L	L/H		
		64	L/L	L/L	L/H		
		128	L/L	L/L	L/L	L/H	
		256	L/L	L/L	L/L	L/H	
		512	L/L	L/L	L/L	L/L	L/H
		1024	L/L	L/L	L/L	L/L	L/H
	11	16	Not Allowed				
		32	L/H	H/L	L/H		
		64	L/H	H/L	L/H		
		128	L/H	H/L	L/L	L/H	
		256	L/H	H/L	L/L	L/H	
		512	L/H	H/L	L/L	L/L	L/H
		1024	L/H	H/L	L/L	L/L	L/H

Note: 1. H = HIGH
L = LOW

F

Table 6b. RAMSEL Operation Source = Bank B; Target = Bank A Operation: Complex Multiply + FFT/IFFT

Source/ Target CR2[6:5]	Addressing Sequence CR1[7:6]	Single Transform Size	Pass W [1,2] Read/Write	Pass 0 Read/Write	Pass 1 Read/Write	Pass 2 Read/Write	Pass 3 Read/Write	Pass 4 Read/Write
11	00	16	L/H	H/H	H/H			
		32	L/H	H/H	H/H	H/H		
		64	L/H	H/H	H/H	H/H		
		128	L/H	H/H	H/H	H/H	H/H	
		256	L/H	H/H	H/H	H/H	H/H	
		512	L/H	H/H	H/H	H/H	H/H	H/H
		1024	L/H	H/H	H/H	H/H	H/H	H/H
	01	16	L/L	L/H	H/H			
		32	L/L	L/H	H/H	H/H		
		64	L/L	L/H	H/H	H/H		
		128	L/L	L/H	H/H	H/H	H/H	
		256	L/L	L/H	H/H	H/H	H/H	
		512	L/L	L/H	H/H	H/H	H/H	H/H
		1024	L/L	L/H	H/H	H/H	H/H	H/H
	10	16	L/L	L/L	L/H			
		32	L/L	L/L	L/L	L/H		
		64	L/L	L/L	L/L	L/H		
		128	L/L	L/L	L/L	L/L	L/H	
		256	L/L	L/L	L/L	L/L	L/H	
		512	L/L	L/L	L/L	L/L	L/L	L/H
		1024	L/L	L/L	L/L	L/L	L/L	L/H
	11	16	Not Allowed					
		32	L/L	L/H	H/L	L/H		
		64	L/L	L/H	H/L	L/H		
		128	L/L	L/H	H/L	L/L	L/H	
		256	L/L	L/H	H/L	L/L	L/H	
		512	L/L	L/H	H/L	L/L	L/L	L/H
		1024	L/L	L/H	H/L	L/L	L/L	L/H

Notes: 1. H = HIGH
L = LOW

2. Pass "W" is the complex multiplication pass for FFT/IFFTs that perform complex multiplication prior to the transform.

Figure 3. Input/Clock Timing

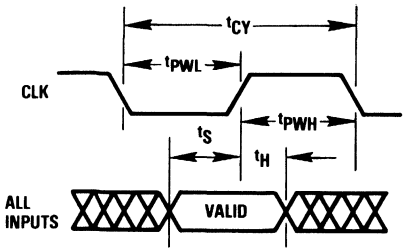


Figure 4. Read Cycle Timing

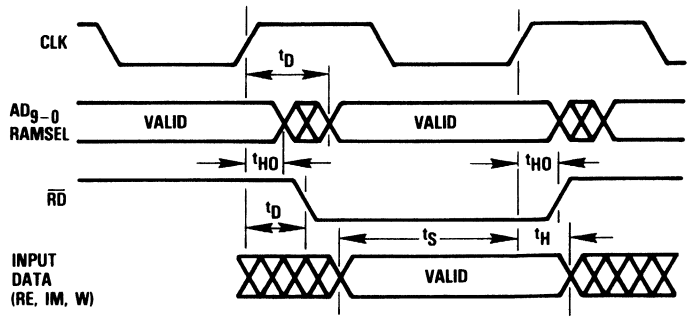


Figure 5. Write Cycle Timing

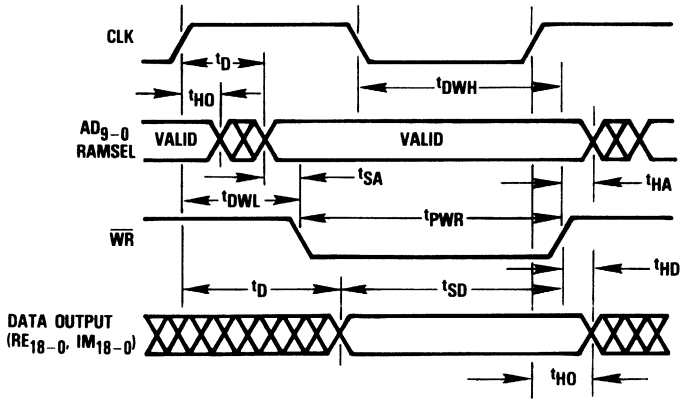


Figure 6. Scaler Timing

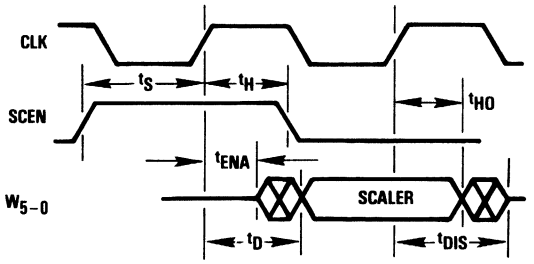


Figure 7. RESET Timing

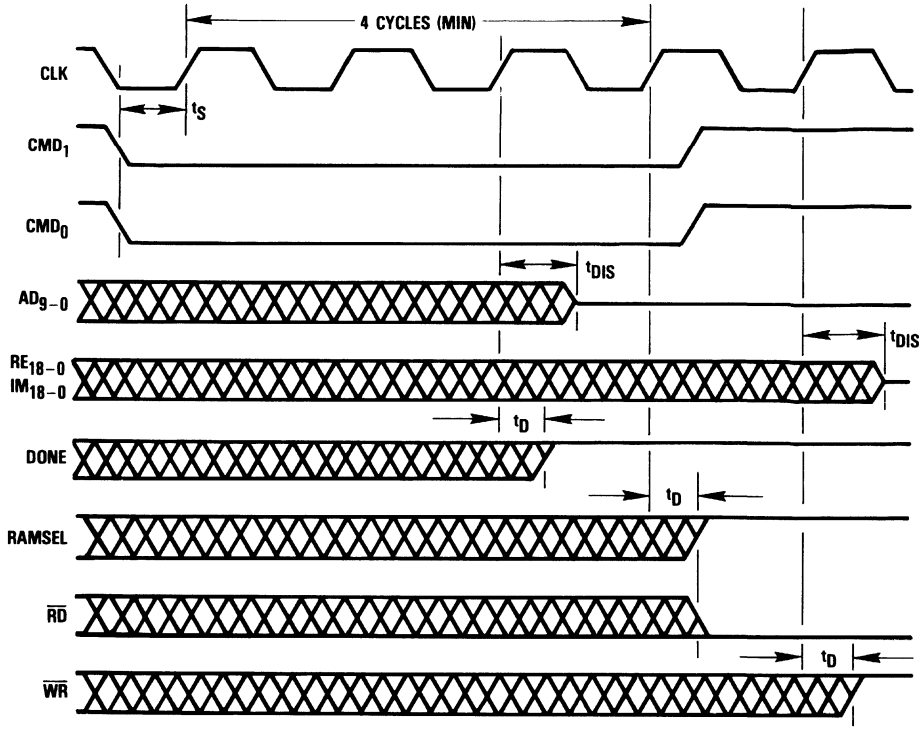


Figure 8. Configuration Register Load Timing

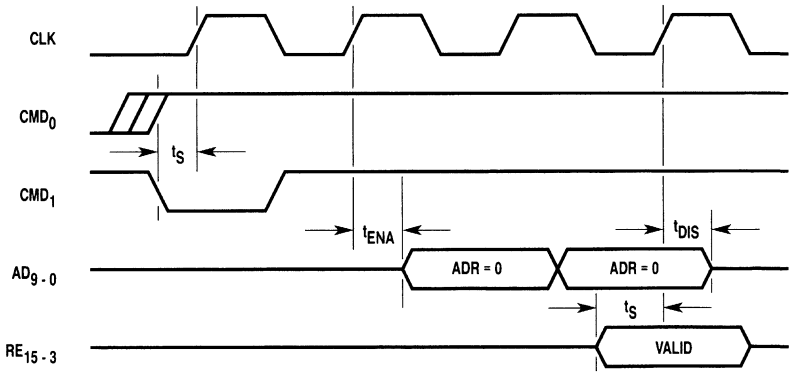


Figure 9. START Timing (Shown for FFT/IFFT with Windowing)

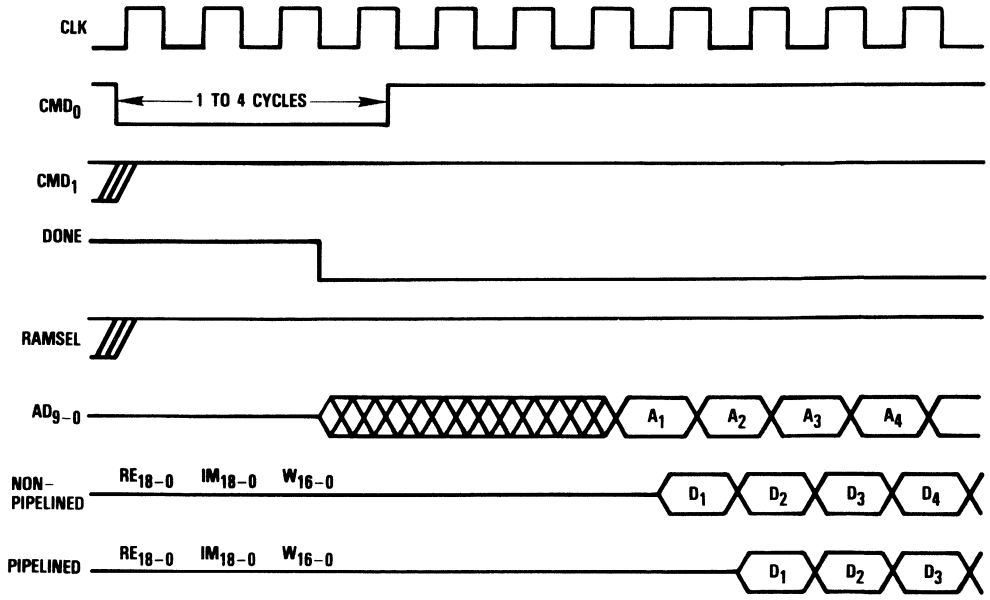


Figure 10. DONE Timing (Shown for FFT/IFFT)

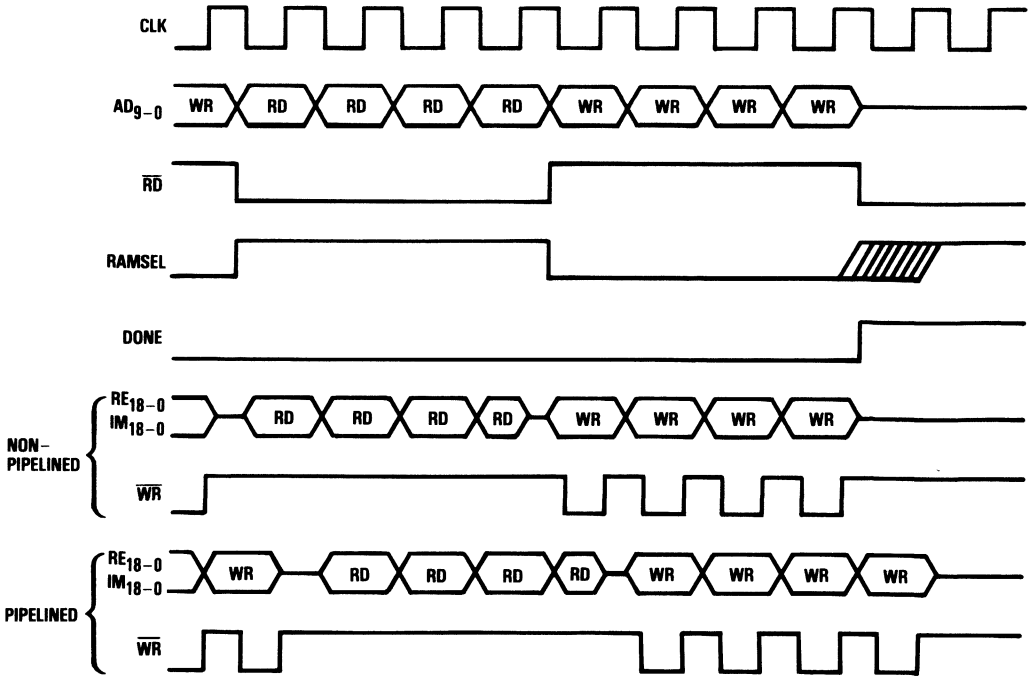
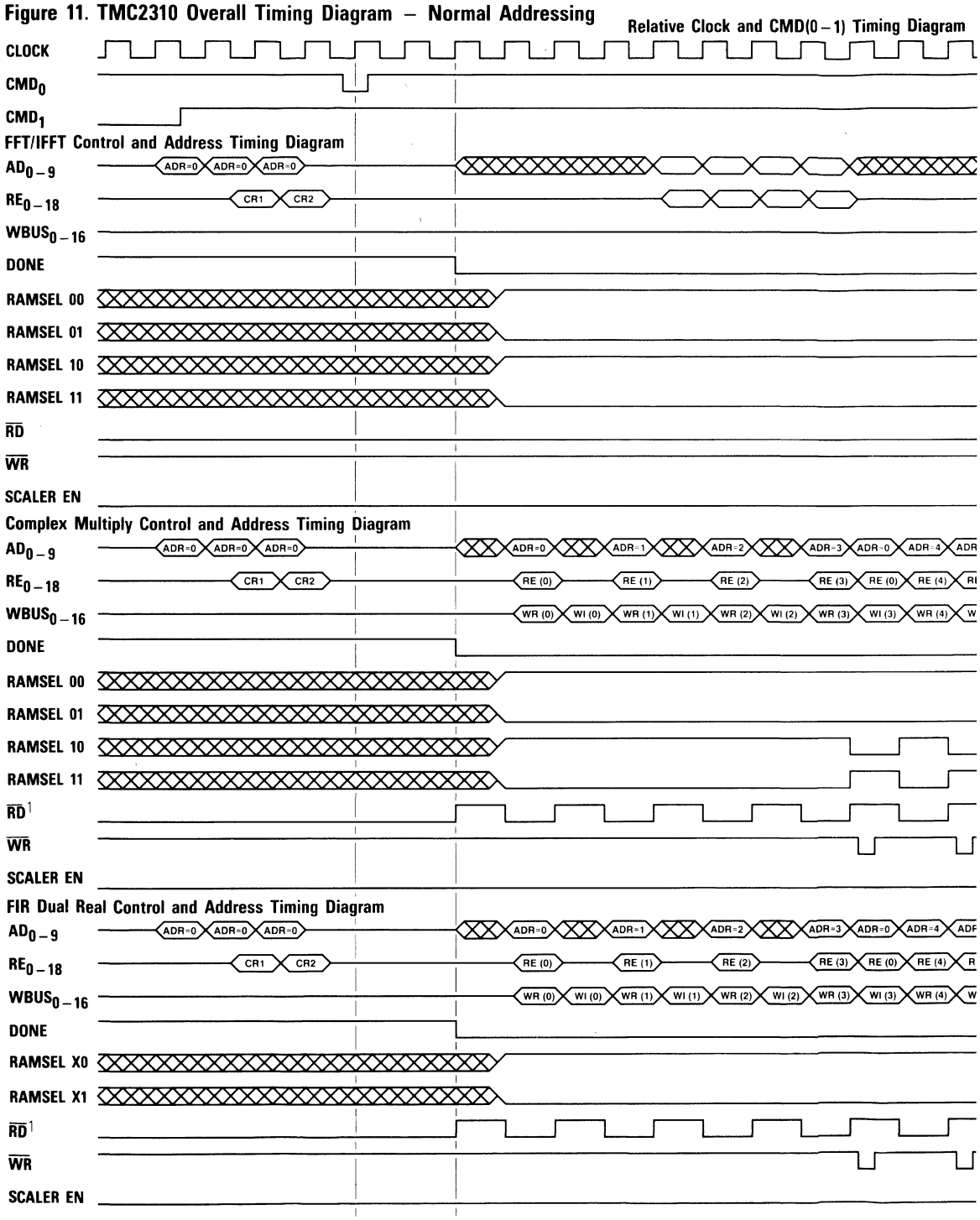
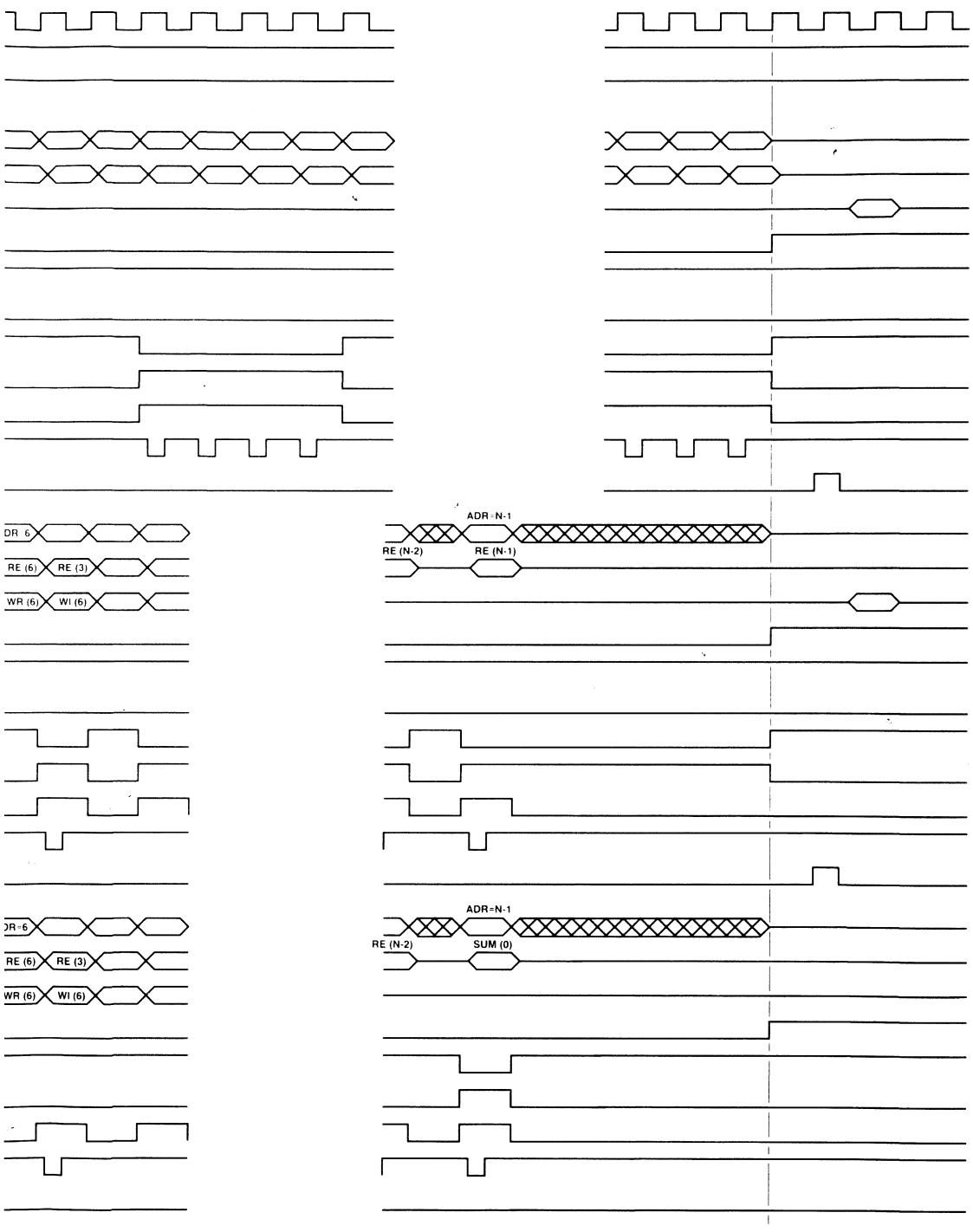


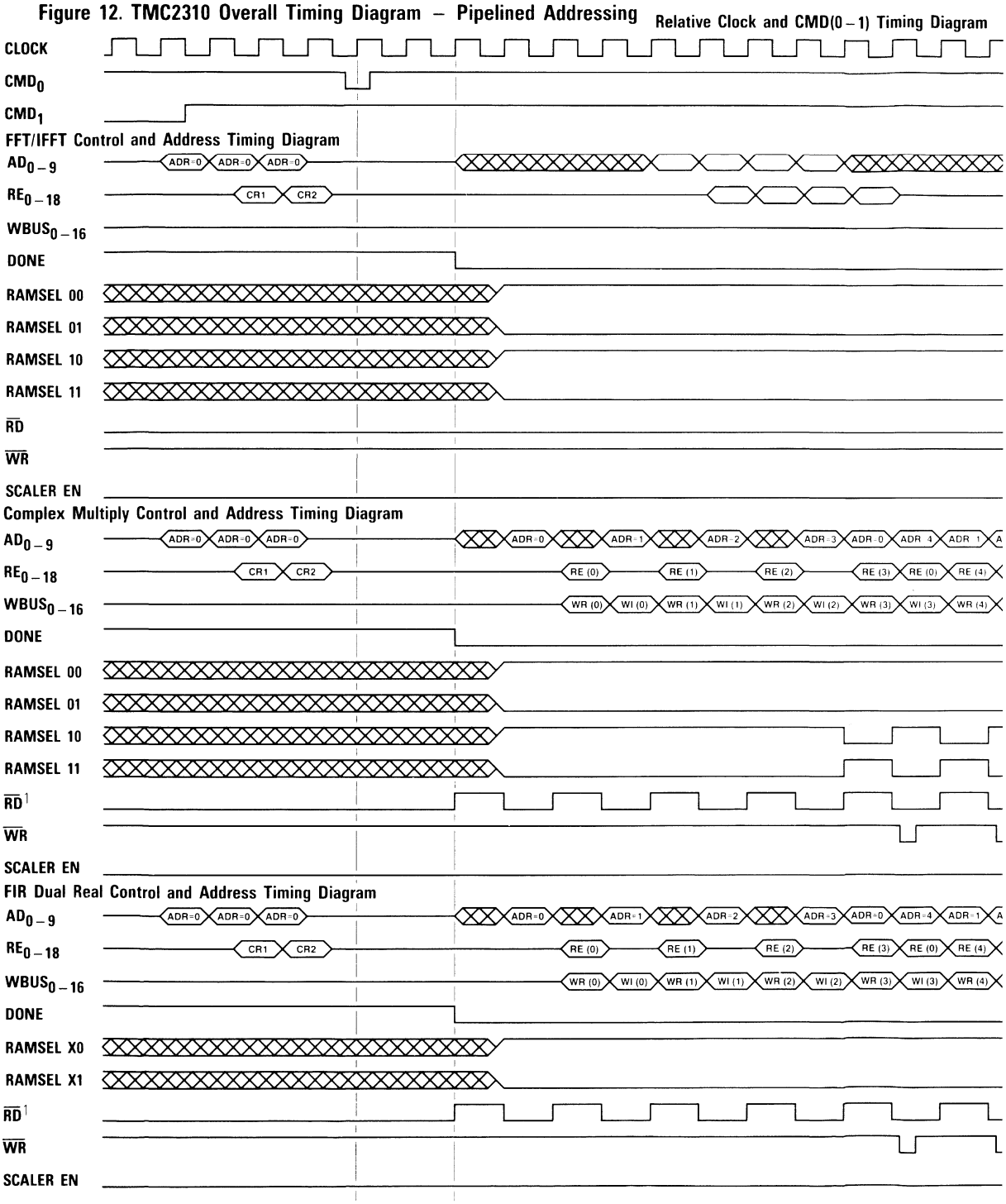
Figure 11. TMC2310 Overall Timing Diagram – Normal Addressing




DR 6
RE (6)
RE (3)
WR (6)
WI (6)
ADR=N-1
RE (N-2)
RE (N-1)
DR=6
RE (6)
RE (3)
WR (6)
WI (6)
ADR=N-1
RE (N-2)
SUM (0)

F

Figure 12. TMC2310 Overall Timing Diagram – Pipelined Addressing



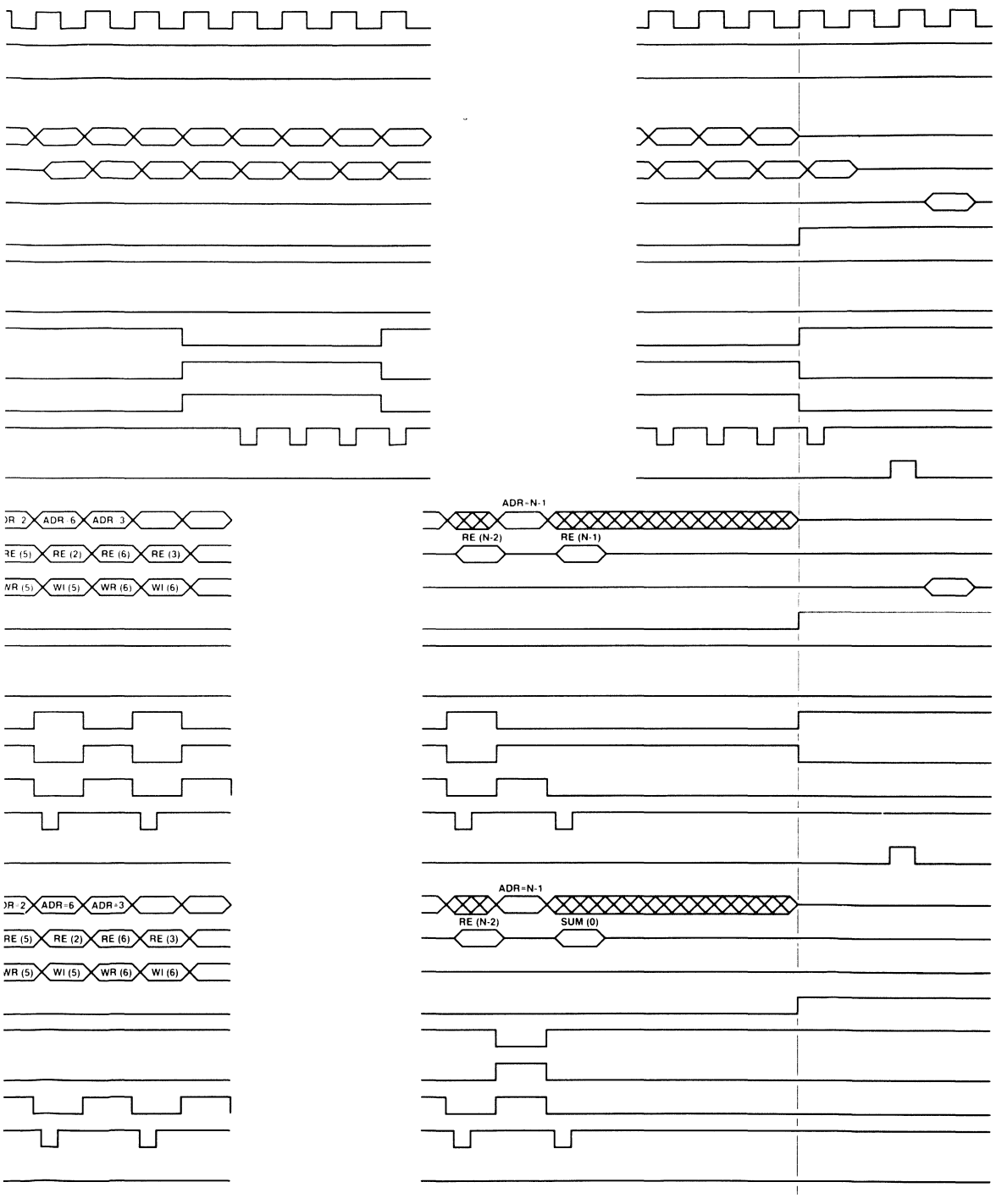

ADR-N-1
RE (N-2)
RE (N-1)
ADR-N-1
RE (N-2)
SUM (0)

Figure 13. Equivalent Input Circuit

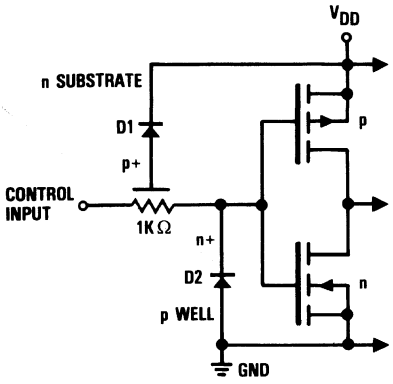
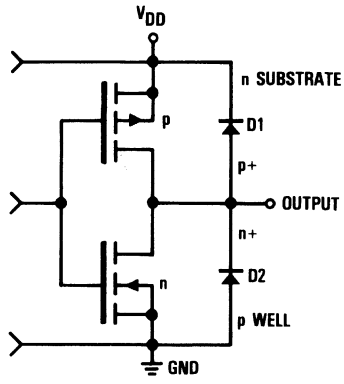


Figure 14. Equivalent Output Circuit



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage [2]	−0.5 to (V_{DD} + 0.5)V
Forced current [3,4]	−3.0 to 6.0mA
Short−circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	+175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Extended −1 Min	Extended −1 Nom	Extended −1 Max	Extended Min	Extended Nom	Extended Max	Units
V_{DD}	Supply Voltage	4.75	5.0	5.25				4.5	5.0	5.5	V
t_{CY}	Clock Cycle Time	50			50			66			ns
t_{PWH}	Clock Pulse Width HIGH	25			25			30			ns
t_{PWL}	Clock Pulse Width LOW	20			20			25			ns
t_S	Input Setup Time	7			9			11			ns
t_H	Input Hold Time	1			2			2			ns
V_{IL}	Input Voltage, Logic LOW			0.8						0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0						2.0			V
V_{IHC}	Input Voltage, Clock HIGH	2.2						2.3			V
I_{OL}	Output Current, Logic LOW			4.0						4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0						−2.0	mA
T_A	Ambient Temperature, Still Air	0		70							°C
T_C	Case Temperature							−55		125	°C

F

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V, DONE = HIGH		5		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz		150		160	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		−10		−10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = 4mA		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = −2mA	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		−20		−20	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		20		20	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		−180		−180	mA
I_{OSW}	Short-Circuit Output Current for WR	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		−180		−180	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended −1 Min	Extended −1 Max	Extended Min	Extended Max	Units
t_D	Delay Clock to Output	V_{DD} = Min, Load = 25pF							
		RE_{18-0}, IM_{18-0}		19		20		25	ns
		AD_{9-0}, RAMSEL		18		18		20	ns
		$\overline{RD}$, DONE		15		16		18	ns
		Scaler (W_{5-0})		32		38		40	ns
t_{HO}	Output Hold Time	V_{DD} = Min, Load = 25pF							
		RE_{18-0}, IM_{18-0}	4				2		ns
		AD_{9-0}, RAMSEL	4				2		ns
		$\overline{RD}$, DONE	2				2		ns
		Scaler (W_{5-0})	5				5		ns
t_{SA}	Setup Time AD_{9-0} to $\overline{WR}$ LOW	V_{DD} = Min, Load = 25pF	0				0		ns
t_{HA}	Hold Time AD_{9-0} to $\overline{WR}$ HIGH	V_{DD} = Min, Load = 25pF	10				5		ns
t_{SD}	Setup Time Data to $\overline{WR}$ HIGH (Data Valid to end of $\overline{WR}$)	V_{DD} = Min, Load = 25pF	24				22		ns
t_{HD}	Hold Time Data to $\overline{WR}$ HIGH (Data Hold from end of $\overline{WR}$)	V_{DD} = Min, Load = 25pF	10				10		ns
t_{PWR}	$\overline{WR}$ Pulse Width LOW	V_{DD} = Min, Load = 25pF	15				14		ns
t_{DWL}	Delay, Clock HIGH to $\overline{WR}$ LOW	V_{DD} = Min, Load = 25pF	11	25			10	28	ns
t_{DWH}	Delay, Clock LOW to $\overline{WR}$ HIGH	V_{DD} = Min, Load = 25pF	7	18				22	ns
t_{ENA}	Three-State Enable Delay	V_{DD} = Min, Load = 25pF		20				21	ns
t_{DIS}	Three-State Disable Delay	V_{DD} = Min, Load = 25pF		14				16	ns

Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

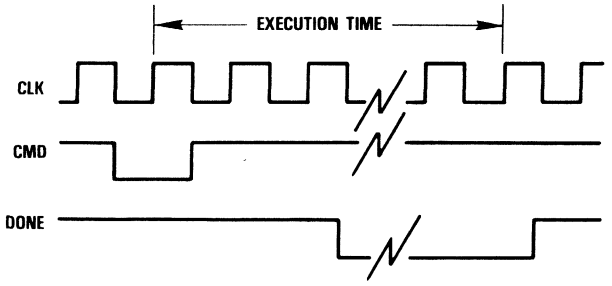
Table 7. Performance Benchmarks

Operation	Number of Points	Execution [1] Cycles	Execution Cycles (Multiple Transform Mode)	Execution Time (20MHz)	Execution Time (20MHz) (Multiple Transform)
FFT/IFFT	16	87	64/Transform + 23	4.35 μS	3.2 μS/Transform + 1.25 μS
(Real Window/No Window)	32	223	192/Transform + 31	11.15 μS	9.6 μS/Transform + 1.55 μS
	64	415	384/Transform + 31	20.75 μS	19.2 μS/Transform + 1.55 μS
	128	1063	1024/Transform + 39	53.15 μS	51.2 μS/Transform + 1.95 μS
	256	2087	2048/Transform + 39	104.35 μS	102.4 μS/Transform + 1.95 μS
	512	5167	5120/Transform + 47	258.35 μS	256.0 μS/Transform + 2.35 μS
	1024	10,287	N/A	514.35 μS	N/A
FFT/IFFT	16	132	96/Transform + 36	6.6 μS	4.8 μS/Transform + 1.8 μS
(w/Complex Multiply)	32	300	256/Transform + 44	15.0 μS	12.8 μS/Transform + 2.2 μS
	64	556	512/Transform + 44	27.8 μS	25.6 μS/Transform + 2.2 μS
	128	1332	1280/Transform + 52	66.6 μS	64.0 μS/Transform + 2.6 μS
FIR Filtering	–		2 Cycles/Point + 9		100ns/Point + 450ns
Multiplication					
Multiply – Accumulate					
Magnitude Squared	–		2 Cycles/Point + 15		100ns/Point + 750ns

Note: 1. Execution times are valid for all FFT addressing and scaling modes.
Execution time is defined as the number of clocks from CMD = START until DONE = HIGH (see below).
The number of clock cycles is obtained in the following manner:
Clock Cycles = (Num. of Passes) • (2•Total Num. of Points) + (Num. of Passes) • 8 + 7
= (2•Total Num. of Butterflies) + (Processing Overhead).

F

Figure 15. Execution Cycle Time



Note: 1. For multiple transforms, the total time can be obtained by multiplying the value in the table by the number of concurrent transforms.
Example: 16 transforms of length 64 – points:
From Table 7.: 384 clocks per transform + 31 cycles overhead.
Therefore, the total number of cycles is:
Total = (384/transform) • (16 transforms) + 31 = 6175 cycles.

Applications

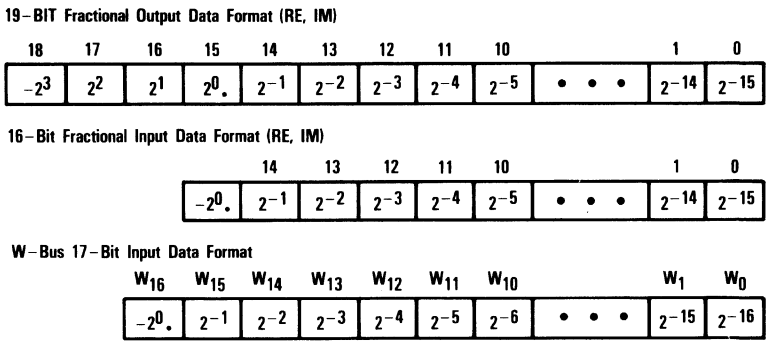
Data Formats

The input and output data formats are shown in Figure 16. Data is output on the RE and IM buses using the two's complement 19-bit data format. Input data must conform to the specified 16-bit data format detailed in Figure 16. During the first pass of any operation data input on the RE and IM buses may require scaling in order to be processed correctly by the device's arithmetic elements. Data input scaling parameters are specified according to the manual scale control set in CR1 or the input scaler select set in CR2. Only the sixteen Least Significant Bits (LSBs) or "shifted" LSBs will be passed to the arithmetic elements. If no data shift is performed, bits RE_{15} and IM_{15} must be sign extended into the three Most Significant Bits (RE_{18-16}, IM_{18-16}) to conform to the internal two's complement data buses. To perform FFTs the device supports an 18 x 17-bit multiply, however, inputs exceeding the 16-bit formats shown above may produce an intermediate overflow within the device's arithmetic elements.

The user is responsible for monitoring and accomodating data overflow for single pass instructions and for multiple pass transforms which utilize manual scaling. During multiple pass transforms, shifting can also be performed automatically (except for the first pass) by selecting the auto scale feature. If an operation may cause an overflow, sufficient memory width must be provided or data shifting performed to prevent loss of significant data. However, certain operations never cause overflow. For example, multiplication of two inputs which are both less than 1.0 will produce a result of less than 1.0. Since the MSBs of the output will always be a sign extension of the result, they can be ignored. This can simplify the memory arrangement by allowing the use of 16-bit memory systems (see Interfacing to Memory).

The W-Bus data may be reduced to 16-bit format to simplify memory interfacing. To maintain maximum accuracy, this can be accomplished in one of two ways. If using only positive window or filter coefficients, the MSB (W_{16}) may be connected to GND through a pull-down resistor (see Interfacing to 16-Bit Memory Systems). If both positive and negative coefficients are used, the LSB (W_0) can be connected to GND through a pull-down resistor.

Figure 16. Data Bus Formats



FIR Filter Operation

The TMC2310 performs both adaptive and non-adaptive coefficient Finite Inpulse Response (FIR) filters by performing a linear convolution between filter coefficients and input data. External data memory is used to store data samples and coefficients. For an N-tap filter, the data (RE, IM) memory retains the N most recent data samples and the window/coefficient memory stores the N filter coefficients.

The output of an N-tap, FIR filter is given by the convolution equation:

$$y(n-N+1) = \sum_{k=0}^{N-1} h(k)x(n-k)$$

The convolution is accomplished by multiplying data in the RE and IM memories with filter coefficients stored in external RAM or ROM and input on the W-Bus. During the multiplication/accumulation, the RE and IM data are shifted down in memory by one address in preparation for the next pass.

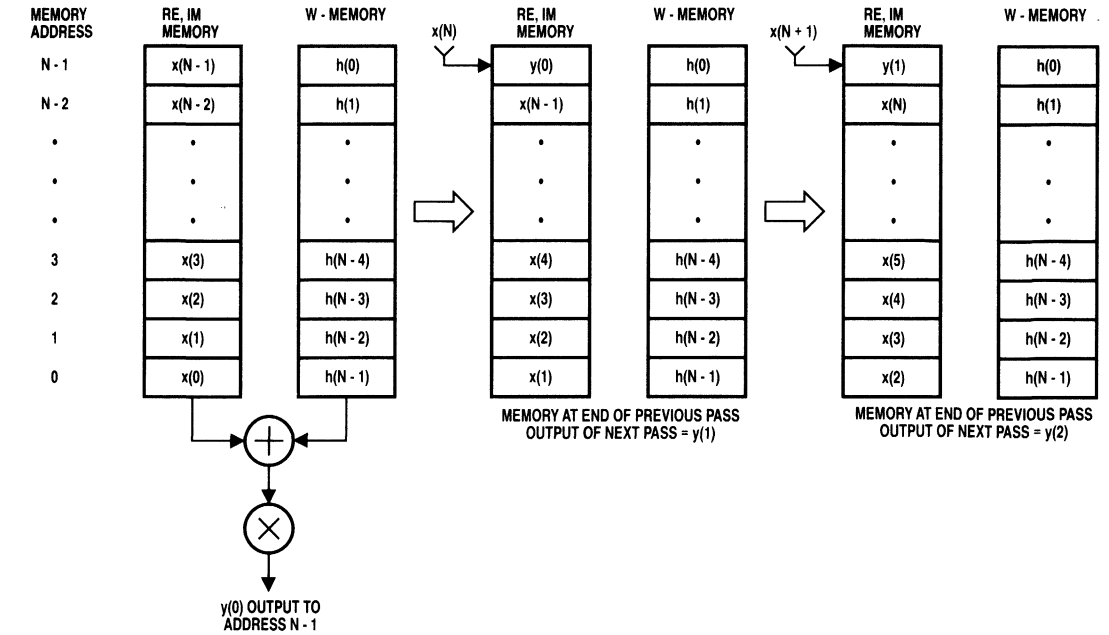
At the start of a pass, the N-most recent data samples (x(n)) are stored in memory addresses from 0 through N−1 in ascending order (oldest sample in address 0).

The filter coefficients are stored in window/coefficient memory in corresponding addresses but in reversed order. After the START command, the coefficients and data are multiplied and accumulated term-by-term, while each value in RE and IM memory is shifted down by one memory location (with RAMSEL=HIGH). Upon completion of the pass, the RE and IM data have been shifted by one location, and the final accumulated result (y(n)) is output to address=N−1 with RAMSEL=LOW. In preparation for the next pass, the result at memory address N−1 is read by the host system. Execution stops at the end of each pass to allow time to read this result and to load the next data sample. To produce the next convolution output, this new data input is stored in location N−1, and a START command is re-issued. This operation is repeated for each output point y(n).

A diagram of the ordering of data samples and filter coefficients before and after successive passes is shown in *Figure 17*. An examination of the arrangement of coefficients (h(k)) and data samples (x(n)) shows that the FIR filter equation is calculated by summing the product of filter coefficients and data points in corresponding addresses.

F

Figure 17. FIR Filter Operation



FIR Filter Operation (cont.)

The filter order (tap length) is set by the "single transform length" and "number of transform" parameters in CR1 and CR2 respectively. The allowable filter sizes are 16 to 1024 taps, in multiples of 16. The throughput rate is two clock cycles per tap, per channel.

Both the 2-Real and Real/Imaginary FIR filtering are performed as described above. The "FIR 2-Real" (CR1[14:11] = 1001) instruction utilizes one set of filter coefficients for both the $RE_{18\text{-}0}$ and $IM_{18\text{-}0}$ data. The FIR Real-Imaginary instruction allows the use of separate filter coefficients for RE and IM data. This allows simultaneous filtering of two independent Real data sets with different filter functions. Coefficients for each set are input on alternate clock cycles through the W-Bus with the use of the $\overline{RD}$ option available in CR2[4].

Adaptive FIR Filtering

Adaptive FIR filtering performs modification of filter coefficients concurrently with the convolution. Adaptive filtering operates differently than non-adaptive FIR filtering. As indicated before, the output y(n), can be obtained by convolving input data with filter coefficients:

$$y(n) = \sum_{k=0}^{N-1} h'(k)x(n-k)$$

Adaptive filters produce an error term for each filter output:

[Actual Filter Output] – [Desired Filter Output] = Error

or,

$$y(n) - y(n)' = \sigma(n)$$

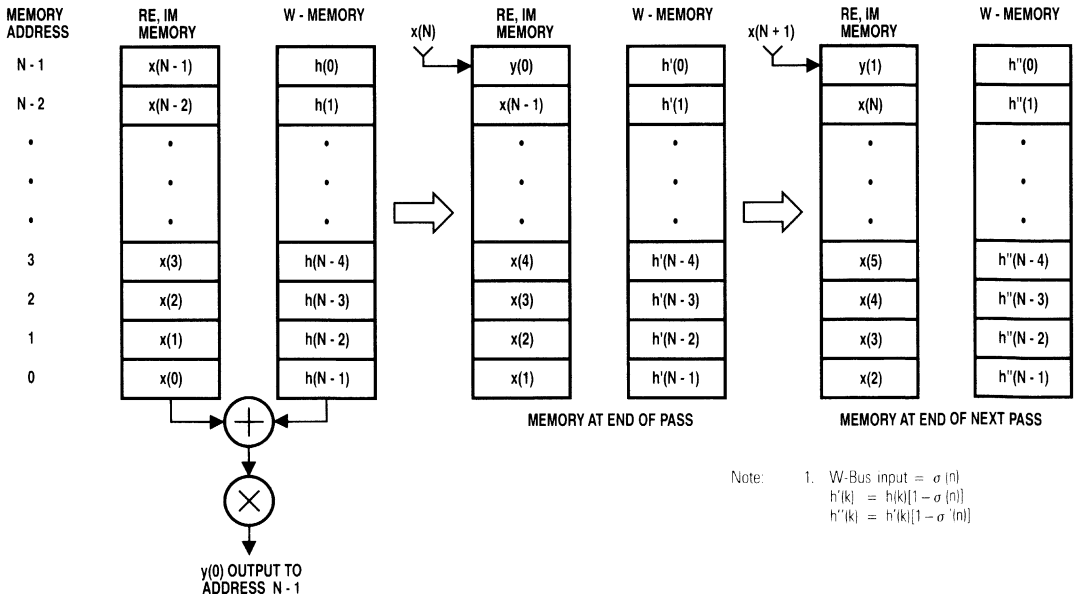
The error term is used to update the filter coefficients for the next data pass. The memory arrangement for adaptive filtering uses the RE memory for data storage and IM memory for existing and modified filter coefficients. During the pass, the data (x(n)) are shifted down one address in memory while the product of data and coefficients is being accumulated (with RAMSEL = HIGH). Concurrent with the determination of the convolution sum and the data shifting in the RE data memory, the filter coefficients are modified by the function:

$$h'(n) = [1 - \sigma(n)]h(n)$$

Where the h' are the filter coefficients used for the next pass.

The update value σ is input on the W-Bus on every read cycle and the modified filter coefficients are stored in IM memory. The operation is shown in *Figure 18*.

Figure 18. Adaptive Filtering



Note: 1. W-Bus input = $\sigma(n)$
$h'(k) = h(k)[1 - \sigma(n)]$
$h''(k) = h'(k)[1 - \sigma'(n)]$

Interfacing to Memory

Using the TMC2310 with Lower Resolution Data

The TMC2310 allows data inputs of up to 16 bits for all operations without the risk of an internal overflow. When using data values that are smaller than 16 bits it is recommended that they be placed in the upper MSBs of the RE and IM data ports. For instance, when using 12-bit initial inputs for an FFT operation the real and imaginary data should be placed on both RE_{18-7} and IM_{18-7}, respectively. Using the upper MSBs of each 19-bit data port allows the device to operate in either the AUTO or MANUAL scale mode. Configuration Register 1, CR1[4:3], must be set to perform a right shift of 3 bits on the data input during the first pass. Results from the first pass have the potential of growing up to 19 bits, therefore, to maintain maximum precision the outputs should be contained in 19-bit wide memory.

Initial data inputs can be connected to the 12 LSBs, however, since the device uses a two's complement data format each input must be sign extended into RE_{18} and IM_{18}, the MSBs. For operations that require multiple passes (i.e., FFT/IFFT) intermediate results will carry less precision. This will result in a reduction in the overall accuracy of the transform operation.

Interfacing to 16-Bit Memory Systems

The TMC2310 outputs 19 bits of significant data to external memory in order to increase arithmetic precision and minimize roundoff error. To obtain the best results, the memory system should support all 19 data bits. In order to reduce the number of memory devices, the system can be configured with 16-bit wide data memories. While this configuration may reduce system size and cost, there will be a decrease in accuracy due to truncation of the output data. In a 16-bit memory system, data should be left-justified (connected to the 16 MSBs) with the 3 LSBs connected to pull-up (or pull-down) resistors. Configuration Register 1 is programmed to perform auto or manual data scaling with a right shift of 3 bits performed on the data during the first pass (CR[4:3] = 11). The 16 MSBs of the output are stored into memory, truncating the three LSBs.

In systems utilizing data windowing, the user may connect either the LSB or the MSB of the W-Bus to ground through a pull-down resistor of 5 kOhms. If both positive and negative window values are to be used, the MSB is required (two's complement format) and the LSB may be grounded. For positive magnitude window functions, the MSB will always be zero, and can therefore be connected to ground through a 5 kOhm resistor.

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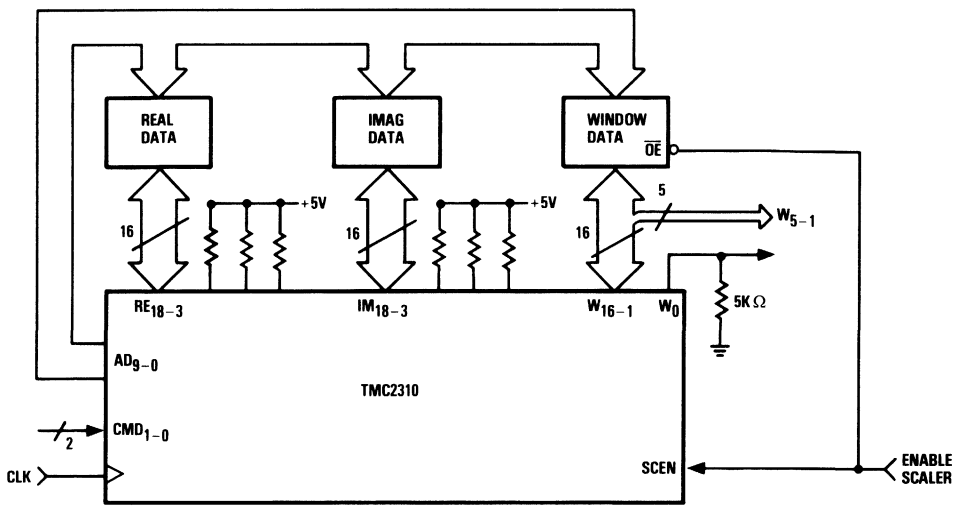
Figure 19. Interfacing to 16-Bit Memories



Pipelined vs. Non – Pipelined Addressing

Operation of the TMC2310 at its maximum clock rate requires the use of high – speed data memory. By including a special addressing mode, slower memory can be used by the addition of high – speed external address registers. The TMC2310 has been designed to allow the user to make system tradeoffs between memory cost and device count.

Normally, a memory address is output and the data strobed into or out of memory within a single clock cycle. Therefore, the following relationship must be met:

$$t_{CY} \quad [t_{DO}(\text{TMC2310 Addr. Out}) + t_{ACC}(\text{memory}) + t_S(\text{TMC2310 Data In})]$$

or equivalently, the memory access time must meet the requirement:

$$t_{ACC}(\text{memory}) \quad [t_{CY} - t_D(\text{TMC2310}) - t_S(\text{TMC2310})]$$

Use of the "Pipelined Addressing" mode alters the above relationship. In pipelined mode, the address and controls ($\overline{RD}$ and RAMSEL) appear one cycle earlier. For a read operation, the data will be input to the TMC2310 on the following cycle. For a write operation, the output data and the $\overline{WR}$ strobe will occur one cycle after the address and controls. For proper synchronization, the address, $\overline{RD}$ and RAMSEL outputs must be externally registered. The requirement for external memory speed becomes:

$$t_{ACC}(\text{memory}) \quad [t_{CY} - t_D(\text{external register}) - t_S(\text{TMC2310})]$$

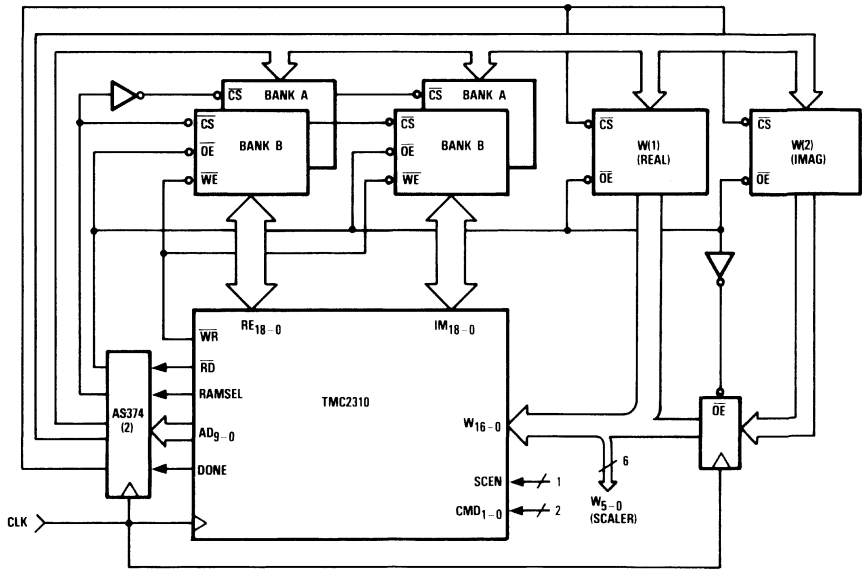
By substitution of the appropriate parameters into the above equation, it can be seen that the use of an external high – speed register ('AS374, F374, etc.) results in a substantial reduction of memory speed (access time) requirements.

Typical System Configuration

Figure 20 shows a typical system configuration utilizing many of the described techniques. The system includes "pipelined addressing", evident by the use of external registers on the TMC2310 memory address and controls. The system also includes a banked (Bank A and Bank B) memory system which may consists of single port or multi – port memory. (External host interface to memories is not shown.)

Finally, the diagram shows a system utilizing two window memories (for dual real and complex operations). If only one window memory is required (Real Windows) then the Imaginary memory, W(2), and associated output register and inverter may be deleted. For a single window memory, the chip select of W(1) can be connected to a LOW and the output enable connected to the DONE flag to disable the memory when the device is idle.

Figure 20. Typical System Configuration



Bit – Reverse Addressing for Input Data

The radix – 2, Decimation – In – Time (DIT) FFT/IFFT algorithm performed by the TMC2310 requires data scrambling during the first butterfly pass (Refs. [2],[3]). The scrambling amounts to a bitwise reversal of the address index during the first pass of the FFT. A flow diagram for a general, radix – 2, 16 – point FFT is shown in Figure 21. By a close examination of the figure, it can be seen that the first butterfly is performed on data points X(0) and X(8) with results stored in X(0) and X(1). It is apparent that results must be written to a secondary memory to prevent the loss of the unused data point X(1).

The TMC2310 allows several addressing options for transforms. While these modes have no effect on speed or processing time, they do affect system memory requirements. If the input data samples are stored in memory in sequential order, then the TMC2310 must perform the bit – reversed addressing (CR1[7:6] = 01) during the first butterfly pass. To accomodate the data scrambling and prevent overwriting of unused data, the user must provide additional "scratch pad" memory for intermediate storage during this pass. The RAMSEL output is used to toggle between the two banks during reads and writes of the first pass. RAMSEL must be connected either to the "chip enables" of separate memories or to an additional address line (for a paged memory system). At the completion of the transform, data will be in memory in sequential (frequency or time) order.

A transform can be done without the scratch pad memory by initially storing the data in scrambled order. This is accomplished by a simple reverse ordering of the address lines between the host system address generator (counters, etc.) and the data memory (Figure 22). The transform is then performed "in – place" (no bit – reverse, CR1[7:6] = 00). Since the input data has been "pre – scrambled", the TMC2310 will read and write data to memory addresses in a sequence that requires no additional memory. Final results will be available in sequential, frequency bin order. In either case, if windowing is performed, the user must store the window function either in sequential or scrambled order to match that of the input data.

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Figure 21. 16 – Point FFT

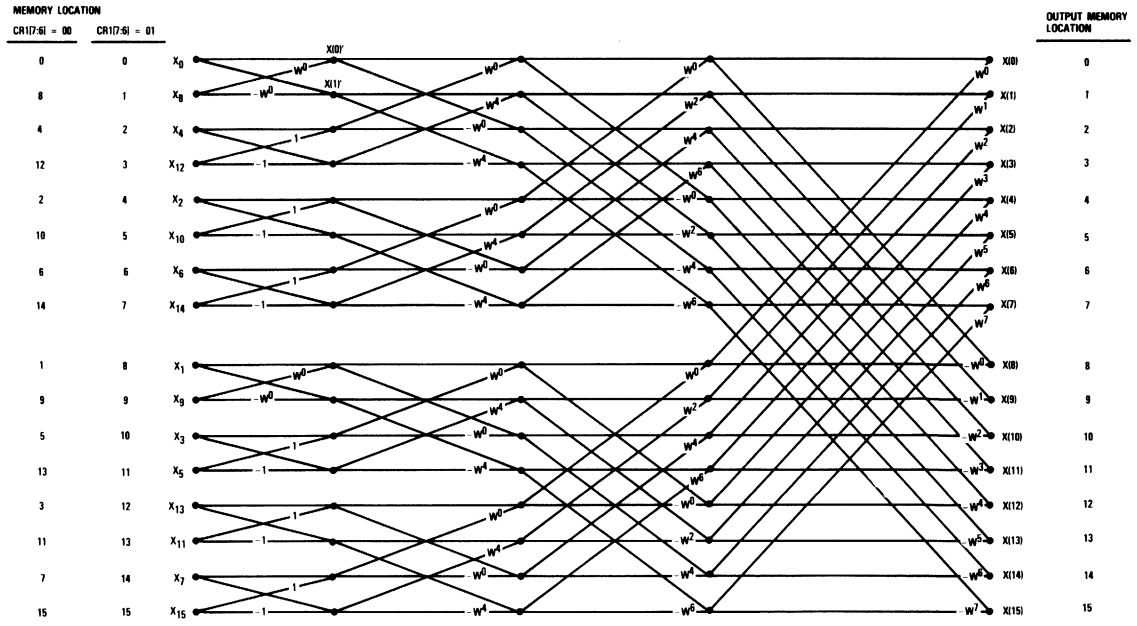
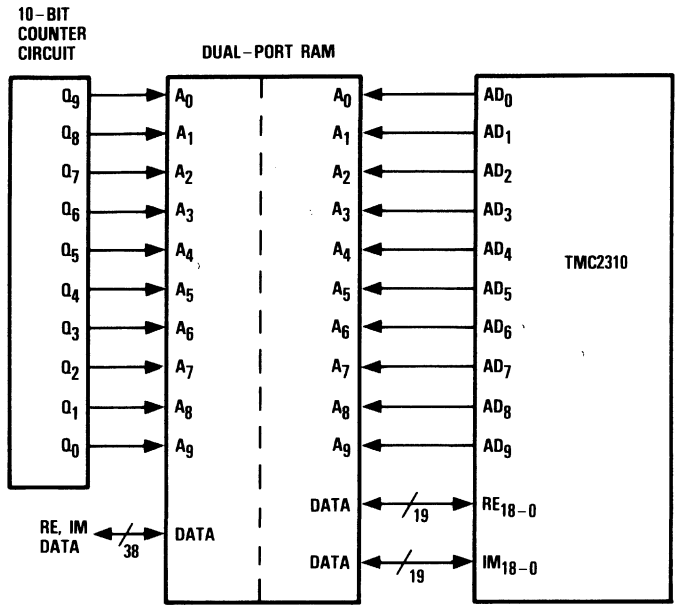


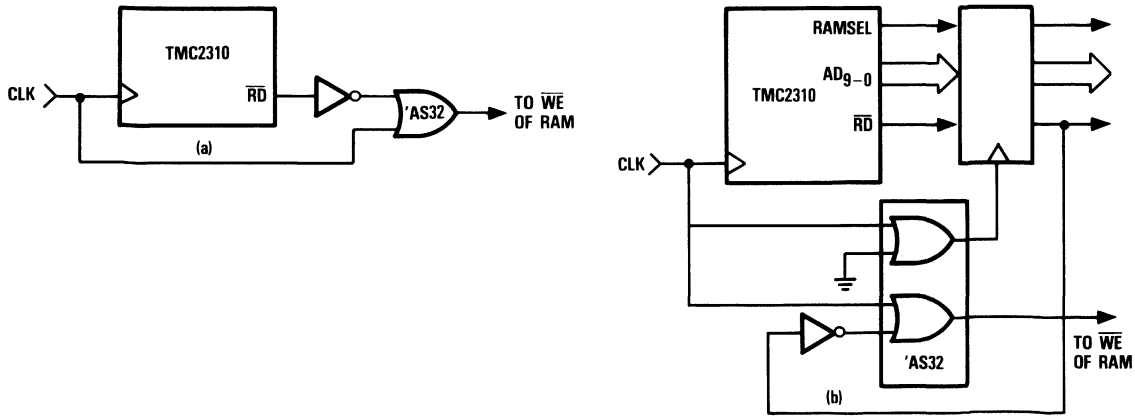
Figure 22. Bit-Reversed Input Data for 1024-Point Transform



Alternate Method For Write Strobe Generation

The high-speed operation of the TMC2310 requires the use of fast random addess memory. In some instances, the pulse-width and timing of the TMC2310's $\overline{WR}$ may not meet the system requirements. As an alternative, the user can use the $\overline{RD}$ output used to generate a write strobe for memory. Since $\overline{RD}$ is normally LOW and goes HIGH only during write cycles, the user can gate $\overline{RD}$ with the system clock to create an active LOW write (enable) strobe. Implementing the write strobe in this method may give better system timing and performance. The strobe will be the LOW portion of the system clock. *Figure 23, part (a)* shows external generation of a write strobe in non-pipelined addressing systems, and *part (b)* for pipelined systems utilizing the external address registers. The external register (74AS821) is clocked by a delayed system clock (through the AS32) to guarantee a valid memory address until WE goes HIGH.

Figure 23. Generating a Write Strobe



Scale Factor (W_{3-0})

In the inverse FFT, the final exponent read at this port will be the true binary exponent for the emerging real and imaginary data. In the forward FFT, this value will exceed the true exponent by N, where the total number of transform points is 2^N. The format for this exponent is 4-bit unsigned integer.

References

[1] Harris, F.J., "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform," Proceedings of the IEEE, Vol. 66, No. 1, January, 1978, pp 51-83.

[2] Oppenheim, A.V., Schafer, R.W., "Digital Signal Processing," Prentice-Hall, Inc., 1975.

[3] Rabiner, L.R., Gold, B., "Theory and Applications of Digital Signal Processing," Prentice-Hall, Inc., Copyright-Bell Laboratories.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2310G5V	EXT–T_C = –55°C to 125°C	MIL-STD-883, 15MHz	88 Pin Ceramic Pin Grid Array	2310G5V
TMC2310G5V1	EXT–T_C = –55°C to 125°C	MIL-STD-883, 20MHz	88 Pin Ceramic Pin Grid Array	2310G5V1
TMC2310H7C	STD–T_A = 0°C to 70°C	Commercial, 20MHz	89 Pin Plastic Pin Grid Array	2310H7C
TMC2310L4V	EXT–T_C = –55°C to 125°C	MIL-STD-883, 15MHz	100 Leaded Ceramic Chip Carrier	2310L4V
TMC2310L4V1	EXT–T_C = –55°C to 125°C	MIL-STD-883, 20MHz	100 Leaded Ceramic Chip Carrier	2310L4V1
TMC2310L6V	EXT–T_C = –55°C to 125°C	MIL-STD-883, 15MHz	132 Leaded CERQUAD	2310L6V
TMC2310L6V1	EXT–T_C = –55°C to 125°C	MIL-STD-883, 20MHz	132 Leaded CERQUAD	2310L6V1

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TMC2311

CMOS Fast Cosine Transform Processor
12 Bits, 15 Million Pixels Per Second

The TMC2311, a high-speed algorithm specific processor, computes the one or two dimensional forward discrete cosine transform (DCT) of an 8 or 8x8 point array of contiguous 9-bit data or the inverse DCT of 12-bit data. Output precision in all cases is 12 bits. It complies with the CCITT Specialists' Group on Visual Telephony (SG XV) accuracy specification for inverse DCT. With its internal coefficient ROM, data transpose RAM, address generators, and sequencer, the TMC2311 accepts high level instructions from a host processor and raw 8x8 blocked data from an external memory and returns transformed data to a second external memory. The TMC2311 also includes a defeatable adder-subtractor for linear predictive coding and differential pulse code modulation. The pipelined TMC2311 can transform continuous 8x8 pixel data blocks at a rate of one per 4.48μs.

Operating under a system clock of up to 30MHz, the TMC2311 accepts each incoming data block in row-major ("line-by-line") format at two clock cycles per pixel. Output data are written in column-major format, i.e., down the left-most column of the block, then down the next column to the right, etc., also at two clock cycles per pixel. In the inverse DCT mode, the chip accepts column-major data and return row-major data. Thus, a pair of TMC2311 chips can transform an image and return it to its original spatial domain, with or without any intervening operation, such as compression, transmission and re-expansion.

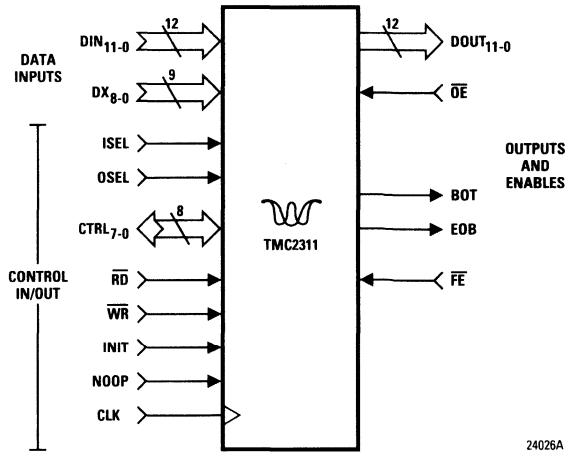
Built with TRW's one-micron double level metal OMICRON-C™ low-power CMOS process, the TMC2311 is available in a 68-lead plastic chip carrier.

Features

- Stand Alone Execution Of 8-Point Forward Or Inverse Cosine Tranform
- Continuous 8x8-Point 2-D DCTs Every 4.48μs Including Memory Transpose And Data Loading/Unloading
- On-Chip Cosine Coefficient ROM
- On-Chip Data Transpose Memory With Direct Transpose Mode
- Auxiliary Adder With Optional Clipped Outputs For Linear Predictive Coding And Differential Pulse Code Modulation
- Two's Complement 12-Bit Data I/O Format
- Two's Complement 9-Bit Add/Subtract Input
- Full CCITT SGXV Compatibility
- All Inputs And Outputs TTL Compatible
- 68 Pin Plastic Chip Carrier

F

Logic Symbol



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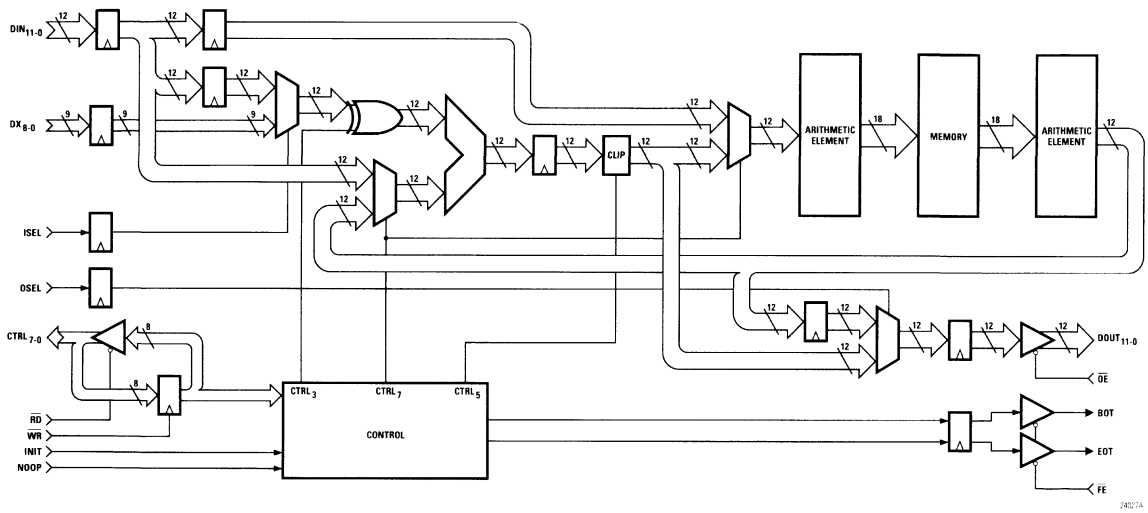
Applications

- Image Processing, Graphics
- Pulse And Image Compression
- Video Teleconferencing
- Linear Predictive Coding
- Differential Pulse Code Modulation
- Electronic Publishing
- Medical Imaging And Archiving

Associated Products

- TMC2312 — Quantizer/Huffman Encoder
- TMC2313 — Huffman Decoder/Dequantizer
- TMC2220 — 4x32 Correlator
- TMC2250 — 2-D 3x3 FIR Filter
- TMC2272 — Colorspace Converter

Figure 1. Functional Block Diagram



Functional Description

The TMC2311 comprises five internal blocks: a controller, two arithmetic elements, a data transpose memory and an auxiliary adder circuit (*Figure 1*). Each arithmetic element (AE) can compute an 8-point 1-dimensional DCT in 16 clock cycles. When the device is configured to perform 2-dimensional transforms, the first AE computes the DCT of each consecutive row of 8 pixels. The results of each 8x1 DCT are written into the intermediate memory. After eight 1-dimensional transforms are computed, the device computes the DCT of each consecutive 8-pixel column, while (if so instructed) computing the DCTs of the rows of the next block of data. The auxiliary adder/subtractor can be used with a forward and inverse transform in linear predictive coding applications. The adder can also be used alone to perform differential pulse code modulation without the cosine transform. In all modes and configurations the device operates on continuous data at a rate of up to 15 Megapels/second and can perform a complete 8x8 DCT every 128 clock cycles.

Control

The control block includes the chip's preprogrammed controller, sequencer, and microcode generator. The host system needs only to load a single 8-bit control word on C_{7-0} and then strobe the INIT pin. The chip will proceed automatically through the chosen operation without further supervision.

Arithmetic Element #1

Comprising a multiplier and two adder/subtractors, bypassable processor AE1 performs a series of one-dimensional 8-point forward or inverse DCTs on the incoming data, writing its 8-point transform results into the transpose memory.

Data Transpose Memory

This two-port 64-word RAM collects each group of eight consecutive 8-point transformed data sets from AE1 and then passes them to AE2 while collecting the next group, thereby acting as a large pipeline buffer. When enabled, the DTM accepts each 64-point data block in row-major sequence and returns the same data in column-major order, effecting a "corner turn." Bypassing this block leaves the data sequence unchanged.

Arithmetic Element #2

Identical to AE1, bypassable data processor AE2 performs eight 8- point one-dimensional transforms on each 64-point block of data. Each transform pulls one data point from each of the eight transforms done by AE1, completing the 8x8 two-dimensional transform. For one-dimensional transforms, either AE can be bypassed.

Auxiliary Adder

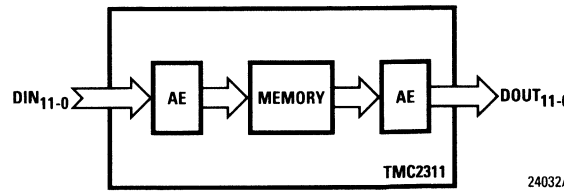
The remaining circuitry in *Figure 1* can be employed as either a presubtractor or a post-adder. (See *Applications Discussions* of *Linear Predictive Coding*, *Differential Pulse Code Modulation*, and *Interframe Coding*.) As instructed by $CTRL_3$ (INVERT), $CTRL_7$ (XSEL), ISEL, and OSEL, this adder combines the 9-bit two's complement data entering on port DX_{8-0} with either the incoming or emerging data stream.

Operating Modes

The TMC2311's five operating modes are selected by control pins $CTRL_{2-0}$. The device can be configured in the following ways:

The device will perform a two-dimensional transform if $CTRL_{2-0}$ = 000 or 001. AE1 performs a one-dimensional DCT (IDCT if $CTRL_3$ = 1) on each of eight 8-pixel rows of data supplied row-by-row to DIN_{11-0}. Results from each block of eight transforms are fed via the Transpose Memory to AE2, which performs a one-dimensional DCT (IDCT) on each of the eight 8-pixel columns of data, in turn (*Figure 2*).

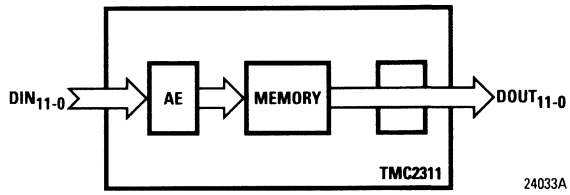
Figure 2. 2-D Transform (With Transpose)



The device can also perform one-dimensional DCTs (IDCTs) with or without memory transpose.

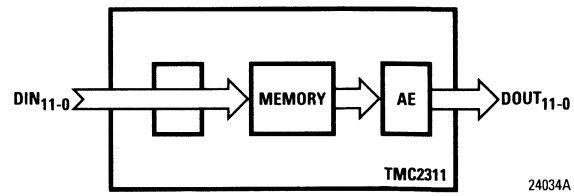
When $CTRL_{2-0}$ = 010, the chip will transform eight 8-point rows of incoming data, then transpose the results without transforming the columns (*Figure 3*).

Figure 3. 1-D Transform With 8x8 Transpose



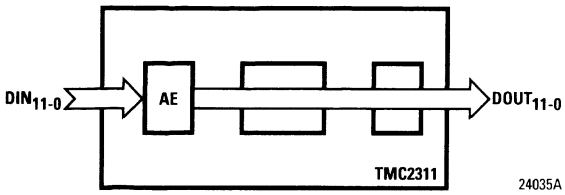
When $CTRL_{2-0}$ = 011, the device accepts eight 8-point rows of data and transposes them before AE2 performs one-dimensional DCTs (IDCTs) of the columns (*Figure 4*).

Figure 4. 8x8 Transpose With 1-D Transform



The device can also perform one-dimensional transforms without transposes. When $CTRL_{2-0}$ = 100 or 101, AE1 performs a one-dimensional DCT or IDCT on each incoming 8-point row of data (*Figure 5*).

Figure 5. 1-D Transform (Without Transpose)



Finally, the device will perform the memory transpose with no DCT when $CTRL_{2-0}$ = 110 or 111 (*Figure 6*).

Figure 6. Memory Transpose (Without Transform)

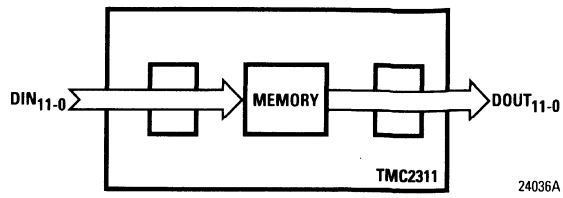


Table 1 summarizes the operation of controls $CTRL_7$, $CTRL_3$, ISEL, and OSEL, which "fine tune" the mode selection by programming the presubtractor/postadder and the transform direction. (Where a full two- dimensional FCT or IFCT is needed, $CTRL_{2-0}$ must be set to 011. $CTRL_7$=1 then enables presubtraction and OSEL=1 enables postaddition, as desired by the user.)

Table 1. Operating Mode Configurations

Application	Function	Device Configuration			
		$CTRL_7$	$CTRL_3$	ISEL	OSEL
2D DCT	2D FCT	0	0	X	0
2D IDCT	2D IFCT	0	1	X	0
Interframe Compress	2D FCT, Presubtract	1	0	0	0
Interframe Decompress	2D IFCT, Post Add	0	1	0	1
LPC	2D FCT, Presubtract	1	0	0	0
ILPC	2D IFCT, Post Add	0	1	0	1
LPC Directly Out	DOUT=DIN-DX	1	0	0	1
ILPC Directly Out	DOUT=DIN+DX	1	1	0	1
DPCM Directly Out	DOUT(k)=DIN(k)-DIN(k-1)	1	0	1	1
IDPCM Directly Out	DOUT(k)=DIN(k)+DIN(k-1)	1	1	1	1
DPCM w/ Transpose	DOUT(k)=DIN(k)-DIN(k-1)	1	0	1	0
IDPCM w/ Transpose	DOUT(k)=DIN(k)+DIN(k-1)	1	1	1	0

Notes: LPC/ILPC Linear Predictive Coding (Forward/Inverse)
DPCM/IDPCM Differential Pulse Code Modulation (Forward/Inverse)

Signal Definitions

Control

INIT — Single pass "start" command. INIT=0 resets the internal logic and output flags and updates the $CTRL_{7-0}$ parameters. INIT is registered and must be LOW for at least 3 clock cycles. INIT returning HIGH starts the transform. The first data point is loaded two cycles later.

NOOP — Input clock disable. NOOP=1 freezes operation of the device on the next CLK rising edge. Operation commences from where it stopped one cycle after NOOP returns LOW.

$\overline{WR}$ — Control word preload command. $\overline{WR}$=0 loads CTRL7-0 parameters into the device's preload register. The next INIT rising edge transfers the preloaded parameters into the chip's working registers.

$\overline{RD}$ — Control word (READ) command. $\overline{RD}$=0 allows the preloaded parameters $CTRL_{7-0}$ to be read.

$CTRL_{2-0}$ — MODE Control. Defines the internal configuration (mode) of the device, selecting either 2-dimensional or 1-dimensional transforms and/or the access to the internal Transpose Memory (***Figures 2*** through ***6***.)

$CTRL_{2-0}$	Operation
000	2–D Transform
001	2–D Transform
010	1–D Transform, Transpose
011	Transpose, 1–D Transform
100	1–D Transform
101	1–D Transform
110	Transpose
111	Transpose

$CTRL_3$ — Inverse Transform Enable (INV). INV=0 selects a forward DCT. If INV=1, the device will compute the Inverse DCT. INV also inverts the data to one side of the auxiliary adder. When and only when INV=0, data from the multiplexer which selects the DX port or delayed DIN port will be inverted.

$CTRL_4$ — Automatic Reinitialization (AUTOINIT). AI=0 allows continuous operation of device. When AI=1, the device will halt at the end of the specified transform.

$CTRL_5$ — Arithmetic Limit (CLIP). CLIP=1 saturates data outputs to 9 bits. CLIP is useful when presubtraction or postaddition is used with the DCT or IDCT.

$CTRL_6$ — Flag Control (FC). FC determines when the output flags, BOT and EOB, appear. When FC=0, both flags are output with the corresponding data result. When FC=1, the flags appear two clock cycles earlier.

$CTRL_7$ — Auxiliary Adder Select (XSEL). XSEL controls two multiplexers within the auxiliary adder circuitry. The first mux feeds the non-inverted input to the adder either the DIN port (XSEL=1) or outputs from the core of the device (XSEL=0). The second mux selects the data entering the core of the device from either the input port (XSEL=0) or adder output (XSEL=1). See ***Applications, Operating Mode Configurations***.

ISEL — Input Data Select. ISEL=0 connects the inverted (optional) input of the auxiliary adder to the DX port. When ISEL=1, the DIN port is connected, via a one data cycle delay. Output from this mux to the adder is inverted when INV=0. See ***Applications, Operating Mode Configurations***.

OSEL — Output Data Select. When OSEL=0, data results from the device core pass to the final output register. When OSEL=1, results from the adder pass to the final output register. See ***Applications, Operating Mode Configurations***.

$\overline{OE}$ — Asynchronous active LOW OUTPUT ENABLE for data output port, $DOUT_{11-0}$. When $\overline{OE}$=1, every output is forced into a high-impedance state.

$\overline{FE}$ — Active LOW asynchronous output FLAG ENABLE. When $\overline{FE}$=1, BOT and EOB are forced into a high-impedance state.

Data Inputs

DIN_{11-0} Data INput Port (12-bit two's complement format). DIN is the input port for both FORWARD and INVERSE transforms. DIN11 is the MSB. For two dimensional forward transforms, data precision is limited to 9 bits, DIN_{8-0}, and must be sign-extended into the remaining MSBs. Data exceeding the lower 9-bit range may cause an internal overflow. For INVERSE transforms, the entire 12-bit input port may used without risk of overflow.

DX_{8-0} Auxiliary Data Input Port (9-bit two's complement format). Feeds one side of auxiliary adder. DX_8 is the MSB. Auxiliary inputs can be provided to the device for linear predictive coding (LPC) where pixel differences are transformed. In the FORWARD direction, inputs supplied to the DX port (and selected via ISEL) will be subtracted from pixel values input simultaneously on the DIN port. In the INVERSE direction, DX inputs will be added to outputs following the desired tranform operation. The DX inputs must be delayed so that they appear at the adder simultaneously with the corresponding pixel outputs.

Data Outputs

$DOUT_{11-0}$ Data OUTput Port (12-bit, two's complement format). DOUT is the output port for both FORWARD and INVERSE transforms. $DOUT_{11}$ is the MSB. When CLIP=1, all data outputs are clipped to 9 bits, $DOUT_{8-0}$, with sign extension into the remaining MSBs. DOUT is forced into a high-impedance state when $\overline{OE}$=1.

Output Flags

BOT Beginning Of Transform. Toggles LOW to denote the first result of each one-dimensional 8-point transform or the first result of each 8-point row or column of a two-dimensional transform. When FC=0, BOT will appear simultaneously with the corresponding result. When FC=1, BOT will appear one data I/O cycle earlier.

EOB End Of Block. Toggles LOW to signal the last result of the entire (8 or 64 point) transform field. When FC=0, EOB appears simultaneously with the last data result. When FC=1, EOB appears two cycles earlier.

Clock

CLK Data Path Clock. The device operates with a clock of 0 to 30MHz. All internal operations are referenced to the rising edges of CLK; I/O operations except $CTRL_{7-0}$ read and write, to alternate rising edges of CLK.

Power

V_{DD}, GND The TMC2311 operates from a single +5 Volt supply. All V_{DD} and GND pins must be connected.

Table 2. Data Formats and Bit Weighting

	11	10	9	8	7	6	5	4	3	2	1	0
Input Data Format – Forward Transforms												
DIN	S	S	S	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Input Data Format – Inverse Transforms												
DX:	-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
				-2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Output Data Format – Forward Transforms												
DOUT:	-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Output Data Format – Inverse Transforms												
	S	S	S	-2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Notes: S = Sign Extension.
In forward transforms, system should feed two's complement sign bit to DIN_{11-8} for 9-bit data size.
In inverse transforms, chip will output two's complement sign bit into pins $DOUT_{11-8}$.

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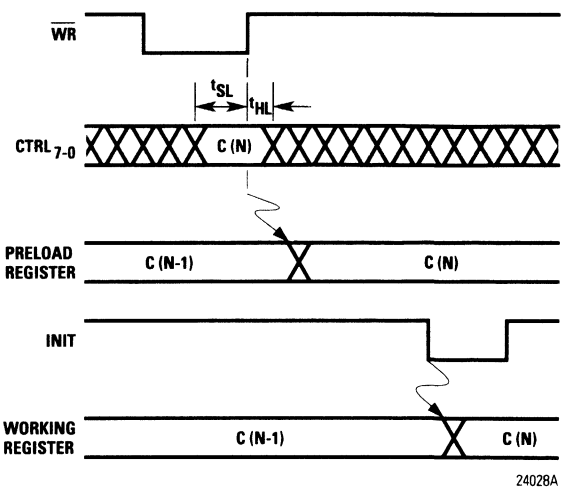
Operation and Timing

Initialization

Control Word Preload Timing

The self-sequencing TMC2311 requires no cycle-to-cycle supervision by the host system. On the rising edge of $\overline{WR}$, the user loads an 8-bit control word ($CTRL_{7-0}$) which sets 5 device parameters: mode and direction of the transform, continuous (or non-continuous) device operation, format of output data and timing of the output flags. The control parameters preloaded via $CTRL_{7-0}$ are registered internally and updated by the INIT signal. Control load timing is displayed in *Figure 7*.

Figure 7. Control Preload Timing



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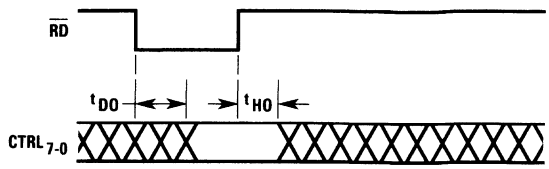
Control Word Read Timing

The TMC2311 also permits the user to read the preloaded control word value back through $CTRL_{7-0}$, a bidirectional port. When $\overline{RD}$=0, the $CTRL_{7-0}$ port outputs the control information stored in the device (*Figure 8*).

Figure 8. Control Read Timing



Data Input Timing

After the TMC2311 is initialized, data are input to DIN_{11-0} and DX_{8-0} on alternate rising edges of the device system clock. When the device is set for forward DCTs with transpose, data inputs are accepted in row-major format, i.e., line-by-line through the 8x8 transform window. When the device performs inverse DCTs, inputs are accepted in column-major format. Following the rising edge of INIT command, data inputs can be continuously loaded into the device on alternate rising edges of the system clock (*Figure 9*).

Data Output Timing

Results are output at half the system clock rate. The initial result latency and the number of results depends on the device operation specified by $CTRL_{2-0}$. Once the first result reaches the output port, remaining results will appear continuously. When the TMC2311 is set to perform forward DCTs with transpose, output data are written in column-major format. In the inverse direction, data results are returned row-by-row (*Figure 10*).

Figure 9. Data Input Timing

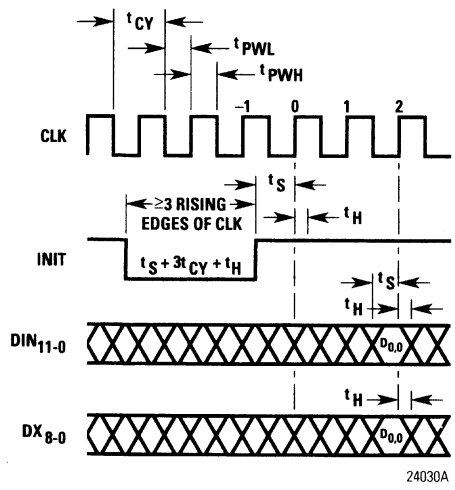
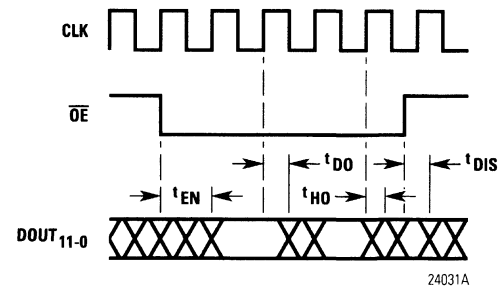


Figure 10. Data Output Timing



Overall Timing

The TMC2311 will expect data in groups of 8 or 64 points at regular intervals based on the mode of operation defined by $CTRL_{2-0}$. Results will be returned by the TMC2311 in similar groups following a predetermined initial latency. For applications that use the auxiliary adder ahead of the core of the device, corresponding DX and DIN inputs should be presented simultaneously to the device. Applications that use the adder after the DCT/memory core must account for the device's internal latency (*Table 3*). Each DX port input must be timed to appear at the adder one data cycle ahead of its corresponding output.

Table 3. Data Output Latency

$CTRL_{2-0}$	Operation	Latency*
000	2-D Transform	232 clocks
001	2-D Transform	232
010	1-D Transform, Transpose	200
011	Transpose, 1-D Transform	200
100	1-D Transform	56
101	1-D Transform	56
110	Transpose	168
111	Transpose	168

*cycles after INIT goes high

If AUTOINIT ($CTRL_4$)=0, the device will operate continuously with no interruption between transforms. Otherwise the device will halt after the specified number of data points have been processed. When AUTOINIT=1, device operation will resume with the next INIT signal.

The TMC2311 also provides two output flags to differentiate between the rows/columns of the transform window and between individual transform blocks. The Beginning Of Transform (BOT) flag goes LOW with the first data result of each 8x1 transform row or column. A second flag, End Of Block, EOB, delineates transform blocks. EOB will go LOW when the last data point of each 8x1 (one dimensional mode) or 8x8 (two dimensional mode) transform is output. The user can program these flags to appear with their respective data (FC=0) or one data cycle earlier (FC=1). *Figure 11* shows the overall timing of a forward 2-D DCT with pre-subtraction and FC=0. *Figure 12* shows the overall timing of an inverse 2-D DCT with post addition and FC=1, demonstrating the timing for inputs to auxiliary port DX_{8-0} and the shift in flag timing.

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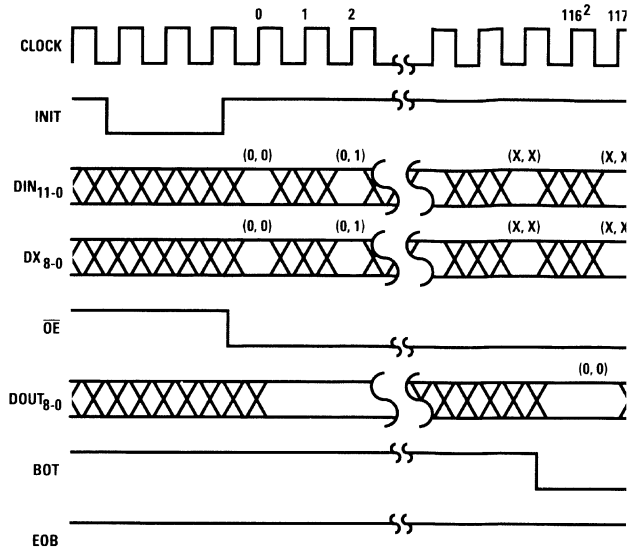
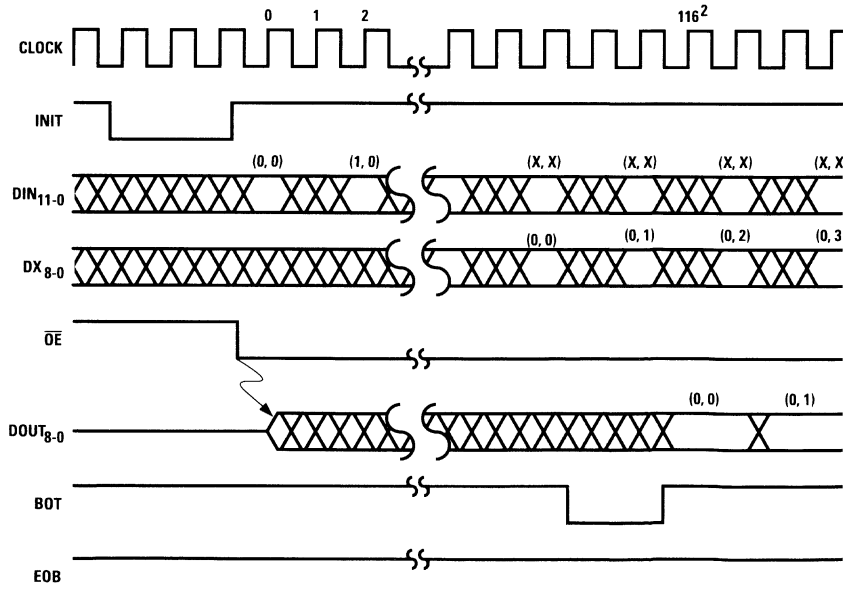
Figure 11. Overall Timing - Forward Transform (Flag Control=0)

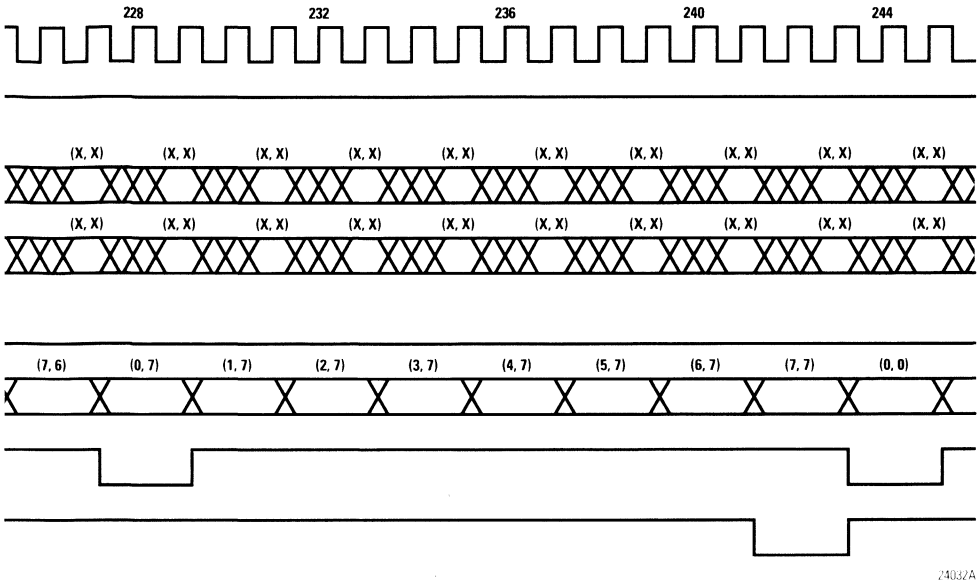


Notes: 1. DIN_{11-0} (i,j) aligned with DX_{8-0} (i,j), but alignment with $DOUT_{11-0}$ is mode-dependent.
2. $DOUT_{11-0}$ (0,0) is valid on CLK rising edge 116 in two-dimensional transfer modes only.

Figure 12. Overall Timing - Inverse Transform (Flag Control=1)



Notes: 1. DX_{8-0} (i,j) precedes $DOUT_{11-0}$ (i,j) by two CLK cycles, but alignment with DIN_{11-0} is mode-dependent.
2. $DOUT_{11-0}$ (0,0) is valid on CLK rising edge 116 in two-dimensional transform modes only.



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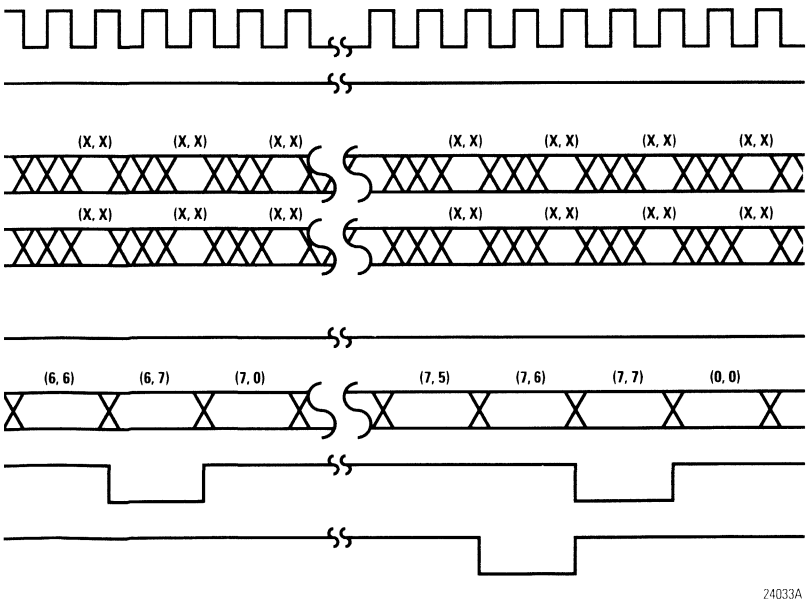

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Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage[2] ..... −0.5 to (V_{DD} + 0.5)V

Output

Applied Voltage[2] ..... −0.5 to (V_{DD} + 0.5V)

Forced Current,[3,4] ..... −3.0 to +6.0mA

Short Circuit Duration

(single output in HIGH state to ground) ..... 1 second

Temperature

Operating, Case ..... −60 to +130°C

Junction ..... +175°C

Lead, Soldering (10 seconds) ..... +300°C

Storage. ..... −65 to +150°C

Notes: 1. Absolute maximum ratings are limiting values applied individually while all other parameter are within specified operating conditions. Functional operation under any of these conditions is NOT implied.

2. Applied voltage must be current limited to specified range, and measured with respect to GND.

3. Forcing voltage must be limited to specified range.

4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{DD}	Supply Voltage	4.75	5.0	5.25	V
t_{CY}	Cycle Time				
	TMC2311	37			ns
	TMC2311-1	34.5			ns
	TMC2311-2	28			ns
t_{PWL}	Clock Pulse Width, LOW	8			ns
t_{PWH}	Clock Pulse Width, HIGH	8			ns
t_S	Input Setup Time	11			ns
t_H	Input Hold Time	0			ns
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
I_{OL}	Output Current, Logic LOW			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70	°C
T_C	Case Temperature				°C

Electrical characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{DDQ}	Supply Current, Quiescent[2]	V_{DD}=Max, V_{IN}=0V, TS=5V		30	mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, f=30MHz, TS=5V		130	mA
I_{IL}	Input Current, Logic LOW	V_{DD}=Max, V_{IN}=0V		–10	µA
I_{IH}	Input Current, Logic HIGH	V_{DD}=Max, V_{IN}=V_{DD}		+10	µA
V_{OL}	Output Voltage, Logic LOW	V_{DD}=Min, I_{OL}=Max		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD}=Min, I_{OH}=Max	2.4		V
I_{OZL}	Hi-Z Output Leakage Current,	V_{DD}=Max, V_{IN}=0V Output LOW		–40	mA
I_{OZH}	Hi-Z Output Leakage Current,	V_{DD}=Max, V_{IN}=0V Output HIGH		+40	mA
I_{OS}	Short Circuit Output Current	V_{DD}=Max, Output HIGH one pin to ground one second duration max.		–45	mA
C_I	Input Capacitance	T_A=25°C, f=1MHz		10	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		10	pF

Note: 1. Actual test conditions may vary from those shown above, but guarantee operation as specified.
2. Following power-on, the TMC2311 must be clocked for at least 10 clock cycles before the clock is disabled.

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Switching characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
t_{DO}	Output Delay	V_{DD}=Min, C_{Load}=40pF		16	ns
	TMC2311			16	
	TMC2311-1			16	
	TMC2311-2			12	
t_{HO}	Output Hold Time	V_{DD}=Max, C_{Load}=40pF	4		ns
t_{ENA}	Three-State Output Enable Delay	V_{DD}=Min, C_{Load}=40pF		16	ns
	TMC2311			16	
	TMC2311-1			16	
	TMC2311-2			12	
t_{DIS}	Three-State Output Disable Delay	V_{DD}=Min, C_{Load}=40pF		22	ns

Note: 1. All transitions except for t_{DIS} and t_{ENA} are measured at a 1.5V level.

Figure 13. Equivalent Input Circuit

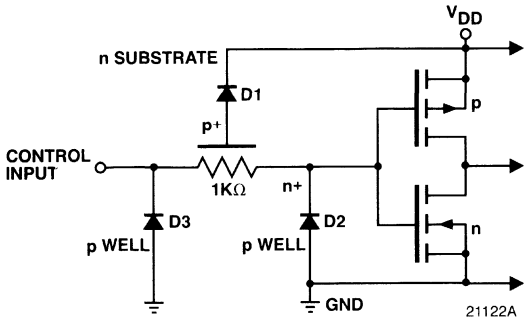
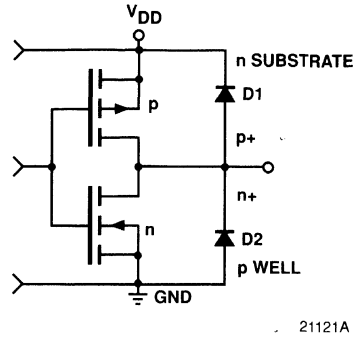


Figure 14. Equivalent Output Circuit



Applications Discussions

Frequency Domain Coding - Basic System

Frequency domain coding entails partitioning an image into (for example) 8x8 pixel blocks, then determining the two-dimensional spatial frequency spectrum of each block. In image compression, each component is then quantized by a frequency-specific factor, which tends to be smaller (more precise) for the dominant lower- frequency components and larger (coarser) for the less crucial higher-frequency components. Quantization effects compression by reducing the number of bits per frequency bin and by zeroing out high-frequency, low-energy bins. Following the quantizer, the scaled frequency data are then (arithmetic or Huffman) coded into a format that will allow them to be transmitted (or archived) even more economically. In particular, the JPEG modified Huffman coding represents each string of "zeroed out" bins with a compact code.

The transmitted images are reconstructed by reversing these operations. Coded information is received and restored to frequency information through a decoder. The received (or retrieved) data then pass through an inverse quantizer that restores the most important frequency components, albeit at somewhat grainier than original levels. Finally, the image is reconstructed by the inverse DCT. In practice, compression ratios of up to 20:1 can provide visually acceptable results with still images.

The basic compression circuit (*Figure 15*) shows a sample implementation of an intraframe compressor. The system contains an encoder comprising the TMC2311 DCT chip, a quantizer and a coder. Images are reconstructed in a complementary system with a decoder, a dequantizer, and a TMC2311 (inverse) DCT chip.

Figure 15. Basic System

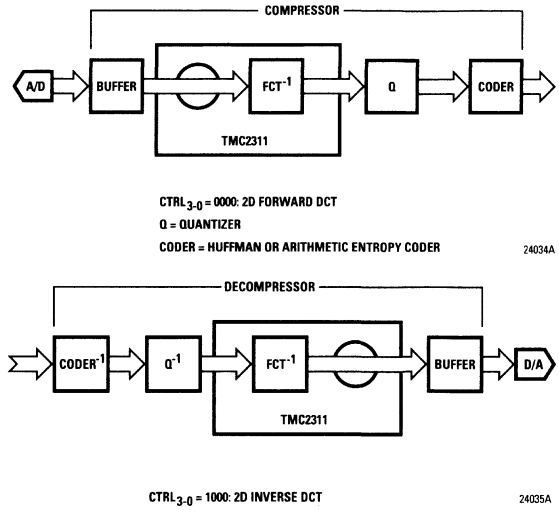
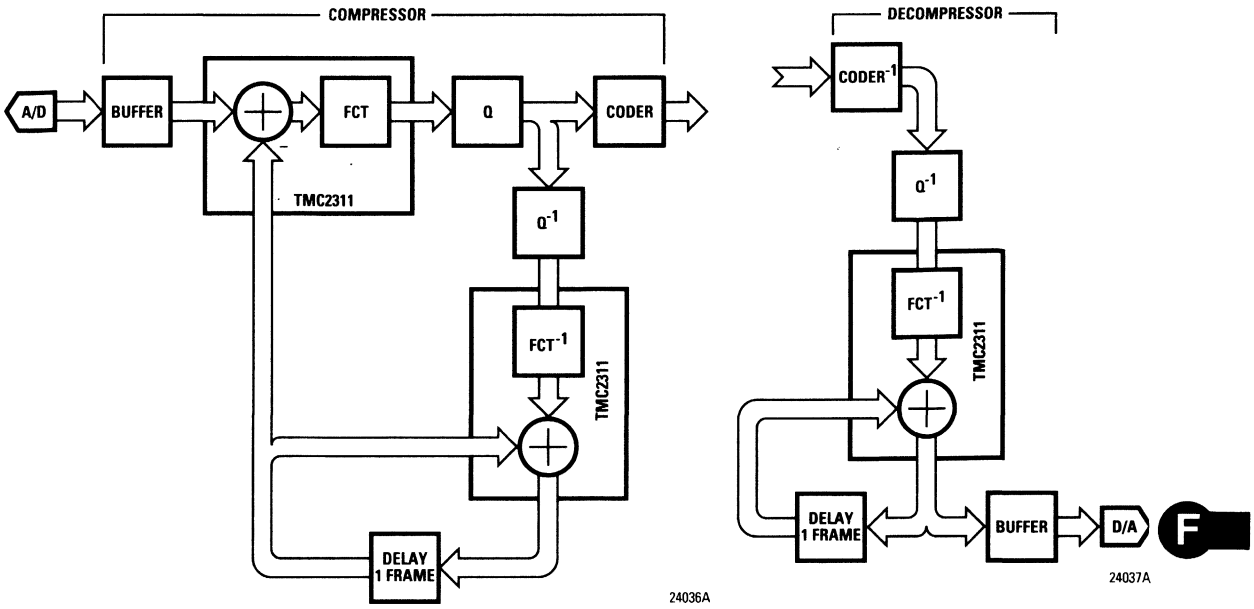


Figure 16. Interframe Compression System



Interframe Compression

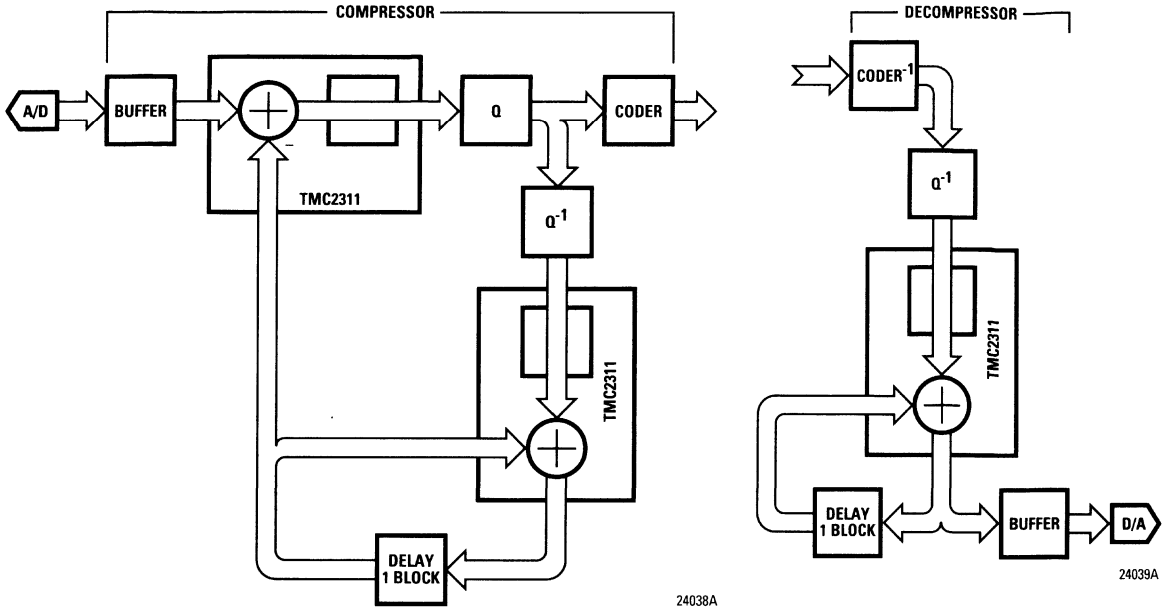
Figure 16 shows a moving picture extension of frequency domain coding, which processes differences between the corresponding pixels of successive image frames. Interframe compression describes areas of change within a moving image by comparing each new frame against earlier frames. Prior to the DCT, a block from the new frame is subtracted from the corresponding block of the previous frame. The resulting differences are transformed, quantized, coded, and transmitted. The compressed data are then reconstructed by reversing the processing steps: decode, dequantize, inverse DCT, then accumulate differences from frame to frame. Transforming only these differences increases the achievable compression.

Linear Predictive Coding System

Many critical biomedical and defense applications require that images be compressed and then restored "losslessly," i.e., without degradation. One technique, referred to as Linear Predictive Coding (LPC), has been very effective in speech compression. For image compression, LPC entails coding the differences between the current and previous pixel blocks of the same frame. This technique of intraframe compression can be used with or without the DCT. Much of the *Figure 16* interframe compression architecture can also be applied here, although the delay block now corresponds to delay within a single frame.

To obtain lossless compression, the user may code the differences between pixel blocks directly, without the DCT. This variety of intraframe compression, demonstrated in *Figure 17*, uses just the auxiliary adder of the TMC2311. In the forward direction, the differences are computed and transferred to the quantizer and coder circuitry where they are readied for transmission. In the inverse direction, the reconstruction process involves inverse coding and quantization, followed by cumulative addition of the image differences by the TMC2311's auxiliary adder.

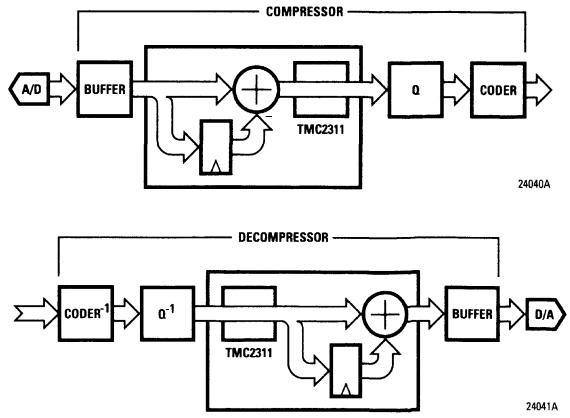
Figure 17. Linear Predictive Coding System (No Cosine Transform)



Differential Pulse Code Modulation

Another linear prediction algorithm, differential pulse code modulation, (DPCM) uses the differences between individual pixels on each line of the image. These differences are quantized, coded and transmitted (or archived). This technique is also used where lossless compression is required. The system shown in *Figure 18* illustrates the use of the auxiliary adder circuit of the TMC2311. The device incorporates a special input delay path that allows a previous pixel value to be added or subtracted from the current input pixel value. The results are then either fed into the device core to perform a transpose function or output directly from the adder. In the forward direction the pixel differences are fed to the quantizer and coder blocks of the system and transmitted. In the inverse direction the coded information is reconstructed by inverse coding followed by inverse quantization and finally the accumulation of pixel differences in the TMC2311.

Figure 18. Differential Pulse Code Modulation System (No Cosine Transform)



Package Interconnections

Signal Type	Signal Name	Function	Value	R1 Package Pin
Power	V_{DD}	Supply Voltage	+5.0V	2 10 17 33 53 68
	GND	Ground	0.0V	1 4 9 13 18 26 35 52 67
Clock	CLK	System Clock	TTL	65
Inputs	DIN_{11-0}	Data Inputs	TTL	44 45 46 47 48 49 50 51 54 55 56 57
	DX_{8-0}	Aux Adder In	TTL	34 36 37 38 39 40 41 42 43
Outputs	$DOUT_{11-0}$	Data Outputs	TTL	5 6 7 8 11 12 14 15 16 19 20 21
	BOT	Begin Transform	TTL	22
	EOB	End Of Block	TTL	23
Control	INIT	Initialize	TTL	60
	NOOP	No Operation	TTL	61
	$\overline{WR}$	Control Preload	TTL	66
	$\overline{RD}$	Read Control	TTL	64
	ISEL	Input Data Select	TTL	59
	OSEL	Output Select	TTL	58
	$\overline{OE}$	Output Enable	TTL	3
	$\overline{FE}$	Flag Enable	TTL	62
	$CTRL_{7-0}$	Control Params	TTL	32 31 30 29 28 27 25 24
	DNR	Test Pin	—	63
Do Not Connect				

Ordering Information

Product Number	Data Rate MHz	Temperature Range	Screening	Package	Package Marking
TMC2311R1C	13.5	STD-T_A = 0°C to 70°C	Commercial	68 Pin PLCC	2311R1C
TMC2311R1C1	14.5	STD-T_A = 0°C to 70°C	Commercial	68 Pin PLCC	2311R1C1
TMC2311R1C2	17.8	STD-T_A = 0°C to 70°C	Commercial	68 Pin PLCC	2311R1C2

TMC2330

CMOS Coordinate Transformer
16 x 16 Bit, 25MOPS

The TMC2330 VLSI circuit converts bidirectionally between Cartesian (real and imaginary) and Polar (magnitude and phase) coordinates at up to 25MOPS (Million Operations Per Second).

In its Rectangular-To-Polar mode, the TMC2330 can extract phase and magnitude information or backward "map" from a rectangular raster display to a radial (e.g., range-and-azimuth) data set.

The Polar-To-Rectangular mode executes direct digital waveform synthesis and modulation. With its 32-bit phase accumulator, the chip can generate and frequency or phase-modulate quadrature sinusoidal waveforms with a frequency resolution of 0.006Hz at a 25MHz clock rate. The TMC2330 greatly simplifies real-time image-space conversions between the radially-generated image scan data found in radar, sonar, and medical imaging systems, and raster-oriented display formats.

All input and output data ports are registered, and a new transformed data word pair is available at the output every 40ns. The user-configurable phase accumulator structure, input clock enables, and asynchronous three-state output bus enables simplify interfacing. All signals are TTL compatible.

Fabricated in TRW's OMICRON-C™ one-micron CMOS process, the TMC2330 operates at up to the 25MHz maximum clock rate over the full commercial (0 to 70°C) temperature and supply voltage ranges, and is available in a low-cost 120 pin plastic pin grid array package. The MIL-STD-883C version, the TMC2330L5V, is housed in a ceramic chip carrier and is specified over the full extended (−55 to 125°C) case temperature range.

Features

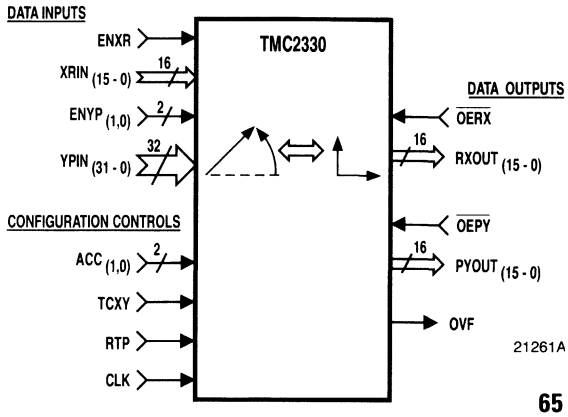
- Rectangular-To-Polar Or Polar-To-Rectangular Conversion At Guaranteed 25MOPS Pipelined Throughput Rate
- Polar Data: 16-Bit Magnitude, 32-Bit Input/16-Bit Output Phase
- 16-Bit User-Selectable Two's Complement Or Sign-And-Magnitude Rectangular Data Formats
- Input Register Clock Enables And Asynchronous Output Enables Simplify Interfacing
- User-Configurable Phase Accumulator For Waveform Synthesis And Amplitude, Frequency, Or Phase Modulation
- Magnitude Output Data Overflow Flag (In Polar-To-Rectangular Mode)
- Low Power Consumption CMOS Process
- Single +5V Power Supply
- Available In A 120 Pin Plastic Pin Grid Array Package
- Available In A 132 Leaded CERQUAD

F

Applications

- Scan Conversion (Phased Array To Raster)
- Vector Magnitude Estimation
- Range And Bearing Derivation
- Spectral Analysis
- Digital Waveform Synthesis, Including Quadrature Functions
- Digital Modulation And Demodulation

TMC2330 Logic Symbol



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40G06721 Rev. B−11/90
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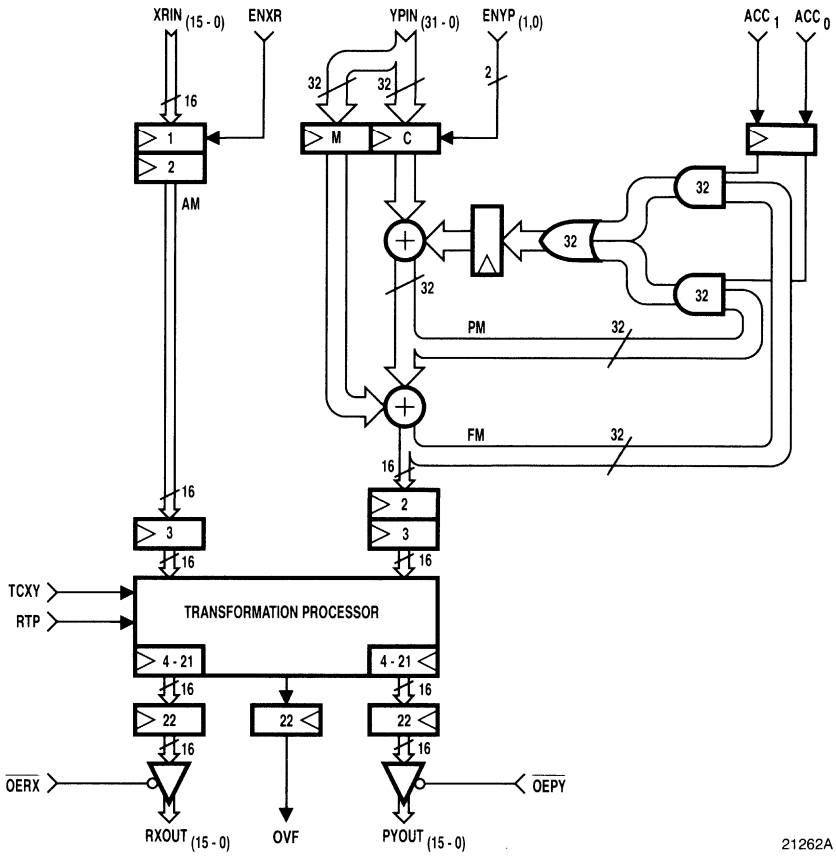
Functional Block Diagram



Functional Description

General Information

The TMC2330 converts between Rectangular (Cartesian) and Polar (Phase and Magnitude) coordinate data word pairs. The user selects the numeric format and transformation to be performed (Rectangular-To-Polar or Polar-To-Rectangular), and the operation is performed on the data presented to the inputs on the next clock. The transformed result is then available at the outputs 22 clock cycles later, with new output data available every 40ns. All input and output data ports are registered, with input clock enables and asynchronous high-impedance output enables to simplify connections to system buses.

When executing a Rectangular-To-Polar conversion, the input ports accept 16-bit Rectangular coordinate words, and the output ports generate 16-bit magnitude and 16-bit phase data. The user selects either two's complement or sign-and-magnitude Cartesian data format. Polar magnitude data are always in magnitude format only. Since the phase angle word is modulo 2π, it may be regarded as either unsigned or two's complement format (*Tables 1 and 2*).

In Polar-To-Rectangular mode, the input ports accept 16-bit Polar magnitude and 32-bit phase data, and the output ports produce 16-bit Rectangular data words. Again, the user selects between two's complement or sign-and-magnitude Cartesian data format. The dual 32-bit phase accumulator input registers are useful in signal synthesis applications, storing high-accuracy (0.006Hz at the maximum clock rate) phase increment values with minimal accumulation error. This allows the TMC2330 to generate precision quadrature waveforms unattended, once the accumulator has been enabled. The flexible input phase accumulator structure supports

General Information (cont.)

frequency or phase modulation, as determined by the input register clock enable $ENYP_{1,0}$ and accumulator control word $ACC_{1,0}$. The 16 MSBs (Most Significant Bits) of phase data are used in the transformation itself.

Signal Definitions

Power

V_{DD}, GND — The TMC2330 operates from a single +5V supply. All power and ground pins must be connected.

Clock

CLK — The TMC2330 operates from a single clock. All enabled registers are strobed on the rising edge of CLK, which is the reference for all timing specifications.

Inputs/Outputs

$XRIN_{15\text{-}0}$ — $XRIN_{15\text{-}0}$ is the registered Cartesian X-coordinate or Polar Magnitude (Radius) 16-bit input data port. $XRIN_{15}$ is the MSB.

$YPIN_{31\text{-}0}$ — $YPIN_{31\text{-}0}$ is the registered Cartesian Y-coordinate or Polar Phase angle 32-bit input data port. The input phase accumulators are fed through this port in conjunction with the input enable select $ENYP_{1,0}$. When RTP is HIGH (Rectangular-To-Polar), the input accumulators are normally not used. The 16 MSBs of YPIN are the input port, and the lower 16 bits become "don't cares" if ACC=00. $YPIN_{31}$ is the MSB.

$RXOUT_{15\text{-}0}$ — $RXOUT_{15\text{-}0}$ is the registered Polar Magnitude (Radius) or X-coordinate 16-bit output data port. This output is forced into the high-impedance state when $\overline{OERX}$=HIGH. $RXOUT_{15}$ is the MSB.

$PYOUT_{15\text{-}0}$ — $PYOUT_{15\text{-}0}$ is the registered Polar Phase angle or Cartesian Y-coordinate 16-bit output data port. This output is forced to the high-impedance state when $\overline{OEPY}$=HIGH. $PYOUT_{15}$ is the MSB.

Controls

ENXR — The value presented to the input port XRIN is latched into the input registers on the current clock when ENXR is HIGH. When ENXR is LOW, the value stored in the register remains unchanged.

$ENYP_{1,0}$ — The value presented to the YPIN input port is latched into the phase accumulator input registers on the current clock, as determined by the control inputs $ENYP_{1,0}$, as shown below:

$ENYP_{1,0}$	Instruction
00	No registers enabled, current data held
01	M register input enabled, C data held
10	C register input enabled, M data held
11	M register set to 0, C register input enabled

where C is the Carrier register and M is the Modulation register, and 0=LOW, 1=HIGH. See the *Functional Block Diagram*.

RTP — This registered input selects the current transformation mode of the device. When RTP is HIGH, the TMC2330 executes a Rectangular-To-Polar conversion. When RTP is LOW, a Polar-To-Rectangular conversion will be performed. The input and output ports are then configured to handle data in the appropriate coordinate system. This is a static input. See the *Timing Diagram*.

$ACC_{1,0}$ — In applications utilizing the TMC2330 to perform waveform synthesis and modulation in the Polar-To-Rectangular mode (RTP=LOW), the user determines the internal phase Accumulator structure implemented on the next clock by setting the accumulator control word $ACC_{1,0}$, as shown below:

$ACC_{1,0}$	Configuration
00	No accumulation performed
01	PM accumulator path enabled
10	FM accumulator path enabled
11	(Nonsensical) logical OR of PM and FM

where 0=LOW, 1=HIGH. See the *Functional Block Diagram*.

The accumulator will roll over correctly when full-scale is exceeded, allowing the user to perform continuous phase accumulation through 2π radians, or 360 degrees.

Controls (cont.)

$ACC_{1,0}$ (cont.) Note that the accumulators will also function when RTP = HIGH (Rectangular-To-Polar), which is useful when performing backward mapping from Cartesian to polar coordinates. However, most applications will require that $ACC_{1,0}$ be set to 00 to avoid accumulating the Cartesian Y input data.

TCXY The format select control sets the numeric format of the Rectangular data, whether input (RTP = HIGH) or output (RTP = LOW). This control indicates two's complement format when TCXY = HIGH, and sign-and-magnitude when LOW. This is a static input. See the *Timing Diagram*.

OVF When RTP = LOW (Polar-To-Rectangular), the Overflow Flag will go HIGH on the clock that the magnitude of either of the current Cartesian coordinate outputs exceeds the maximum range. It will return LOW on the clock that the Cartesian out-put value(s) return to full-scale or less. See the *Applications Discussion* section. Overflow is not possible in Rectangular-To-Polar mode (RTP = HIGH).

$\overline{OERX}$, $\overline{OEPY}$ Data in the output registers are available at the outputs of the device when the respective asynchronous Output Enables are LOW. When $\overline{OERX}$ or $\overline{OEPY}$ is HIGH, the respective output port(s) is in the high-impedance state.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins	L5 Package Pins
Power	V_{DD}	Supply Voltage	C3, E3, H3, L4, L6, L8, L11, F11, E11, C11, C8, C6	1, 9, 21, 37, 45, 53, 67, 87, 91, 99, 112, 120
	GND	Ground	D3, E2, F2, G3, K3, L3, L7, K11, J11, G11, E12, D11, C10, C9, C7, C5, C4	5, 11, 14, 17, 29, 33, 49, 75, 83, 89, 95, 104, 108, 116, 124, 129
Clock	CLK	System Clock	F3	13
Inputs	$XRIN_{15-0}$	X or Radius Data	F12, F13, G13, G12, H13, H12, H11, J13, J12, K13, K12, L13, L12, M13, M12, N13	86, 85, 84, 82, 81, 80, 79, 78, 77, 76, 74, 73, 71, 69, 68, 66
	$YPIN_{31-0}$	Y or Phase Data	L10, N12, N11, M10, L9, N10, M9, N9, M8, N8, N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, N2, M2, N1, L2, M1, L1, K2, J3, K1, J2, J1	61, 60, 59, 58, 57, 56, 55, 54, 52, 51, 50, 48, 47, 46, 44, 43, 42, 41, 40, 39, 38, 36, 34, 31, 30, 28, 27, 26, 25, 24, 23, 22
Outputs	$RXOUT_{15-0}$	Radius or X Data	D13, D12, C13, B13, C12, A13, B12, A12, B11, A11, B10, A10, B9, A9, B8, A8	90, 92, 93, 94, 96, 97, 100, 102, 105, 106, 107, 109, 110, 111, 113, 114
	$PYOUT_{15-0}$	Phase or Y Data	A7, A6, B6, A5, B5, A4, B4, A3, A2, B3, A1, B2, B1, C2, C1, D2	117, 118, 119, 121, 122, 123, 125, 126, 127, 130, 132, 3, 4, 6, 7, 8
Controls	ENXR	X or Radius In Enable	M11	63
	$ENYP_{1,0}$	Y or Phase In Enable	G1, G2	18, 16
	RTP	Conversion Select	E1	12
	$ACC_{1,0}$	Accumulate Control	H2, H1	20, 19
	TCXY	Cartesian Data Format	F1	15
	$\overline{OERX}$	Radius or X Out Enable	E13	88
	$\overline{OEPY}$	Phase or Y Out Enable	D1	10
Flags	OVF	Overflow Flag	B7	115
No Connect	NC	No Connect Pins	–	2, 32, 35, 62, 64, 65, 72, 98, 101, 103, 128, 131
		Index Pin	D4	–

Static Control Inputs

The controls RTP and TCXY determine the transformation mode and the assumed numeric format of the Rectangular data. The user must exercise caution when changing either of these controls, as the new transformed results will not be seen the at the outputs until the entire internal pipe (22 clocks) has been flushed. Thus, these controls are considered static.

Table 1. Data Input/Output Formats – Integer Format

Port	RTP	TCXY	Bit # 31	30	29	. . .	16	15	14	. . .	0	Format	
XRIN	0	X						2^{15}	2^{14}	. . .	2^{0}.		U
XRIN	1	0						NS	2^{14}	. . .	2^{0}.		S
XRIN	1	1						-2^{15}	2^{14}	. . .	2^{0}.		T
YPIN	0	X	$\pm 2^{0}$.	2^{-1}	2^{-2}	. . .	2^{-15}	2^{-16}	2^{-17}	. . .	2^{-31}	$(x\pi)$T/U	
YPIN	1	0	NS	2^{14}	2^{13}		2^{0}.						S
YPIN	1	1	-2^{15}	2^{14}	2^{13}	. . .	2^{0}.						T
RXOUT	0	0						NS	2^{14}	. . .	2^{0}.		S
RXOUT	0	1						-2^{15}	2^{14}	. . .	2^{0}.		T
RXOUT	1	X						2^{15}	2^{14}	. . .	2^{0}.		U
PYOUT	0	0						NS	2^{14}	. . .	2^{0}.		S
PYOUT	0	1						-2^{15}	2^{14}	. . .	2^{0}.		T
PYOUT	1	X						$\pm 2^{0}$.	2^{-1}	. . .	2^{-15}	$(x\pi)$T/U	

Table 2. Data Input/Output Formats – Fractional Format

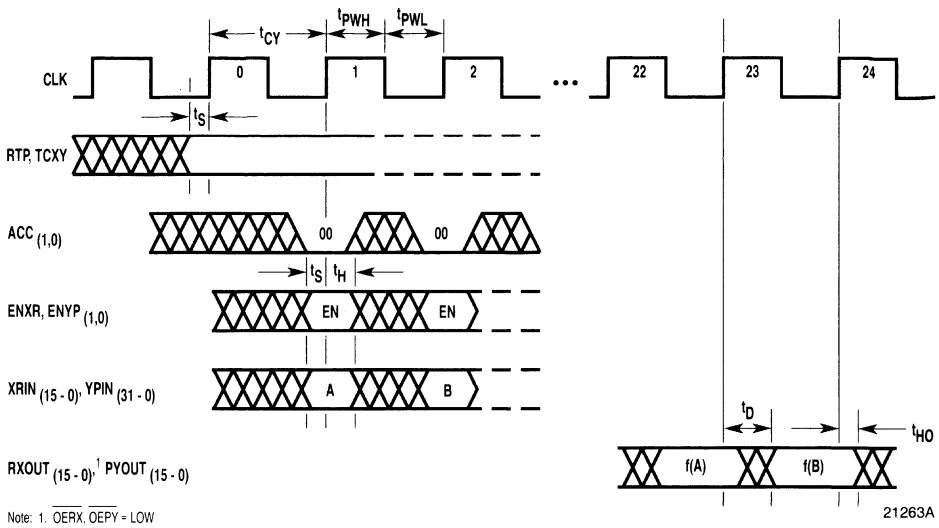
Port	RTP	TCXY	Bit # 31	30	29	. . .	16	15	14	. . .	0	Format	
XRIN	0	X						2^{0}.	2^{-1}	. . .	2^{-15}		U
XRIN	1	0						NS.	2^{-1}	. . .	2^{-15}		S
XRIN	1	1						-2^{0}.	2^{-1}	. . .	2^{-15}		T
YPIN	0	X	$\pm 2^{0}$.	2^{-1}	2^{-2}	. . .	2^{-15}	2^{-16}	2^{-17}	. . .	2^{-31}	$(x\pi)$T/U	
YPIN	1	0	NS.	2^{-1}	2^{-2}	. . .	2^{-15}						S
YPIN	1	1	-2^{0}	2^{-1}	2^{-2}	. . .	2^{-15}						T
RXOUT	0	0						NS.	2^{-1}	. . .	2^{-15}		S
RXOUT	0	1						-2^{0}.	2^{-1}	. . .	2^{-15}		T
RXOUT	1	X						2^{0}	2^{-1}	. . .	2^{-15}		U
PYOUT	0	0						NS.	2^{-1}	. . .	2^{-15}		S
PYOUT	0	1						-2^{0}.	2^{-1}	. . .	2^{-15}		T
PYOUT	1	X						$\pm 2^{0}$.	2^{-1}	. . .	2^{-15}	$(x\pi)$T/U	

Notes:

1. -2^{15} denotes two's complement sign bit.
2. NS denotes negative sign, i.e., '1' negates the number.
3. $\pm 2^{0}$ denotes two's complement sign or highest magnitude bit – since phase angles are modulo 2π and phase accumulator is modulo 2^{32}, this bit may be regarded as $+\pi$ or $-\pi$.
4. All phase angles are in terms of π radians, hence notation "$x\pi$".
5. If A_{CC} = 00, YPIN (15-0) are "don't cares."
6. Formats:
   T = Two's Complement
   S = Signed Magnitude
   U = Unsigned

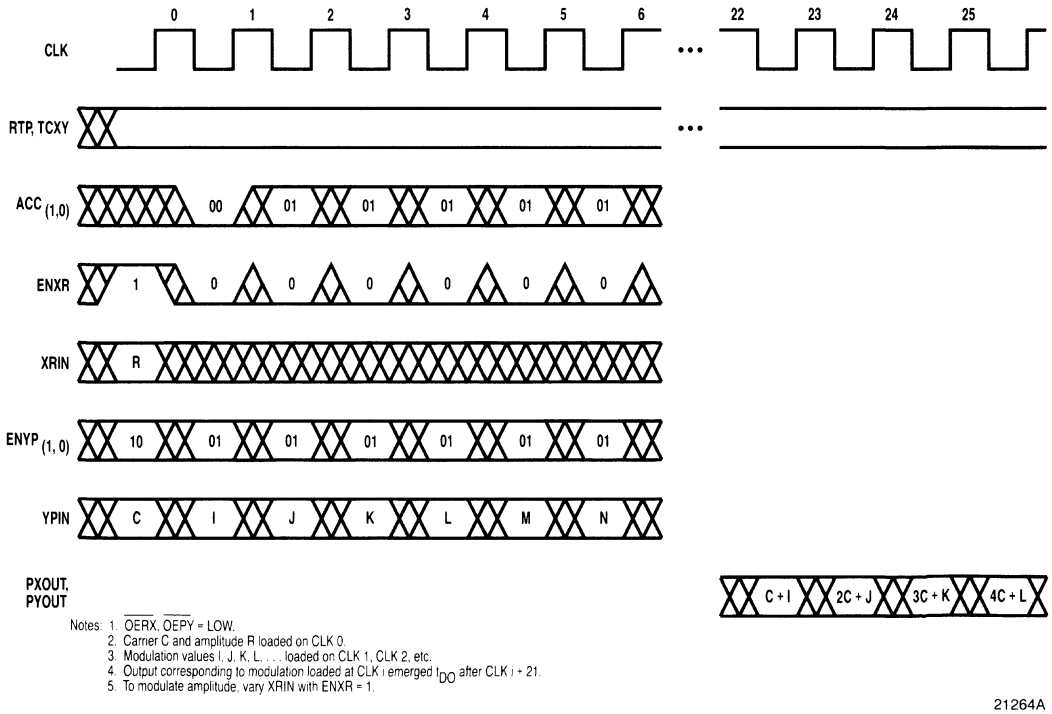
HEX	U	T	S
FFFF	65535	−1	−32767
– –	– –	– –	– –
8001	32769	−32767	−1
8000	32768	−32768	0
7FFF	32767	32767	32767
– –	– –	– –	– –
0001	1	1	1
0000	0	0	0

Figure 1. Timing Diagram – No Accumulation



Note: 1. $\overline{OERX}$, $\overline{OEPY}$ = LOW

Figure 2. Timing Diagram – Phase Modulation



Notes: 1. $\overline{OERX}$, $\overline{OEPY}$ = LOW.
2. Carrier C and amplitude R loaded on CLK 0.
3. Modulation values I, J, K, L, . . . loaded on CLK 1, CLK 2, etc.
4. Output corresponding to modulation loaded at CLK i emerged t_{DO} after CLK i + 21.
5. To modulate amplitude, vary XRIN with ENXR = 1.

Figure 3. Equivalent Input Circuit

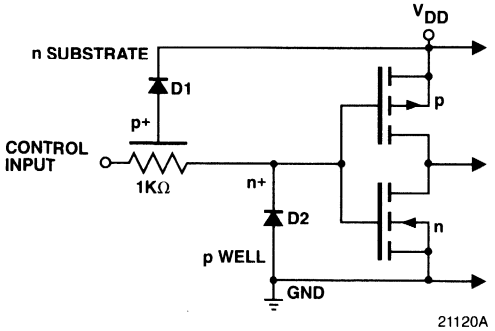


Figure 4. Equivalent Output Circuit

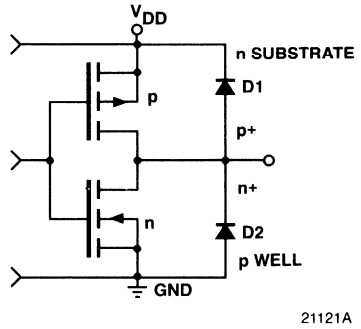
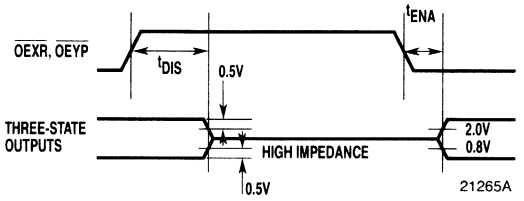


Figure 5. Transition Levels for Three-State Measurements



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Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output Voltage	
Applied voltage	−0.5 to (V_{DD} + 0.5)V [2]
Forced current	−6.0 to 6.0mA [3,4]
Short-circuit duration (single output in HIGH state to ground)	1 Second
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
V_{DD}	Supply Voltage		4.75	5.25	4.5	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8		0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0		2.0		V
I_{OL}	Output Current, Logic LOW			8.0		8.0	mA
I_{OH}	Output Current, Logic HIGH			−4.0		−4.0	mA
t_{CY}	Cycle Time	V_{DD} = Min	50		55		ns
		TMC2330-1	40		45		ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD} = Min	10		11		ns
		TMC2330-1	8		8		ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD} = Min	8		8		ns
		TMC2330-1	6		6		ns
t_S	Input Setup Time		12		13		ns
		TMC2330-1	10		11		ns
t_H	Input Hold Time		1		2		ns
		TMC2330-1	1		2		ns
T_A	Ambient Temperature, Still Air		0	70			°C
T_C	Case Temperature				−55	125	°C

Electrical characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		10		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz $\overline{OERX}$ and $\overline{OEPY}$ = V_{DD}		160		160	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		−10		−10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		−40		−40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.	−20	−100	−20	−100	μA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but specified operation is guaranteed.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		22		25	ns
		TMC2330-1		20		23	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF		4		4	ns
		TMC2330-1		4		4	ns
t_{ENA}	Output Enable Delay	V_{DD} = Min, C_{LOAD} = 40pF		13		17	ns
		TMC2330-1		12		15	ns
t_{DIS}	Output Disable Delay	V_{DD} = Min, C_{LOAD} = 40pF		14		14	ns
		TMC2330-1		13		13	ns

Applications Discussion

Numeric Overflow

Because the TMC2330 accommodates 16-bit unsigned radii and 16-bit signed Cartesian coordinates, Polar-To-Rectangular conversions can overflow for incoming radii greater than 32767 = 7FFFh and will overflow for all incoming radii greater than 46341 = B505h. (In signed magnitude mode, a radius of 46340 = B504h will also overflow at all angles.) The regions of overflow and of correct conversion are illustrated in *Figure 6*.

In signed magnitude mode, overflows are circularly symmetrical – if a given radius overflows at an angle P, it will also overflow at the angles $\pi - P$, $\pi + P$, and $-P$. This is because $-X$ will overflow if and only if X overflows, and $-Y$ will overflow if and only if Y overflows.

In two's complement mode, the number system's asymmetry complicates the overflow conditions slightly. An input vector with an X component of $-32768 = 8000h$ will not overflow, whereas one with an X component of $+32768$ will. *Table 3* summarizes several simple cases of overflow and near-overflow.

Numeric Underflow

In RTP = 1 (Rectangular-To-Polar mode), if XRIN = YPIN = 0, the angle is undefined. Under these conditions, the TMC2330 will output the expected radius of 0 (RXOUT = 0000) and an angle of 1.744 radians (PYOUT = 4707). This angle is an artifact of the CORDIC algorithm and is not flagged as an error, since the angle of any 0 length vector is arbitrary.

Table 3a. X-Dimensional Marginal Overflows

TC YPIN	OV RXOUT	CORRECT X
0 0000 = 0	1 0000 = +0	+32768
0 8000 = π	1 8000 = −0	−32768
1 0000 = 0	1 8000 = −32768	+32768
1 8000 = π	0 8000 = −32768	−32768

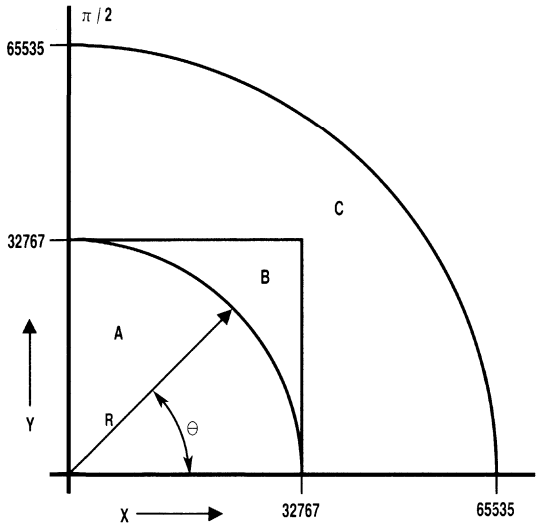
In all cases, RTP = 0 (Polar-To-Rectangular mode) and XRIN = 8000 (incoming radius = 32768).

Table 3b. Maximal Overflow (Radius In = 65535)

TC YPIN	OV RXOUT	CORRECT X
0 0000 = 0	1 7FFF = +32767	+65535
0 8000 = π	1 FFFF = −32767	−65535
1 0000 = 0	1 FFFF = −1	+65535
1 8000 = π	1 0001 = +1	−65535

In all cases, RTP = 0 (Polar-To-Rectangular mode) and XRIN = 7FFF (incoming radius = 65535, which will always overflow).

Figure 6. First Quadrant Coordinate Relationships



$X = R(\cos\Theta)$
$Y = R(\sin\Theta)$

and

$R = \sqrt{X^2 + Y^2}$
$\Theta = \tan^{-1}(Y/X)$

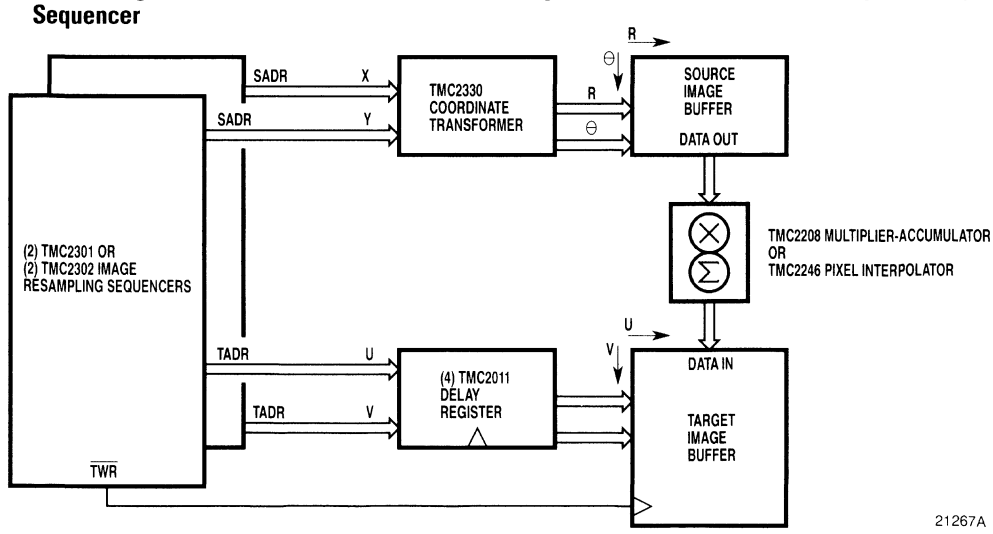
If R < 32768, overflow will not occur (region A).
If R > 32767, overflow will occur (region C) if |X| > 32767 or |Y| > 32767.
If R > 32767, overflow will not occur (region B) if |X| < 32768 and |Y| < 32768.

21266A

Performing Scan Conversion with the TMC2330

Medical Imaging Systems such as Ultrasound, MRI, and PET, and phased array Radar and Sonar systems generate radial-format coordinates (range or distance, and bearing) which must be converted into raster-scan format for further processing and display. Utilizing the TRW TMC2301 Image Resampling Sequencer, a minimum chipcount Scan Converter can be implemented which utilizes the trigonometric translation performed by the TMC2330 to backwards-map from a Cartesian coordinate set into the Polar source image buffer address space.

Figure 7. Block Diagram of Scan Converter Circuit Utilizing TMC2330 and TMC2301 Image Resampling Sequencer



21267A

As shown in *Figure 7*, the TMC2330 transforms the Cartesian source image addresses from the TMC2301 directly to vector distance and angle coordinates, while the TMC2301 writes the resulting resampled pixel values into the target memory in raster fashion. Note that the ability to perform this spatial transformation in either direction gives the user the freedom to process images in either coordinate space, with little restriction. Image manipulation such as zooms or tilts can easily be included in the transformation by programming the desired image manipulation into the TMC2301's transformation parameter registers.

Statistical Evaluation of Double Conversion

In this empirical test, 10,000 random Cartesian vectors were converted to and from polar format by the TMC2330. The resulting Cartesian pairs were then compared against the original ones. The unrestricted data base represents uniform sampling over a square bounded by $-32769 < x < 32768$ and $-32769 < y < 32768$.

The results of the 10,000-vector study were as follows:

Mean Error (X)	= +0.0052 LSB
Mean Error (Y)	= +0.0031 LSB
Mean Absolute Error (X)	= 0.662 LSB
Mean Absolute Error (Y)	= 0.664 LSB
Root Mean Square Error (X)	= 1.025 LSB
Root Mean Square Error (Y)	= 1.020 LSB
Max Error (X)	= +4/−5 LSB
Max Error (Y)	= +5/−4 LSB

Since this is a double conversion (rectangular to polar and back) which includes a wide variety of "good case" and "bad case" vectors, the chip should perform even better in many actual systems. Repeating the experiment and restricting the original data set to an annulus defined by $8196 < R < 32768$ reduced the mean square error to 0.89 LSB and the peak error to ±4 LSB (x or y). These latter results are more germane to synthesizer, demodulator, and other applications in which the amplitude can be restricted to lie between quarter and full scale.

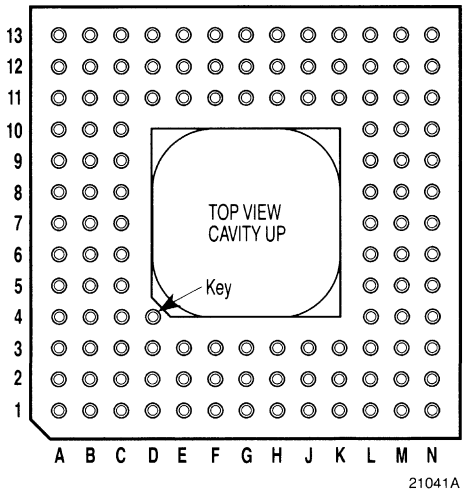
F

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2330H5C1	STD−T_A=0°C to 70°C	Commercial	120 Pin Plastic Pin Grid Array	2330H5C1
TMC2330H5C	STD−T_A=0°C to 70°C	Commercial	120 Pin Plastic Pin Grid Array	2330H5C
TMC2330L5V1	EXT−T_C=−55°C to 125°C	MIL-STD-883B	132 Leaded CERQUAD	2330L5V1
TMC2330L5V	EXT−T_C=−55°C to 125°C	MIL-STD-883B	132 Leaded CERQUAD	2330L5V

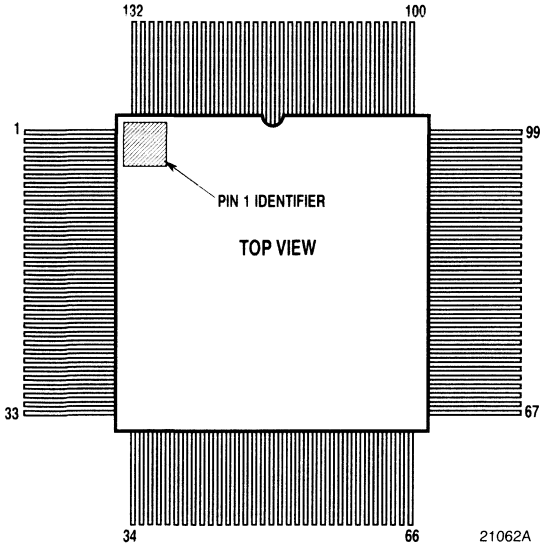
Pin Assignments – 120 Pin Plastic Pin Grid Array, H5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	$PYOUT_5$	B3	$PYOUT_6$	C5	GND	E1	RTP	G11	GND	K1	$YPIN_2$	L10	$YPIN_{31}$	M12	$XRIN_1$
A2	$PYOUT_7$	B4	$PYOUT_9$	C6	V_{DD}	E2	GND	G12	$XRIN_{12}$	K2	$YPIN_4$	L11	V_{DD}	M13	$XRIN_2$
A3	$PYOUT_8$	B5	$PYOUT_{11}$	C7	GND	E3	V_{DD}	G13	$XRIN_{13}$	K3	GND	L12	$XRIN_3$	N1	$YPIN_8$
A4	$PYOUT_{10}$	B6	$PYOUT_{13}$	C8	V_{DD}	E11	V_{DD}	H1	ACC_0	K11	GND	L13	$XRIN_4$	N2	$YPIN_{10}$
A5	$PYOUT_{12}$	B7	OVF	C9	GND	E12	GND	H2	ACC_1	K12	$XRIN_5$	M1	$YPIN_6$	N3	$YPIN_{12}$
A6	$PYOUT_{14}$	B8	$RXOUT_1$	C10	GND	E13	$\overline{OERX}$	H3	V_{DD}	K13	$XRIN_6$	M2	$YPIN_9$	N4	$YPIN_{15}$
A7	$PYOUT_{15}$	B9	$RXOUT_3$	C11	V_{DD}	F1	TCXY	H11	$XRIN_9$	L1	$YPIN_5$	M3	$YPIN_{11}$	N5	$YPIN_{17}$
A8	$RXOUT_0$	B10	$RXOUT_5$	C12	$RXOUT_{11}$	F2	GND	H12	$XRIN_{10}$	L2	$YPIN_7$	M4	$YPIN_{13}$	N6	$YPIN_{19}$
A9	$RXOUT_2$	B11	$RXOUT_7$	C13	$RXOUT_{13}$	F3	CLK	H13	$XRIN_{11}$	L3	GND	M5	$YPIN_{16}$	N7	$YPIN_{21}$
A10	$RXOUT_4$	B12	$RXOUT_9$	D1	$\overline{OEPY}$	F11	V_{DD}	J1	$YPIN_0$	L4	V_{DD}	M6	$YPIN_{18}$	N8	$YPIN_{22}$
A11	$RXOUT_6$	B13	$RXOUT_{12}$	D2	$PYOUT_0$	F12	$XRIN_{15}$	J2	$YPIN_1$	L5	$YPIN_{14}$	M7	$YPIN_{20}$	N9	$YPIN_{24}$
A12	$RXOUT_8$	C1	$PYOUT_1$	D3	GND	F13	$XRIN_{14}$	J3	$YPIN_3$	L6	V_{DD}	M8	$YPIN_{23}$	N10	$YPIN_{26}$
A13	$RXOUT_{10}$	C2	$PYOUT_2$	D11	GND	G1	$ENYP_1$	J11	GND	L7	GND	M9	$YPIN_{25}$	N11	$YPIN_{29}$
B1	$PYOUT_3$	C3	V_{DD}	D12	$RXOUT_{14}$	G2	$ENYP_0$	J12	$XRIN_7$	L8	V_{DD}	M10	$YPIN_{28}$	N12	$YPIN_{30}$
B2	$PYOUT_4$	C4	GND	D13	$RXOUT_{15}$	G3	GND	J13	$XRIN_8$	L9	$YPIN_{27}$	M11	ENXR	N13	$XRIN_0$



Pin Assignments – 132 Leaded CERQUAD, L5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{DD}	23	$YPIN_1$	45	V_{DD}	67	V_{DD}	89	GND	111	$RXOUT_2$
2	NC	24	$YPIN_2$	46	$YPIN_{18}$	68	RXIN1	90	$RXOUT_{15}$	112	VDD
3	$PYOUT_4$	25	$YPIN_3$	47	$YPIN_{19}$	69	RXIN2	91	V_{DD}	113	$RXOUT_1$
4	$PYOUT_3$	26	$YPIN_4$	48	$YPIN_{20}$	70	GND	92	$RXOUT_{14}$	114	$RXOUT_0$
5	GND	27	$YPIN_5$	49	GND	71	$RXIN_3$	93	$RXOUT_{13}$	115	OVF
6	$PYOUT_2$	28	$YPIN_6$	50	$YPIN_{21}$	72	NC	94	$RXOUT_{12}$	116	GND
7	$PYOUT_1$	29	GND	51	$YPIN_{22}$	73	$RXIN_4$	95	GND	117	$PYOUT_{15}$
8	$PYOUT_0$	30	$YPIN_7$	52	$YPIN_{23}$	74	$RXIN_5$	96	$RXOUT_{11}$	118	$PYOUT_{14}$
9	V_{DD}	31	$YPIN_8$	53	V_{DD}	75	GND	97	$RXOUT_{10}$	119	$PYOUT_{13}$
10	$\overline{OEPY}$	32	NC	54	$YPIN_{24}$	76	$RXIN_6$	98	NC	120	V_{DD}
11	GND	33	GND	55	$YPIN_{25}$	77	$RXIN_7$	99	V_{DD}	121	$PYOUT_{12}$
12	RTP	34	$YPIN_9$	56	$YPIN_{26}$	78	$RXIN_8$	100	$RXOUT_9$	122	$PYOUT_{11}$
13	CLK	35	NC	57	$YPIN_{27}$	79	$RXIN_9$	101	NC	123	$PYOUT_{10}$
14	GND	36	$YPIN_{10}$	58	$YPIN_{28}$	80	$RXIN_{10}$	102	$RXOUT_8$	124	GND
15	TCXY	37	V_{DD}	59	$YPIN_{29}$	81	$RXIN_{11}$	103	NC	125	$PYOUT_9$
16	$ENYP_0$	38	$YPIN_{11}$	60	$YPIN_{30}$	82	$RXIN_{12}$	104	GND	126	$PYOUT_8$
17	GND	39	$YPIN_{12}$	61	$YPIN_{31}$	83	GND	105	$RXOUT_7$	127	$PYOUT_7$
18	$ENYP_1$	40	$YPIN_{13}$	62	NC	84	$RXIN_{13}$	106	$RXOUT_6$	128	NC
19	ACC_0	41	$YPIN_{14}$	63	ENXR	85	$RXIN_{14}$	107	$RXOUT_5$	129	GND
20	ACC_1	42	$YPIN_{15}$	64	NC	86	$RXIN_{15}$	108	GND	130	$PYOUT_6$
21	V_{DD}	43	$YPIN_{16}$	65	NC	87	V_{DD}	109	$RXOUT_4$	131	NC
22	$YPIN_0$	44	$YPIN_{17}$	66	$XRIN_0$	88	$\overline{OERX}$	110	$RXOUT_3$	132	$PYOUT_5$



Correlators

TRW is the industry-leader in correlators for high-performance communications, signal, radar and image processing applications. Correlators measure the similarity between two digital signal streams, which is key to pattern recognition and data synchronization applications. All TRW correlators are TTL compatible.

Correlators

Product	Description	Size	Clock Rate [1] (MHz)	Power [1] (Watts)	Package	Grades [2]	Notes	Page
TDC2023-1	Correlator	64 x 1	30	0.4	B2, B724 Pin DIP	C, V, SMD	Pin Compatible with TDC1023.	G5
					C3 28 Contact CC	V, SMD	Threshold Flag.	
-			25	0.4	B2,B7 24 Pin DIP	C, V, SMD		G5
					C3 28 Contact CC	V, SMD		
TMC2220-1	Correlator	4 x 32	20	0.3	G8 69 Pin PGA	C, V	Programmable.	G17
					H8 69 Pin PPGA	C	Optional I&Q Modes.	
-			17	0.3	G8 69 Pin PGA	C, V		
					H8 69 Pin PPGA	C		
TMC2221-1	Correlator	1 x 128	20	0.3	B6 28 Pin DIP	C, V	Programmable.	G17
-			17	0.3	B6 28 Pin DIP	C, V		

Notes: 1. Guaranteed. See product specifications for test conditions.

2. C = Commercial, $T_A = 0°C$ to $70°C$.
V = MIL-STD-883 Compliant, $T_C = -55°C$ to $125°C$
SMD = Available per Standardized Military Drawing, $T_C = -55°C$ to $125°C$.

TDC1023
Use TMC2023 for New Designs

Digital Output Correlator
64-Bit

The TRW TDC1023 is a monolithic, all-digital 64-bit correlator with a 7-bit three-state buffered digital output. This device consists of three 64-bit independently clocked shift registers, one 64-bit reference holding latch, and a 64-bit independently clocked digital summing network. The device is capable of a 17MHz parallel correlation rate.

The 7-bit threshold register allows the user to preload a binary number from 0 to 64. Whenever the correlation is equal to or greater than the number in the threshold register, the threshold flag goes HIGH.

The 64-bit mask shift register (M register) allows the user to mask or selectively choose "no compare" bit positions enabling total word length flexibility.

The reference word is serially shifted into the B register. By clocking the R latch, the data is parallel-loaded into the R reference latch. This allows the user to serially load a new reference word into the B register while correlation is taking place between the A register and R latch. The two words are continually compared bit-for-bit by exclusive-OR circuits. Each exclusive-OR provides one bit to the digital summer. The output is a 7-bit word representing the sum of positions which agree at any one time between the A register and R latch.

A control provides either true or inverted binary output formats.

Features

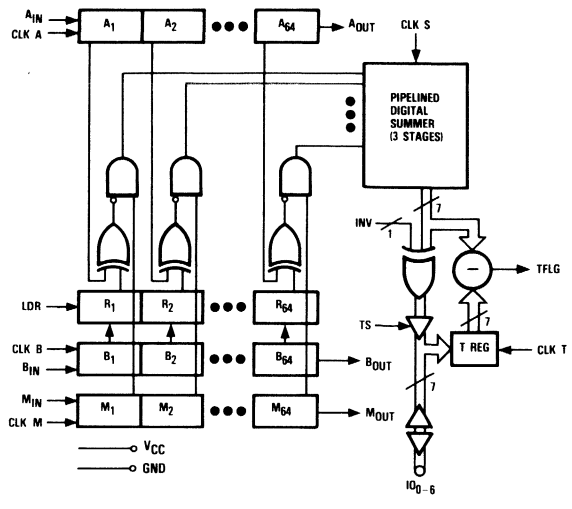
- 17MHz Correlation Rate
- TTL Compatible
- All Digital
- Single +5V Power Supply
- Serial Data Input, Parallel Correlation Output
- Programmable Word Length
- Independently Clocked Registers
- Available In 24 Pin DIP
- Output Format Flexibility
- Three-State Outputs

Applications

- Check Sorting Equipment
- High-Density Recording
- Bar Code Identification
- Radar Signature Recognition
- Video Frame Synchronization
- Electro-Optical Navigation
- Pattern And Character Recognition
- Cross-Correlation Control Systems
- Error Correction Coding
- Asynchronous Communication

G

Functional Block Diagram



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40G00283 Rev. H – 11/90
Printed in the U.S.A.

TMC2023

CMOS Digital Output Correlator
64-Bit, 30MHz

The TMC2023 is a monolithic 64-bit correlator with a 7-bit three-state buffered digital output. This device consists of three 64-bit independently clocked shift registers, one 64-bit reference holding latch, and a 64-bit independently clocked digital summing network. The device is capable of a 30MHz parallel correlation rate.

The 7-bit threshold register allows the user to preload a binary number from 0 to 64. Whenever the correlation is equal to or greater than the number in the threshold register, the threshold flag goes HIGH.

The 64-bit shift mask register (M register) allows the user to mask or selectively choose "no compare" bit positions enabling total word length flexibility.

The reference word is serially shifted into the B register. By clocking the R latch, the data is parallel-loaded into the R reference latch. This allows the user to serially load a new reference word into to the B register while correlation is taking place between the A register and the R latch. The two words are continually compared bit-by-bit by exclusive-OR circuits. Each exclusive-OR provides one bit to the digital summer. The output is a 7-bit word representing the sum of positions which agree at any one time between the A register and R latch. A control provides either true or inverted binary output formats.

Built with TRW's one-micron double level metal OMICRON-C™ low power CMOS process, the TMC2023 is available in a 24 pin CERDIP package and 28 contact chip carrier. The CMOS TMC2023 is pin compatible with the bipolar TDC1023.

Features

- 30MHz Correlation Rate (Worst Case Commercial)
- All Inputs And Outputs TTL Compatible
- Serial Data Input, Parallel Correlation Output
- Programmable Word Length
- Independently Clocked Registers
- Programmable Threshold Detection And Flag Output
- Available In 24 Pin CERDIP And 28 Contact Chip Carrier
- Available To Standard Military Drawing (SMD)
- Pin Compatible With TDC1023
- Output Format Flexibility
- Three-State Outputs
- Low Power CMOS

Applications

- Check Sorting Equipment
- High Density Recording
- Bar Code Identification
- Radar Signature Recognition
- Video Frame Synchronization
- Electro-Optical Navigation
- Pattern And Character Recognition
- Cross-Correlation Control Systems
- Error Correction Coding
- Asynchronous Communication
- Matched Filtering

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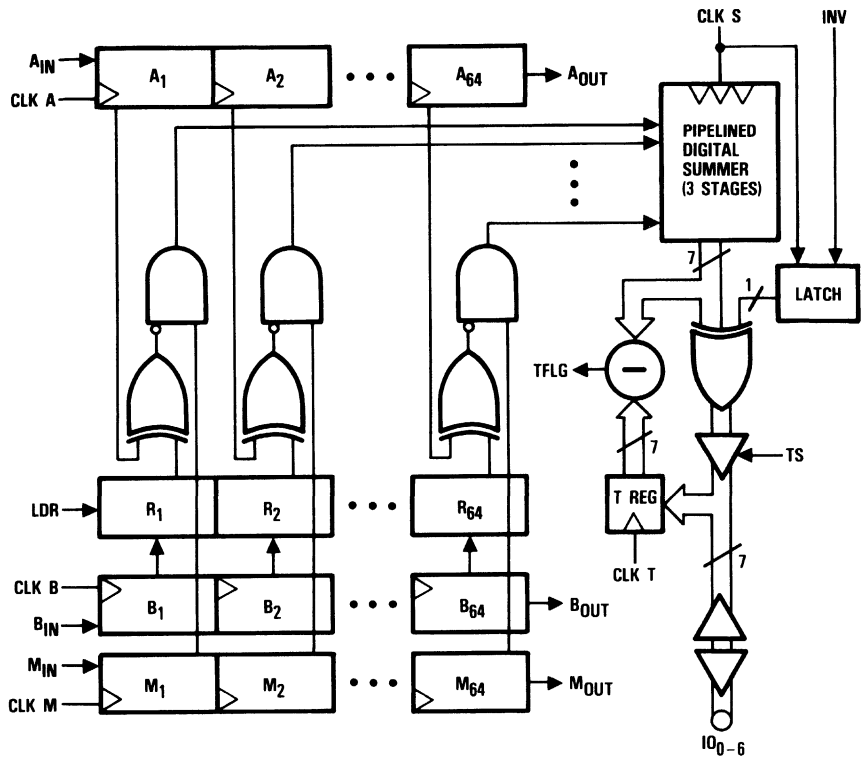
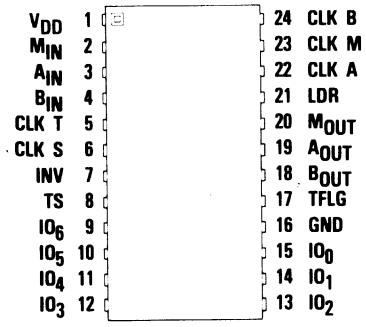
40G05746 Rev. C – 11/90
Printed in the U.S.A.

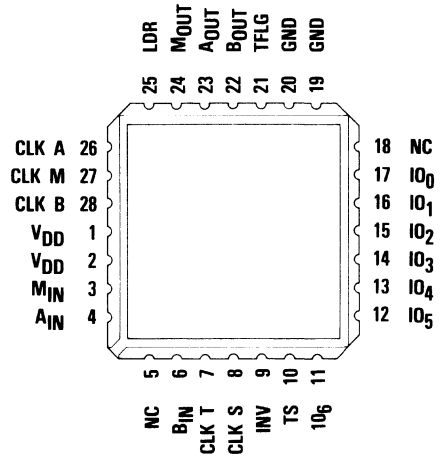
Functional Block Diagram



Pin Assigments



24 Pin CERDIP – B2, B7 Package



28 Contact Chip Carrier – C3 Package

Functional Description

General Information

The TMC2023 consists of an input section and an output section. The input section contains the A, B, and M registers, an R latch, XOR/AND logic and a pipelined summer network. The output section consists of threshold, inversion and three-state logic.

Signal Definitions

Power

V_{DD}, GND — The TMC2023 operates from a single +5V supply. All V_{DD} and GND pins must be connected.

Control

INV — Control that inverts the 7-bit digital output. When a HIGH level is applied to this pin, the outputs IO_{0-6} are logically inverted. See the ***Timing Diagrams*** for setup and hold requirements.

TS — The three-state control enables and disables the output buffers. A HIGH level applied to this pin forces outputs into the high-impedance state. This control also allows loading of the internal threshold register.

LDR — Control that allows parallel data to be loaded from the B register into the reference latch for correlation. If LDR is held HIGH, the R latch is transparent.

Clocks

CLK A, CLK M, CLK B — Input clocks. Clock input pins for the A, M, and B registers, respectively. Each register may be independently clocked.

CLK T — Threshold register clock. Clock input used to load the T register.

CLK S — Digital summer clock. Clock input that allows independent clocking of the pipelined summer network.

Data Inputs

M_{IN} — Mask Register Input. Allows the user to choose "no-compare" bit positions. A "0" in any bit location will result in a no-compare state for that location (bit position masked).

A_{IN}, B_{IN} — Shift register inputs to the A and B 64-bit serial registers.

Data Outputs

IO_{0-6} — Bi-directional data pins. When Outputs are enabled (TS LOW), data is a 7-bit binary representation of the correlation between the unmasked portions of the R latch and the A register. IO_6 is the MSB. These pins also serve as parallel inputs to load the threshold register. Data present one setup time before CLK I goes HIGH will be latched into the threshold register.

TFLG — The TFLG output goes HIGH whenever the correlation score is equal to or greater than the number loaded into the T register (0 to 64).

B_{OUT}, A_{OUT}, M_{OUT} — Shift register outputs of the three 64-bit shisft registers: B, A, and M, respectively. These outputs may be used to cascade multiple devices.

No Connect

NC — These pins are not functional and should be left unconnected.

G

Package Interconnections

Signal Type	Signal Name	Function	B2, B7 Package Pins	C3 Package Pins
Power	GND	Ground	16	19, 20
	V_{DD}	Supply Voltage	1	1, 2
Control	INV	Invert Output	7	9
	TS	Three-State Enable	8	10
	LDR	Load Reference	21	25
Clocks	CLK A	A Register Clock	22	26
	CLK M	M Register Clock	23	27
	CLK B	B Register Clock	24	28
	CLK T	Threshold Register Clock	5	7
	CLK S	Digital Summer Clock	6	8
Data Inputs	M_{IN}	Mask Register Input	2	3
	A_{IN}	Shift Register Input	3	4
	B_{IN}	Shift Register Input	4	6
Data Outputs	IO_{6-0}	Correlation Score	9, 10, 11, 12, 13, 14, 15	11, 12, 13, 14, 15, 16, 17
	TFLG	Threshold Flag	17	21
	B_{OUT}	Shift Register B	18	22
	A_{OUT}	Shift Register A	19	23
	M_{OUT}	Shift Register M	20	24
No Connects	NC	No Connect	None	5, 18

Timing Diagrams

Continuous Correlation

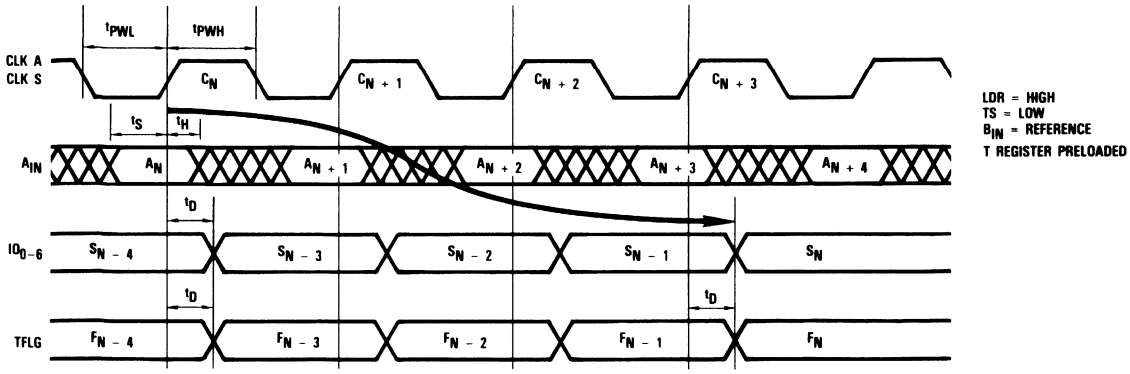
The TMC2023 contains three 1 x 64 serial shift registers (A, B, and M). The operation of these registers is identical and each has its own input, output, and clock. As shown in the timing diagram (***Figure 1***), valid data is loaded into register A (B, M) on the rising edge of CLK A (CLK B, CLK M). Data is valid if present at the input for a setup time of at least t_S before and a hold time of t_H after the rising clock edge.

The summing process is initiated when the comparison result between the A register and R latch is clocked into the summing network by a rising edge of CLK S. Typically, CLK A and CLK S are tied together so that a new correlation score is computed for each new alignment of the A register and R latch. When LDR goes HIGH, the contents of register B are copied into the R latch. With LDR LOW, a new template may be entered serially into register B, while parallel correlation takes place between register A and the R latch. In the case of continuous correlation, LDR is held HIGH so that the R latch contents continuously track those of the B register.

The summing network consists of three pipelined stages. Therefore, the total correlation score for a given set of A and B register contents appears at the summer output three CLK S cycles later. Data on the output pins IO_{0-6} is available after an additional propagation delay, denoted t_D on the timing diagram (***Figure 1***).

The correlation result is compared with the contents of the threshold register. TFLG goes HIGH if the correlation equals or exceeds the threshold value. TFLG is valid after a delay of t_D (ns) from the third CLK S rising edge.

Figure 1. Continuous Correlation

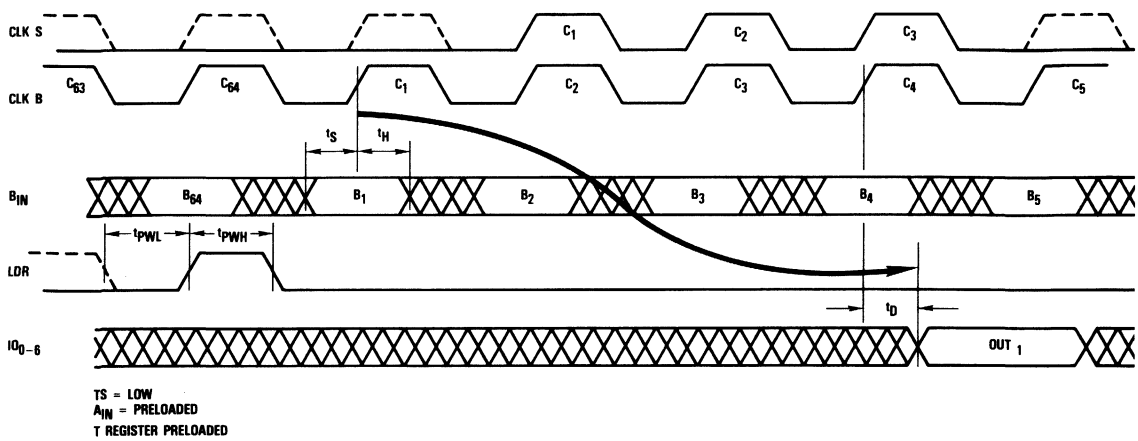


Cross Correlation

When LDR goes HIGH, the B register contents are copied into the reference latch (R latch). This useful feature allows correlation to take place between data in the R latch and the A register while a new reference is being serially clocked into the B register. If the new reference is n bits long, it requires n rising edges of CLK to load this data into the B register. For the timing diagram (see *Figure 2*), n=64. LDR is set HIGH during the final (n^{th}) CLK B cycle, so that the new reference word is copied into the R latch. The minimum LOW and HIGH level pulse widths for LDR are shown as t_{PWL} (ns) and t_{PWH} (ns), respectively.

After the new reference is loaded, the data to be correlated is clocked through the A register. Typically, CLK A and CLK S can be tied together. This allows a new correlation score to be computed for each shift of the A register data relative to the fixed reference word in the R latch. The digital summer is internally partitioned into three pipelined stages. Therefore, a correlation score for a particular alignment of the A register data and the R latch reference appears at the summer output three CLK S cycles later. After an additional output delay of t_D (ns), the correlation data is valid at the output pins (IO_{0-6}). If this correlation result is equal to or exceeds the value in the threshold register, then TFLG goes HIGH. TFLG is valid t_D (ns) after the third rising edge of CLK S.

Figure 2. Cross-Correlation



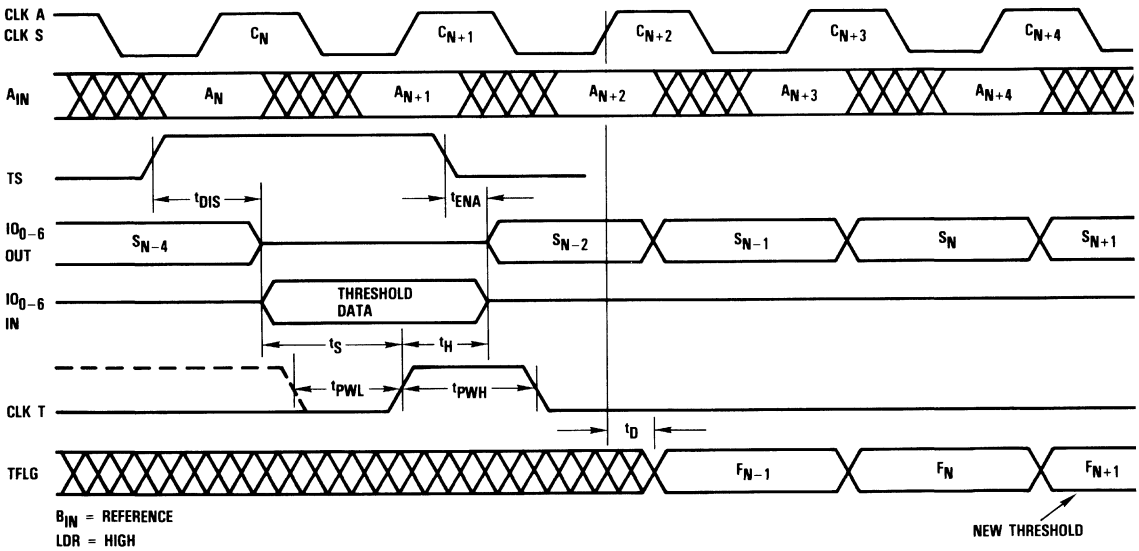
Threshold Register Load

The timing sequence for loading the threshold (T) register is shown in *Figure 3*. The T register holds the 7-bit threshold value to be compared with each correlation result. The rising edge of CLK T loads the data present on the IO_{0-6} pins into the T register. T flag logic is pipelined 3 stages, with the summer. The new value loaded into the threshold register will affect the TFLG on the third CLK S (plus an output delay t_D) following the T register load.

The output buffers must be in a high-impedance state (disabled) when the T register is programmed from an external source. After a delay of t_{DIS} (ns) from the time TS goes HIGH, the output buffers are disabled. The data pins IO_{0-6} may then be driven externally with the new threshold data. The data must be present for a setup time of t_S (ns) before and t_H (ns) after the rising edge of CLK T for correct operation. The minimum LOW and HIGH level pulse widths for CLK T are shown below as t_{PWL} (ns) and t_{PWH} (ns), respectively.

After TS is set LOW, there is an enable delay of t_{ENA} (ns) before the internal correlation data is available at pins IO_{0-6}.

Figure 3. Threshold Register Load



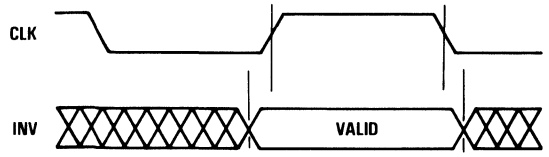
Invert Control Timing

Most applications will hardwire the INVert control HIGH or LOW depending on system requirements. In the few situations in which the control is used dynamically, the user must observe special timing constraints.

Because INVERT governs logic located between the master and slave latches of the data output register, its setup and hold requirements differ from those of the data and other controls. The device will respond to changes on INV whenever CLOCK is HIGH and will ignore it when CLOCK is LOW. To minimize the data output delay and to avoid inducing errors, the user should observe the following timing constraints:

1) Set INVERT to the desired state for the next output on or before the rising edge of CLOCK (*Figure 4*). If INVERT is asserted a few nano-seconds after the rising edge, the data output may be correspondingly delayed.
2) More importantly, keep INVERT in the desired state until after the falling edge of CLOCK, to avoid corrupting the output data. If INVERT is changed several nanoseconds before the falling edge of CLOCK, the data will likewise change. If it is changed just before the falling edge, an indeterminate output may result.

Figure 4. Invert Control Timing



Mask Register

In addition to the A and B shift references, the TMC2023 has another independently clocked register: the M, or mask register. The M register functions identically to the A and B register, except that its parallel outputs are ANDed with the exclusive-ORed outputs from the A register and R latch.

Many uses of the TMC2023 digital correlator require disabling the correlation between certain bit positions (A_i and R_i) of input words A and R. While correlation data is being clocked into the A and/or B register, a mask word may be entered into the M register. Where no comparison is to be made, zeroes are entered in those M register positions. The exclusive-OR result between each bit position is ANDed with a bit from the M register. Thus, if a particular mask bit (M_i) is zero, the output correlation between A and B for that bit position will be disabled. Consequently, a zero correlation is presented to the digital summer for each masked bit position.

The Mask register is useful for changing correlation word length and location within the registers. Where a word is undefined or no correlation is to take place, the M register should contain zeroes.

The M register is useful for building logic functions. Note that for each bit A_i and R_i, the correlation logic is:

$$A_i + R_i \qquad A_i\overline{R}_i + \overline{A}_iR_i \ (A_i \text{ exclusive-OR } R_i)$$

This result is complemented at the input of the AND gates and ANDed with the mask bit (M_i) resulting in:

$$\overline{[A_i\,\overline{R}_i + \overline{A}_iR_i]} \cdot M_i$$

The last step, performed in the digital summer, is to sum the above result over all bit positions simultaneously for a correlation at time K:

$$C(K) = \sum_{i=1}^{n} \overline{[A_i\overline{R}_i + \overline{A}_iR_i]} \cdot M_i$$

where:

$i = 1, 2, 3...$
$n =$ correlation word length

Figure 5. Equivalent Input Circuit

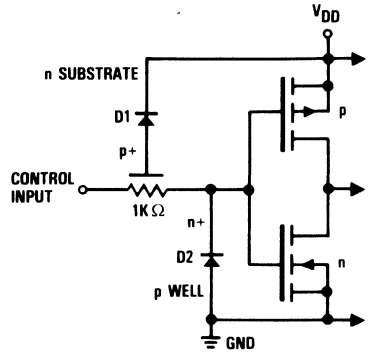


Figure 6. Equivalent Output Circuit

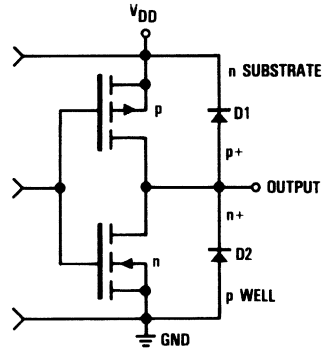
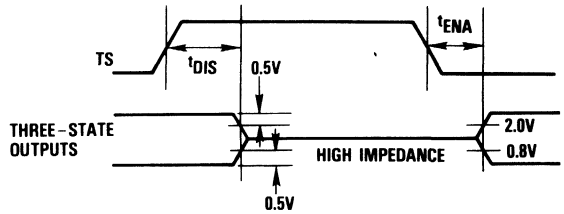


Figure 7. Threshold Levels for Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage [2]	−0.5 to (V_{DD} + 0.5)V
Forced current [3,4]	−3.0 to +6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 Second
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

		Temperature Range												
		Standard						Extended						
		−1						−1						
Parameter		**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Units**
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.5	5.0	5.5	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW CLK A, B, M, S, T, LDR	12			15			14			15			ns
t_{PWH}	Clock Pulse Width, HIGH CLK A, B, M, S, T, LDR	12			15			14			15			ns
t_S	Data Input Setup Time	8			12			10			14			ns
t_H	Data Input Hold Time	0			0			0			0			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			2.0			2.0			V
V_{IHC}	Input Voltage, Logic HIGH A, B, M, S CLKs	2.0			2.0			2.4			2.4			V
I_{OL}	Output Current, Logic LOW			4.0			4.0			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70	0		70							°C
T_C	Case Temperature							−55		125	−55		125	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V, TS = 5V		5		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 30MHz, TS = 5V		30		35	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	−10		−10		μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		+10		+10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW [2]	V_{DD} = Max, V_{IN} = 0V [1]	−40		−40		μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH [2]	V_{DD} = Max, V_{IN} = V_{DD}		+40		+40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		−100		−100	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Notes:
1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Due to the IO_{0-6} and T register interconnections, these values are the I_{IH} and I_{IL} of the T register.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range: Standard −1 Min	Standard −1 Max	Standard Min	Standard Max	Extended −1 Min	Extended −1 Max	Extended Min	Extended Max	Units
F_{SH}	Shift-In Clock Rate	V_{DD} = Min	30		25		30		25		MHz
F_C	Correlation Rate	V_{DD} = Min [2]	30		25		30		25		MHz
t_D	Digital Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		20		24		23		25	ns
t_{ENA}	Three-State Output Enable Delay	V_{DD} = Min, C_{LOAD} = 40pF		16		20		20		25	ns
t_{DIS}	Three-State Output Disable Delay	V_{DD} = Min, C_{LOAD} = 40pF		16		20		18		24	ns

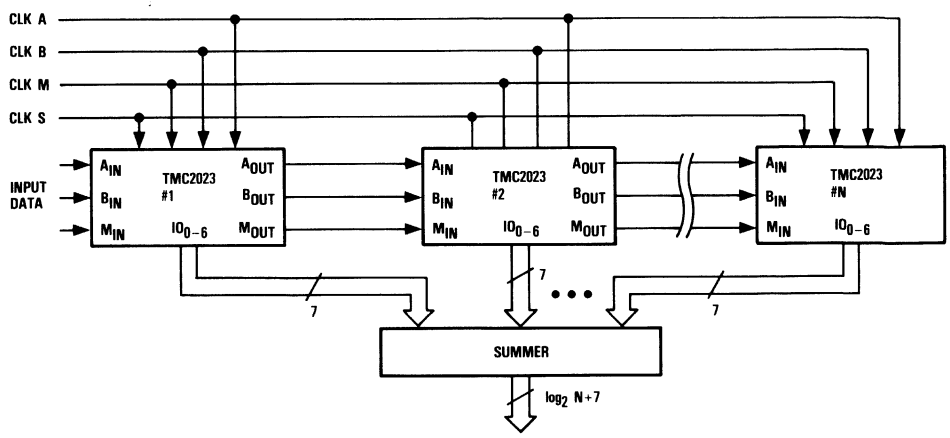
Notes:
1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 7.
2. Synchronous clocking: CLK A = CLK B = CLK M = CLK S.

G

Application Notes

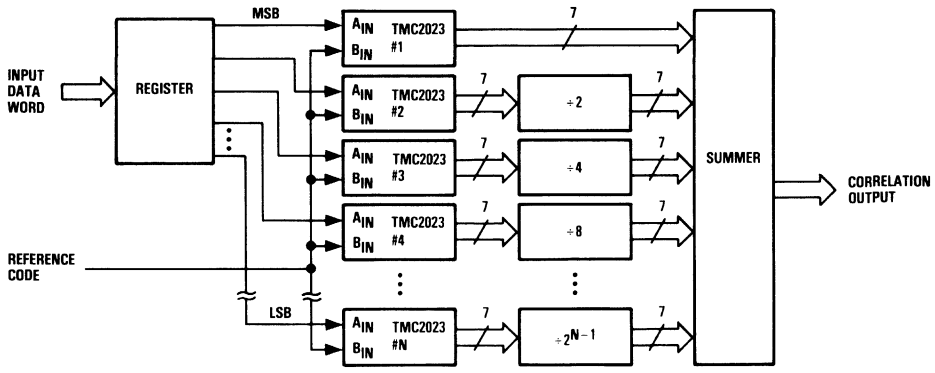
The TMC2023 can be cascaded to implement correlations of more than 64 bits. Typically, all clocks are tied together and the A, B, and M outputs of preceding stages are connected to the respective inputs of subsequent stages. An external summer is required to generate the composite correlation score. Use of the T register and TFLG require additional hardware for this configuration.

Figure 8. Cascading for Extended-Length Correlation



When comparing a multi-bit word to a single-bit reference, the outputs from the individual correlators must be appropriately weighted. This weighting reflects the relative importance of the different bit positions. Normally simple shifts (division by 2, 4, 8,...) provide the required weighting.

Figure 9. Multi-Bit x 1-Bit Correlation

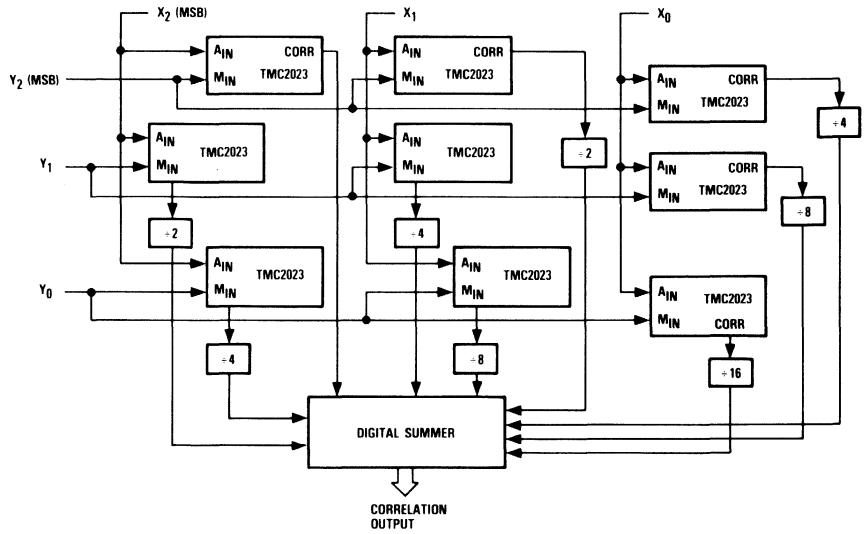


The correlation of two multi-bit words requires evaluating the term:

$$R(M) = \sum_{n=1}^{N} h(n) \cdot (M+n)$$

An example of two 3-bit words is shown in *Figure 10*.

Figure 10. Multi-Bit Correlation



Standard Military Drawing

These devices are also available as products manufactured, tested, and screened in compliance with Standard Military Drawings (SMDs). The nearest vendor equivalent product is shown below; however, the applicable SMD is the sole controlling document defining the SMD product.

SMD	Nearest Equiv. TRW Product	Speed	Package
5962-89711-01JA	TMC2023B7V	25MHz	24 Pin CERDIP 0.6" Wide
5962-89711-02JA	TMC2023B7V1	30MHz	24 Pin CERDIP 0.6" Wide
5962-89711-01LA	TMC2023B2V	25MHz	24 Pin CERDIP 0.3" Wide
5962-89711-02LA	TMC2023B2V1	30MHz	24 Pin CERDIP 0.3" Wide
5962-89711-013A	TMC2023C3V	25MHz	28 Contact Chip Carrier
5962-89711-023A	TMC2023C3V1	30MHz	28 Contact Chip Carrier

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2023B2C	STD–T_A = 0°C to 70°C	Commercial, 25MHz	24 Pin CERDIP	2023B2C
TMC2023B2V	EXT–T_C = –55°C to 125°C	MIL-STD-883, 25MHz	24 Pin CERDIP	2023B2V
TMC2023B2C1	STD–T_A = 0°C to 70°C	Commercial, 30MHz	24 Pin CERDIP	2023B2C1
TMC2023B2V1	EXT–T_C = –55°C to 125°C	MIL-STD-883, 30MHz	24 Pin CERDIP	2023B2V1
TMC2023B7C	STD–T_A = 0°C to 70°C	Commercial, 25MHz	24 Pin CERDIP	2023B7C
TMC2023B7V	EXT–T_C = –55°C to 125°C	MIL-STD-883, 25MHz	24 Pin CERDIP	2023B7V
TMC2023B7C1	STD–T_A = 0°C to 70°C	Commercial, 30MHz	24 Pin CERDIP	2023B7C1
TMC2023B7V1	EXT–T_C = –55°C to 125°C	MIL-STD-883, 30MHz	24 Pin CERDIP	2023B7V1
TMC2023C3V	EXT–T_C = –55°C to 125°C	MIL-STD-883, 25MHz	28 Contact Hermetic Ceramic Chip Carrier	2023C3V
TMC2023C3V1	EXT–T_C = –55°C to 125°C	MIL-STD-883, 30MHz	28 Contact Hermetic Ceramic Chip Carrier	2023C3V1

TMC2220/TMC2221

CMOS Programmable Digital Output Correlators

4 x 32 Bit, 20MHz
1 x 128 Bit, 20MHz

The TMC2220 20MHz, TTL compatible CMOS correlator is composed of four separate 1 x 32 correlator modules. The correlation scores of the four modules are weighted, combined and output on two separate parallel, three-state ports.

Each module contains a 32-bit serial data register, a 32-bit serial reference preload register, a 32-bit parallel reference latch and a 32-bit parallel mask latch. Correlation is performed by 32 exclusive-NOR (XNOR) gates. Each XNOR gate compares one (single bit) data word against a corresponding (single bit) reference word. While correlation is being performed between the data and the present reference, the next reference pattern may be preloaded through one of two multiplexed input ports. Shorter sampling windows and bipolar correlation are also supported. Each module outputs a 6-bit binary correlation score. Either an unsigned (range 0 through 32) or bipolar (range −16 through +16) representation may be selected. The outputs of each pair of correlator modules is added, with user-selected weighting factors, producing intermediate correlation scores which can be combined or output directly to the main or auxiliary output ports.

Since the four modules can be cascaded serially or in parallel, the TMC2220 supports numerous single and dual channel applications involving 1, 2 or 4-bit wide data and window lengths up to 32, 64, 96 or 128 bits. Multiple devices can be combined to support large correlation operations.

The TMC2221 combines the four 32-bit modules in series for a fixed channel configuration of 1-bit by 128. The reduced complexity and package size of the TMC2221 is ideal for applications requiring less versatility than the TMC2220. By making use of the mask function, any size single channel length of up to 128 bits is possible.

With the TMC2221, the reference word is serially loaded through the single two-input multiplexed reference port of the first correlator module. Although the configuration is fixed, the reference loading process and basic operation for each module is similar to that of the TMC2220. The outputs are summed with equal weighting, and the result is output through the single 8-bit output port. Unsigned magnitude or two's complement (bipolar) output score may be selected.

Features

- 20MHz Continuous Correlation Rate
- Fully Programmable Masking
- Two's Complement Or Unsigned Magnitude Correlation Score
- User-Programmable Reference Load Multiplexing
- Channel Weighting And Output Formatting (TMC2220)
- Multi-Bit, Dual-Channel Or Non-Coherent (Quadrature) Correlation (TMC2220)
- Single +5V Power Supply
- Low Power CMOS Construction
- Three-State TTL Compatible Outputs
- TMC2220 Available In 68 Pin Grid Array And 69 Pin Plastic PGA Packages
- TMC2221 Available In 28 Pin CERDIP

Applications

- Signal Detection
- Radar Signature Recognition
- Secure Communications
- Robotics/Automated Assembly
- Automatic Test Equipment
- Electro-Optical Navigation
- Pattern And Character Recognition
- Assembly Line Inspection

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FAX: (619) 455-6314

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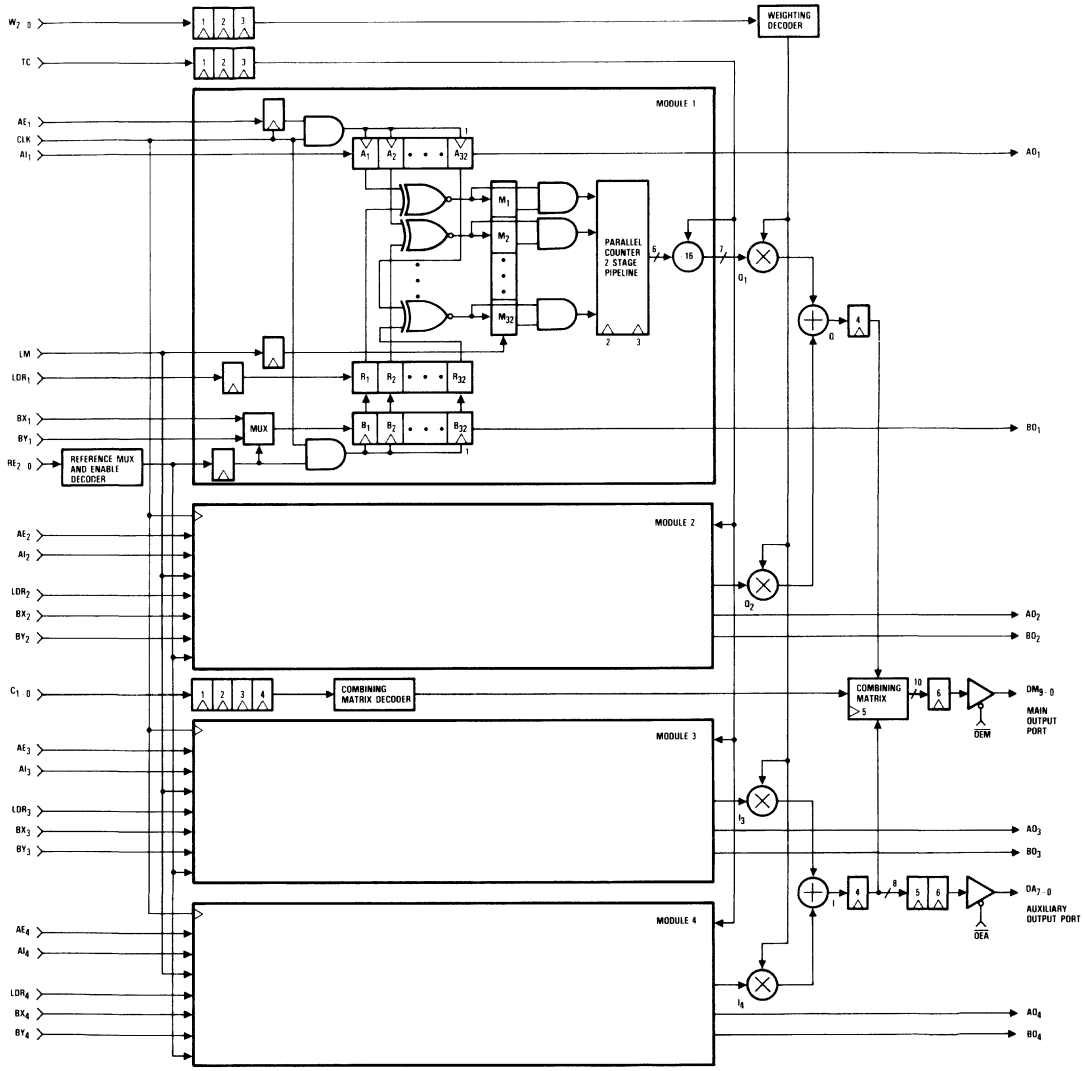
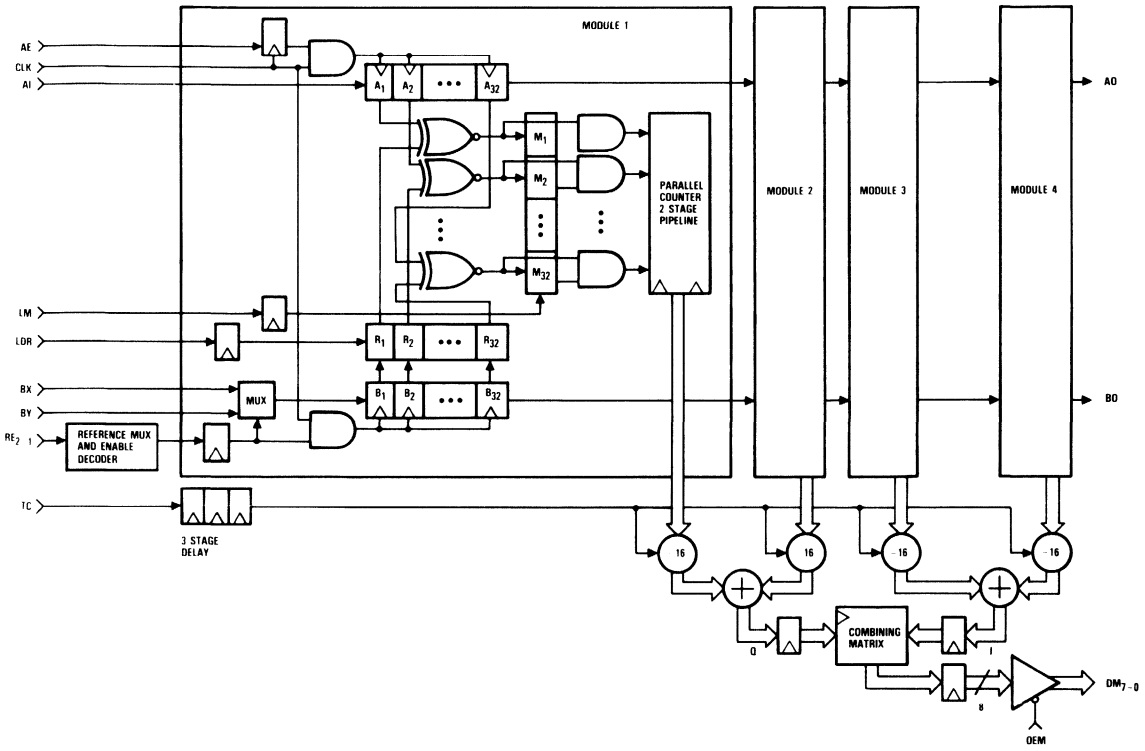
TMC2220 Functional Block Diagram



Functional Block Diagram



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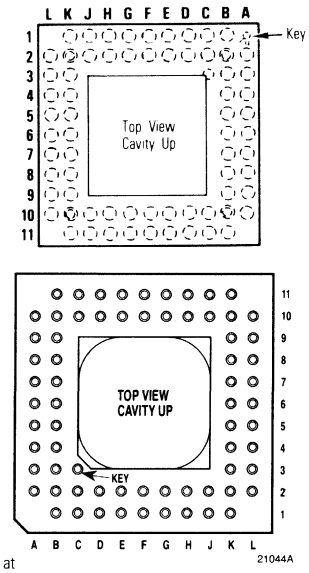
TMC2220 Pin Assignments

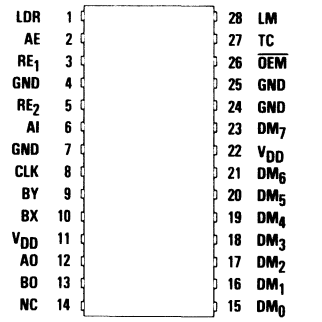
68 Pin Grid Array – G8 Package
69 Pin Plastic Pin Grid Array – H8 Package [1]

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B2	DA_1	K2	GND	K10	RE_2	B10	LDR_4
B1	DA_0	L2	V_{DD}	K11	AI_2	A10	AE_4
C2	DM_0	K3	GND	J10	BY_2	B9	LDR_3
C1	DM_1	L3	$\overline{OEM}$	J11	BX_2	A9	AE_3
D2	DM_2	K4	W_2	H10	AI_1	B8	$\overline{OEA}$
D1	DM_3	L4	W_1	H11	BY_1	A8	V_{DD}
E2	DM_4	K5	W_0	G10	BX_1	B7	AO_4
E1	DM_5	L5	C_1	G11	GND	A7	BO_4
F2	V_{DD}	K6	C_0	F10	CLK	B6	AO_3
F1	DM_6	L6	TC	F11	GND	A6	BO_3
G2	DM_7	K7	LM	E10	BY_3	B5	DA_7
G1	DM_8	L7	LDR_1	E11	BX_3	A5	DA_6
H2	DM_9	K8	AE_1	D10	AI_3	B4	DA_5
H1	BO_1	L8	LDR_2	D11	BY_4	A4	DA_4
J2	AO_1	K9	AE_2	C10	BX_4	B3	DA_3
J1	BO_2	L9	RE_0	C11	AI_4	A3	DA_2
K1	AO_2	L10	RE_1	B11	V_{DD}	A2	GND



Note: 1. Pin D4 is a mechanical orientation pin on the H8 package at manufacturer's option.

TMC2221 Pin Assignments



28 Pin CERDIP – B6 Package

Functional Description

General Information

The TMC2220 consists of four independent 1 x 32 correlator channels with weighted correlation scores which are combined and output on the two output ports (main and auxiliary). By taking advantage of the instruction set and I/O structure, the TMC2220 can be adapted to a wide variety of applications.

The TMC2221 consists of the four 1 x 32 correlator modules cascaded internally for a single 1 x 128 correlator. The outputs of each module are given a unity weighting, summed and placed on the output port.

Correlator Channel Modules

Each of the four modules (i = 1 to 4) contains two 32-bit serial synchronous shift registers, A_i (data) and B_i (reference preload); two 32-bit parallel latches, R_i (reference) and M_i (mask); 32 exclusive-NOR gates; 32 AND gates; a 32-bit parallel binary counter with a 6-bit unsigned output and a defeatable half-scale (-16) subtractor with a 7-bit two's complement output.

Whenever a given A_i or B_i register is enabled, the next rising edge of the clock loads the value at the corresponding A_i or BX_i/BY_i input port into the first cell of the register, and shifts the contents of each cell to the next, overwriting the contents of the last cell. These serial-in, parallel-tapped registers form the first of six registers which account for the six internal delays. After an output buffer delay t_D, the new contents of the last cell of A_i and B_i become available at the outputs AO_i and BO_i respectively. These outputs are used for cascading multiple devices. In addition, the B_i input multiplexer selects which of two input ports, BX_i or BY_i, is to be used on that cycle.

The reference latch R_i tracks the contents of B_i when control LDR_i was HIGH on the previous cycle and holds when LDR_i was LOW. A HIGH on LDR_i transfers the contents of B_i in parallel into R_i on the next clock cycle where correlation takes place. When LDR_i is held HIGH, R_i is transparent, enabling direct correlation between A_i and B_i.

Each of the 32 outputs of R_i is correlated against the corresponding tap of A_i by an XNOR gate whose output is connected to both the masking AND gate and the masking latch M_i.

Each M_i tracks if LM was HIGH on the previous cycle and holds if LM was LOW. When LM is held HIGH, all M_i latches are transparent and the output of each XNOR gate is sent to both inputs of the corresponding AND gate to prevent masking or disabling from occurring. A LOW on LM loads the next unmasked correlation pattern (from the XNOR gates) into each M_i. Wherever the latch holds a logic one, normal correlation is enabled; wherever it is a logic zero, correlation is masked by the AND gate.

A 32-bit parallel counter encodes the number of logic ones emerging from the AND gates as a 6-bit binary number between 0 and 32 (100000). The clock drives the two pipeline registers in the counter (the second and third registers in the six register pipeline).

The 6-bit unsigned binary output of each parallel counter then enters a half-scale subtractor where it passes unchanged if the pipelined control TC is LOW and is reduced by 16 if TC is HIGH. If TC is HIGH, the range of correlation scores becomes -16 through +16 where +16 denotes a perfect match between the contents of A_i and those of R_i with no masking. A score of -16 denotes that no unmasked data bit matches the corresponding reference bit (anti-correlation). The TC control is pipelined by 3 registers, such that it is aligned with new data entering the A_i or B_i register.

Weighting and Merging Circuitry

On the TMC2220, the 7-bit two's complement output of each correlator module (Q_1, Q_2, I_3, I_4) is multiplied by a factor of 0, 1, 2, 3, 4 or 5 according to controls W_{2-0}. The outputs of each pair of multipliers is then added and the results Q and I are loaded into the fourth pipeline register.

Following two additional pipeline delays from the fifth and sixth registers, correlation sum I is available on the TMC2220 at the 8-bit auxiliary output port, DA_{7-0}, if the buffer is enabled ($\overline{OEA}$ = LOW).

Under controls C_{1-0}, the TMC2220 combiner blends Q and I into a single final correlation score which is sent to the 10-bit main output port, DM_{9-0}, if $\overline{OEM}$ is LOW. The combiner pipeline register stage 5 and the main output register stage 6 are balanced by the auxiliary port double output register. In the simplest mode, the combiner outputs correlation sum Q permitting the TMC2220 to be used in two separate correlator channels. In this application, the combined results from modules 1 and 2 emerge through DM_{9-0} while the results from modules 3 and 4 emerge through DA_{7-0}. In the three remaining modes, the output at the main port will reflect the correlations of all four modules.

In the second mode, the combiner outputs the unweighted sum, Q + I. In the third mode, it outputs the weighted sum, Q + I/2, for single channel binary applications. In the fourth mode, the combiner extracts the absolute values of Q and I and adds the greater magnitude value to one half of the lesser value. This final mode is an approximation of the Pythagorean vector magnitude formula:

$$M = (X^2 + Y^2)^{1/2}$$

The TMC2220 contains a total of five pipeline registers plus the data and reference preload shift registers making the total delay six clock cycles. Instructions and data paths are pipelined so the instructions presented on a given clock cycle apply to the value entering registers A_i and B_i. Instructions RE, LM, LDR and AE, all of which enable registers or latches, must be set one cycle early (see timing diagram).

For the TMC2221, the correlation score of each module is passed unchanged (TC = LOW) or reduced by sixteen (TC = HIGH). Each module score is given a unity weighting then sent to the combining matrix where the four scores are added and output on the 8-bit data bus if $\overline{OEM}$ is LOW.

In magnitude mode (TC = LOW) and masking disabled, a perfect match between the data and reference will produce a correlation score of 128 (10000000_B) and correlation score of 0 shall indicate no matches (anti-correlation). In two's complement mode (TC = HIGH), perfect correlation will produce a score of 64 (01000000_B) and anti-correlation shall have an output of −64 (11000000_B). A total of five register delays plus the input register cause the result to be available on the sixth clock cycle after the loading of the input data.

Signal Definitions

Power

V_{DD}, GND — The TMC2220/TMC2221 operate from a single +5V power supply. All power and ground pins must be connected.

Inputs

AI_{1-4} — Each data input is a single-bit serial input to the A_i register of each correlator module.

BX_{1-4}, BY_{1-4} — The main, BX_i, and alternate, BY_i, reference preload inputs to the B_i register of each correlator module are selected by controls RE_{2-0}.

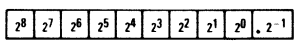
Outputs

AO_{1-4} — Each cascade data output is a single-bit serial output from the A_i register of each correlator module.

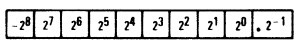
BO_{1-4} — Each cascade reference preload output is a single-bit serial output from the B_i register of each correlator module.

DM_{9-0} — The 10-bit main correlation output (TMC2220 only) is a combination of the four module output scores, Q_1, Q_2, I_3, I_4, which are dependent on the W_{2-0} weighted adder and C_{1-0} combining matrix controls. The main output port is enabled by $\overline{OEM}$.

The TMC2220 10-bit output format is:



if TC is LOW

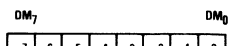


if TC is HIGH

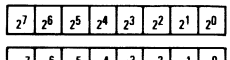
The TMC2221 has an 8-bit correlation output DM_{7-0} which always outputs the sum:

$$Q_1 + Q_2 + I_3 + I_4$$

Where each term is either unsigned magnitude or magnitude minus 16 depending on the TC control. The TMC2221 8-bit output format is:



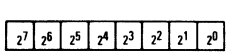
if TC is LOW



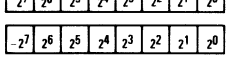
if TC is HIGH

DA_{7-0} — (TMC2220 only) The 8-bit auxiliary correlation output is the sum of two module output scores, I_3 and I_4, which are dependent on the W_{2-0} weighted adder controls. The auxiliary output port is enabled by $\overline{OEA}$.

The 8-bit binary output format is:



if TC is LOW



if TC is HIGH

G

Clocks

CLK — The clock for A_i data and B_i reference preload registers can be toggled at up to 20MHz. All registers are strobed on the rising edge of CLK and dependent on the registered enable controls, AE_i for the A_i registers, and RE_{2-0} for the B_i registers. The pipeline delay registers for the controls, W_{2-0}, C_{1-0} (TMC2220 only) and TC are also strobed on the rising edge of CLK.

Controls

AE_{1-4} — The clock enable for the four A_i data registers is a registered, active HIGH control. When AE_i is LOW on the previous cycle, no shifting of data occurs on A_i. AE_i is read on the rising edge of CLK, thus the shifting of data in A_i will occur on the next rising edge of CLK.

C_{1-0} — (TMC2220 only) These pipelined instructions select the function to be executed by the combining matrix and output through the main output port, DM_{9-0}.

LDR_{1-4} — The Load Reference control copies the contents of register B_i into latch R_i for correlation. If LDR_i was LOW on the previous clock cycle, the present contents of the latch remain in R_i. If LDR_i was HIGH, R_i is transparent and the B_i are values used in the current correlation.

LM — The Load Mask control allows the user to mask or select "no compare" bit positions in each channel. Inputs shifted into A_i and B_i produce a correlation pattern as the desired mask. Control LM must be HIGH on the previous cycle to track and LOW to store the pattern in the mask latches M_i. If no masking is required, LM is kept HIGH, making M_i transparent.

$\overline{OEA}$ — (TMC2220 only) The asynchronous output enable for the auxiliary output port, DA_{7-0}, is an active LOW control. When $\overline{OEA}$ is HIGH, the output is in a high-impedance state.

$\overline{OEM}$ — The asynchronous output enable for the main output port, DM_{9-0} (DM_{7-0} on the TMC2221), is an active LOW control. When $\overline{OEM}$ is HIGH, the output is in a high-impedance state.

RE_{2-0} — The encoded clock enable and load selector controls determine the various combinations of BX_i and BY_i reference inputs that may be selected for the four reference preload registers B_i. The B_i register clocks may also be selectively enabled. Like LDR, LM and AE_i, this control is delayed by one clock cycle. (RE_{2-1} used on the TMC2221 to select BX or BY.) See Table 1.

TC — The Two's Complement control forces the outputs of the four correlator modules to be unipolar (0 to 32) or bipolar (-16 to +16). When TC is LOW, the outputs of the correlator modules are passed unchanged to the weighting circuitry. When TC is HIGH, 16 is subtracted from each correlator output which is then interpreted as a two's complement value.

W_{2-0} — (TMC2220 only) The weighted adder controls determine the relative weightings of the four correlation module scores.

TMC2220 Package Interconnections

Signal Type	Signal Name	Function	G8, H8 Package Pins
Power	V_{DD}	Supply Voltage	F2, L2, B11, A8
	GND	Ground	K2, K3, G11, F11, A2
Inputs	AI_{1-4}	Data Input	H10, K11, D10, C11
	BX_{1-4}	Main Reference Preload	G10, J11, E11, C10
	BY_{1-4}	Alternate Reference Preload	H11, J10, E10, D11
Outputs	AO_{1-4}	Data Output	J2, K1, B6, B7
	BO_{1-4}	Reference Preload Output	H1, J1, A6, A7
	DM_{9-0}	Main Port	H2, G1, G2, F1, E1, E2, D1, D2, C1, C2
	DA_{7-0}	Auxiliary Port	B5, A5, B4, A4, B3, A3, B2, B1
Clock	CLK	Master Clock	F10
Controls	AE_{1-4}	Register Clock Enable	K8, K9, A9, A10
	C_{1-0}	Combining Matrix	L5, K6
	LDR_{1-4}	Reference Load	L7, L8, B9, B10
	LM	Mask Load	K7
	$\overline{OEA}$	Auxiliary Port Output Enable	B8
	$\overline{OEM}$	Main Port Output Enable	L3
	RE_{2-0}	Reference Load Select	K10, L10, L9
	TC	Two's Complement	L6
	W_{2-0}	Module Weighting Factor	K4, L4, K5

TMC2221 Package Interconnections

Signal Type	Signal Name	Function	B6 Package
Power	V_{DD}	Supply Voltage	11, 22,
	GND	Ground	4, 7, 24, 25
Inputs	AI	Data Input	6
	BX	Main Reference Preload	10
	BY	Alternate Reference Preload	9
Outputs	AO	Data Output	12
	BO	Reference Preload Output	13
	DM_{7-0}	Main Port	23, 21, 20, 19, 18, 17, 16, 15
Clock	CLK	Master Clock	8
Controls	AE	Register Clock Enable	2
	LDR	Reference Load	1
	LM	Mask Load	28
	$\overline{OEM}$	Port Output Enable	26
	RE_{2-1}	Reference Load Select	5, 3
	TC	Two's Complement	27
No Connection	NC		14

Table 1. Reference Preload Register Input and Enable Operation

RE_i Controls	Selected Reference Port (TMC2220)				Selected Reference Port (TMC2221)
RE_{2-0}	1	2	3	4	
000	Dis	Dis	Dis	Dis	Dis
001	Dis	Dis	Dis	BX_4	
010	Dis	Dis	BY_3	BX_4	BY
011	Dis	Dis	BY_3	BY_4	
100	BX_1	BX_2	BX_3	BX_4	BX
101	BY_1	BX_2	BX_3	BX_4	
110	BY_1	BX_2	BY_3	BX_4	BY
111	BY_1	BY_2	BY_3	BY_4	

Notes:

1. Dis = B_i register disabled (hold mode).
2. LSB (RE_0) not used on the TMC2221.

Table 2. Module Weighting Factor Operation (TMC2220 Only)

W_i Controls W_{2-0}	Internal Channel Configuration	
	Q	I
000	$Q_1 + Q_2$	$I_3 + I_4$
001	$3Q_1 + Q_2$	$3I_3 + I_4$
010	$4Q_1 + Q_2$	$4I_3 + I_4$
011	Q_2	I_4
100	Q_1	I_3
101	$3Q_1 + 2Q_2$	$3I_3 + 2I_4$
110	$4Q_1 + 2Q_2$	$4I_3 + 2I_4$
111	$5Q_1 + 2Q_2$	$5I_3 + 2I_4$

Table 3. Combining Matrix Operation (TMC2220 Only)

C_i Controls C_{1-0}	Main Output Port Function DM_{9-0}
00	Q
01	Q + I/2
10	Q + I
11	Max (|Q|, |I|) + 1/2 Min (|Q|, |I|)[1]

Notes:

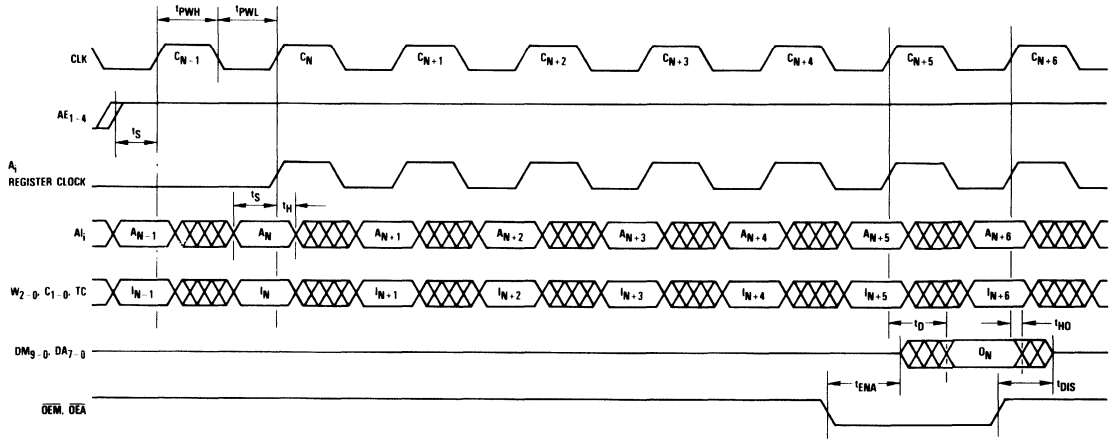
1. The larger magnitude value of Q or I plus one-half of the smaller magnitude value.
2. The TMC2221 always outputs the sum $Q_1 + Q_2 + I_3 + I_4$.

Sliding Correlation Timing

The TMC2220 and TMC2221 have a six register pipeline. There are registers for the input data and reference, parallel counter, weighting circuitry, combining matrix, and output. CLK is used to load all A_i, B_i and instruction pipeline registers. With the register controls enabled, a data or reference word is loaded into its respective A_i or B_i register on every rising edge of CLK. Data A_N enters register A_i on the rising edge of clock C_N. The reference latch is static if the previous LDR_i was LOW or tracks B_i if LDR_i was HIGH. If reference preload is not desired, holding control LDR_i HIGH makes latch R_i transparent and direct correlation between A_i and B_i occurs. Data is valid if present at the input for a setup time t_S before and a hold time t_H after the rising clock edge. Setup and hold time requirements also apply to instructions and controls, however, AE, LDR, LM and RE must be valid one cycle before taking effect.

Because of the six internal pipeline delays, the correlation score for a given set of A_i and B_i register contents appears at the output ports six clock cycles plus an output delay t_D later. When the main and auxiliary (TMC2220 only) output ports are enabled ($\overline{OEM}$ = LOW and $\overline{OEA}$ = LOW), the correlation score O_N of data window A_{N-31} through A_N is output after rising clock edge C_{N+5} (A_{N-127} through A_N on the TMC2221). Instructions TC, W and C are registered and pipelined so that the instructions will be aligned with the data. The instructions I_N (see timing diagram) which are loaded on rising clock edge C_N apply to a correlation between data and reference words N-31 (N-127) through N. Masking is assumed to be preset (previous LM = LOW) or unused (previous LM = HIGH). The same timing applies if the reference is shifting and data is fixed.

Figure 1. Sliding Correlation Timing



Reference Register Load Timing

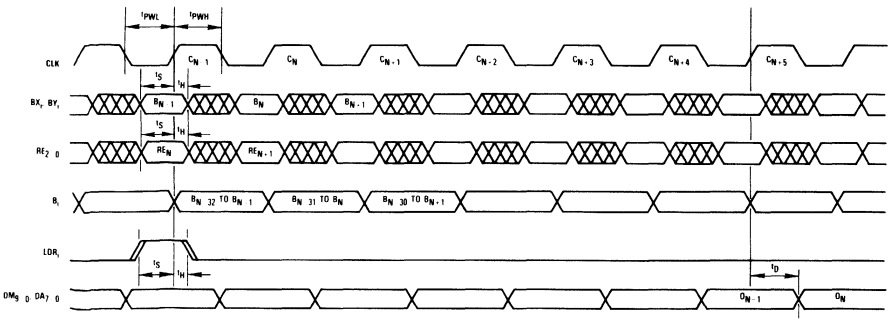
The HIGH on LDR_i transfers the contents of B_i in parallel into R_i in the next clock period. R_i tracks B_i when control LDR_i is HIGH and holds when LDR_i is LOW. N rising edges of CLK are required to load N reference words into the reference preload register B_i. The rising edge of clock C_N loads reference word B_N so that B_i contains words B_{N-31} through B_N.

Figure 2 illustrates the LDR_i instruction timing to transfer reference window B_{N-31} through B_N into the reference latch. With this timing, correlation against the old reference pattern is preserved during the "LDR" clock cycle and that correlation against the new reference pattern B_{N-31} to B_N should commence immediately after the "LDR" clock cycle. The user must meet the normal input setup and hold time requirements and setup the instruction one clock cycle before the desired transfer.

A completely new reference can be loaded into latch R on every 32nd clock cycle. With the output ports enabled, the correlation score O_N (correlation between data A_{N-31} through A_N and reference B_{N-31} through B_N) is available an output delay t_D after the rising edge of clock C_{N+5} because of the six register pipeline.

Operation of the TMC2221 is similar to the operation described for the TMC2220 except the length of the reference word is 128 bits rather than 32. The reference register will therefore contain the pattern B_{N-127} through B_N, and correlation occurs between this reference and data A_{N-127} through A_N. A new reference word therefore requires 128 clock cycles to completely load the new value. With the output ports enabled, the correlation score O_N (correlation between data A_{N-127} through A_N and reference B_{N-127} through B_N) is available an output delay t_D after the rising edge of clock C_{N+5}.

Figure 2. Reference Latch Load Timing

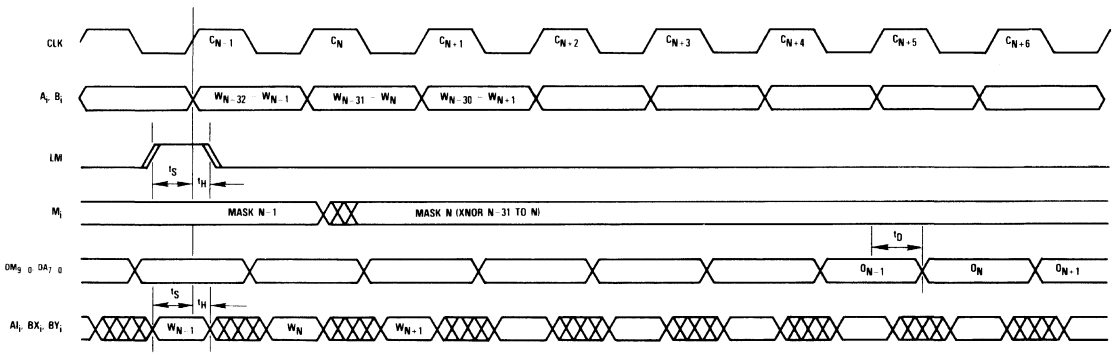


Mask Register Loading

Control LM latches a mask pattern into M_i which selectively disables word positions in each correlator module. Masking latch M_i tracks the XNOR output if, on the the previous clock cycle, LM was HIGH and holds if LM was LOW. Figure 3 illustrates the TMC2220 LM timing to latch a mask generated by the exclusive NOR of A_{N-31} through A_N with R_{N-31} through R_N. LM must be set HIGH t_S before the rising edge of clock C_{N-1} to load the mask for A_{N-31} thru A_N. LM must be set LOW before the next rising edge of C_N to ensure words N–31 to N remain latched as the mask pattern. A completely new mask may be loaded on every 32nd clock cycle. However, to permit time for data and reference loading, mask loading is generally limited to every 64th clock cycle. The first correlation score which reflects mask N is output t_D after the rising edge of clock cycle C_{N+6}.

Operation of the TMC2221 is similar that of the TMC2220 but requires 128 clock cycles to completely load a new mask pattern. To permit time to load new data and a new reference pattern once the mask is loaded, an additional 128 clock cycles is required. Therefore, mask loading is generally limited to every 256 clock cycles in the TMC2221. The mask pattern loaded will be the exclusive–NOR of A_{N-127} through A_N with R_{N-127} through R_N.

Figure 3. Masking Latch Load Timing



Applications Discussion

The TMC2220 architecture provides the flexibility for a number of configurations. The cascade outputs and the internal weighting and adder logic allow a single TMC2220 to be configured as four independent 32-bit correlators, independent 96-bit and 32-bit correlators, two independent 64-bit correlators, or as a single 128 x 1 correlator. The TMC2220 may also be cascaded serially or in parallel to increase the length or width of correlation.

To increase the correlation length in a single TMC2220 system, the cascade outputs of a module (AO_i, BO_i) can be connected to the inputs of the next module (AI_{i+1}, BI_{i+1}). When using this configuration, the input enables and load controls should be connected together. Figure 4 shows the configuration for a dual 64 x 1 correlation. In this application, the outputs of module 1 are connected to the inputs of module 2 and the outputs of module 3 are connected to the inputs of module 4. The weighting logic is set for 1:1 weighting and the combining logic is set to output $Q_1 + Q_2$ on the main output DM_{9-0}, and $I_3 + I_4$ on the auxiliary output DA_{7-0}.

Figure 4. Dual 64 x 1 Configuration

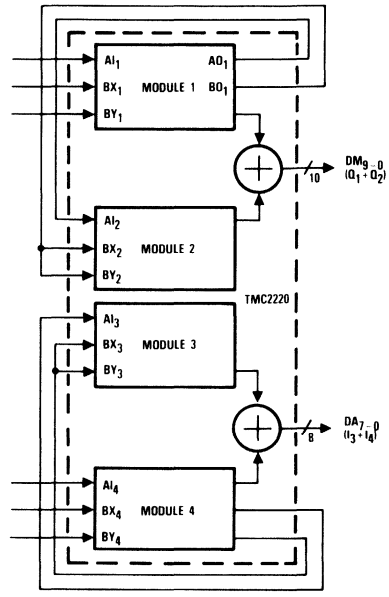


Figure 5. Cascading the TMC2220 for Extended-Length Correlation

Figure 5 shows an example of multi-bit correlation with extended length. This example shows 4-bit correlation with a length of 64-bits. The outputs of the two TMC2220s must be externally added to obtain the 64-bit correlation score. The weighting and combining of the module correlation scores should be set as required by the application.

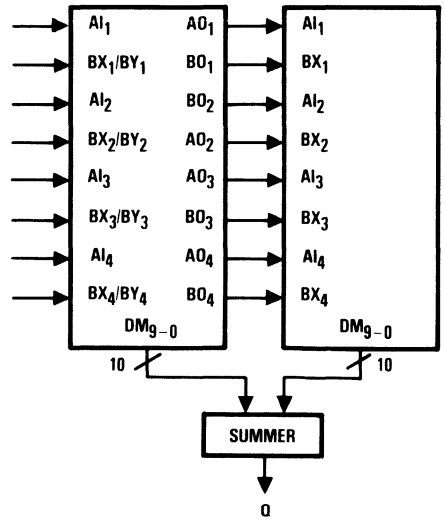


Figure 6. 8-Bit Correlation with the TMC2220

Figure 6 shows an example of 8-bit, two's complement correlation. Two TMC2220s are used in parallel and externally summed to obtain the properly weighted correlation score. To obtain a properly weighted correlation score, each bit of the output must be multiplied by an appropriate binary scaling factor. The 8-bit data input and reference are connected as shown. The weighting control of each TMC2220 is set for 4:1 weighting (W_{2-0} = 010). This multiplies the upper two bits of each TMC2220 by a factor of 4 (Q_1, I_3). The next step is to multiply the 2nd and 4th bits (Q_2, I_4) by a factor of 2. An equivalent operation is to divide the 1st and 3rd bits by 2. This operation is accomplished by setting the combining logic to output the sum Q + I/2 (C_{1-0} = 01). The final output of each TMC2220 will be equivalent to:

$$DM_{9-0} = (4 \times Q_1) + (2 \times I_3) + (1 \times Q_2) + (1/2 \times I_4)$$

Setting the weighting and combining controls as described will produce a correlation score with each bit properly weighted based on its 4-bit binary position. The final step is to multiply the correlation output of the most-significant TMC2220 (bits 7-4) by a factor of 16 then combine the outputs of the two TMC2220s. This is done using external adder circuitry. Multiplication is performed by simply shifting the output lines of the upper TMC2220 by four places at the input to the adder logic. The output of the summer, therefore, shall give the binary weighted correlation score of a quantized 8-bit input. The same circuit can be used with unsigned data if the inverter on the most-significant-bit of the reference input is omitted.

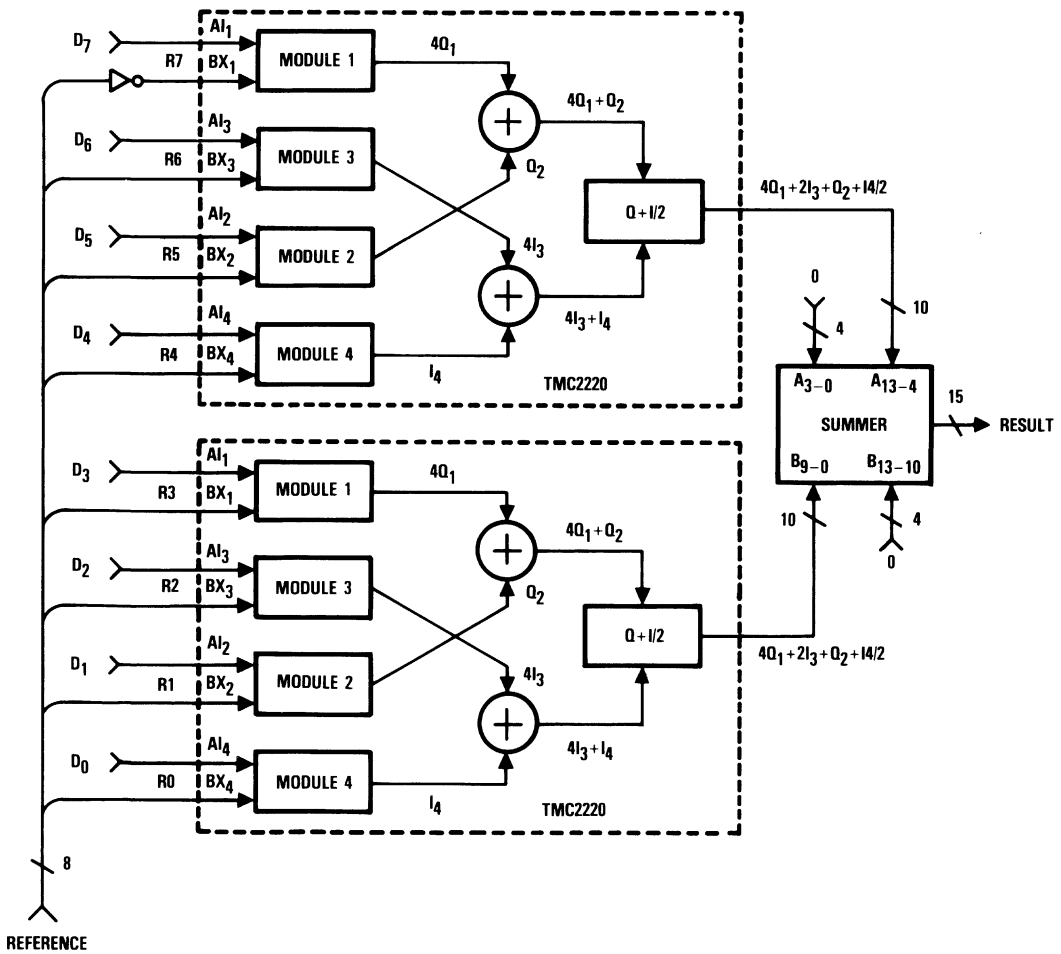
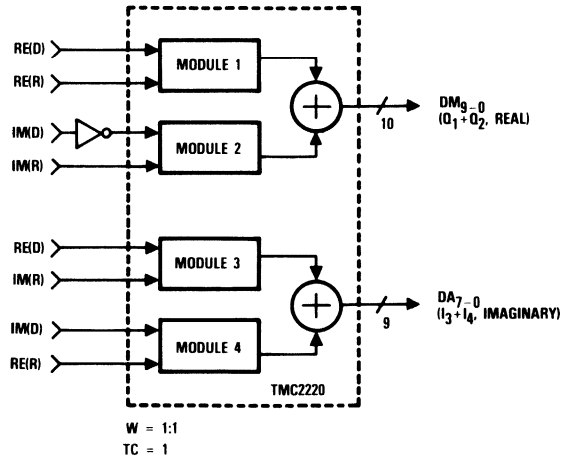


Figure 7. Full Complex Correlation with the TMC2220

Figure 7 is an example of full complex correlation. In this example, separate real and imaginary terms are multiplied and summed internally to provide a real and imaginary result. This method preserves the phase information of the input. Inputs are connected as shown in the figure. The imaginary term in Im(D) x Im(R) is negated (inverted) for proper sign in the summation. The TMC2220 is set for 1:1 ($Q_1 + Q_2$, $I_3 + I_4$) weighting, two's complement mode, and the combining control is set to output Q on the main output and I on the auxiliary output. All 32 internal taps are used.



A simple example would be to find a sine wave in a demodulated data stream. The references would be set to:

$$Re(R) = Cos(\omega t) \text{ and } Im(R) = Sin(\omega t)$$

where, ω is the modulation frequency. Each term is set to:

1 for positive and 0 for negative

The data inputs are set to:

$$Re(D) = data_{in} \times Cos(ft) \text{ and } Im(D) = data_{in} \times Sin(ft)$$

where, f is the mixer or carrier frequency.

G

Figure 8. Complex Correlation with Magnitude Result

Figure 8 is similar to full complex correlation, however, in this example the output is magnitude only. This application is used when the phase relationship is not required. The inputs are connected as in the previous example, however, rather than a full complex output, the outputs are combined internally to:

$$\text{Max}(|Q|, |I|) + 1/2 \text{ Min}(|Q|, |I|)$$

(C_{1-0} = 11) to obtain the approximate magnitude output. Multiplying the output by 15/16 will reduce the error in the magnitude approximation.

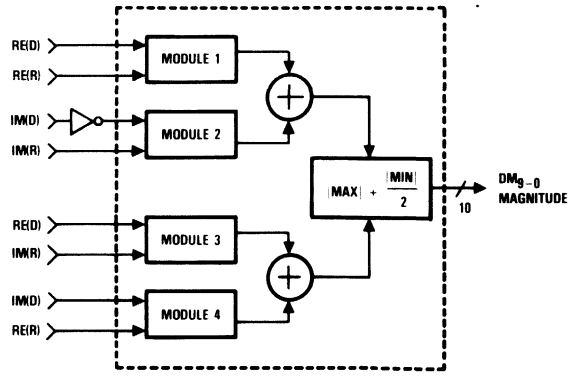


Figure 9. Cascading the TMC2221 for Extended-Length Correlation

The TMC2221 can be cascaded to implement correlations of more than 128-bits. Typically all clocks, reference inputs and enables are connected together and the A and B outputs of preceding stages are connected to the respective inputs of subsequent stages. An external summer is required to generate the composite correlation score.

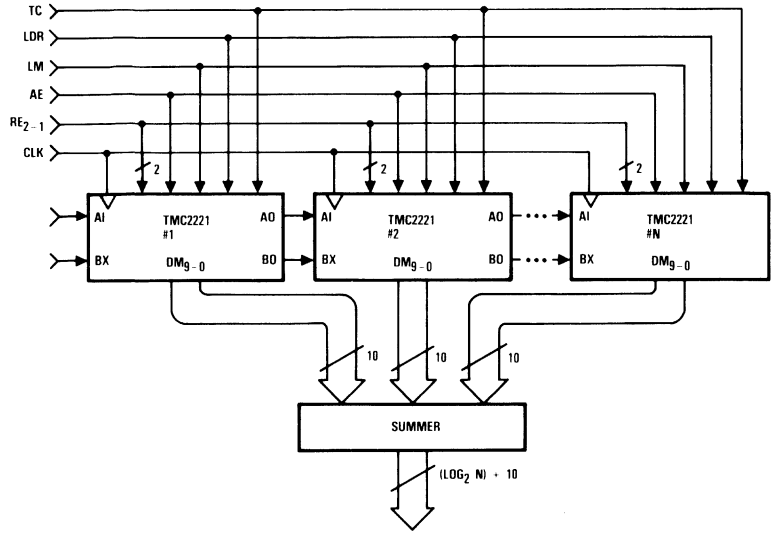


Figure 10. Multi-Bit x 1 Bit Correlation

The TMC2221 may also be used to compare multi-bit words with a single-bit reference. When this is done, the output of each TMC2221 must be appropriately weighted to the adder circuitry. The weighting reflects the relative importance of the different bit positions. Weighting can normally be accomplished by simple bit shifts at the input to the summer.

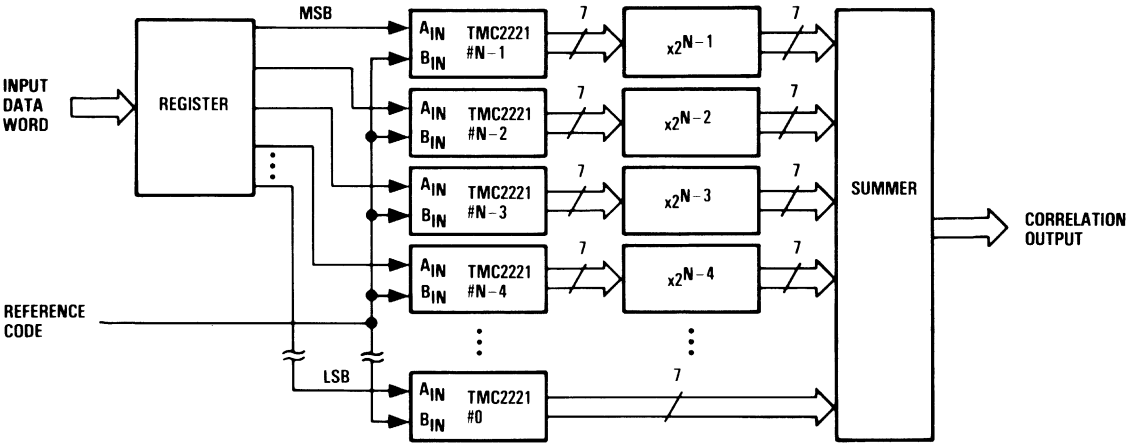


Figure 11. Equivalent Input Circuit

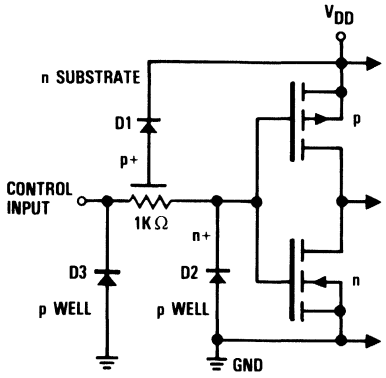


Figure 12. Equivalent Output Circuit

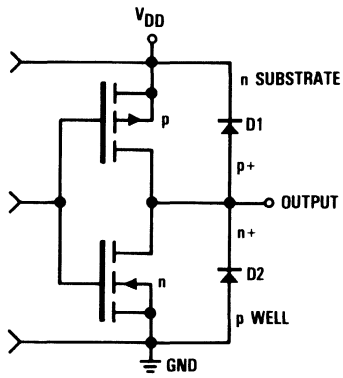
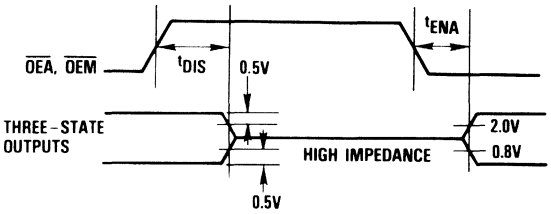


Figure 13. Threshold Levels for Three-State Measurements



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Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} +0.5V)
Output	
Applied voltage [2]	−0.5 to (V_{DD} +0.5V)
Forced current [3,4]	−1.0 to +6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			-2.0			-2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				-55		125	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V, $\overline{OEM}$, $\overline{OEA}$ = 5V		10		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz, $\overline{OEM}$, $\overline{OEA}$ = 5V		70		80	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	-40		-40		μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		+40		+40	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V	-40		-40		μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		+40		+40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		-150		-150	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note:

1. Actual test conditions may vary from those shown, but guarantee operation as specified

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range								Units
			Standard				Extended				
			-1				-1				
			Min	Max	Min	Max	Min	Max	Min	Max	
F_C	Clock (Correlation) Rate	V_{DD}=Min		20		17		20		17	MHz
t_{PWL}	Clock Pulse Width, LOW	V_{DD}=Min	25		30		25		30		ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD}=Min	15		15		15		15		ns
t_S	Input Setup Time		15		15		17		17		ns
t_H	Input Hold Time		0		0		0		0		ns
t_D	Output Delay	V_{DD}=Min, C_{LOAD}=40pF		25		25		25		25	ns
t_{HO}	Output Hold Time	V_{DD}=Max, C_{LOAD}=40pF	3		3		3		3		ns
t_{ENA}	Three-State Output Enable Delay [1]	V_{DD}=Min, C_{LOAD}=40pF		17		17		17		17	ns
t_{DIS}	Three-State Output Disable Delay [1]	V_{DD}=Min, C_{LOAD}=40pF		22		22		22		22	ns

Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2220G8C	STD – T_A=0°C to 70°C	Commercial, 17MHz	68 Pin Grid Array	2220G8C
TMC2220G8V	EXT – T_C= –55°C to 125°C	MIL-STD-883, 17MHz	68 Pin Grid Array	2220G8V
TMC2220G8C1	STD – T_A=0°C to 70°C	Commercial, 20MHz	68 Pin Grid Array	2220G8C1
TMC2220G8V1	EXT – T_C= –55°C to 125°C	MIL-STD-883, 20MHz	68 Pin Grid Array	2220G8V1
TMC2220H8C	STD – T_A=0°C to 70°C	Commercial, 17MHz	69 Pin Plastic Pin Grid Array	2220H8C
TMC2220H8C1	STD – T_A=0°C to 70°C	Commercial, 20MHz	69 Pin Plastic Pin Grid Array	2220H8C1
TMC2221B6C	STD – T_A=0°C to 70°C	Commercial, 17MHz	28 Pin CERDIP	2221B6C
TMC2221B6V	EXT – T_C= –55°C to 125°C	MIL-STD-883, 17MHz	28 Pin CERDIP	2221B6V
TMC2221B6C1	STD – T_A=0°C to 70°C	Commercial, 20MHz	28 Pin CERDIP	2221B6C1
TMC2221B6V1	EXT – T_C= –55°C to 125°C	MIL-STD-883, 20MHz	28 Pin CERDIP	2221B6V1

Vector Arithmetic/Filters

Vector processing, also know as systolic processing, operates in parallel on an array of data, or on a data stream. Very high processing throughput rates are thus achieved.

TRW's vector processors include FIR filters (the TDC1028, TMC2242, and TMC2243), which all operate at video word rates. The TMC2246 Image Filter supports fast pixel manipulation of a 1 or 2-dimensional picture. The TMC2249 is ideal for mixing two digital video streams, while the TMC2250 and TMC2255 perform high-speed matrix multiplication and convolution.

Vector Arithmetic/Filters

Product	Description	Size	Clock Rate [1] (MHz)	Power [1] (Watts)	Package		Grades [2]	Notes	Page
TMC1028	Digital FIR Filter	4 x 4 x 8	10	3.7	J4	48 Pin DIP	C, A	Cascadeable.	H3
TMC2242-1	Half-Band Digital Filter	12/16-Bit	40	0.5	R2	44 Lead PLCC	C	2:1 Interpolate or Decimate.	H15
-			30	0.5	R2	44 Lead PLCC	C	Low-Pass ($-6dB@0.25F_S$)	
TMC2243	Video Filter	10 x 10 x 3	20	0.5	G8	69 Pin PGA	C, V	Cascadeable.	H29
					H8	69 Pin PPGA	C		
TMC2246-1	Image Filter	10 x 11 Bit	40	0.5	H5	121 Pin PPGA	C	Four-Pixel Interpolator.	H43
					L5	132 Lead CERQUAD	V		
-			30	0.5	H5	121 Pin PPGA	C		
					L5	132 Lead CERQUAD	V		
TMC2249-1	Digital Mixer	12 x 12 x 2	30	0.5	H5	121 Pin PPGA	C	Cascadeable.	H55
					L5	132 Lead CERQUAD	V	Programmable Delays.	
-			25	0.5	H5	121 Pin PPGA	C		
					L5	132 Lead CERQUAD	V		
TMC2250-2	Matrix Multiplier	12 x 10 x 9	40	1.2	H5	121 Pin PPGA	C	2D Convolution 3 x 3, 2 x 4.	H69
-1			36	1.2	H5	121 Pin PPGA	C	1D Convolution, 9 Taps.	
					G1	121 Pin PGA	V	3 x 3 Matrix x 3 x 1 Vector.	
-			30	1.2	H5	121 Pin PPGA	C		
					G1	121 Pin PGA	V		
TMC2255-1	2D Convolver	5 x 5 x 8-Bit	12.5	0.6	R1	68 Lead PLCC	C	3 x 3, Symmetric 5 x 5	H89
-			10	0.6	R1	68 Lead PLCC	C	2D Convolver.	

Notes: 1. Guaranteed. See product specifications for test conditions.

2. A = High Reliability, $T_C = -55°C$ to $125°C$.
C = Commercial, $T_A = 0°C$ to $70°C$.
V = MIL-STD-883 Compliant, $T_C = -55°C$ to $125°C$

TDC1028

Digital FIR Filter
Building Block, 10MHz

The TDC1028 is a video-speed, TTL compatible bit-slice building block for Finite Impulse Response (FIR) digital filters and multi-bit digital correlators. It is used independently in the coefficient and signal data word dimensions as a bit-slice processor. Word lengths can be multiples of four bits. Two's complement or unsigned magnitude operation is independently selectable for both coefficients and signal data words.

The TDC1028 provides eight delay stages, eight multipliers, and eight adders in a single integrated circuit. Eight coefficient storage registers are also provided for ease in programming filter characteristics and to make correlation possible. One coefficient may be changed every clock cycle. The delay registers and the adder pipeline registers have been merged for efficiency.

Features

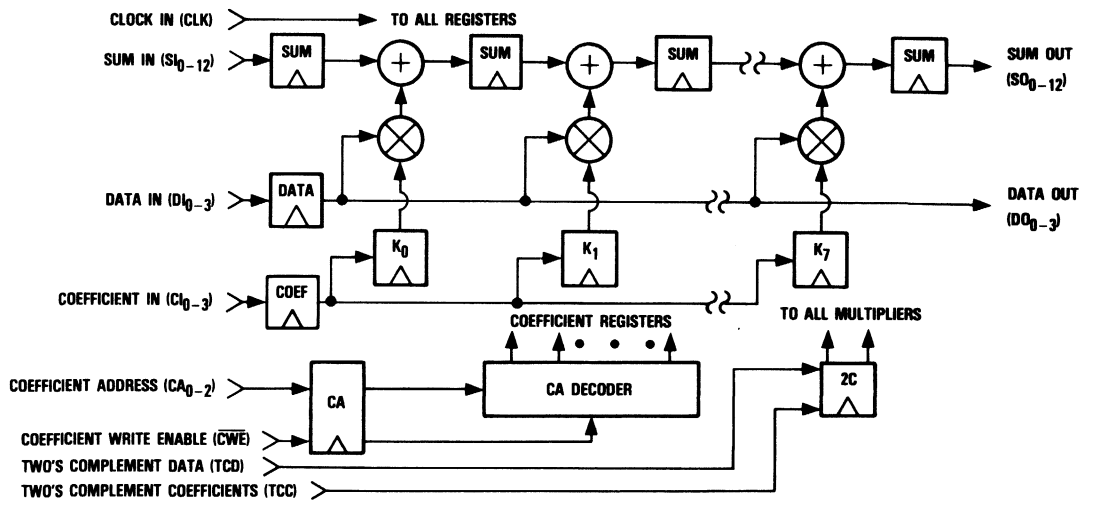
- 10MHz Throughput Rate
- Eight Coefficients
- Cascadable (To > 36 Taps) Without External Components
- 4-Bit Coefficient And Signal Data Words
- Independently Expandable Coefficient And Signal Word Length
- Independently Selectable Format For Coefficients And Signal Data Words (Two's Complement Or Unsigned Magnitude)
- Available In A 48 Pin Hermetic Ceramic DIP Package
- Radiation Hard Bipolar Process
- Single +5V Power Supply
- TTL Compatible

Applications

- Digital Video Filters
- Matched Filters
- Pulse Compression
- Multi-Bit Correlation
- Waveform Synthesis
- Adaptive Filters

H

Functional Block Diagram



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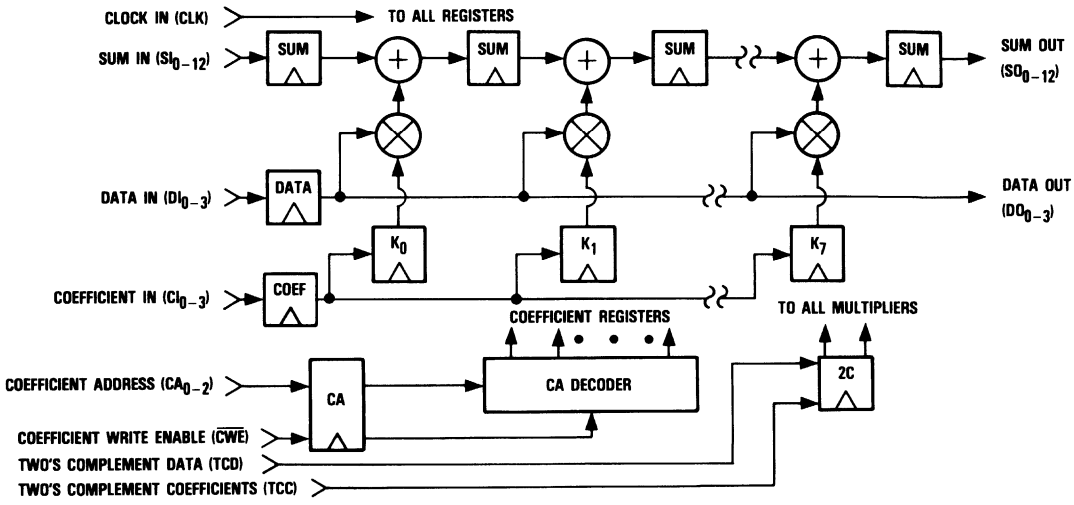
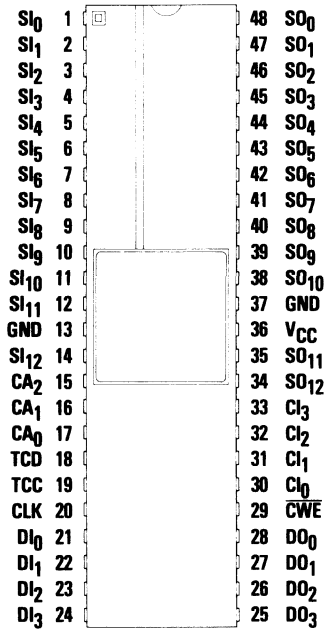
Functional Block Diagram



Pin Assignments



48 Lead DIP - J4 Package

Functional Description

General Information

The TDC1028 has four internal functions: delay, multiplication, addition, and coefficient storage. These functions are connected to form a building block for finite impulse response filters or correlators. Cascading inputs are provided to allow the construction of filters or correlators of arbitrary length. The basic word size for coefficients and data is four bits. The order of the operations has been changed from the canonical form to permit the merging of delay and pipelining registers (see Figure 1).

Power

The TDC1028 operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J4 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 36
GND	Ground	0.0V	Pins 13,37

Inputs

The TDC1028 has three types of inputs: signal data, coefficients, and sum (cascading) inputs.

Name	Function	Value	J4 Package
DI_3	Signal Data Input MSB	TTL	Pin 24
DI_2		TTL	Pin 23
DI_1		TTL	Pin 22
DI_0	Signal Data Input LSB	TTL	Pin 21
CI_3	Coefficient Input MSB	TTL	Pin 33
CI_2		TTL	Pin 32
CI_1		TTL	Pin 31
CI_0	Coefficient Input LSB	TTL	Pin 30
SI_{12}	Cascading Sum Input MSB	TTL	Pin 14
SI_{11}		TTL	Pin 12
SI_{10}		TTL	Pin 11
SI_9		TTL	Pin 10
SI_8		TTL	Pin 9
SI_7		TTL	Pin 8
SI_6		TTL	Pin 7
SI_5		TTL	Pin 6
SI_4		TTL	Pin 5
SI_3		TTL	Pin 4
SI_2		TTL	Pin 3
SI_1		TTL	Pin 2
SI_0	Cascading Sum Input LSB	TTL	Pin 1

Data Outputs

The TDC1028 has two outputs: a sum output and a data output. The data output is used to connect one TDC1028 to the next (cascading) for greater filter or correlation length. The sum output is used both for cascading and signal output.

Name	Function	Value	J4 Package
SO_{12}	Sum Output MSB	TTL	Pin 34
SO_{11}		TTL	Pin 35
SO_{10}		TTL	Pin 38
SO_9		TTL	Pin 39
SO_8		TTL	Pin 40
SO_7		TTL	Pin 41
SO_6		TTL	Pin 42
SO_5		TTL	Pin 43
SO_4		TTL	Pin 44
SO_3		TTL	Pin 45
SO_2		TTL	Pin 46
SO_1		TTL	Pin 47
SO_0	Sum Output LSB	TTL	Pin 48
DO_3	Data Output MSB	TTL	Pin 25
DO_2		TTL	Pin 26
DO_1		TTL	Pin 27
DO_0	Data Output LSB	TTL	Pin 28

Clocks

The TDC1028 operates synchronously from a single master clock, which can be clocked at up to 10MHz. All internal circuitry is static; there is no minimum clock frequency required. The rising edge of CLK latches the Coefficient Input (CI_{3-0}), the Coefficient Address (CA_{2-0}), and the Coefficient Write Enable control ($\overline{CWE}$). If $\overline{CWE}$ is LOW, a new coefficient will be loaded into the selected coefficient register at the next rising edge of CLK, as shown in Figure 4.

Name	Function	Value	J4 Package
CLK	Clock	TTL	Pin 20

Controls

The TDC1028 has six control inputs. TCC and TCD control the interpretation of the data and coefficients as two's complement or unsigned magnitude numbers. These inputs provide two's complement operation for the respective input when a logic HIGH is applied, and unsigned magnitude operation when a logic LOW is applied. One active LOW input ($\overline{CWE}$) controls the writing of a coefficient, and three inputs (CA_{2-0}) control the selection of which coefficient is to be written.

Name	Function	Value	J4 Package
TCC	Two's Complement Coefficients	TTL	Pin 19
TCD	Two's Complement Data	TTL	Pin 18
$\overline{CWE}$	Coefficient Write Enable	TTL	Pin 29
CA_2	Coefficient Address MSB	TTL	Pin 15
CA_1		TTL	Pin 16
CA_0	Coefficient Address LSB	TTL	Pin 17

Figure 1.

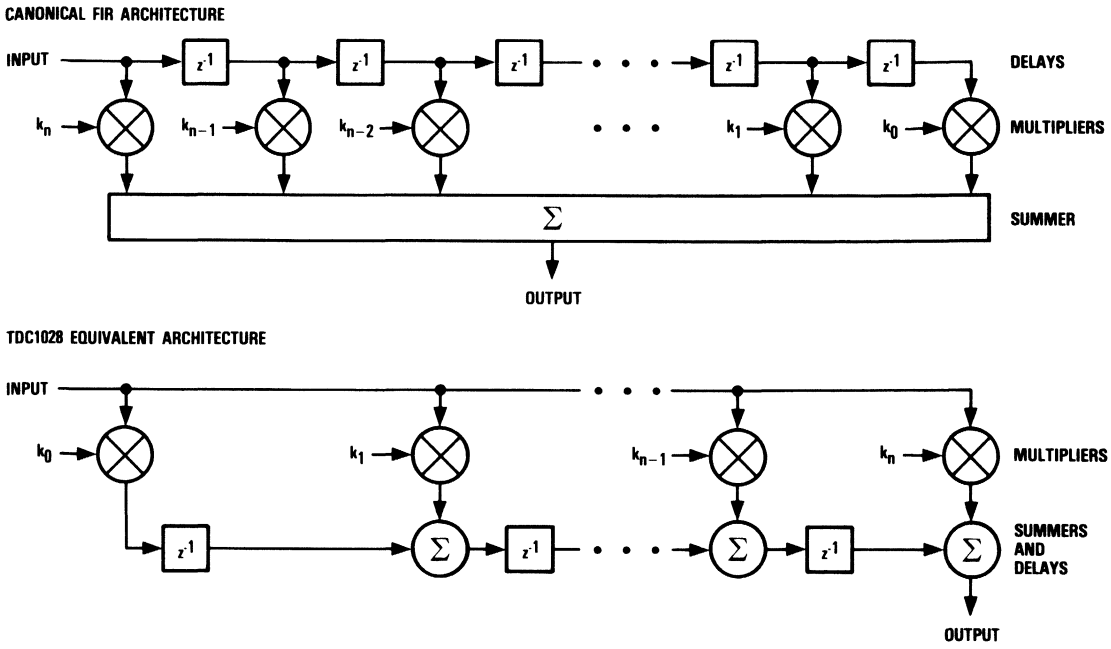


Figure 2.

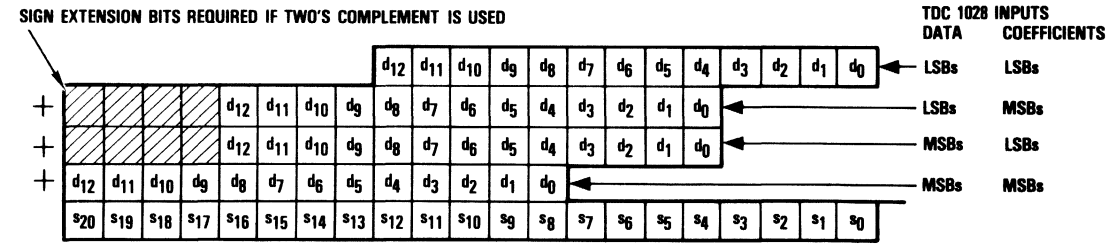


Figure 3.

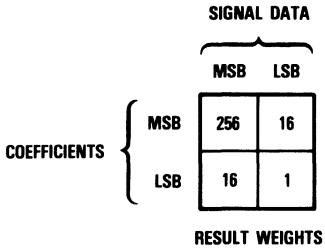


Figure 4.

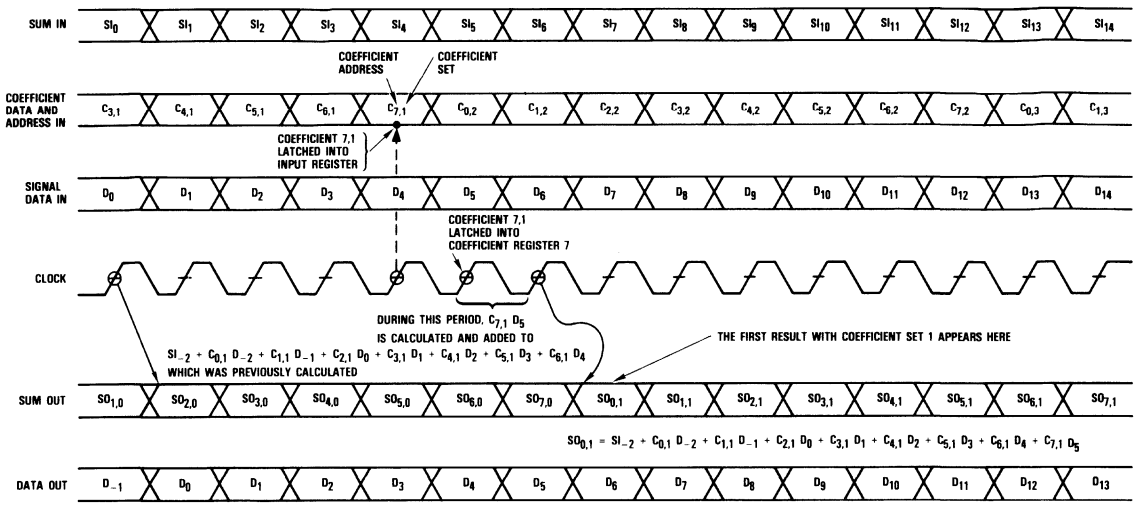


Figure 5.

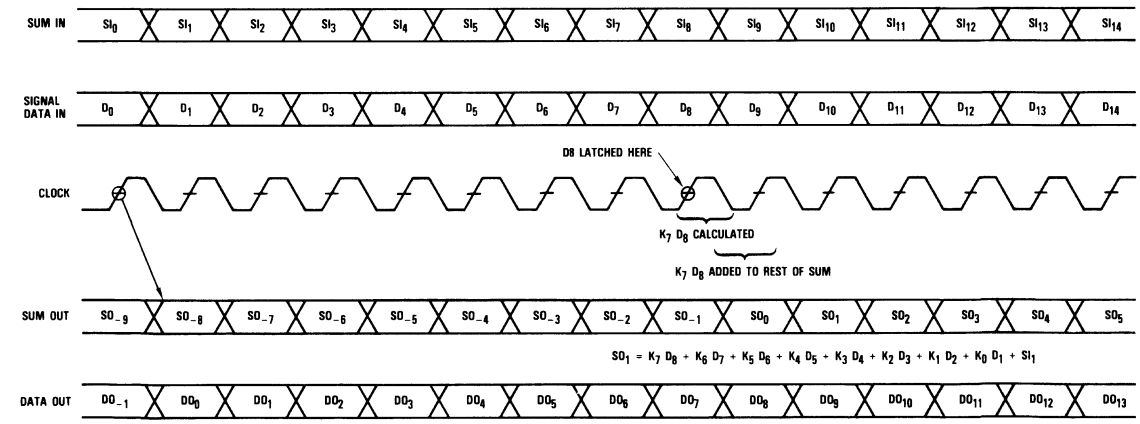


Figure 6. Equivalent Input Circuit

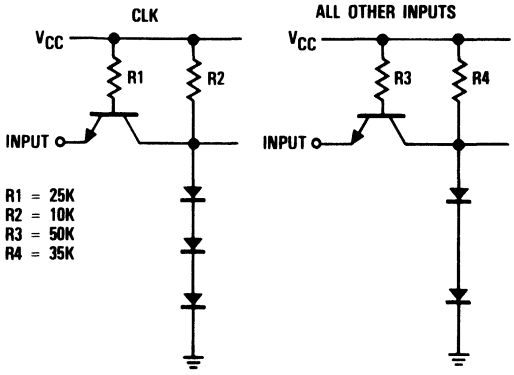


Figure 7. Equivalent Output Circuit

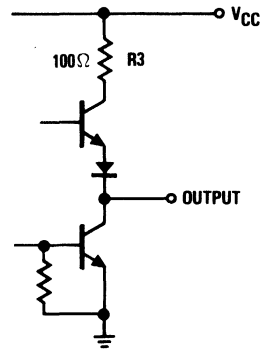
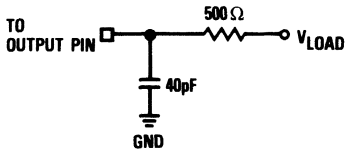


Figure 8. Test Load



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Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage (measured to D_{GND})	−0.5 to +5.5V [2]
Applied current, externally forced	−1.0 to +6.0mA [3,4]
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−55 to +125°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to 150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	41			65			ns
t_{PWH}	Clock Pulse Width, HIGH	55			65			ns
t_{CY}	Clock Cycle Time	100			135			ns
t_S	Input Setup Time							
	Data In, Sum In	15			15			ns
	Coefficient In, Coefficient Address In	25			25			ns
	Coefficient Write Enable	30			30			ns
t_H	Input Hold Time (All inputs)	5			5			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = Max, Static					
		T_A = 0°C to 70°C		700			mA
		T_A = 70°C		550			mA
		T_C = −55°C to 125°C				900	mA
		T_C = 125°C				500	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.4V					
		Data Inputs		−0.4		−0.4	mA
		Clock Input		−1.0		−1.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V					
		Data Inputs		75		75	μA
		Clock Input		75		75	μA
I_I	Input Current, Max Input Voltage	V_{CC} = Max, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{OS}	Short-Circuit Output Current	V_{CC} = Max, Output HIGH, one pin to ground, one second duration		−50		−50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

H

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{CY}	Cycle Time	V_{CC} = Min		100		135	ns
t_D	Output Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		30		35	ns

Note:

1. All transitions are measured at a 1.5V level.

Application Notes

More than one TDC1028 may be connected together to form filters of greater length, greater signal data resolution, and/or greater coefficient resolution.

The simplest form of expansion is length. Each TDC1028 has a data and a sum input, and a data and a sum output. To make a filter of greater length, connect the data and sum outputs to the data and sum inputs of the next device, as shown in Figures 2 and 3. This procedure is used for each section of a filter built with higher resolution for signal data and coefficients. Note that the sum inputs of the first device in a series (the one to which signal data is directly applied) must be supplied with a "zero" input (that is, all sum input pins must be grounded). This form of expansion is also used in combination with increased resolution, and is directly applicable to those cases.

Two options are available for increased resolution. The first method uses external adders and pipeline registers, the second uses the internal adders and pipeline registers of the TDC1028. Block diagrams of these methods are shown in Figures 9 and 10. The second method significantly increases latency; the output experiences a significant delay with respect to that of an ideal but causal Finite Impulse Response filter.

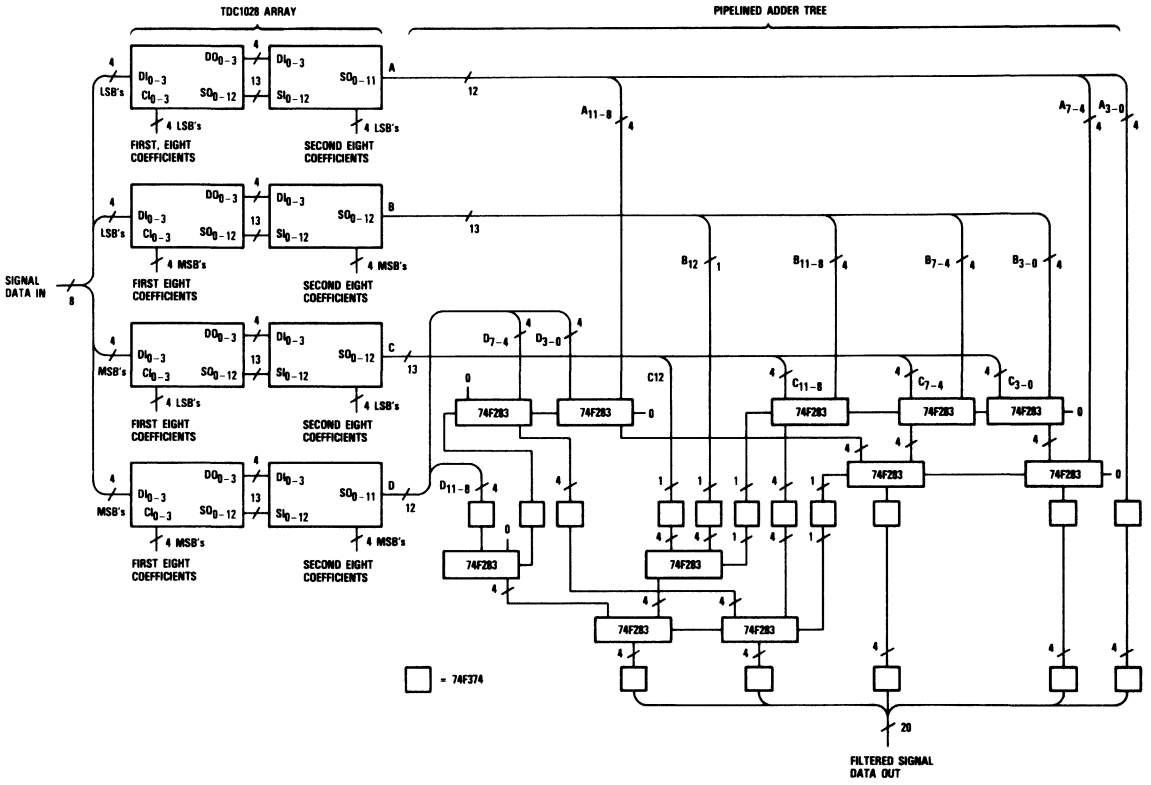
This section discusses the increasing of signal data and coefficient resolution when both signal data and coefficients are given in two's complement notation. For additional information, refer to TRW LSI Products Application Note TP-22.

The basic approach is to divide the word that requires greater resolution into two or more parts of four bits each. A separate section will be needed for every four bits or fraction thereof. Usually, both signal data words and coefficients will be divided. Next, a filter section is assigned to each possible combination of non-overlapping 4-bit groups of signal data with 4-bit groups of coefficients. (A filter section is assigned for each element in the cross-product of the signal data and coefficient data word spaces.) This process is shown in Figure 3, which illustrates division into 4-bit segments, used with both options for increasing resolution.

The choice is made between the adder option and the no-adder option. If the adder option is chosen, a pipelined adder must be designed using MSI components. A complete 16-tap filter using 8-bit signal data words and 8-bit coefficients is shown in Figure 9. Care must be taken to assure that the outputs of each of the sections are properly weighted. Note that the Two's Complement Data (TCD) pin should be active only in the sections which have the MSD of the data word as the input. Likewise, the Two's Complement Coefficient (TCC) pin should be active only on the sections which have the MSD of the coefficient word as the input.

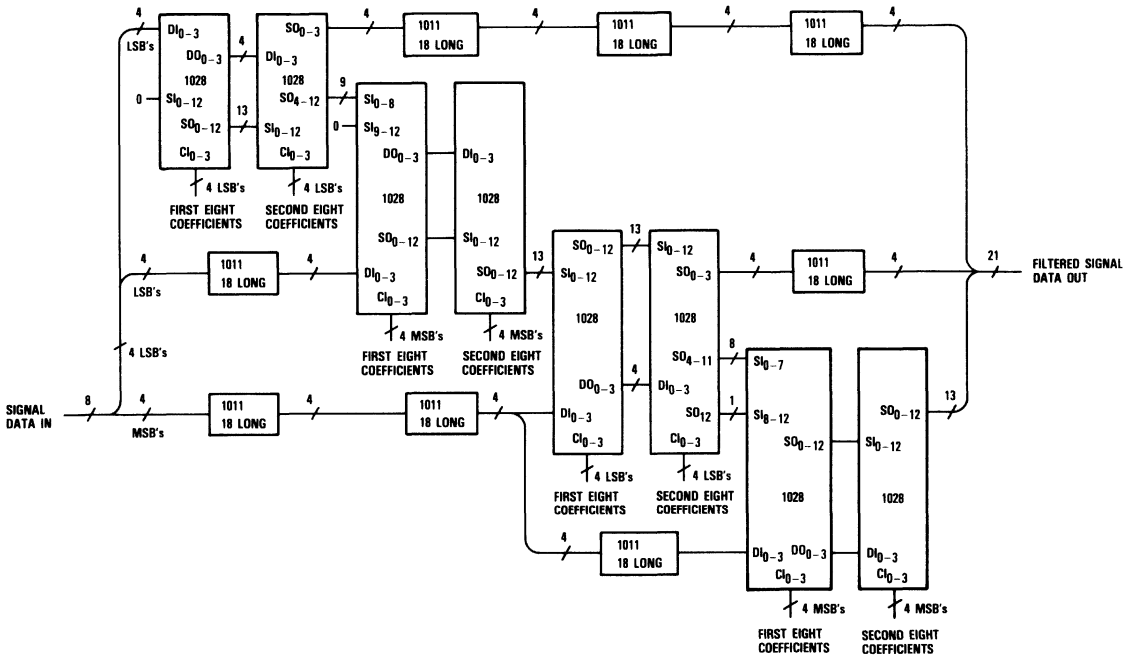
However, another approach is possible. The TDC1028 has internal adders which are not used in the above configuration. Those are the adders in the first device in each section. By introducing suitable delays, these adders can be used to increase resolution without using external adders. A sample circuit, a complete 16-tap filter using 8-bit signal data words and 8-bit coefficients, is shown in Figure 10. Notice that this introduces an eighteen sample delay in the signal path. The necessary 8-bit wide by 9 or 18 stage long shift registers are provided by TRW's TDC1011.

Figure 9.


TDC1028 ARRAY
PIPELINED ADDER TREE
SIGNAL DATA IN
LSB's
MSB's
FIRST EIGHT COEFFICIENTS
SECOND EIGHT COEFFICIENTS
4 LSB's
4 MSB's
74F283
74F374
FILTERED SIGNAL DATA OUT

H

Figure 10.



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1028J4C	STD–T_A = 0°C to 70°C	Commercial	48 Pin Hermetic Ceramic DIP	1028J4C
TDC1028J4A	EXT–T_C = –55°C to 125°C	High Reliability	48 Pin Hermetic Ceramic DIP	1028J4A

TMC2242

Half-Band Interpolating/Decimating Digital Filter
12 Bits, 40MHz

The TMC2242 is a fixed-coefficient, linear-phase half-band (low-pass) digital filter VLSI circuit which can also be used to halve or double a digital signal's sample rate. When used as a decimating post-filter with a double-speed oversampling video A/D converter, it greatly reduces the cost and complexity of the associated analog antialias pre-filter, such as that required for broadcast video chrominance bandwidth limiting. When used as an interpolating pre-filter with a double-speed oversampling D/A converter, the TMC2242 can simplify the corresponding analog reconstruction post- filter. The only user "programming" required is selection of mode (interpolate, decimate, or neither) and rounding.

The TMC2242 accepts 12-bit two's complement data at up to 40 million samples per second and outputs saturated, two's complement or offset binary data, rounded to 9 to 16 bits. Within the 40MHz I/O limit, the TMC2242's output sample rate can be 1/2, 1, or 2 times its input sample rate.

The filter is flat within $\pm$0.02dB from 0 to 0.22F_S, with stopband attenuation of greater than 59.4dB from 0.28F_S to the Nyquist frequency. The response is 6dB down at 0.25F_S. Symmetric-coefficient FIR filters such as the TMC2242 have linear phase response. Although most users will be pleased with the results obtained with one TMC2242 in the system, full compliance with the SMPTE 601 standard of –12dB at 0.25F_S requires two devices cascaded serially.

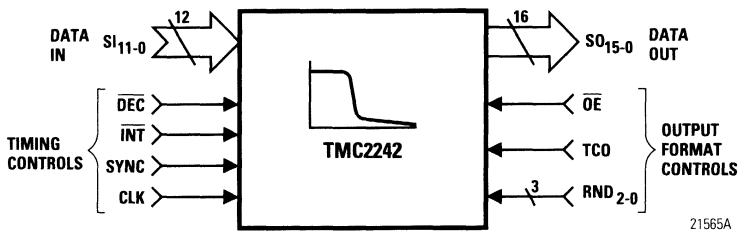
Fabricated using TRW's proprietary OMICRON-C one-micron CMOS process, the TMC2242 operates at a guaranteed clock rate of 40MHz over the standard temperature and supply voltage ranges and is available in a 44 lead plastic chip carrier.

Features

- 40MHz Guaranteed Maximum Clock Rate
- User-Selectable 2:1 Decimation, 1:2 Interpolation
- Frequency Response +/-0.02dB In Passband
- Stopband (0.28 to 0.5 x F_S) Rejection 59.4dB
- Two-Device Cascade Meets CCITT Recommendation 601 Low-Pass Filter Requirements
- Dedicated 12-Bit Two's Complement Input Data Port And 16-Bit Output Data Port With User-Selectable Rounding To 9 Through 16 Bits
- Two's complement Or Inverted Offset Binary Output Format
- Build-In Limiter Prevents Overflow
- Single +5V Power Supply
- Compact 44 Lead Plastic Chip Carrier Package

H

Logic Symbol



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40G06433 Rev. A – 9/90
Printed in the U.S.A.

Applications

- Low-Cost, Industry-Standard Video Chrominance Bandwidth Limiting (Anti- Aliasing)
- Simple, High-Performance Video Reconstruction Post-Filtering
- General Digital-Domain High-Performance Low-Pass Filtering, Requiring:
  - — Passband Below (0.22) x F_S
  - — Stopband Above (0.28) x F_S
- General Digital-Domain Waveform Reconstruction Post-Filtering
- Telecommunications Systems
- Digitally Synthesized Radio
- Radar

Functional Description

The TMC2242 implements a fixed-coefficient linear-phase Finite Impulse Response (FIR) filter of 55 effective taps, with special rate-matching input and output structures to facilitate 1:2 decimation and 2:1 interpolation. In the straight-through mode (equal input and output clock rates), the filter and input and output registers will operate at the guaranteed maximum clock rate of 40MHz. The total internal pipeline latency from the input of an impulse to the corresponding output peak is 33 cycles; the 55-value output response begins after 6 clock cycles and ends after 60 cycles.

To perform interpolation, the chip slows the effective input register clock rate to half the internal and output rates. The TMC2242 internally inserts zeroes between the incoming data samples to "pad" the input data rate to match the output rate.

To perform decimation, the chip sets the output register clock rate to half of the input and internal rates. One output is then obtained for every two inputs.

In interpolation or decimation mode, the SYNC control is first held HIGH, then brought LOW with the first data input value. SYNC is held LOW until resynchronization is desired. For interpolation, input values should be presented at the first rising edge of CLK for which SYNC=0 and at every alternate CLK rising edge thereafter.

Figure 1. Functional Block Diagram

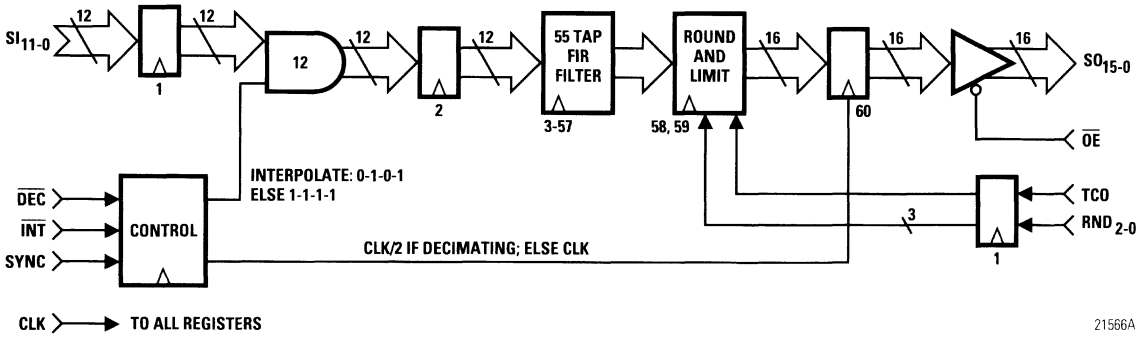


Figure 2A. Transfer Function of TMC2242 Half-Band FIR Filter

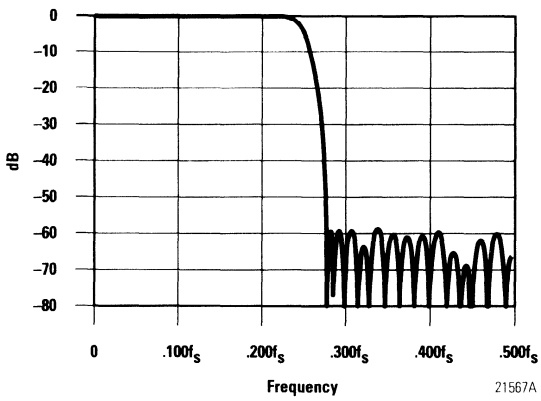
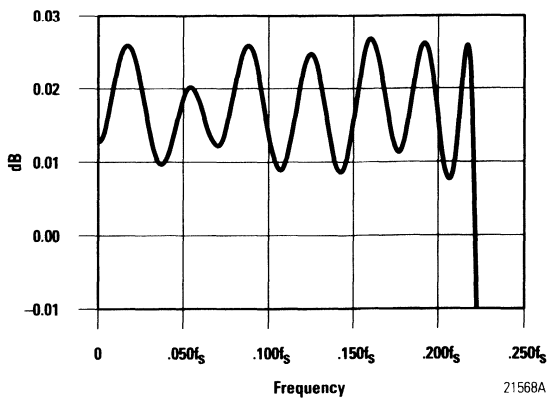


Figure 2B. Passband Detail of TMC2242 Transfer Function



The input data word format is always two's complement. The output data format is two's complement when TCO is HIGH and inverted offset binary when TCO is LOW. The output data can thus be processed further or routed directed to a Digital-to-Analog converter for reconstruction. The user can tailor the output data word width to his system requirements using the Rounding control. As shown in *Table 1*, the output is half-LSB rounded to the resolution selected by the value of $RND_{2\text{-}0}$. The bits below the LSB are then zero-filled. The asynchronous three-state output enable control simplifies interfacing to a bus.

Signal Definitions

Clock

CLK — The TMC2242 operates from a single master Clock. All internal registers (except output register in decimate mode) are strobed on the rising edge of Clock, and all timing specifications are referenced to the rising edge of Clock.

SYNC — The user synchronizes the incoming data with the TMC2242 by holding SYNC HIGH on Clock N, and then LOW on Clock N+1, when the first data word is presented to the input $SI_{11\text{-}0}$. If $\overline{DEC}$=$\overline{INT}$ (passthrough mode), SYNC is inactive. SYNC may be held LOW until resynchronization is desired, or it may be toggled at 1/2 the clock rate.

Inputs

$SI_{11\text{-}0}$ — Data presented to the registered 12-bit two's complement data input port $SI_{11\text{-}0}$ will be latched internally on the current Clock, or on every other Clock if in INTERPOLATE mode. SI_{11} is the MSB.

Outputs

$SO_{15\text{-}0}$ — The current result is available at the registered 16-bit output port $SO_{15\text{-}0}$, half-LSB rounded as determined by the rounding control word $RND_{2\text{-}0}$. SO_{15} is the MSB.

Note: TMC2242's limiter ensures that an internal overflow will generate a valid full-scale (7FFF positive or 8000 negative) output. The chip's D.C. gain is 1.0015=0.0126dB; 0.5007 = –3.004dB in INTERPOLATE mode.

Controls

TCO — When the Two's Complement format Control TCO is HIGH, all output data are presented in signed two's complement format. When LOW, the output is inverted offset binary, obtained inside the chip by inverting bits SO_{14} through SO_0, leaving SO_{15} unchanged.

$\overline{INT}$ — When the input interpolation control $\overline{INT}$ is LOW, the input register is driven at full clock speed and the chip inserts zeroes between samples, "padding" the input to match the output rate and effectively halving the input data rate and the output amplitude. The TMC2242 then interpolates between these

alternate input data points to achieve a full output data rate.

$\overline{DEC}$ — When the decimation output control $\overline{DEC}$ is LOW, the output register is driven at half clock speed, decimating the output data stream.

Note: When $\overline{INT}$=$\overline{DEC}$, both the input and output registers run at the full clock rate.

$RND_{2\text{-}0}$ — These three pins set the position of the effective least significant bit of the output port by adding a rounding bit to the next lower internal bit and zeroing all outputs below the rounding bit. See *Table 1*.

Note: The above controls, TCO, $\overline{DEC}$, $\overline{INT}$, and $RND_{2\text{-}0}$ determine the device function, numeric format, and rounding of the data. The user must exercise caution when changing them, since they will impact work in progress in the chip's 60 clock internal pipeline.

$\overline{OE}$ — The output data port $SI_{15\text{-}0}$ is in the high-impedance state when the asynchronous output enable is HIGH. When $\overline{OE}$ is LOW, the port is enabled.

Power

V_{DD}, GND — The TMC2242 operates from a single +5V supply. All power and ground pins must be connected.

Table 1. Input and Output Data Formats and Bit Weighting, TCO=1[1]

Bit Weight - Output Port During Interpolation Only[2]

-2^1	2^0	2^{-1}	•••	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}

Bit Weight - All other I/O

-2^0	2^{-1}	2^{-2}	•••	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	Rounding $RND_{2\text{-}0}$

Input SI_{11}	SI_{10}	SI_9	•••	SI_4	SI_3	SI_2	SI_1	SI_0					—
Output													
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3	SO_2	SO_1	SO_0r	000
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3	SO_2	SO_1r	0	001
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3	SO_2r	0	0	010
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7	SO_6	SO_5	SO_4	SO_3r	0	0	0	011
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7	SO_6	SO_5	SO_4r	0	0	0	0	100
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7	SO_6	SO_5r	0	0	0	0	0	101
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7	SO_6r	0	0	0	0	0	0	110
SO_{15}	SO_{14}	SO_{13}	•••	SO_8	SO_7r	0	0	0	0	0	0	0	111

Note:
1. When TCO=0, most significant bit of output is positive instead of negative.
2. During interpolation, device DC gain is approximately 0.5.
3. Where "r" indicates the half-LSB-rounded bit, 0 the zeroed LSBs, and a minus sign a sign bit.

Table 2. Hexadecimal Impulse Response and Decimal Equivalents of Coefficients

Inpulse Out[1]	Decimal Equivalent	
FFF2	–.000875473	coef #1, 55
0000	.0	coef #2, 54=0
0017	.001390457	
0000	.0	
FFDB	–.002265930	
0000	.0	
0039	.003501892	
0000		
FFA8	–.005355835	
0000		
007D	.007621765	
0000		
DD51	–.01071167	
0000		
00F3	.01483154	
0000		
FEB5	–.02018738	
0000		
01CA	.02796364	
0000		
FD79	–.03949928	
0000		
03CD	.05937767	
0000		
F95E	–.1036148	
0000		
145B	.3180542	coef #27, 29
2010	.5009766	coef #28 (center)

Note: 1. Input=0,0,400,0,0,...
$\overline{INT}$=DEC=1
TCO=1

Table 3. Input Transition Response

	INPUT	OUTPUT				
		$\overline{INT}$=DEC TCO=0	$\overline{INT}$=DEC TCO=1	$\overline{INT}$=0 DEC=1 TCO=1	$\overline{INT}$=1 DEC=0 TCO=1	
	400	XX	XX	XX	XX	
	400	XX	XX	XX	XX	
>55 cycles	•	•	•	•	•	
	•	•	•	•	•	
	•	•	•	•	•	
	400	3FE7	4018	2008	4018	DC gain[1]
	400	3FE7	4018	2010	4018	
	000					
	•					
	•					
	000	3B90	446F	245F	446F	Max ringing
	000	3B90	446F	2010	446F	
	000	4FEB	3014	1004	1004	
	000	6FFB	1004	0000	1004	
	000	846F	FBA9	FBA9	FBA9	Min ringing
	•	•	•			
	•	•	•			
	•	•	•			
	000	7FFF	0000	0000	0000	Steady state

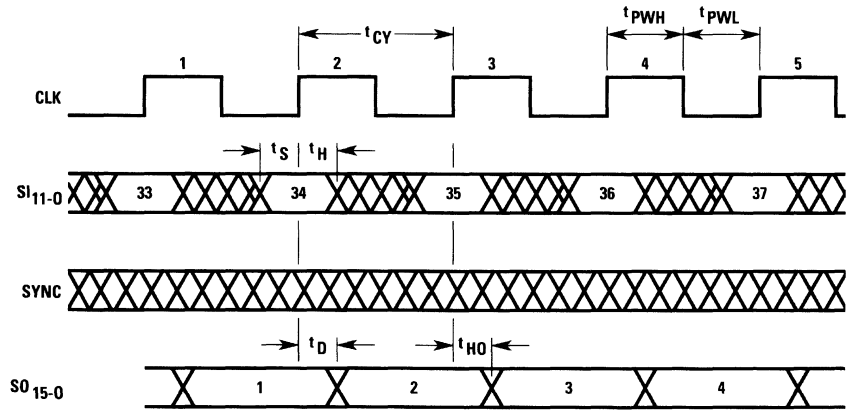
Note: 1. In interpolation, steady-state output will oscillate approximately 0.1%, as here between 2008 and 2010.

H

Package Interconnections

Signal Type	Name	Function	R2 Package
Timing Controls	$\overline{INT}$	Interpolate	44
	$\overline{DEC}$	Decimate	1
	SYNC	Synchronization	43
	CLK	System Clock	42
Data Inputs	SI_{11-0}	Input Data Port	40, 37, 36, 35, 34, 33, 32, 31, 30, 27, 26, 25
Data Outputs	SO_{15-0}	Output Data Port	4, 5, 6, 7, 8, 9 10, 11, 14, 15, 16, 17, 18, 19, 20, 21
	$\overline{OE}$	Output Enable	3
Output Controls	RND_{2-0}	Rounding	22, 23, 24
Power	V_{DD}	Supply Voltage	13, 29, 38
	GND	Ground	12, 28, 39, 41

Figure 3. Timing Diagram — Equal Rate Mode $\overline{INT}$=$\overline{DEC}$



Note: Values at SO_{15-0} are impulse response centers (peaks) corresponding to inputs bearing the same numbers. Thus, the input-to-center latency is 33 registers (clock cycles).

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Figure 4. Timing Diagram - Decimination $\overline{INT}$=1, $\overline{DEC}$=0

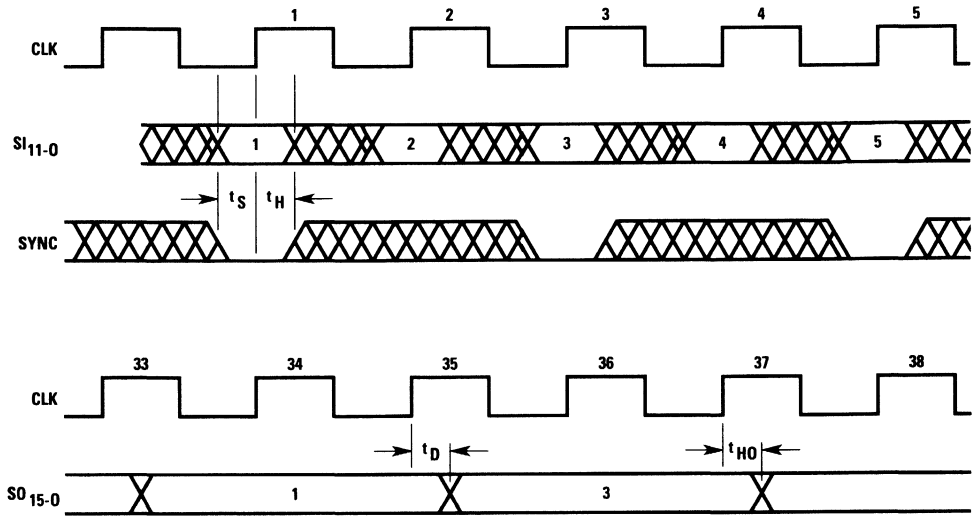

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Figure 5. Timing Diagram - Interpolation $\overline{INT}$=0, $\overline{DEC}$=0

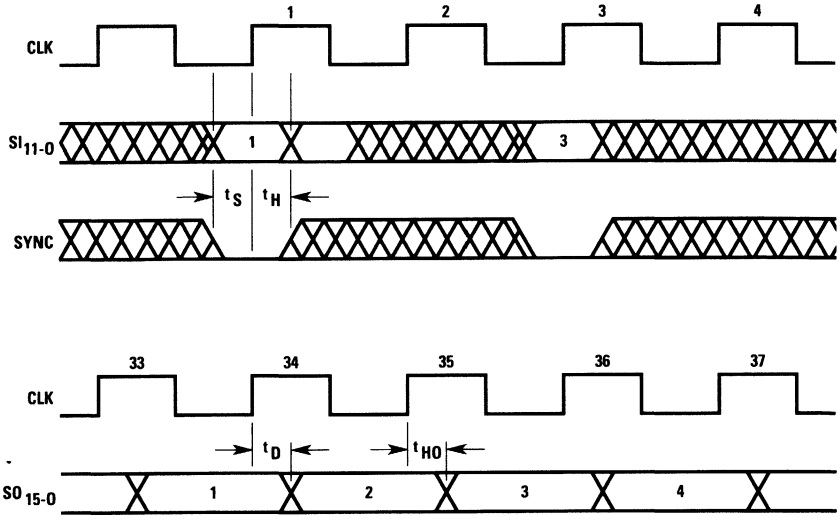

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Figure 6. Impulse Response - Equal I/O Rate Mode $\overline{INT}$=$\overline{DEC}$

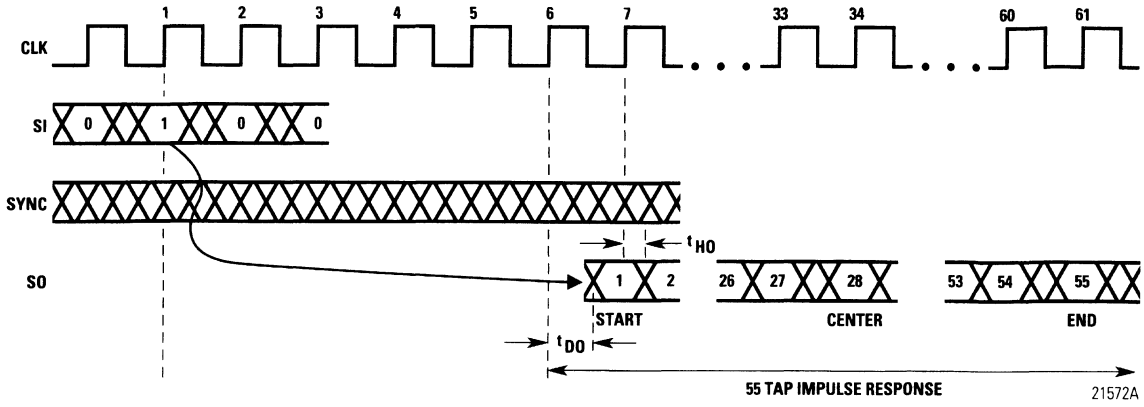


Figure 7. Impulse Response - Interpulate Mode $\overline{DEC}$=1, $\overline{INT}$=0

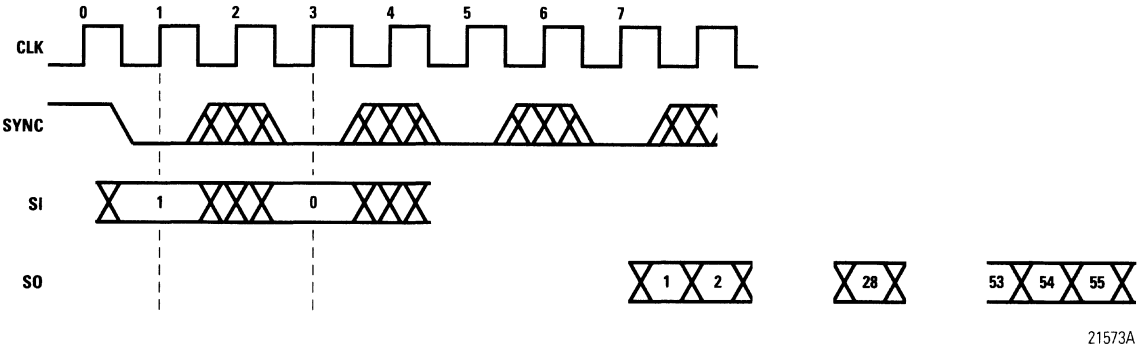


Figure 8. Impulse Response - Decimate Mode $\overline{DEC}$=0, $\overline{INT}$=1

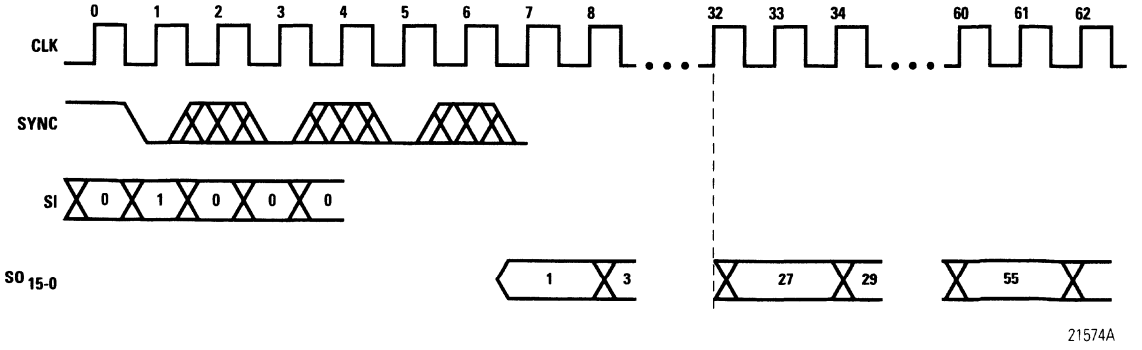


Figure 9. Equivalent Input Circuit

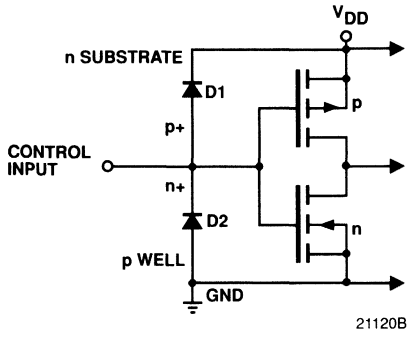


Figure 10. Equivalent Output Circuit

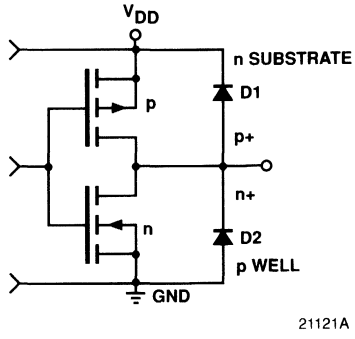
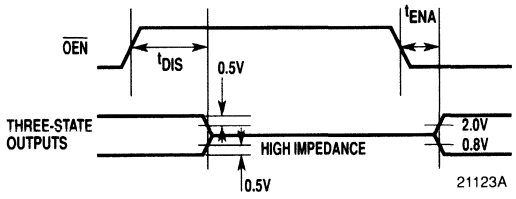


Figure 11. Threshold Levels for Three-State Measurement



Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage[2]	−0.5 to (V_{DD} + 0.5)V[2]
Forced current[3,4]	−6.0 to 6.0mA[3,4]
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating case	−60 to +130°C
junction	175°C
Lead soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range Standard Min	Temperature Range Standard Max	Units
V_{DD}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Voltage, Logic LOW		0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0		V
I_{OL}	Output Current, Logic LOW		8.0	mA
I_{OH}	Output Current, Logic HIGH		−4.0	mA
t_{CY}	Cycle Time			
	TMC2242	33		ns
	TMC2242-1	25		ns
t_{PWL}	Clock Pulse Width, LOW	10		ns
t_{PWH}	Clock Pulse Width, HIGH	10		ns
t_S	Input Setup Time			
	TMC2242	10		ns
	TMC2242-1	8		ns
t_H	Input Hold Time	0		ns
T_A	Ambient Temperature, Still Air °C	0	70	°C

Electrical characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD}=Max, V_{IN}=0V		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD}=Max, $\overline{OE}$=V_{DD}, f=10MHz			mA
		f=20MHz		140	mA
I_{IL}	Input Current,Logic LOW	V_{DD}=Max, V_{IN}=0V		10	µA
I_{IH}	Input Current,Logic HIGH	V_{DD}=Max, V_{IN}=V_{DD}		−10	µA
V_{OL}	Output Voltage,Logic LOW	V_{DD}=Min, I_{OL}=Max		0.4	V
V_{OH}	Output Voltage,Logic HIGH	V_{DD}=Min, I_{OH}=Max	2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD}=Max, V_{IN}=0V		40	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD}=Max, V_{IN}=V_{DD}		−40	µA
I_{OS}	Short-Circuit Output Current	V_{DD}=Max, Output HIGH, one pin to ground, one second duration max.	20	80	µA
C_I	Input Capacitance	T_A=25°C, f=1MHz		10	pF
C_O	Output Capacitance	T_A=25°C, f=1MHz		10	pF

Note: 1. Actual test conditions may vary from those shown, but specified operation is guaranteed.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
t_D	Output Delay	V_{DD}=Min, C_L=25pF			
	TMC2242			20	ns
	TMC2242-1			16	ns
t_{HO}	Output Hold	V_{DD}=Max, C_L=25pF	3		ns
t_{ENA}	Output Enable	V_{DD}=Min, C_L=25pF			
	TMC2242			20	ns
	TMC2242-1			15	ns
t_{DIS}	Output Disable	V_{DD}=Min, CL=25pF			
	TMC2242			20	ns
	TMC2242-1			15	ns

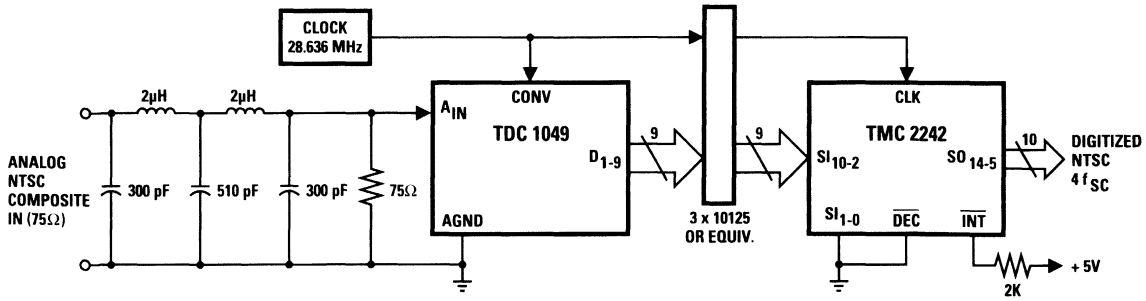
Applications Discussion

Digitizing Composite NTSC Video

The TMC2242 is well suited for filtering digitized composite NTSC-encoded analog video. *Figure 12* shows a simple and cost-effective circuit built around the device. The TDC1049 9-bit Analog-to-Digital converter is a popular choice for digitizing high-quality video, offering a 30MHz maximum clock rate and 16MHz input bandwidth at moderate cost. The relative timing of the TDC1049 and TMC2242 clocks must accommodate the delay through the 10125 ECL-to-TTL converter, the TDC1049 output delay, and the TMC2242 input setup and hold times.

H

Figure 12. Digitizing NTSC Video Using the Decimation Mode



Antialiasing Prefilter
- 0.012dB @ 5.75MHz
- 3dB @ 9.3MHz
- 48dB @ 21.5MHz

TDC1049 ADC
15MHz Input BW
28.636MSPS Clock
D_1 =MSB, D_9 =LSB

TMC2242 Half-Band Filter
2:1 Decimation Mode
Data in @ 28.636MSPS
Data Out @ 14.318MSPS
SI_{10} =MSB, SI_2 =LSB
SO_{14} =MSB, SO_5 =LSB
10 Bits Output Precision
TCO=1

21575A

In *Figure 13*, an interpolating TMC2242 drives a fast D/A converter to reconstruct an analog NTSC composite waveform. The TDC1112 12-bit Digital- to-Analog converter features extremely low glitch energy for accurate waveform generation, and settling to ± 1/2 LSB in less than 30nsec. The same *(Figure 12)* 75-ohm analog filter is used, this time after the DAC. The user must maintain the correct timing between the TTL Clock and the ECL Clock, including the delay introduced by the 10124 TTL-ECL converter. See the *Timing Diagram* and the *TDC1012 datasheet*. Lower-speed applications can employ the TTL-input TDC1012 DAC without the level translators *(Figure 14)*.

Figure 13. High Speed Interpolation Application

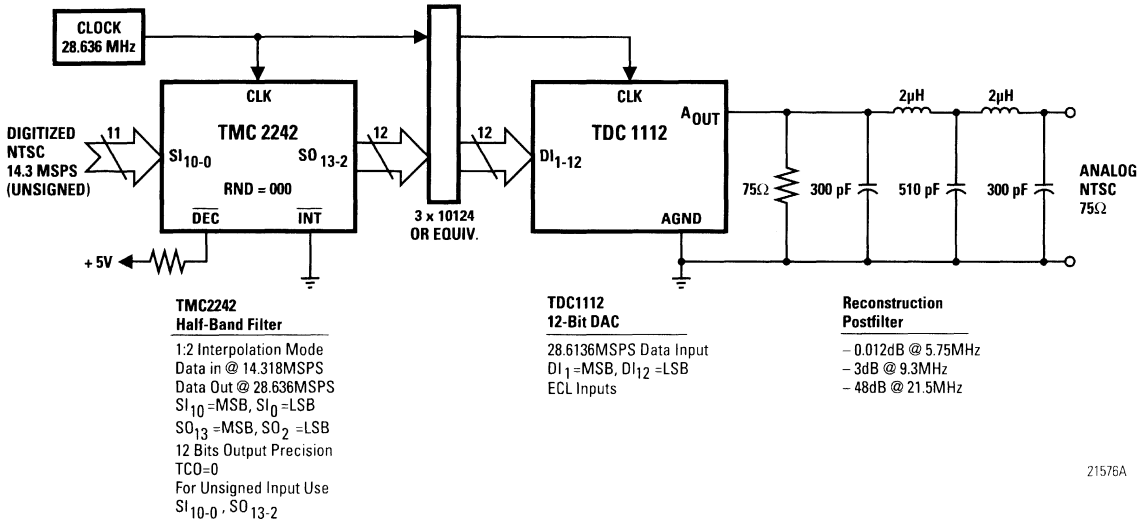
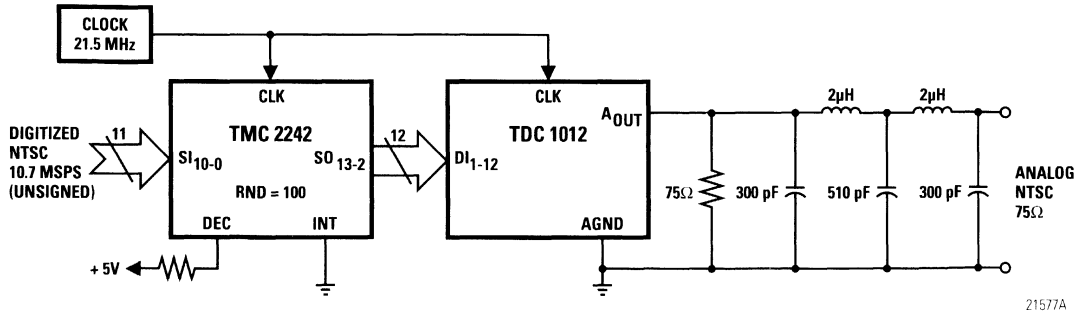
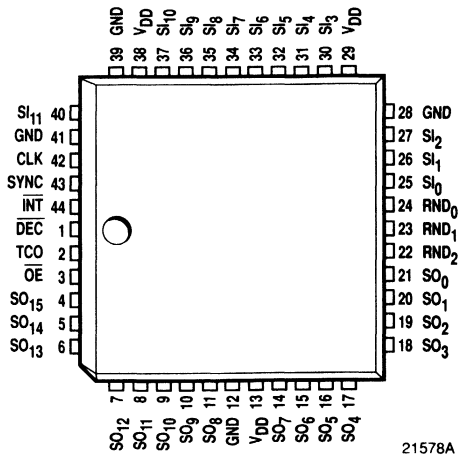


Figure 14. Medium Speed Interpolation Application



Pin Assignments – 44 Lead Plastic Chip Carrier - R2 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	$\overline{DEC}$	12	GND	23	RND_1	34	SI_7
2	TCO	13	V_{DD}	24	RND_0	35	SI_8
3	$\overline{OE}$	14	SO_7	25	SI_0	36	SI_9
4	SO_{15}	15	SO_6	26	SI_1	37	SI_{10}
5	SO_{14}	16	SO_5	27	SI_2	38	V_{DD}
6	SO_{13}	17	SO_4	28	GND	39	GND
7	SO_{12}	18	SO_3	29	V_{DD}	40	SI_{11}
8	SO_{11}	19	SO_2	30	SI_3	41	GND
9	SO_{10}	20	SO_1	31	SI_4	42	CLK
10	SO_9	21	SO_0	32	SI_5	43	SYNC
11	SO_8	22	RND_2	33	SI_6	44	$\overline{INT}$



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Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2242R2C	STD-T_A=0°C to 70°C	Commercial	44 Lead Plastic Chip Carrier	2242R2C
TMC2242R2C1	STD-T_A=0°C to 70°C	Commercial	44 Lead Plastic Chip Carrier	2242R2C1

All parameters in this specification are guaranteed by design, characterization, sample testing ot 100% testing, as appropriate.
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TMC2243

CMOS FIR Filter
10 x 10 Bit, 20MHz

The TMC2243 is a video speed three stage 10 x 10 bit FIR (Finite Impulse Response) filter integrated circuit composed of three registered multiplier – adders concatenated into a one – dimensional systolic array. Utilizing two's complement representation, the TMC2243 accepts one 10 – bit data point,updates one 10 – bit coefficient, and produces one 16 – bit rounded, filtered output point every 50 nanoseconds.

The TMC2243 has features which facilitate longer FIR filters, a 16 – bit Sum – In port and user programmable pipeline registers. Enabling these registers allows the insertion of a zero – coefficient stage before each regular filter stage for up to six stages per TMC2243. Larger FIR filters can be built by cascading Sum – In and Sum – Out.

Coefficients are stored in 3 registers and are addressed via the 2 – bit Write Enable control, allowing one coefficient to be changed per clock cycle. All Data, Sum – In, Sum – Out and instruction inputs are registered on the rising edge of clock.

The 16 MSBs of the 23 – bit internal summation path are available at the Sum – In and Sum – Out ports. Six bits of cumulative word growth are provided internally. Data Overflow is indicated by an output flag.

Built with TRW's one – micron double level metal OMICRON – C™ CMOS process, the TMC2243 is available in a 68 pin grid array.

Features

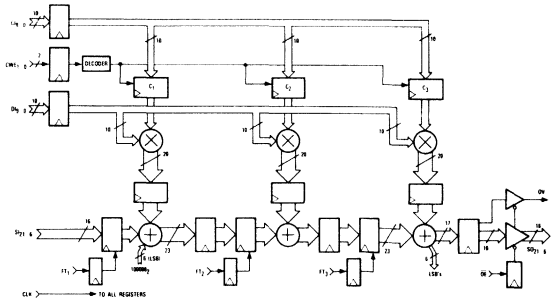
- 20MHz Data Input And Computation Rate
- 10 x 10 Bit Multiplication With 23 – Bit Extended Precision Sum Of Products (Overflow, Plus 16 Output And 6 Guard Bits)
- Up To 3 Zero And 3 Non – Zero Stages Per Device
- Two's Complement Arithmetic
- 16 – Bit Sum – In And Sum – Out Ports For Cascading
- Internal 1/2 LSB Rounding
- All Inputs And Outputs Are Registered
- One Coefficient Update Per Clock Cycle
- Low Power Consumption CMOS Process
- Single +5V Power Supply
- Available In 68 Pin Grid Array And 69 Pin Plastic PGA

Applications

- FIR Filters
- Adaptive Filters
- Multi – Bit Correlation
- One And Two Dimension Video Filtering
- Radar Signal Processors
- One And Two Dimension Convolution
- Arithmetic Element For Systolic Array Processors

H

Functional Block Diagram



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La Jolla, CA 92038

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FAX: (619) 455-6314

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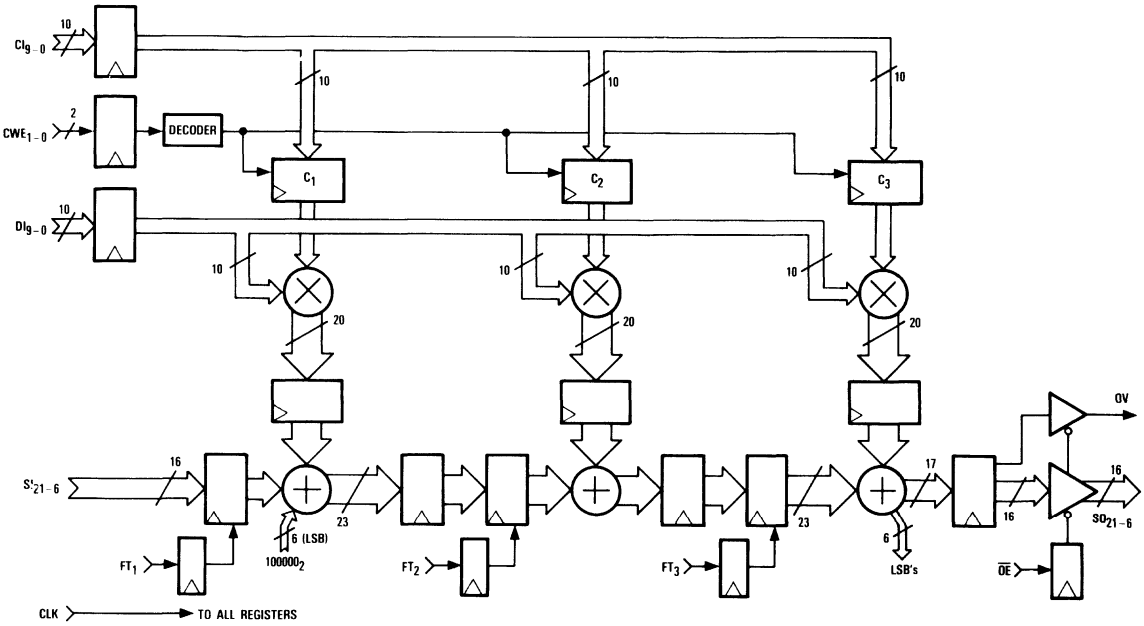
Functional Block Diagram

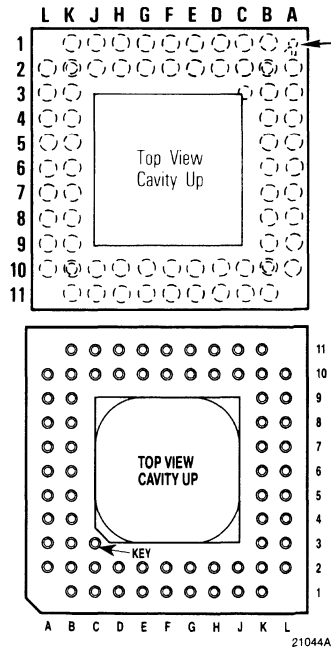


Pin Assignments

63 Pin Grid Array – G8 Package
69 Pin Plastic Pin Grid Array – H8 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B2	GND	K2	DI_1	K10	GND	B10	OV
B1	V_{DD}	L2	DI_0	K11	SI_{18}	A10	SO_{21}
C2	$\overline{OE}$	K3	CI_0	J10	SI_{17}	B9	SO_{20}
C1	FT_0	L3	CI_1	J11	SI_{16}	A9	SO_{19}
D2	FT_1	K4	CI_2	H10	SI_{15}	B8	SO_{18}
D1	FT_2	L4	CI_3	H11	SI_{14}	A8	SO_{17}
E2	CWE_0	K5	CI_4	G10	SI_{13}	B7	SO_{16}
E1	CWE_1	L5	CI_5	G11	SI_{12}	A7	SO_{15}
F2	DI_9	K6	V_{DD}	F10	SI_{11}	B6	SO_{14}
F1	DI_8	L6	CI_6	F11	SI_{10}	A6	SO_{13}
G2	DI_7	K7	CI_7	E10	SI_9	B5	SO_{12}
G1	DI_6	L7	CI_8	E11	SI_8	A5	SO_{11}
H2	DI_5	K8	CI_9	D10	SI_7	B4	SO_{10}
H1	DI_4	L8	SI_{21}	D11	SI_6	A4	SO_9
J2	DI_3	K9	SI_{20}	C10	V_{DD}	B3	SO_8
J1	DI_2	L9	SI_{19}	C11	V_{DD}	A3	SO_7
K1	GND	L10	CLK	B11	GND	A2	SO_6

Note: Pin D4 is a mechanical orientation pin on the H8 package at manufacturer's option.



Functional Description

General Information

The TMC2243 consists of three identical arithmetic cells, each of which contains a 10 x 10 two's complement multiplier and a 23-bit adder. Each cell receives the current data (DI) from the Data input register, multiplies it by a locally stored Coefficient (CI_i), and adds it to the Sum $SI_{(i-1)}$ received from the previous cell. The result,

$$SI_i = DI \times CI_i + SI_{(i-1)},$$

then goes to the next cell via two serial pipeline registers. When only one pipeline register is enabled, stages (i-1) and i are sequential. When both registers are enabled, there is a stage with a zero coefficient between them.

The input arithmetic cell receives $SI_{(i-1)}$ via the 16-bit Sum-In port (registered when FT_1 = LOW), filling the six lower bits with 100 000 (1/2 LSB) for internal rounding. The output cell outputs the 16 MSBs (V_{21} through V_6) of SO_i through a register to the Sum-Out port. The Overflow flag is set when the final output exceeds 16 bits and resets with the output of the next nonoverflowing result. Sum-Out and the Overflow Flag can be forced to high-impedance with the Output Enable control. See Figure 1.

The two-bit Write Enable control specifies the loading of the three coefficient registers (one per arithmetic cell) with data appearing at the Coefficient Input port.

Signal Definitions

Power

V_{DD}, GND — The TMC2243 operates from a single +5V supply.

Clock

CLK — The TMC2243 has a single clock input. The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of clock.

Inputs

DI_{9-0} — DI_9 through DI_0 is the 10-bit registered Data Input; DI_9 is the MSB (sign bit) and DI_0 is the LSB. Data is in two's complement representation, and is clocked into the data register on each rising edge of clock. See Figure 1.

SI_{21-6} — SI_{21} through SI_6 is the 16-bit Sum-In port. SI_{21} is the MSB (sign bit). Sum-In is truncated to bit SI_6 (plus the 1/2 LSB rounding bit in SI_5)and is in two's complement representation. See Figure 1. The Sum-In port is registered, on the rising edge of clock, only when FT_1 =LOW. Unique input setup requirements must be observed when operating in the feedthrough mode (FT_1 = HIGH). See text.

CI_{9-0} — CI_9 through CI_0 is the 10-bit registered Coefficient Input; CI_9 is the MSB (sign bit) and CI_0 is the LSB. Each coefficient and its write enable address (CWE_{1-3}) are registered on the same clock. The coefficient is then latched into the indicated register (C_{1-3}) at the rising edge of the next clock. The contents of this bus are ignored if a coefficient register is not selected (CWE = 00). The format of CI_{9-0} is identical to that of DI_{9-0}.

Outputs

SO_{21-6} — SO_{21} through SO_6 is the three-state 16-bit registered Sum-Out port; SO_{21} is the MSB (sign bit). For maximum precision, the internal products and accumulations are 23 bits but Sum-Out is internally truncated to 16 bits, and excludes the overflow bit and the 6 LSBs. The format is identical to that of SI_{21-6}. See Figure 1.

Controls

CWE_{1-0} The two bits of the registered Coefficient Write Enable control indicate which of the coefficient registers is to receive a new coefficient at the beginning of the next clock cycle.

CWE_{1-0}	Coefficient Register Selected
00	Holds all coefficients unchanged.
01	C_1
10	C_2
11	C_3

FT_{3-1} These registered Feed Through controls select clocked (FT_i = LOW) or feedthrough (FT_i = HIGH) operation for each of the pipeline registers. Setting FT_i = LOW inserts a zero coefficient stage, or additional register, before the ith non-zero stage.

$\overline{OE}$ Output Enable is a registered three-state enable control which forces the Sum-Out port and Overflow to the high-impedance state when HIGH. These outputs are enabled when $\overline{OE}$ is LOW.

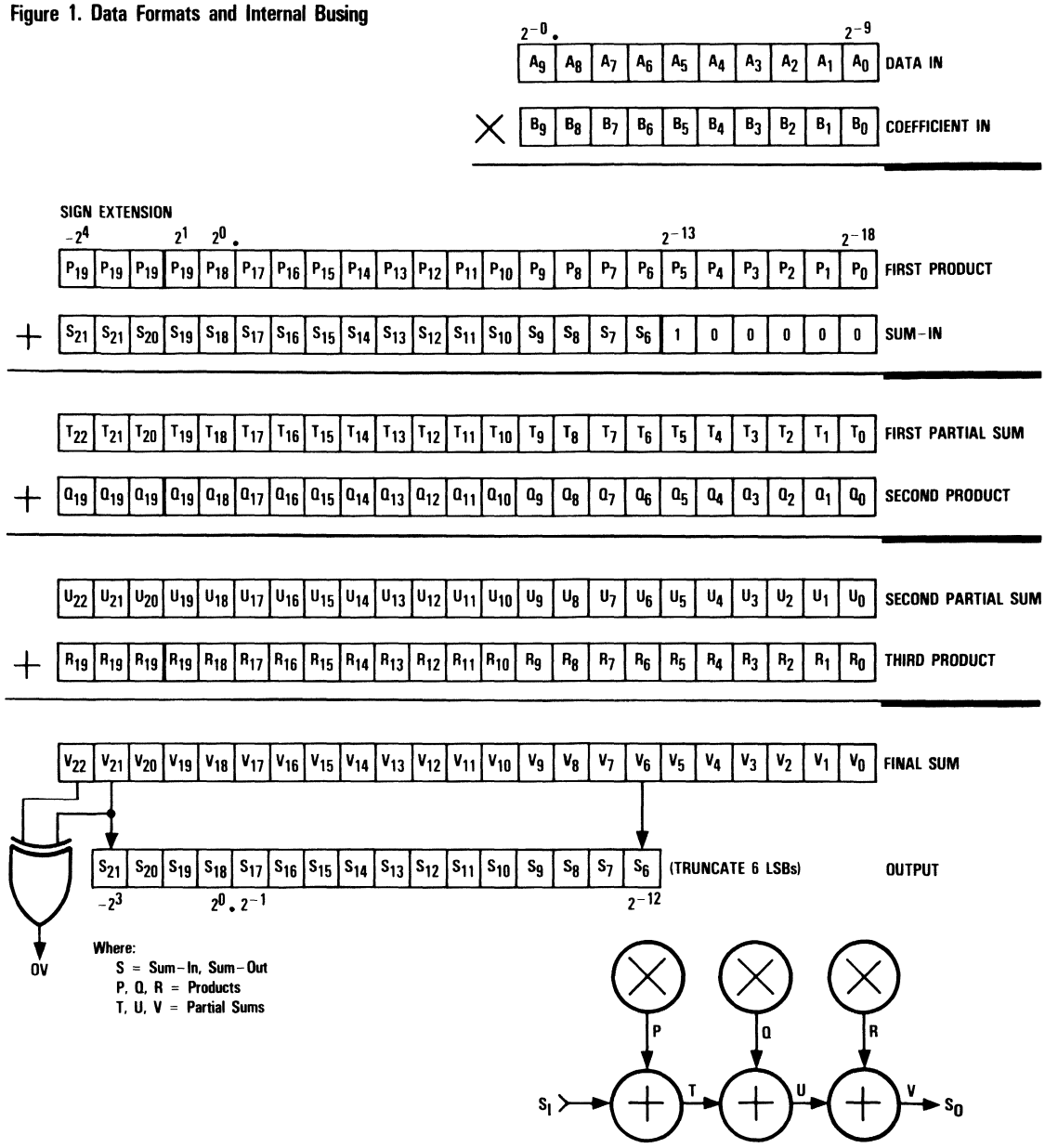
Flags

OV The Overflow Flag is a registered three-state output which goes HIGH whenever the summation result exceeds 16 bits and is reset to LOW on the next nonoverflowing result.

Package Interconnections

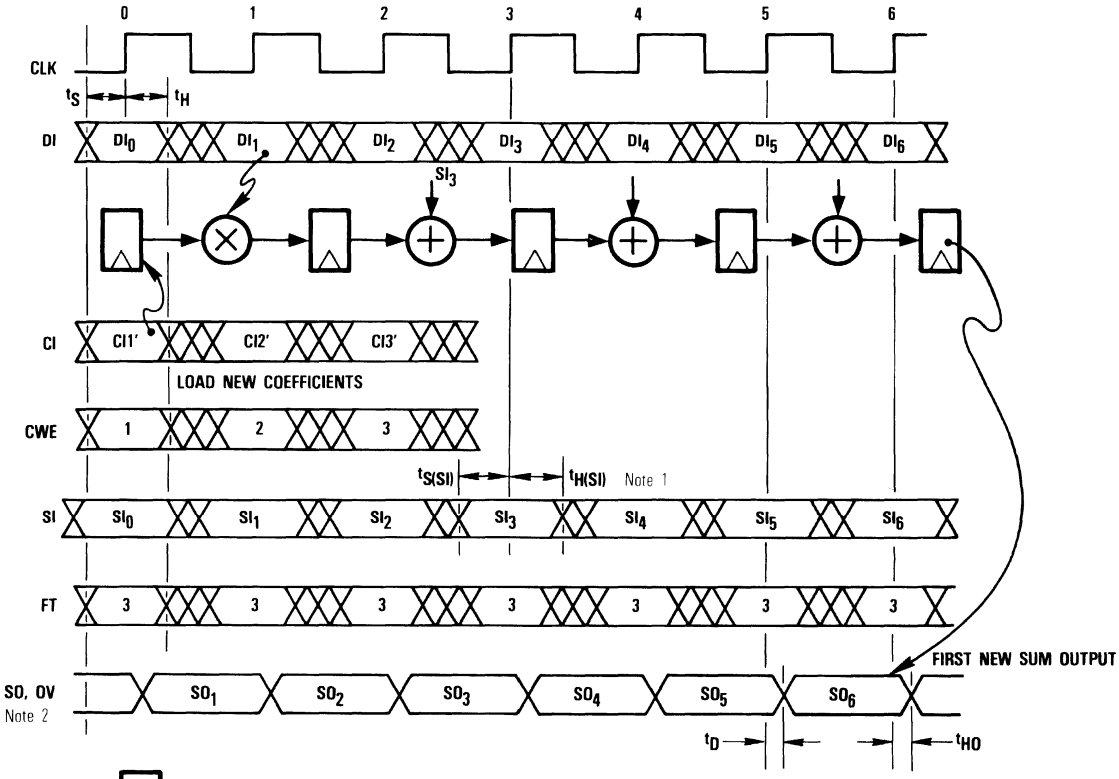
Signal Type	Signal Name	Function	G8, H8 Package Pins
Power	V_{DD}	Supply Voltage	B1, K6, C10, C11
	GND	Ground	B2, K1, K10, B11
Inputs	DI_{9-0}	Data Input	F2, F1, G2, G1, H2, H1, J2, J1, K2, L2
	SI_{21-6}	Sum Input	L8, K9, L9, K11, J10, J11, H10, H11, G10, G11, F10, F11, E10, E11, D10, D11
	CI_{9-0}	Coefficient Input	K8, L7, K7, L6, L5, K5, L4, K4, L3, K3
Outputs	SO_{21-6}	Sum Output	A10, B9, A9, B8, A8, B7, A7, B6, A6, B5, A5, B4, A4, B3, A3, A2
Clock	CLK	Master Clock	L10
Controls	CWE_{1-0}	Coefficient Write Enable	E1, E2
	FT_{3-1}	Feedthrough	D1, D2, C1
	$\overline{OE}$	Output Enable	C2
Flag	OV	Overflow	B10

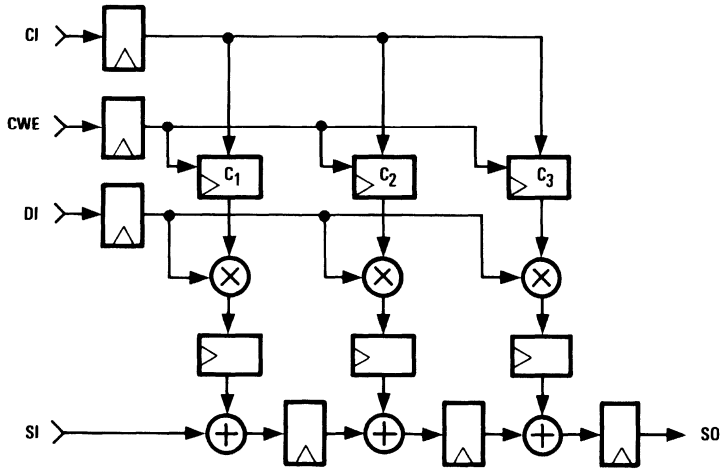
Figure 1. Data Formats and Internal Busing



Because the Sum-In and Sum-Out ports are truncated by 6 bits relative to the external accumulation pipeline, the TMC2243 rounds internally by adding 2^{-13} to each emerging sum of products, effecting half-LSB rounding relative to the output format. The chip internally utilizes all lower-order bits, to 2^{-18}.

Figure 2. Timing Diagram Demonstrating Basic Operation with FT_{1-3} = HIGH (no zero stages)





$$SO_N = SI_{N-3} + C_1DI_{N-5} + C_2DI_{N-4} + C_3DI_{N-3}$$

Notes:

1. Setup and Hold requirements for the Sum Input are similar to the other registered inputs when when FT_1 = LOW. See text.
2. Sum Out and Overflow timing are shown with $\overline{OE}$ = LOW.

The basic equation describing the function of the TMC2243 operating in a fixed state is:

$$SO(N) = SI_{(N-6+FT1+FT2+FT3)} + C_1 \times DI_{(N-7+FT2+FT3)} + C_2 \times DI_{(N-5+FT3)} + C_3 \times DI_{(N-3)}$$

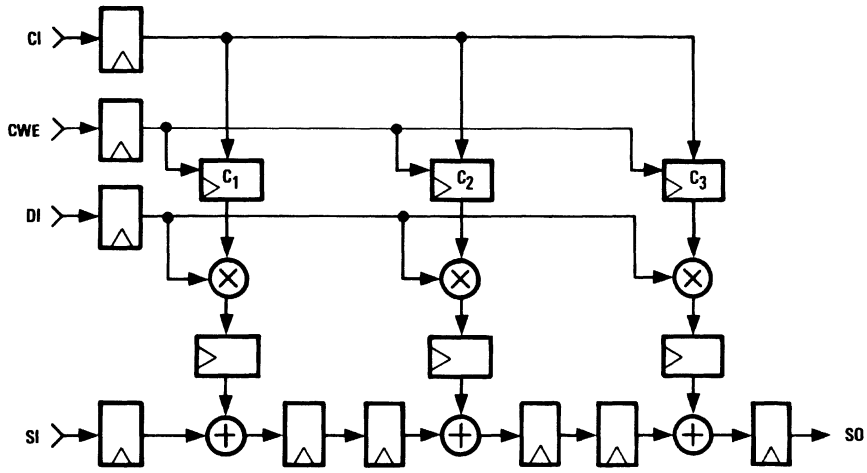
Careful observation of the clock delays shown is basic to construction of a filter algorithm. The operating sequence for the common application with FT_{1-3} = HIGH (no zero stages) is shown in Figure 2. The simplified block diagram demonstrates the clock stages in this configuration. When FT_1 = HIGH, the input feedthrough register is bypassed, and care must be taken to observe the setup requirements on the input of the first adder. Due to the absence of the input register buffer, note that the adder operates on data stable just prior to the arrival of the next clock, and not that setup at the rising edge of the current clock. When FT_1 = LOW the input register latches the input data, and the Sum Input follows setup and hold requirements similar to the other registered inputs of the TMC2243. When FT_1 = HIGH, $t_{S(SI)}$ is guaranteed to allow 20MHz pipelined operation, assuming that input setup is observed, including cascaded operation. See the AC Characteristics table, and Figure 9, Applications Discussion.

Figure 3 shows the effects of the feedthrough registers on filter operation, with two different configurations. The inputs are those presented at the corresponding rising edge of clock, excepting the delayed setup requirements of the Sum Input when FT_1 = HIGH. The outputs are those available up to and including the corresponding edge of clock. Applications utilizing the TMC2243's ability to modify coefficients dynamically are demonstrated in Figure 4, showing the operation of a typical adaptive filter. Note that the Sum Output will be zero in the first few clock cycles of all examples only if the Coefficient Registers are initialized to zero beforehand.

Figure 3. Impulse Response Filter Operation Sequence with $FT_{2,3}$ = LOW

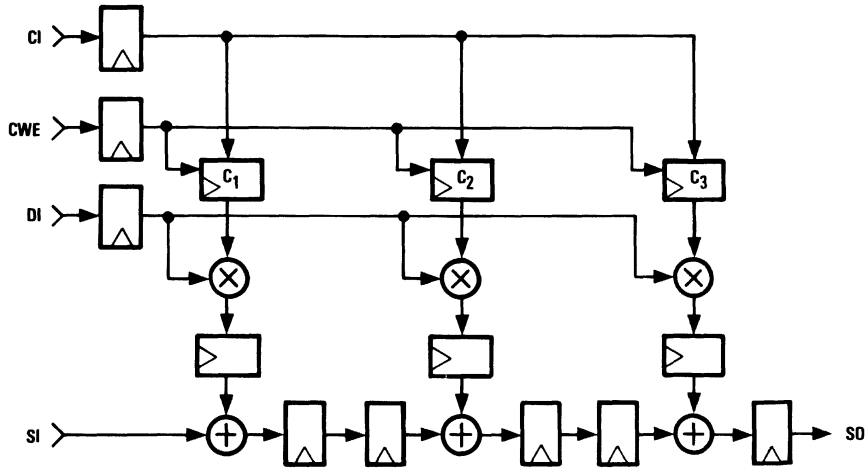
Cycle	SI(A) FT_1 = LOW	SI(B) FT_1 = HIGH	DI	CI	CWE	SO
1	0	0	0	K_0	01	0
2	0	0	0	K_1	10	0
3	0	0	0	K_2	11	0
4	SI_0	0	DI_0	0	00	
5	SI_1	SI_0	DI_1	0	00	0
6	SI_2	SI_1	DI_2	0	00	0
7	SI_3	SI_2	DI_3	0	00	DI_0K_2
8	SI_4	SI_3	DI_4	K_0'	01	DI_1K_2
9	SI_5	SI_4	DI_5	0	00	$DI_0K_1 + DI_2K_2$
10	SI_6	SI_5	DI_6	K_1'	10	$SI_0 + DI_1K_1 + DI_3K_2$
11	SI_7	SI_6	DI_7	0	00	$SI_1 + DI_0K_0 + DI_2K_1 + DI_4K_2$
12	SI_8	SI_7	DI_8	K_2'	11	$SI_2 + DI_1K_0 + DI_3K_1 + DI_5K_2$
13	SI_9	SI_8	DI_9	0	00	$SI_3 + DI_2K_0 + DI_4K_1 + DI_6K_2$
14	0	SI_9	0	0	00	$SI_4 + DI_3K_0 + DI_5K_1 + DI_7K_2$
15	0	0	0	0	00	$SI_5 + DI_4K_0 + DI_6K_1 + DI_8K_2$
16	0	0	0	0	00	$SI_6 + DI_5K_0' + DI_7K_1' + DI_9K_2'$
17	0	0	0	0	00	$SI_7 + DI_6K_0' + DI_8K_1'$
18	0	0	0	0	00	$SI_8 + DI_7K_0' + DI_9K_1'$
19	0	0	0	0	00	$SI_9 + DI_8K_0'$
20	0	0	0	0	00	DI_9K_0'
21	0	0	0	0	00	0

SI(A) is the sequence of Sum Input data with FT_{1-3} = LOW (three zero stages).



$$SO_N = SI_{N-6} + C_1DI_{N-7} + C_2DI_{N-5} + C_3DI_{N-3}$$

SI(B) is the sequence of Sum Input data with FT_1 = HIGH and $FT_{2,3}$ = LOW (two zero stages).

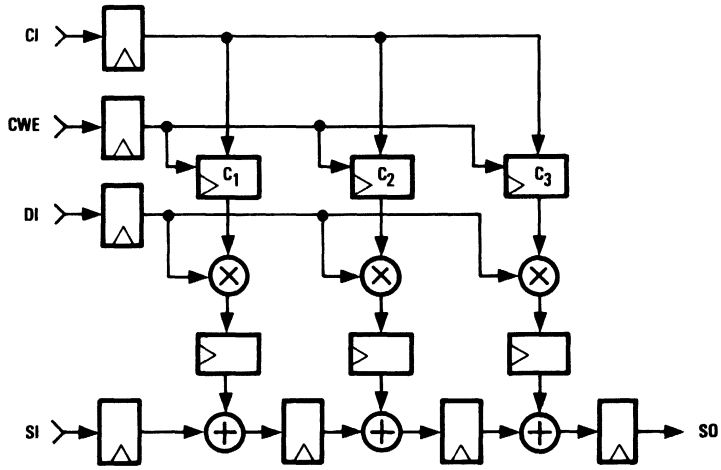


$$SO_N = SI_{N-5} + C_1DI_{N-7} + C_2DI_{N-5} + C_3DI_{N-3}$$

Figure 4. Typical Adaptive Filter Operation Sequence

Cycle	SI	DI	CI	CWE	SO
0	SI_0	DI_0	A_1	01	0
1	SI_1	DI_1	A_2	10	0
2	SI_2	DI_2	A_3	11	0
3	SI_3	DI_3	B_1	01	0
4	SI_4	DI_4	B_2	10	0
5	SI_5	DI_5	B_3	11	0
6	SI_6	DI_6	C_1	01	$SI_2 + A_1DI_1 + A_2DI_2 + A_3DI_3$
7	SI_7	DI_7	C_2	10	$SI_3 + A_1DI_2 + A_2DI_3 + A_3DI_4$
8	SI_8	DI_8	C_3	11	$SI_4 + A_1DI_3 + A_2DI_4 + A_3DI_5$
9	SI_9	DI_9		00	$SI_5 + B_1DI_4 + B_2DI_5 + B_3DI_6$
10	SI_{10}	DI_{10}		00	$SI_6 + B_1DI_5 + B_2DI_6 + B_3DI_7$
11	SI_{11}	DI_{11}		00	$SI_7 + B_1DI_6 + B_2DI_7 + B_3DI_8$
12	SI_{12}	DI_{12}		00	$SI_8 + C_1DI_7 + C_2DI_8 + C_3DI_9$
13	SI_{13}	DI_{13}		00	$SI_9 + C_1DI_8 + C_2DI_9 + C_3DI_{10}$

with FT_1 = LOW and $FT_{2,3}$ = HIGH (one zero stage)



$$SO_N = SI_{N-4} + C_1DI_{N-5} + C_2DI_{N-4} + C_3DI_{N-3}$$

Figure 5. Equivalent Input Circuit

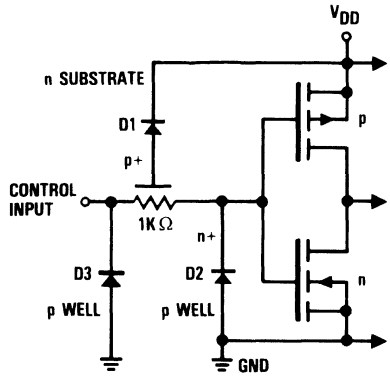


Figure 6. Equivalent Output Circuit

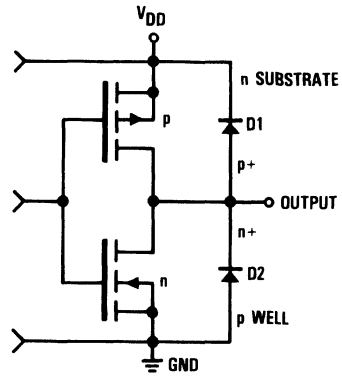


Figure 7. Test Load

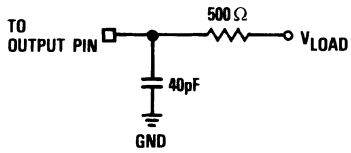
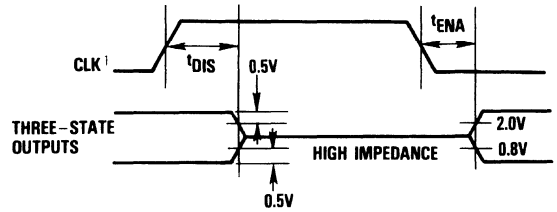


Figure 8. Transition Levels For Three-State Measurements



Note:

1. Assumes $\overline{OE}$ has gone LOW, within the Input Setup requirements.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} +0.5V)
Output	
Applied voltage [2]	−0.5 to (V_{DD} +0.5V)
Forced current [3,4]	−1.0 to 6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW	2.0			2.0			V
V_{IH}	Input Voltage, Logic HIGH			0.8			0.8	V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

H

DC characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V, $\overline{OE}$ = HIGH		15		15	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, $\overline{OE}$ = HIGH					
		f = 20MHz		90		90	mA
		f = 10MHz		48		48	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	-75	75	-75	75	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}	-75	75	-75	75	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V	-40	40	-40	40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}	-40	40	-40	40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max		-150		-150	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note:

1. Actual test conditions may vary from those shown, but guarantee operation as specified.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
t_{CY}	Cycle Time	V_{DD} = Min	50		50		ns
t_{PWL}	Clock Pulse Width LOW	V_{DD} = Min	20		20		ns
t_{PWH}	Clock Pulse Width HIGH	V_{DD} = Min	20		20		ns
t_S	Input Setup Time		15		20		ns
$t_{S(SI)}$	Input Setup Time, SI_{21-6}, FT_1 = HIGH		25		28		ns
	FT_1 = LOW		18		20		ns
t_H	Input Hold Time		2		3		ns
$t_{H(SI)}$	Input Hold Time, SI_{21-6}		5		5		ns
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		30		30	ns
t_{DC}	Output Delay, Cascaded	V_{DD} = Min, C_{LOAD} = 10pF		20		20	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF	5		5		ns
t_{ENA}	Three-State Output, Enable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF		20		25	ns
t_{DIS}	Three-State Output, Disable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF		15		20	ns

Note:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}

Application Discussion

Loading and Updating of Coefficients

Because of the TMC2243's internal architecture, its impulse response is C_3, C_2, C_1, where C_3 is the rightmost coefficient and C_1 is the leftmost. However, for glitchless performance, coefficients must be updated from left to right: C_1 then C_2 then C_3.

For example, consider an adaptive filter whose first set of coefficients is A_i, second set is B_i and third set is C_i (Figure 4). First, the TMC2243 is initialized with A_i. If these are loaded in numerical (left to right) sequence, two of the first three data points can be loaded with them, as shown in Figure 4. Immediately after the third coefficient is loaded, the first coefficient of the next set can be loaded, if desired, along with the third data point.

Table 1. Impulse Response

FT_{3-1}	Response					
000	C_3	0	C_2	0	C_1	0
001	C_3	0	C_2	0	C_1	
010	C_3	0	C_2	C_1	0	
011	C_3	0	C_2	C_1		
100	C_3	C_2	0	C_1	0	
101	C_3	C_2	0	C_1		
110	C_3	C_2	C_1	0		
111	C_3	C_2	C_1			

Notes:
1. C_3 is the rightmost coefficient, C_1 is the leftmost.
2. FT_1 is relevant only if SUMIN is used. When multiple chips are cascaded, FT_1 = LOW places a zero stage between their concatenated impulse responses.

Building Longer Filters

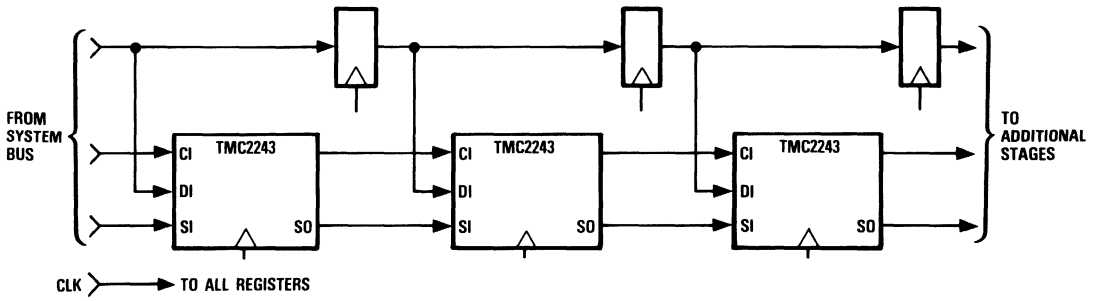
To build a filter of more than three non-zero stages, merely concatenate a series of TMC2243s. The coefficient inputs may be connected to the data bus, a separate common coefficient bus, or separate buses, depending on system architecture, memory and bus resources, and coefficient updating requirements. The data inputs are connected to a common bus. If the first feedthrough register is used (and a zero stage is not desired there), an external register should be inserted in the data input path for proper timing (Figure 9).

The 16-bit Sum-Out port of each TMC2243 is connected to the Sum-In port of the next TMC2243 in the chain; the filter output is the Sum-Out port of the last TMC2243. Since the 6 LSBs of each TMC2243's accumulation pipeline are not output, each TMC2243 incorporates a rounding increment of 1 into the sixth bit, to minimize bias.

When TMC2243s are cascaded in this fashion, the minimum permissible clock period is the sum of the output delay and the Sum-In port's input setup time. When the Input Registers are enabled (that is, FT_1 = LOW), full 20MHz performance can be obtained.

All data and coefficient inputs and outputs are two's complement representation, whose relative scaling is presented in the Data Formats table, Figure 1. Although the data values are shown in fractional format, the user can arbitrarily rescale them, as long as consistency is maintained.

Figure 9. Basic Diagram for Stacking the TMC2243 for High-Speed Operation (no zero tap desired between each TMC2243, all FT_1 = LOW)



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2243G8C	STD–T_A=0°C to 70°C	Commercial	68 Pin Grid Array	2243G8C
TMC2243G8V	EXT–T_C= –55°C to 125°C	MIL-STD-883	68 Pin Grid Array	2243G8V
TMC2243H8C	STD–T_A=0°C to 70°C	Commercial	69 Pin Plastic Pin Grid Array	2243H8C

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TMC2246

CMOS Image Filter

11 x 10 Bit, 40MHz

The TMC2246 is a video speed convolutional array composed of four 11 x 10 bit registered multipliers followed by a summer and an accumulator. All eight multiplier inputs are accessible to the user and may be updated every clock cycle with integer or fractional two's complement data. A pipelined architecture, fully registered input and output ports, and asynchronous three-state output enable control simplify the design of complex systems.

The data or coefficient inputs to the multipliers may be held over multiple clock cycles, providing storage for mixing and filtering coefficients. The 25-bit accumulator path of the TMC2246 allows two bits of cumulative word growth which may be internally rounded to 16 bits. Output data are updated every 25ns clock cycle, and may be held under user control. All data inputs, outputs, and controls are TTL compatible and are registered on the rising edge of clock, except the three-state output enable.

The TMC2246 is uniquely suited to performing pixel interpolation in image manipulation and filtering applications. As a companion to the TRW TMC2301 Image Resampling Sequencer, the TMC2246 Image Filter can execute a bilinear interpolation of an image (4-pixel kernels) at real-time video rates. Larger kernels or other more complex functions can be realized with no loss in performance by utilizing multiple devices.

With unrestricted access to all data and coefficient input ports, the TMC2246 offers considerable flexibility in applications performing digital filtering, adaptive FIR filters, mixers, and other similar systems requiring high-speed processing.

Fabricated using TRWs proprietary OMICRON-C™ one-micron CMOS process, the TMC2246 operates at a guaranteed clock rate of 40MHz over the full temperature and supply voltage ranges, and is available in a 120 pin plastic pin grid array.

Features

- 40MHz Data And Coefficient Input And Computation Rate
- Four 11 x 10 Bit Multipliers With Individual Data And Coefficient Inputs And 25-Bit Accumulator
- User-Selectable Fractional Or Integer Two's Complement Data Formats
- Input And Output Data Latches, With User-Configurable Enables
- User-Selectable 16-Bit Rounded Output
- Fully Registered, Pipelined Architecture
- Low Power Consumption CMOS Process
- Single +5V Power Supply
- Available In A 120 Pin Plastic Pin Grid Array

Applications

- Fast Pixel Interpolation
- Fast Image Manipulation
- Image Mixing And Keying
- High-Performance FIR Filters
- Adaptive Digital Filters
- One And Two Dimensional Image Processing

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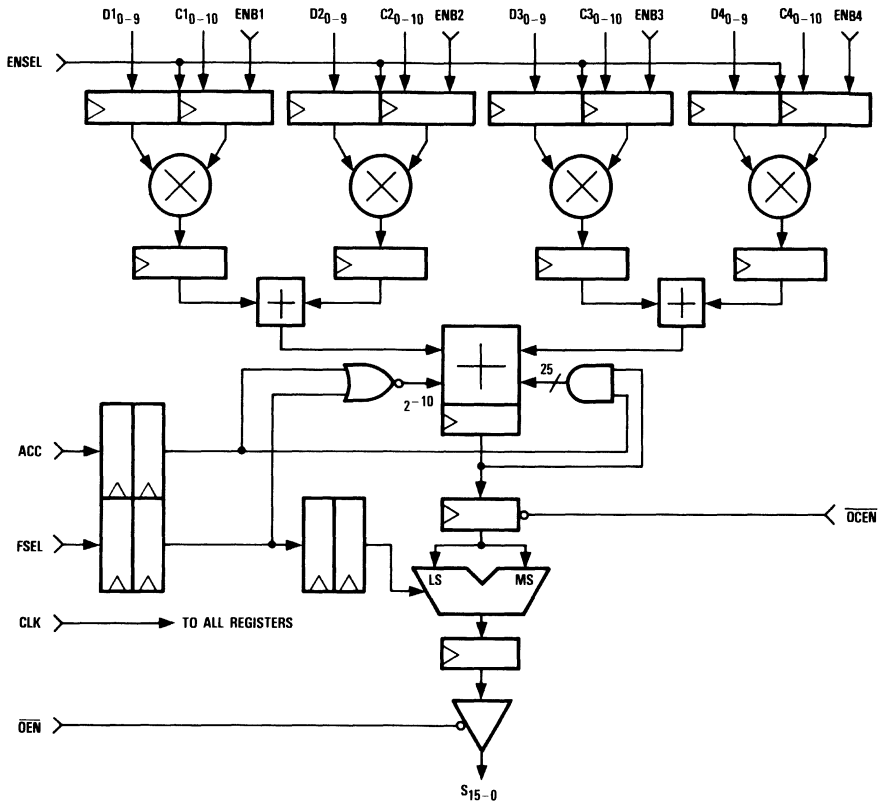
Functional Block Diagram



Functional Description

General Information

The TMC2246 Image Filter is a flexible multiplier-summer array which computes the accumulated sum of four 11 x 10 bit products, allowing word growth up to 25 bits. The inputs are user-configurable, allowing latching of either the 10 or 11-bit input data. The data format is user-selectable between integer or fractional two's complement arithmetic. Total latency from input registers to output data port is five clocks. The output data path is 16 bits wide, providing the lower 16 bits of the accumulator when in integer format or the upper 16 bits of the 25-bit accumulator path when fractional two's complement notation is selected. One-time rounding to 16 bits is performed when accumulating fractional data, which is disabled when operating in integer format to maintain the integrity of the least-significant bits.

Signal Definitions

Power

V_{DD}, GND — The TMC2246 operates from a single +5V supply. All pins must be connected.

Clock

CLK — The TMC2246 operates from a single master clock input. The rising edge of clock strobes all enabled registers. All timing specifications are referenced to the rising edge of clock.

Inputs

D1$_{9-0}$ – D4$_{9-0}$ — D1 through D4 are the 10-bit data input ports. The LSB is Dx$_0$. See *Figure 1*.

Inputs (cont.)

$C1_{10-0}$ – $C4_{10-0}$ C1 through C4 are the 11-bit coefficient input ports. The LSB is Cx_0. See *Figure 1*.

Outputs

S_{15-0} The current 16-bit result is available at the Sum output. The LSB is S_0. See *Figure 1*.

Controls

FSEL Data input during the current clock is assumed to be in fractional two's complement format, rounding to 16 bits is performed as determined by the accumulator control ACC, and the upper 16 bits of the accumulator are output when the registered Format Select input is LOW. When FSEL is HIGH, two's complement integer format is assumed, and the lower 16 bits of the accumulator are presented at the output. No rounding is performed when operating in integer mode. See *Figure 1* and the *Applications Discussion*.

ENSEL The registered Enable Select determines whether the data or the coefficient input registers may be held on the next rising edge of clock, in conjunction with the individual input enables ENB1 – ENB4. See *Figure 2*.

ENB1 – ENB4 When ENBi (i = 1, 2, 3, or 4) is LOW, registers Ci and Di are both strobed by the next rising edge of CLK. When ENBi is HIGH and ENSEL is LOW, Di is strobed, but Ci is held. When ENBi and ENSEL are both HIGH, Di is held and Ci is strobed. See *Figure 2*. Thus, either or both input registers to each multiplier are updated on each clock cycle.

Figure 2. Input Register Control

ENB1 – 4	ENSEL	Input Register Held
1	1	Data i
1	0	Coefficient i
0	X	None

Where X denotes a "Don't Care" condition. Any register not explicitly held is updated on the next rising edge of clock.

ACC When the registered Accumulator control is LOW, no internal accumulation will be performed on the data input during the current clock, effectively clearing the prior accumulated sum. If operating in fractional two's complement format (FSEL = LOW), one-half LSB rounding to 16 bits is performed on the result. This allows the user to perform summations without propagating roundoff errors. When ACC is HIGH, the internal accumulator adds the emerging product to the sum of previous products, without performing additional rounding.

$\overline{OCEN}$ The output of the accumulator is latched into the output register on the next clock when the registered Clock Enable is LOW. When $\overline{OCEN}$ is HIGH the contents of the output register remain unchanged, however accumulation will continue internally if ACC remains HIGH.

$\overline{OEN}$ Data currently in the output registers is available at the output bus S_{15-0} when the asynchronous Output Enable is LOW. When $\overline{OEN}$ is HIGH, the outputs are in the high-impedance state.

H

Figure 1. Data Formats

Fractional Two's Complement Format (FSEL = LOW)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						-2^0	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	DATA (D_{1-4})
					-2^1	2^0	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	COEFFICIENT (C_{1-4})
-2^6	2^5	2^4	2^3	2^2	2^1	2^0	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	SUM

Integer Two's Complement Format (FSEL = HIGH)

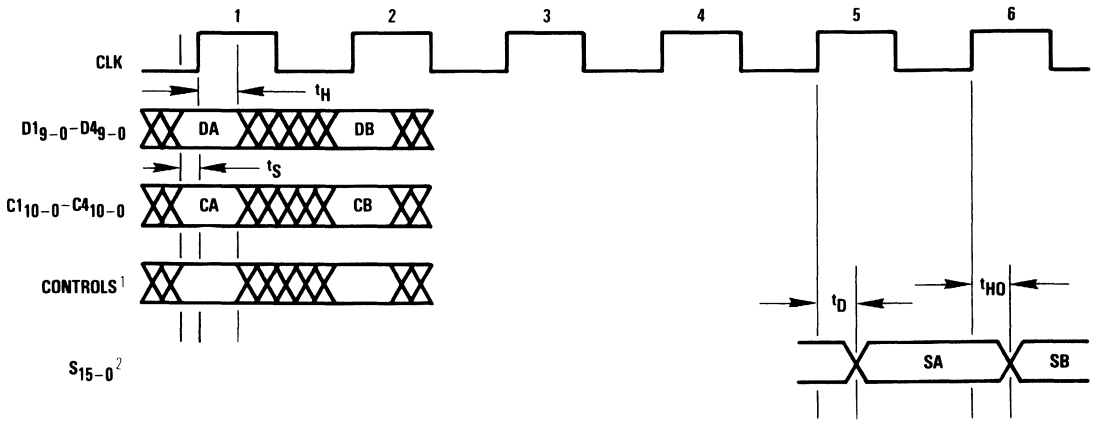
						-2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DATA (D_{1-4})
					-2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	COEFFICIENT (C_{1-4})
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	SUM

Note: A minus sign indicates the sign bit.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins	L5 Package Pins
Power	V_{DD}	Supply Voltage	F3, H3, L7, C8	13, 21, 50, 112
	GND	Ground	E3, G3, J3, L6, H11, C7	9, 17, 25, 46, 79, 116
Clock	CLK	System Clock	C3	2
Inputs	$D1_{9-0}$	D1 Input	M1, K3, L2, N1, L3, M2, N2, L4, M3, N3	28, 29, 30, 31, 35, 36, 37, 38, 39, 40
	$D2_{9-0}$	D2 Input	J12, K13, J11, K12, L13, L12, K11, M13, M12, L11	77, 76, 75, 74, 73, 72, 71, 70, 69, 68
	$D3_{9-0}$	D3 Input	J13, H12, H13, G12, G11, G13, F13, F12, F11, E13	78, 80, 81, 82, 83, 84, 85, 86, 87, 88
	$D4_{9-0}$	D4 Input	B4, C5, A4, B5, A5, C6, B6, A6, A7, B7	125, 124, 123, 122, 121, 120, 119, 118, 117, 115
	$C1_{10-0}$	C1 Input	M4, L5, N4, M5, N5, M6, N6, M7, N7, N8, M8	41, 42, 43, 44, 45, 47, 48, 49, 51, 52, 53
	$C2_{10-0}$	C2 Input	N13, M11, L10, N12, N11, M10, L9, N10, M9, N9, L8	64, 63, 62, 61, 60, 59, 58, 57, 56, 55, 54
	$C3_{10-0}$	C3 Input	E12, D13, E11, D12, C13, B13, D11, C12, A13, C11, B12	89, 90, 91, 92, 93, 94, 95, 96, 97, 101, 102
	$C4_{10-0}$	C4 Input	A8, B8, A9, B9, A10, C9, B10, A11, B11, C10, A12	114, 113, 111, 110, 109, 108, 107, 106, 105, 104, 103
Outputs	S_{15-0}	Sum Output	C1, D2, D1, E2, E1, F2, F1, G2, G1, H1, H2, J1, J2, K1, K2, L1	7, 8, 10, 11, 12, 14, 15, 16, 18, 19, 20, 22, 23, 24, 26, 27
Controls	FSEL	Format Select	B2	3
	ENSEL	Enable Select	A1	130
	ENB1 – ENB4	Input Enables	C4, A2, A3, B3	128, 127, 126, 129
	ACC	Accumulate	B1	4
	$\overline{OCEN}$	Output Register Enable	D3	5
	$\overline{OEN}$	Output Enable	C2	6
No Connect		Not Connected	D4 (Index Pin)	1, 32, 33, 34, 65, 66, 67, 98, 99, 100, 131, 132

Figure 3. Timing Diagram



Notes: 1. Except $\overline{OEN}$.
2. Assumes $\overline{OEN}$ = LOW.

Figure 4. Equivalent Input Circuit

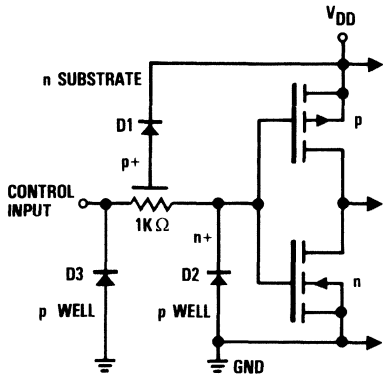


Figure 5. Equivalent Output Circuit

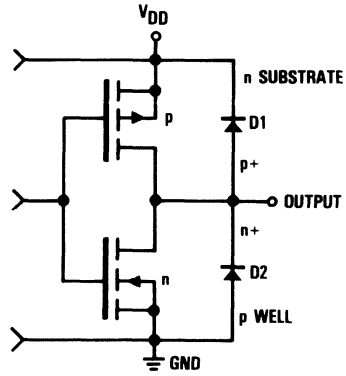
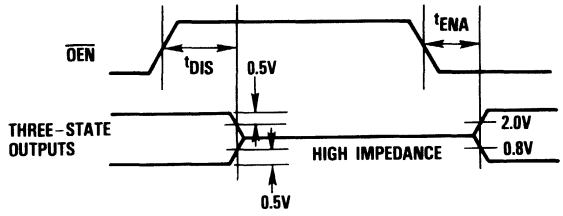


Figure 6. Threshold Levels for Three-State Measurement



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD} + 0.5)V

Output

Applied voltage [2] ..... −0.5 to (V_{DD} + 0.5)V

Forced current [3,4] ..... −6.0 to 6.0mA

Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −60 to +130°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Test Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage		4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW				0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0			2.0			V
I_{OL}	Output Current, Logic LOW				4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH				−2.0			−2.0	mA
t_{CY}	Cycle Time	V_{DD} = Min							
		TMC2246	33						ns
		TMC2246-1	25						ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD} = Min							
		TMC2246	15						ns
		TMC2246-1	10						ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD} = Min	10						ns
t_S	Input Setup Time	TMC2246	10						ns
		TMC2246-1	8						ns
t_H	Input Hold Time		2						ns
T_A	Ambient Temperature, Still Air		0		70				°C
T_C	Case Temperature					−55		125	°C

Electrical characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		6			mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, $\overline{OEN}$ = 5V, f = 30MHz		100			mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	−10		−10		µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	µA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V	−40		−40		µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	µA
I_{OS}	Short-Circuit Output	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		60		60	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but operation is guaranteed as specified.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended [2]		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 25pF					
		TMC2246		15			ns
		TMC2246-1		13			ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 25pF	5				ns
t_{ENA}	Three-State Output Enable Delay [1]	V_{DD} = Min, C_{LOAD} = 25pF		15			ns
t_{DIS}	Three-State Output Disable Delay [1]	V_{DD} = Min, C_{LOAD} = 25pF		20			ns

Notes: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.
2. Consult factory for extended temperature specifications.

H

Applications Discussion

Demonstration of Operation

The versatile input clock enables and unrestricted data and coefficient inputs provided on the TMC2246 allow considerable flexibility in numerous image and signal processing architectures. *Figure 7* shows a typical sequence of operations which clarifies the inherent clock latencies of the device and illustrates fixed coefficient storage, product accumulation, and device reconfiguration prior to beginning a new accumulation. This assumes that the device is set to fractional two's complement mode (FSEL = LOW), with $\overline{OCEN}$ = LOW, $\overline{OEN}$ = LOW, and the input registers configured to hold coefficients only (ENSEL = LOW). X = "don't care."

Figure 7. Typical TMC2246 Operation Sequence

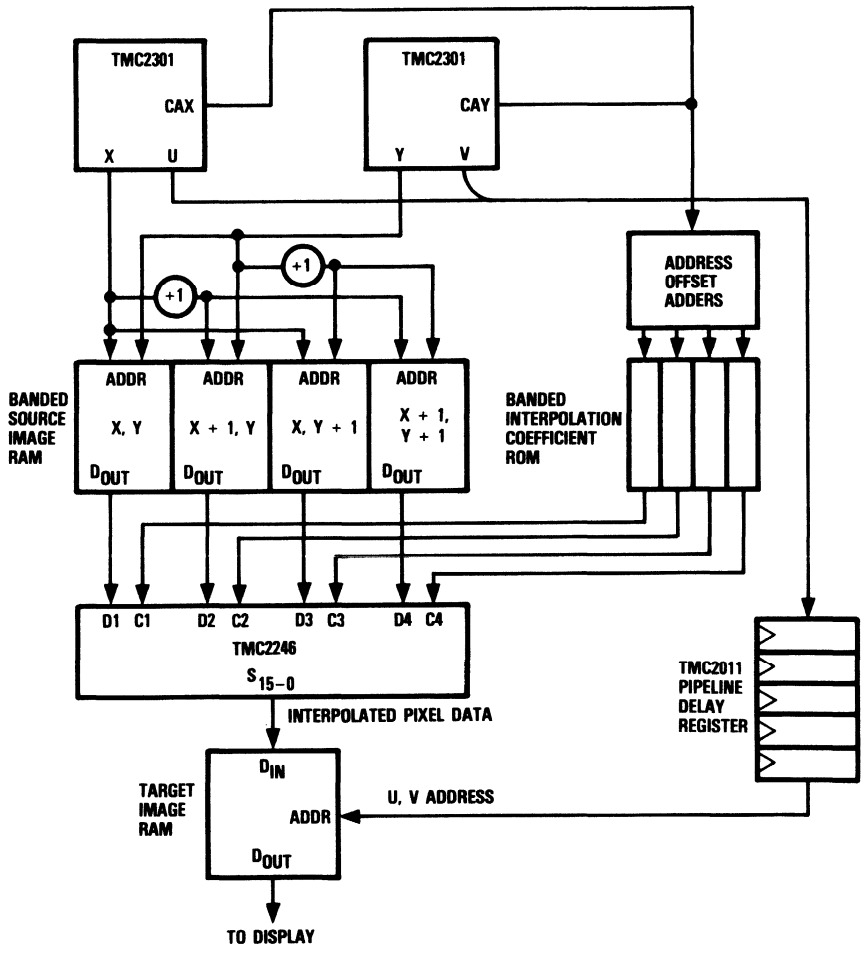
CLK	D1	C1	ENB_1	D2	C2	ENB_2	D3	C3	ENB_3	D4	C4	ENB_4	ACC	Sum
0	–	–	0	–	–	0	–	–	0	–	–	0	–	–
1	D1(1)	C1(1)	1	D2(1)	C2(1)	1	D3(1)	C3(1)	1	D4(1)	C4(1)	1	0	–
2	D1(2)	X	0	D2(2)	X	0	D3(2)	X	1	D4(2)	X	1	1	–
3	D1(3)	C1(3)	0	D2(3)	C2(3)	0	D3(3)	X	0	D4(3)	X	0	1	
4	D1(4)	C1(4)	–	D2(4)	C2(4)	–	D3(4)	C3(4)	–	D4(4)	C4(4)	–	0	
5														$S(5) = D1(1)C1(1) + D2(1)C2(1) + D3(1)C3(1) + D4(1)C4(1) + 2^{-10}$
6														$S(6) = S(5) + D1(2)C1(1) + D2(2)C2(1) + D3(2)C3(1) + D4(2)C4(1)$
7														$S(7) = S(6) + D1(3)C1(3) + D2(3)C2(3) + D3(3)C3(1) + D4(3)C4(1)$
8														$S(8) = D1(4)C1(4) + D2(4)C2(4) + D3(4)C3(4) + D4(4)C4(4) + 2^{-10}$

Notice in this example, operating in fractional two's complement mode, that rounding is imposed on the first cycle only of an accumulation. This avoids the propagation of accumulated roundoff errors.

Using the TMC2246 for Pixel Interpolation

As a companion product to the TMC2301 Image Resampling Sequencer, the TMC2246 offers an excellent tool for performing high-speed pixel interpolation and image filtering. Any pixel resampling operation with multiple-pixel kernels must utilize some parallel-processing technique, such as memory banding, in order to maintain high-speed image throughput rates. Memory Banding utilizes adders to generate parallel offset addresses, allowing the user to access multiple pixel locations simultaneously. Using such techniques, one TMC2246 can perform bilinear interpolation (four-pixel kernel) with no loss in system performance. Larger kernels can be realized in similar systems with additional TMC2246s. See TRW *Application Brief AB-4, "Performing Bilinear Interpolation Using the TMC2301". Figure 8* illustrates a basic pixel interpolation application.

Figure 8. Bilinear Interpolation Using the TMC2246

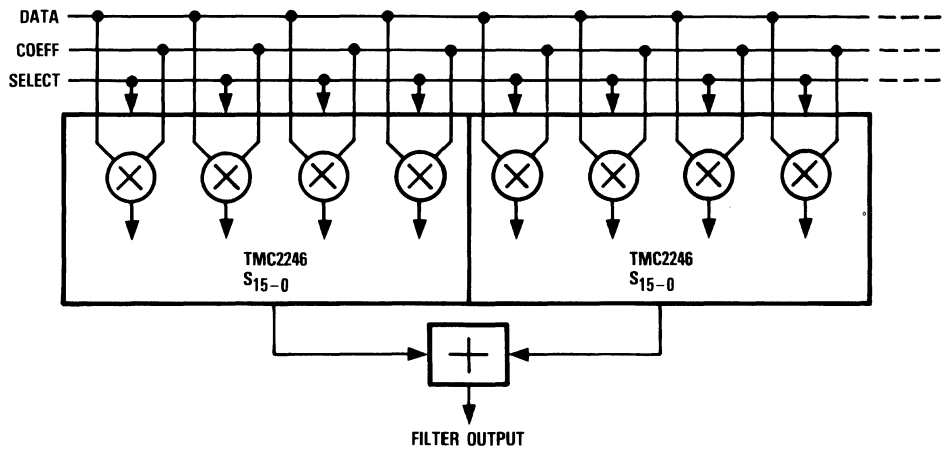


TMC2246 Applications in Digital Filtering

Unrestricted access to all input ports of the TMC2246 allows the user considerable flexiblity in realizing numerous digital filter architectures. *Figure 9* illustrates how the device may be utilized as a flexible high-speed FIR Filter with the ability to modify all of the filter coefficients dynamically or to store a fixed set if desired.

Longer filters, with more taps, are realized by including an external adder (such as the common 74381 type) to cascade multiple TMC2246s. Alternatively, two additional taps and a cascading adder are available in the TRW *TMC2249 Digital Mixer*.

Figure 9. Utilization of the TMC2246 for FIR Filtering

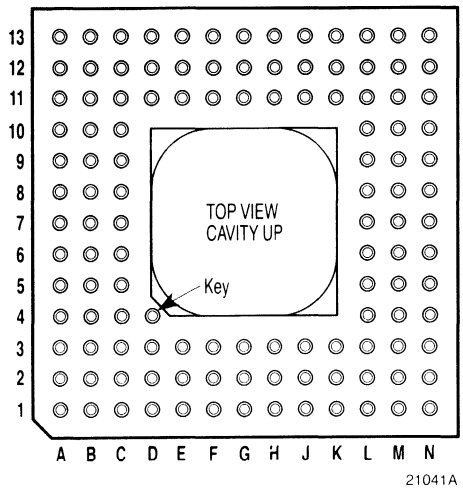


Pin Assignments – 120 Pin Plastic Pin Grid Array, H5 Package

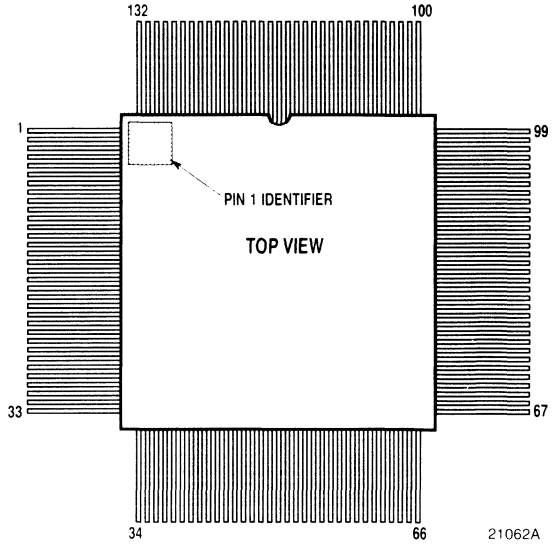
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
C3	CLK	G3	GND	L3	$D1_5$	L7	V_{DD}	L11	$D2_0$	G11	$D3_5$	C11	$C3_1$	C7	GND
B2	FSEL	G1	S_7	M2	$D1_4$	N7	$C1_2$	M12	$D2_1$	G13	$D3_4$	B12	$C3_0$	A7	$D4_1$
B1	ACC	H1	S_6	N2	$D1_3$	N8	$C1_1$	M13	$D2_2$	F13	$D3_3$	A12	$C4_0$	A6	$D4_2$
D3	$\overline{OCEN}$	H2	S_5	L4	$D1_2$	M8	$C1_0$	K11	$D2_3$	F12	$D3_2$	C10	$C4_1$	B6	$D4_3$
C2	$\overline{OEN}$	H3	V_{DD}	M3	$D1_1$	L8	$C2_0$	L12	$D2_4$	F11	$D3_1$	B11	$C4_2$	C6	$D4_4$
C1	S_{15}	J1	S_4	N3	$D1_0$	N9	$C2_1$	L13	$D2_5$	E13	$D3_0$	A11	$C4_3$	A5	$D4_5$
D2	S_{14}	J2	S_3	M4	$C1_{10}$	M9	$C2_2$	K12	$D2_6$	E12	$C3_{10}$	B10	$C4_4$	B5	$D4_6$
E3	GND	K1	S_2	L5	$C1_9$	N10	$C2_3$	J11	$D2_7$	D13	$C3_9$	C9	$C4_5$	A4	$D4_7$
D1	S_{13}	J3	GND	N4	$C1_8$	L9	$C2_4$	K13	$D2_8$	E11	$C3_8$	A10	$C4_6$	C5	$D4_8$
E2	S_{12}	K2	S_1	M5	$C1_7$	M10	$C2_5$	J12	$D2_9$	D12	$C3_7$	B9	$C4_7$	B4	$D4_9$
E1	S_{11}	L1	S_0	N5	$C1_6$	N11	$C2_6$	J13	$D3_9$	C13	$C3_6$	A9	$C4_8$	A3	ENB3
F3	V_{DD}	M1	$D1_9$	L6	GND	N12	$C2_7$	H11	GND	B13	$C3_5$	C8	V_{DD}	A2	ENB2
F2	S_{10}	K3	$D1_8$	M6	$C1_5$	L10	$C2_8$	H12	$D3_8$	D11	$C3_4$	B8	$C4_9$	C4	ENB1
F1	S_9	L2	$D1_7$	N6	$C1_4$	M11	$C2_9$	H13	$D3_7$	C12	$C3_3$	A8	$C4_{10}$	B3	ENB4
G2	S_8	N1	$D1_6$	M7	$C1_3$	N13	$C2_{10}$	G12	$D3_6$	A13	$C3_2$	B7	$D4_0$	A1	ENSEL

Pin Assignments – 132 Leaded CERQUAD, L5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	23	S_3	45	$C1_6$	67	NC	89	$C3_{10}$	111	$C4_8$
2	CLK	24	S_2	46	GND	68	$D2_0$	90	$C3_9$	112	V_{DD}
3	FSEL	25	GND	47	$C1_5$	69	$D2_1$	91	$C3_8$	113	$C4_9$
4	ACC	26	S_1	48	$C1_4$	70	$D2_2$	92	$C3_7$	114	$C4_{10}$
5	OCENB	27	S_0	49	$C1_3$	71	$D2_3$	93	$C3_6$	115	$D4_0$
6	OENB	28	$D1_9$	50	V_{DD}	72	$D2_4$	94	$C3_5$	116	GND
7	S_{15}	29	$D1_8$	51	$C1_2$	73	$D2_5$	95	$C3_4$	117	$D4_1$
8	S_{14}	30	$D1_7$	52	$C1_1$	74	$D2_6$	96	$C3_3$	118	$D4_2$
9	GND	31	$D1_6$	53	$C1_0$	75	$D2_7$	97	$C3_2$	119	$D4_3$
10	S_{13}	32	NC	54	$C2_0$	76	$D2_8$	98	NC	120	$D4_4$
11	S_{12}	33	NC	55	$C2_1$	77	$D2_9$	99	NC	121	$D4_5$
12	S_{11}	34	NC	56	$C2_2$	78	$D3_9$	100	NC	122	$D4_6$
13	V_{DD}	35	$D1_5$	57	$C2_3$	79	GND	101	$C3_1$	123	$D4_7$
14	S_{10}	36	$D1_4$	58	$C2_4$	80	$D3_8$	102	$C3_0$	124	$D4_8$
15	S_9	37	$D1_3$	59	$C2_5$	81	$D3_7$	103	$C4_0$	125	$D4_9$
16	S_8	38	$D1_2$	60	$C2_6$	82	$D3_6$	104	$C4_1$	126	EN3B
17	GND	39	$D1_1$	61	$C2_7$	83	$D3_5$	105	$C4_2$	127	EN2B
18	S_7	40	$D1_0$	62	$C2_8$	84	$D3_4$	106	$C4_3$	128	EN1B
19	S_6	41	$C1_{10}$	63	$C2_9$	85	$D3_3$	107	$C4_4$	129	EN4B
20	S_5	42	$C1_9$	64	$C2_{10}$	86	$D3_2$	108	$C4_5$	130	ENSEL
21	V_{DD}	43	$C1_8$	65	NC	87	$D3_1$	109	$C4_6$	131	NC
22	S_4	44	$C1_7$	66	NC	88	$D3_0$	110	$C4_7$	132	NC



120 Pin Plastic Pin Grid Array – H5 Package



132 Leaded CERQUAD – L5 Package

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2246H5C	STD–T_A=0°C to 70°C	Commercial	120 Pin Plastic Pin Grid Array	2246H5C
TMC2246H5C1	STD–T_A=0°C to 70°C	Commercial	120 Pin Plastic Pin Grid Array	2246H5C1
TMC2246L5V	EXT–T_C= –55°C to 125°C	MIL-STD-883	132 Leaded CERQUAD	2246L5V
TMC2246L5V1	EXT–T_C= –55°C to 125°C	MIL-STD-883	132 Leaded CERQUAD	2246L5V1

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TMC2249

CMOS Digital Mixer

12 x 12 Bit, 30MHz

The TMC2249 is a high-speed digital arithmetic circuit consisting of two 12-bit multipliers, an adder and a cascadeable accumulator. All four multiplier inputs are accessible to the user, and each includes a user-programmable pipeline delay of up to 16 clocks in length. The 24-bit adder/subtractor is followed by an accumulator and 16-bit input port which allows the user to cascade multiple TMC2249s. A new 16-bit accumulated output is available every clock, up to the maximum rate of 30MHz. All inputs and outputs are registered except the three-state output enable, and all are TTL compatible.

The TMC2249 utilizes a pipelined, bus-oriented structure offering significant flexibility. Input register clock enables and programmable input data pipeline delays on each port offer an adaptable input structure for high-speed digital systems. Following the multipliers, the user may perform addition or subtraction of either product, arithmetic rounding to 16 bits, and accumulation and summation of products with a cascading input. The output port allows access to all 24 bits of the internal accumulator by switching between overlapping least and most-significant 16-bit words, and a three-state output enable simplifies a connection to an external system bus.

All programmable features are utilized on a clock-by-clock basis, with internal data and control pipeline registers provided to maintain synchronous operation between incoming data and all available functions within the device.

The TMC2249 has numerous applications in digital processing algorithms, from executing simple image mixing and switching, to performing complex arithmetic functions and complex waveform synthesis. FIR filters, digital quadrature mixers and modulators, and vector arithmetic functions may also be implemented with this device.

Fabricated using TRWs proprietary OMICRON-C™ one-micron CMOS process, the TMC2249 operates at a guaranteed clock rate of 30MHz over the standard commercial temperature and supply voltage ranges, and is available in a low-cost 120 pin plastic pin grid array.

Features

- 30MHz Input And Computation Rate
- Two 12-Bit Multipliers With Separate Data And Coefficient Inputs
- Independent, User-Selectable Pipeline Delays Of 1 to 16 Clocks On All Input Ports
- Separate 16-Bit Input Port Allows Cascading Or Addition Of A Constant
- User-Selectable Rounding Of Products
- Fully Registered, Pipelined Architecture
- Low Power Consumption CMOS Process
- Single +5V Power Supply
- Available In A 120 Pin Plastic Pin Grid Array

Applications

- Video Switching
- Image Mixing
- Digital Signal Modulation
- Complex Frequency Synthesis
- Digital Filtering
- Complex Arithmetic Functions

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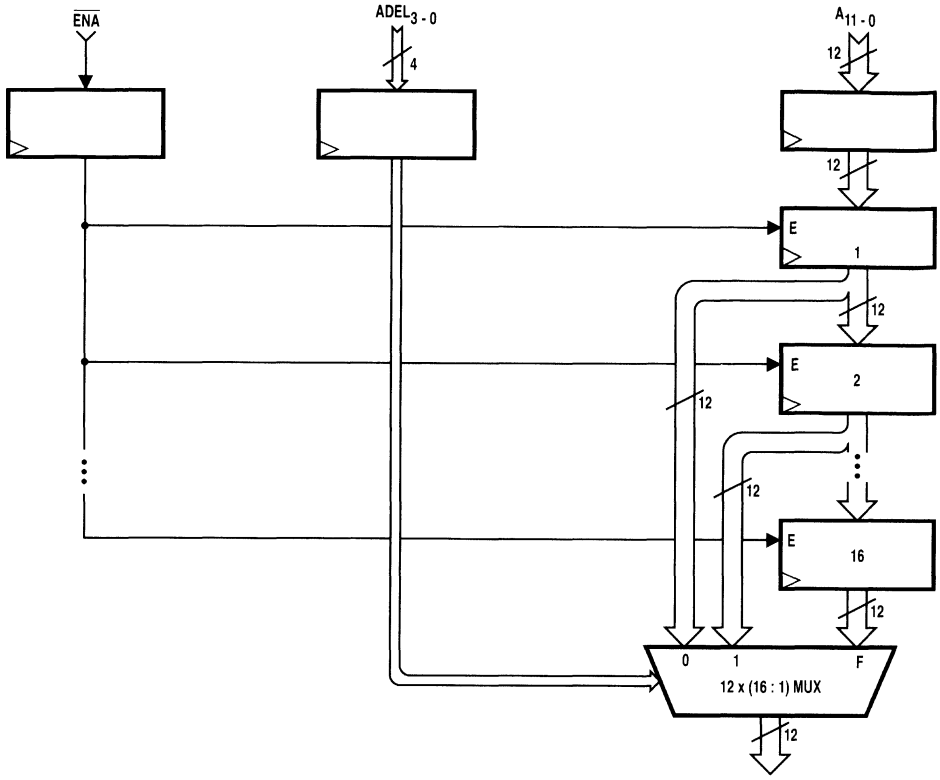
40G06125 Rev. C–11/90
Printed in the U.S.A.

Functional Block Diagram



Functional Description

General Information

The TMC2249 performs the summation of products described by the formula:

$$S(N+6) = A(N-ADEL)\bullet B(N-BDEL)\bullet(-1^{NEG1(N)}) + C(N-CDEL)\bullet D(N-DDEL)\bullet(-1^{NEG2(N)}) + CAS(N+3\bullet FT)$$

where ADEL through DDEL range from 1 to 16 pipe delays. All inputs and controls utilize pipeline delay registers to maintain synchronicity with the data input during that clock, except when the Cascade data input is routed directly to the accumulator by use of the Feedthrough control. One-half LSB rounding to 16 bits may be performed on the sum of products while summing with the cascade input data. The user may access either the upper or lower 16 bits of the 24-bit accumulator by swapping overlapping registers. The output bus has an asynchronous high-impedance enable, to simplify interfacing to complex systems.

Signal Definitions

Power

V_{DD}, GND — The TMC2249 operates from a single +5V supply. All power and ground pins must be connected.

Clock

CLK — The TMC2249 operates from a single master clock input. The rising edge of clock strobes all enabled registers. All timing specifications are referenced to the rising edge of clock.

Inputs

A_{11-0} – D_{11-0} A through D are the four 12-bit registered data input ports. A_0-D_0 are the LSBs. See ***Table 1***. Data presented to the input ports is clocked in to the top of the 16-stage delay pipeline on the next clock when enabled, "pushing" data down the register stack.

CAS_{15-0} CAS is the 16-bit Cascade data input port. CAS_0 is the LSB. See ***Table 1***.

Outputs

S_{15-0} The current 16-bit result is available at the Sum output. The LSB is S_0. The output may be the most or least significant 16 bits of the current accumulator output, as determined by $\overline{SWAP}$. S_0 is the LSB. See ***Table 1***.

Controls

$\overline{ENA}$ – $\overline{END}$ Input data presented to port i11-0 (i = A, B, C, or D) are latched into delay pipeline i, and data already in pipeline i advance by one register position, on each rising edge of CLK for which ENi is LOW. When ENi is HIGH, the data in pipeline i do not move and the value at the input port i will be lost before it reaches the multiplier.

$ADEL_{3-0}$ – $DDEL_{3-0}$ ADEL through DDEL are the four-bit registered input data pipe delay select word inputs. Data to be presented to the multipliers is selected from one of sixteen stages in the input data delay pipe registers, as indicated by the delay select word presented to the respective input port during that clock. The minimum delay is one clock (select word = 0000), and the maximum delay is 16 clocks (select word = 1111). Following powerup these values are indeterminate and must be initialized by the user.

NEG1, NEG2 The products of the multipliers are negated, causing a subtraction to be performed during the internal summation of products, when the Negate controls are HIGH. NEG1 negates the product A x B, while NEG2 acts on the output of the multiplier which generates the product C x D. These controls indicate the operation to be performed on data input during the current clock, when the length controls ADEL – DDEL are set to zero.

RND When the rounding control is HIGH, the sum of products resulting from data input during that clock is rounded to 16 bits. Rounding is performed only during the first cycle of each accumulation sequence, to avoid the accumulation of roundoff errors.

FT When the Feedthrough control is HIGH, the pipeline delay through the cascade data path is minimized to simplify the cascading of multiple devices. When FT is LOW and ADEL through DDEL are all set to 0, the data inputs are aligned, such that $S(n+6) = CAS(n) + A(n)B(n) + C(n)D(n)$. See ***Table 2***.

$\overline{CASEN}$ Data presented at the cascade data input port are latched and accumulated internally when the input enable $\overline{CASEN}$ during that clock is LOW. When $\overline{CASEN}$ is HIGH, the cascade input port is ignored.

ACC When the registered Accumulator control is LOW, no internal accumulation will be performed on the data input during the current clock, effectively clearing the prior accumulated sum. When ACC is HIGH, the internal accumulator adds the emerging product to the sum of previous products.

$\overline{SWAP}$ The user may access both the most and least-significant 16 bits of the 24-bit accumulator by utilizing $\overline{SWAP}$. Normal operation of the device, with $\overline{SWAP}$ = HIGH, outputs the most significant word. Setting $\overline{SWAP}$ = LOW puts a double-register structure into "toggle" mode, allowing the user to examine the LSW on alternate clocks. New output data will not be clocked into the output registers until $\overline{SWAP}$ returns HIGH.

$\overline{OE}$ Data currently in the output registers is available at the output bus S_{15-0} when the asynchronous Output Enable is LOW. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state.

H

Table 1. Data Formats and Bit Weighting

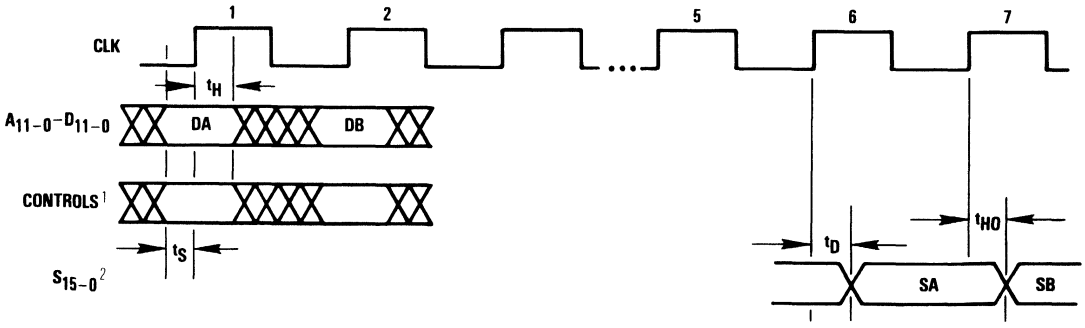
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
				-2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	DATA INPUT ($A_{11-0} - D_{11-0}$)
-2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	CASCADE INPUT (CAS_{15-0})
																SUM (S_{15-0})
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	LSW
-2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	MSW

Note: 1. A minus sign indicates the sign bit.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins	L5 Package Pins
Power	V_{DD}	Supply Voltage	F3, H3, L7, C8	13, 21, 50, 112
	GND	Ground	E3, G3, J3, L6, H11, C7	9, 17, 25, 46, 79, 116
Clock	CLK	System Clock	C3	2
Inputs	A_{11-0}	A Input	N8, M8, L8, N9, M9, N10, L9, M10, N11, N12, L10, M11	52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63
	B_{11-0}	B Input	N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, L4	51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 39, 38
	C_{11-0}	C Input	A9, B9, A10, C9, B10, A11, B11, C10, A12, B12, C11, A13	111, 110, 109, 108, 107, 106, 105, 104, 103, 102, 101, 100
	D_{11-0}	D Input	B8, A8, B7, A7, A6, B6, C6, A5, B5, A4, C5, B4	113, 114, 115, 117, 118, 119, 120, 121, 122, 123, 124, 125
	$ADEL_{3-0}$	A Delay	L11, M12, M13, K11	68, 69, 70, 71
	$BDEL_{3-0}$	B Delay	M2, L3, N1, L2	36, 35, 31, 30
	$CDEL_{3-0}$	C Delay	D11, B13, C13, D12	95, 94, 93, 92
	$DDEL_{3-0}$	D Delay	A2, C4, B3, A1	127, 128, 129, 130
	CAS_{15-0}	Cascade Input	L13, K12, J11, K13, J12, J13, H12, H13, G12, G11, G13, F13, F12, F11, E13, E12	73, 74, 75, 76, 77, 78, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89
Outputs	S_{15-0}	Sum Output	C1, D2, D1, E2, E1, F2, F1, G2, G1, H1, H2, J1, J2, K1, K2, L1	7, 8, 10, 11, 12, 14, 15, 16, 18, 19, 20, 22, 23, 24, 26, 27
Controls	$\overline{ENA} - \overline{END}$	Input Enables	N13, N2, C12, A3	64, 37, 96, 126
	NEG1, NEG2	Negate	B1, D3	4, 5
	RND	Round	C2	6
	FT	Feedthrough	E11	91
	$\overline{CASEN}$	Cascade Enable	D13	90
	ACC	Accumulate	B2	3
	$\overline{SWAP}$	Swap Output Words	K3	29
	$\overline{OE}$	Output Enable	M1	28
No Connect	NC	None	L12	1, 32, 33, 34, 65, 66, 67, 72, 98, 99, 100, 131, 132
		Index Pin	D4	

Figure 1. Timing Diagram



Notes: 1. Except $\overline{OE}$.
2. Assumes $\overline{OE}$ = LOW, and ADEL – DDEL set to 0.

Figure 2. Equivalent Input Circuit

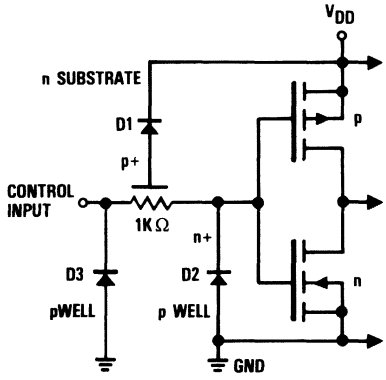


Figure 3. Equivalent Output Circuit

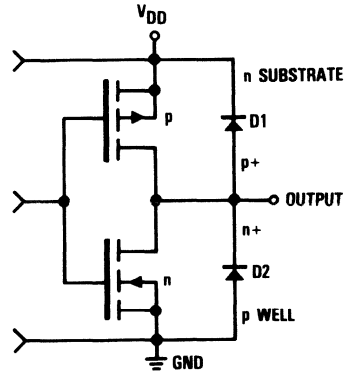
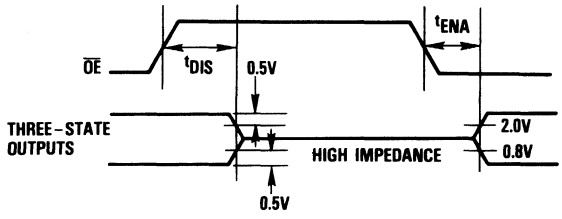


Figure 4. Threshold Levels for Three-State Measurement



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage [2]	−0.5 to (V_{DD} + 0.5)V
Forced current [3,4]	−6.0 to 6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 Second
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Nom	Standard Max	Extended [1] Min	Extended [1] Nom	Extended [1] Max	Units
V_{DD}	Supply Voltage		4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW				0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0			2.0			V
I_{OL}	Output Current, Logic LOW				4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH				−2.0			−2.0	mA
t_{CY}	Cycle Time	V_{DD} = Min							
		TMC2249	40						ns
		TMC2249-1	33						ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD} = Min	15						ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD} = Min	10						ns
t_S	Input Setup Time		8						ns
t_H	Input Hold Time		4						ns
T_A	Ambient Temperature, Still Air		0		70				°C
T_C	Case Temperature					−55		125	°C

Note: 1. Consult factory for extended temperature specifications.

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		6			mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, $\overline{OEN}$ = 5V, f = 25MHz		100			mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	−10		−10		μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V	−40		−40		μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		60		60	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but operation is guaranteed as specified.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 25pF					
		TMC2249		17			ns
		TMC2249-1		15			ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 25pF	5				ns
t_{ENA}	Three-State Output Enable Delay [1]	V_{DD} = Min, C_{LOAD} = 25pF		15			ns
t_{DIS}	Three-State Output Disable Delay [1]	V_{DD} = Min, C_{LOAD} = 25pF		20			ns

Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Applications Discussion

Basic Operation

The TMC2249 is a flexible signal and image processing building block with numerous user-selectable functions which expand it's usefulness. *Table 2* clarifies the operation of the device, demonstrating the various features available to the user and the timing delays incurred.

Table 2. TMC2249 Operation Sequence

CLK	ADEL	A_{11-0}	BDEL	B_{11-0}	CDEL	C_{11-0}	DDEL	D_{11-0}	NEG1	NEG2	CAS_{15-0}	FT	ACC	RND	$\overline{SWAP}$	S_{15-0}
1	0	A(1)	0	B(1)	0	C(1)	0	D(1)	L	L	—	L	L	L	H	—
2	0	A(2)	0	B(2)	0	C(2)	0	D(2)	L	H	—	L	L	L	H	—
3	0	A(3)	0	B(3)	0	C(3)	0	D(3)	H	L	—	L	L	L	H	—
4	0	A(4)	0	B(4)	0	C(4)	0	D(4)	L	L	CAS(4)	L	L	L	H	—
5	0	A(5)	0	B(5)	0	C(5)	0	D(5)	L	L	—	L	L	L	H	—
6	0	A(6)	0	B(6)	0	C(6)	0	D(6)	L	L	—	L	L	H	H	$(A(1)\cdot B(1)+C(1)\cdot D(1))_{ms}$
7	0	A(7)	0	B(7)	0	C(7)	0	D(7)	L	L	—	L	H	H	H	$(A(2)\cdot B(2)-C(2)\cdot D(2))_{ms}$
8	0	A(8)	0	B(8)	0	C(8)	0	D(8)	L	L	CAS(8)	H	L	L	L	$(-A(3)\cdot B(3)+C(3)\cdot D(3))_{ms}$
9	0	A(9)	0	B(9)	0	C(9)	0	D(9)	L	L	—	L	L	L	H	$(A(4)\cdot B(4)+C(4)\cdot D(4)+CAS(4))_{ms}$
10																$(A(5)\cdot B(5)+C(5)\cdot D(5)+CAS(8))_{ms}$
11																$(A(6)\cdot B(6)+C(6)\cdot D(6)+2^7)_{ms}$
12																$(A(7)\cdot B(7)+C(7)\cdot D(7)+S(11))_{ms}$
13																$(S(12))_{ls}$
14																$(A(9)\cdot B(8)+C(7)\cdot D(6))_{ms}$

Where H = HIGH, L = LOW. "ms" indicates most significant output word (bits 23 – 8), "ls" indicates least significant word (bits 15 – 0). The appropriates enables for the indicated data are assumed, otherwise '–' indicates that port not enabled. Note that the output data summation including A(8) – D(8) is lost, since the output on cycle 13 is swapped to the LSW of S(12) on cycle 8.

Digital Filtering

The input structure of the TMC2249 demonstrates great versatility when all four multiplier inputs and the programmable delay registers are utilized. *Tables 3* and *4* demonstrate how a direct-form symmetric FIR filter of up to 32 taps can be implemented. By utilizing the four input delay registers as pipelined storage banks, the user can store up to 32 coefficient-data word pairs, split into alternate "even" and "odd" halves. Two taps of the filter are calculated on each clock, and the user then increments/decrements the delay words (ADEL – DDEL). The sums of products are successively added to the global sum in the internal accumulator. Once all of the products of the desired taps have been summed, the resultant is available at the output. The user then "pushes" a new time-data sample on to the appropriate even or odd data register "stack" and reiterates the summation. Note that the coefficient bank "pointers", the BDEL and DDEL delay words, are alternately incremented and decremented on successive filter passes to maintain alignment between the incoming data samples and their respective coefficients. The effective filter speed is calculated by dividing the clock rate by one-half the number of taps implemented.

Table 3. Using the TMC2249 to Perform FIR Filtering — Initial Data Loading

Register Position (Hex)	Even Data A	Odd Data C	Coefficient B	Storage D
0	x(31)	x(30)	h(0)	h(1)
1	x(29)	x(28)	h(2)	h(3)
2	x(27)	x(26)	h(4)	h(5)
3	x(25)	x(24)	h(6)	h(7)
4	x(23)	x(22)	h(8)	h(9)
5	x(21)	x(20)	h(10)	h(11)
6	x(19)	x(18)	h(12)	h(13)
7	x(17)	x(16)	h(14)	h(15)
8	x(15)	x(14)	h(15)	h(14)
9	x(13)	x(12)	h(13)	h(12)
A	x(11)	x(10)	h(11)	h(10)
B	x(9)	x(8)	h(9)	h(8)
C	x(7)	x(6)	h(7)	h(6)
D	x(5)	x(4)	h(5)	h(4)
E	x(3)	x(2)	h(3)	h(2)
F	x(1)	x(0)	h(1)	h(0)

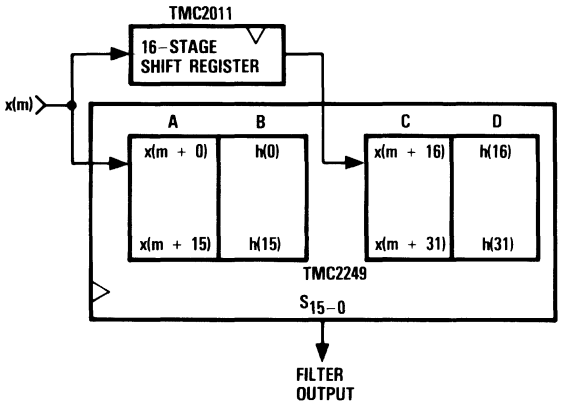
Table 4. FIR Filtering – Operation Sequence

Cycle	Push A	B	Push C	D	ADEL	CDEL	BDEL	DDEL	ACC	ENA	ENC	ENB	END	Convolution Sum	Resultant Output
1	–	–	–	–	0	0	0	0	H	H	H	H	H	x(31)•h(0) + x(30)•h(1)	
2	–	–	–	–	1	1	1	1	H	H	H	H	H	+ x(29)•h(2) + x(28)•h(3)	
3	–	–	–	–	2	2	2	2	H	H	H	H	H	+ x(27)•h(4) + x(26)•h(5)	
4	–	–	–	–	3	3	3	3	H	H	H	H	H	+ x(25)•h(6) + x(24)•h(7)	
5	–	–	–	–	4	4	4	4	H	H	H	H	H	+ x(23)•h(8) + (22)•h(9)	
6	–	–	–	–	5	5	5	5	H	H	H	H	H	+ x(21)•h(10) + x(20)•h(11)	
7	–	–	–	–	6	6	6	6	H	H	H	H	H	+ x(19)•h(12) + x(18)•(13)	
8	–	–	–	–	7	7	7	7	H	H	H	H	H	+ x(17)•h(14) + x(16)•h(15)	
9	–	–	–	–	8	8	8	8	H	H	H	H	H	+ x(15)•h(15) + (14)•h(14)	
10	–	–	–	–	9	9	9	9	H	H	H	H	H	+ x(13)•h(13) + x(12)•h(12)	
11	–	–	–	–	A	A	A	A	H	H	H	H	H	+ x(11)•h(11) + x(10)•h(10)	
12	–	–	–	–	B	B	B	B	H	H	H	H	H	+ X(9)•h(9) + x(8)•h(8)	
13	–	–	–	–	C	C	C	C	H	H	H	H	H	+ x(7)•h(7) + x(6)•h(6)	
14	–	–	–	–	D	D	D	D	H	H	H	H	H	+ x(5)•h(5) + x(4)•h(4)	
15	–	–	–	–	E	E	E	E	H	H	H	H	H	+ x(3)•h(3) + x(2)•h(2)	
16	–	–	x(32)	–	F	F	F	F	H	H	L	H	H	+ x(1)•h(1) + x(0)•h(0)	
17	–	–	–	–	0	0	F	F	H	H	H	H	H	x(31)•h(1) + x(32)•h(0)	
18	–	–	–	–	1	1	E	E	H	H	H	H	H	+ x(29)•h(3) + x(30)•h(2)	
19	–	–	–	–	2	2	D	D	H	H	H	H	H	+ x(27)•h(5) + x(28)•h(4)	
20	–	–	–	–	3	3	C	C	H	H	H	H	H	+ x(25)•h(7) + x(26)•h(6)	31
21	–	–	–	–	4	4	B	B	H	H	H	H	H	+ x(23)•h(9) + x(24)•h(8)	$S = \sum_{k=0} h(k)x(n-k)$
.															
.															
.															

Digital Filtering (cont.)

Alternatively, non-symmetric FIR Filters can be implemented using the TMC2249 in a similar fashion. Here, a shift register is used to delay the incoming data fed to the A input by an amount equal to one-half the length of the filter (the length of the A delay register). As shown in *Figure 5*, the data is then sent to the C input, thus "stacking" the A and C delay registers to create a single N-tap FIR filter. The incremented delay words (ADEL – DDEL) for all four inputs are identical. Again, the filter throughput is equal to the clock speed divided by one-half the number of taps implemented.

Figure 5. Non-Symmetric 32-Tap FIR Filtering Using the TMC2249



Complex Arithmetic Functions

The TMC2249 can also be used to perform complex arithmetic functions. The basic function performed by the device, ignoring the delay controls,

$$SUM = (\pm A \cdot B) + (\pm C \cdot D),$$

can realize in two steps the familiar summation:

$$(P + jR)(S + jT) = \underset{(1)}{(PS - RT)} + j\underset{(2)}{(PT + SR)}$$

by loading the TMC2249 as follows:

	TMC2249 Inputs						
Step	A	B	C	D	NEG1	NEG2	Resultant Output
1	P	S	R	T	L	H	(PS – RT)
2	P	T	R	S	L	L	(PT + SR)

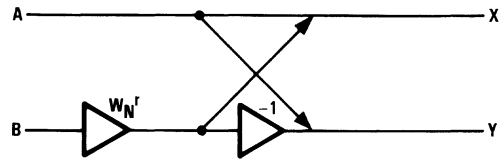
where H and L indicate a logic HIGH and LOW.

Thus we can perform a complex multiplication in two clock cycles. Notice that the user must switch the two components of the second input vector between the B and D inputs to obtain the second complex summation.

Calculating a Butterfly

Taking advantage of the complex multiply which we implemented above using the TMC2249, we can expand slightly to calculate a Radix-2 Butterfly, the core of the Fast Fourier Transform algorithm. To review, the Butterfly is calculated as shown in *Figure 6*.

Figure 6. Signal Flow Diagram of Radix-2 Butterfly



Where $X = A + B(W_N^r)$

$Y = A - B(W_N^r)$,

and W_N^r is the complex phase coefficient, or "twiddle factor" for the N-point transform, which is:

$$W_N^r = e^{-j(2\pi/N)}$$
$$= \cos(2\pi/N) + j(\sin(2\pi/N))$$
$$= Re(W) + jIm(W),$$

with Re and Im indicating the real and imaginary parts of the vector.

Expanding the complex vectors A and B to calculate X and Y, we get:

$$X = (Re(A) + jIm(A)) + (Re(B)Re(W) - Im(B)Im(W) + j(Re(B)Im(W) + Im(B)Re(W))$$
$$= (Re(A) + Re(B)Re(W) - Im(B)Im(W)) + j(Im(A) + Re(B)Im(W) + Im(B)Re(W))$$
$$= Re(X) + jIm(X)$$

and,

$$Y = (Re(A) + jIm(A)) - (Re(B)Re(W) - Im(B)Im(W) + j(Re(B)Im(W) + Im(B)Re(W))$$
$$= (Re(A) - Re(B)Re(W) + Im(B)Im(W)) + j(Im(A) - Re(B)Im(W) - Im(B)Re(W))$$
$$= Re(Y) + jIm(Y)$$

Calculating a Butterfly (cont.)

The butterfly is then neatly implemented in four clocks, as follows:

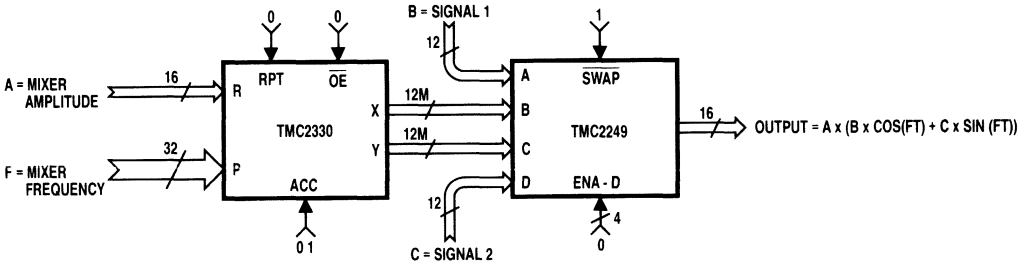
Step	TMC2249 Inputs A	B	C	D	CAS Input	NEG1	NEG2	Resultant Output
1	Re(B)	Re(W)	Im(B)	Im(W)	Re(A)	L	H	Re(X)
2	Re(B)	Re(W)	Im(B)	Im(W)	Re(A)	H	L	Re(Y)
3	Re(B)	Im(W)	Im(B)	Re(W)	Im(A)	L	L	Im(X)
4	Re(B)	Im(W)	Im(B)	Re(W)	Im(A)	H	H	Im(Y)

Notice again that the components of the second vector must be switched by the user on the second half of the computation, as well as the parts of the vector presented to the cascade input.

Quadrature Modulation

The TMC2249 can also be used to advantage as a digital-domain complex frequency synthesizer, as demonstrated in *Figure 7*. Here, orthogonal sinusoidal waveforms are generated digitally by sequentially addressing Sine and Cosine ROMS. These quadrature phase coefficients can then be multiplied with two input signals, such as digitized analog data. The TMC2249 then adds these products, which could be output directly to a high-speed digital-to-analog converter such as the TRW TDC1012 for direct waveform synthesis. This 12-bit, 20MHz DAC is ideally suited to waveform generation, featuring extremely low glitch energy for low spurious harmonics.

Figure 7. Direct Quadrature Waveform Synthesizer Using the TMC2249

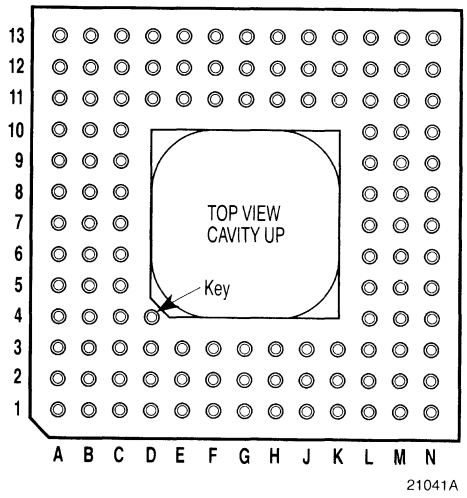


Pin Assignments – 120 Pin Plastic Pin Grid Array, H5 Package

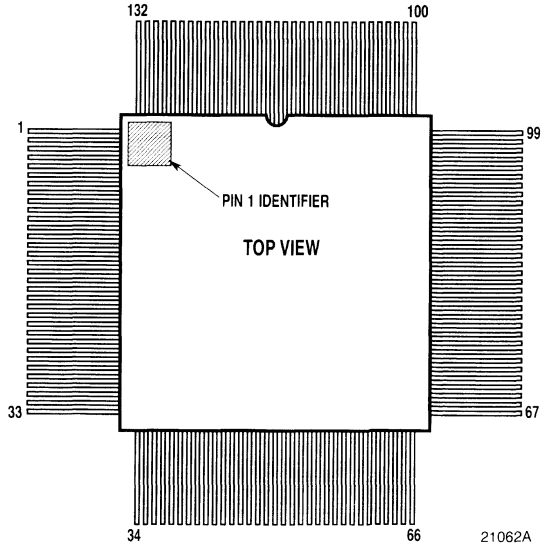
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
C3	CLK	G3	GND	L3	$BDEL_2$	L7	V_{DD}	L11	$ADEL_3$	G11	CAS_6	C11	C_1	C7	GND
B2	ACC	G1	S_7	M2	$\overline{BDEL_3}$	N7	B_{11}	M12	$ADEL_2$	G13	CAS_5	B12	C_2	A7	D_8
B1	NEG1	H1	S_6	N2	$\overline{ENB}$	N8	A_{11}	M13	$ADEL_1$	F13	CAS_4	A12	C_3	A6	D_7
D3	NEG2	H2	S_5	L4	B_0	M8	A_{10}	K11	$ADEL_0$	F12	CAS_3	C10	C_4	B6	D_6
C2	RND	H3	V_{DD}	M3	B_1	L8	A_9	L12	NC	F11	CAS_2	B11	C_5	C6	D_5
C1	S_{15}	J1	S_4	N3	B_2	N9	A_8	L13	CAS_{15}	E13	CAS_1	A11	C_6	A5	D_4
D2	S_{14}	J2	S_3	M4	B_3	M9	A_7	K12	CAS_{14}	E12	$\overline{CAS_0}$	B10	C_7	B5	D_3
E3	GND	K1	S_2	L5	B_4	N10	A_6	J11	CAS_{13}	D13	$\overline{CASEN}$	C9	C_8	A4	D_2
D1	S_{13}	J3	GND	N4	B_5	L9	A_5	K13	CAS_{12}	E11	FT	A10	C_9	C5	D_1
E2	S_{12}	K2	S_1	M5	B_6	M10	A_4	J12	CAS_{11}	D12	$CDEL_0$	B9	C_{10}	B4	D_0
E1	S_{11}	L1	S_0	N5	B_7	N11	A_3	J13	CAS_{10}	C13	$CDEL_1$	A9	C_{11}	A3	$\overline{END}$
F3	V_{DD}	M1	$\overline{OE}$	L6	GND	N12	A_2	H11	GND	B13	$CDEL_2$	C8	V_{DD}	A2	$DDEL_3$
F2	S_{10}	K3	$\overline{SWAP}$	M6	B_8	L10	A_1	H12	CAS_9	D11	$CDEL_3$	B8	D_{11}	C4	$DDEL_2$
F1	S_9	L2	$BDEL_0$	N6	B_9	M11	A_0	H13	CAS_8	C12	$\overline{ENC}$	A8	D_{10}	B3	$DDEL_1$
G2	S_8	N1	$BDEL_1$	M7	B_{10}	N13	$\overline{ENA}$	G12	CAS_7	A13	C_0	B7	D_9	A1	$DDEL_0$

Pin Assignments – 132 Leaded CERQUAD, L5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	23	S_3	45	B_7	67	NC	89	CAS_0	111	C_{11}
2	CLK	24	S_2	46	GND	68	$ADEL_3$	90	CASEN	112	V_{DD}
3	ACC	25	GND	47	B_8	69	$ADEL_2$	91	FT	113	D_{11}
4	NEG1	26	S_1	48	B_9	70	$ADEL_1$	92	$CDEL_0$	114	D_{10}
5	NEG2	27	S_0	49	B_{10}	71	$ADEL_0$	93	$CDEL_1$	115	D_9
6	RND	28	OE	50	V_{DD}	72	NC	94	$CDEL_2$	116	GND
7	S_{15}	29	SWAP	51	B_{11}	73	CAS_{15}	95	$CDEL_3$	117	D_8
8	S_{14}	30	$BDEL_0$	52	A_{11}	74	CAS_{14}	96	ENC	118	D_7
9	GND	31	$BDEL_1$	53	A_{10}	75	CAS_{13}	97	C_0	119	D_6
10	S_{13}	32	NC	54	A_9	76	CAS_{12}	98	NC	120	D_5
11	S_{12}	33	NC	55	A_8	77	CAS_{11}	99	NC	121	D_4
12	S_{11}	34	NC	56	A_7	78	CAS_{10}	100	NC	122	D_3
13	V_{DD}	35	$BDEL_2$	57	A_6	79	GND	101	C_1	123	D_2
14	S_{10}	36	$BDEL_3$	58	A_5	80	CAS_9	102	C_2	124	D_1
15	S_9	37	ENB	59	A_4	81	CAS_8	103	C_3	125	D_0
16	S_8	38	B_0	60	A_3	82	CAS_7	104	C_4	126	END
17	GND	39	B_1	61	A_2	83	CAS_6	105	C_5	127	$DDEL_3$
18	S_7	40	B_2	62	A_1	84	CAS_5	106	C_6	128	$DDEL_2$
19	S_6	41	B_3	63	A_0	85	CAS_4	107	C_7	129	$DDEL_1$
20	S_5	42	B_4	64	ENA	86	CAS_3	108	C_8	130	$DDEL_0$
21	V_{DD}	43	B_5	65	NC	87	CAS_2	109	C_9	131	NC
22	S_4	44	B_6	66	NC	88	CAS_1	110	C_{10}	132	NC



120 Pin Plastic Pin Grid Array – H5 Package



132 Leaded CERQUAD – L5 Package

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2249H5C	STD–T_A=0°C to 70°C	Commercial	120 Pin Plastic Pin Grid Array	2249H5C
TMC2249H5C1	STD–T_A=0°C to 70°C	Commercial	120 Pin Plastic Pin Grid Array	2249H5C1
TMC2249L5V	EXT–T_C= –55°C to 125°C	MIL-STD-883	132 Leaded CERQUAD	2249L5V
TMC2249L5V1	EXT–T_C= –55°C to 125°C	MIL-STD-883	132 Leaded CERQUAD	2249L5V1

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TMC2250

Matrix Multiplier

12 x 10 Bits, 40MHz

The TMC2250 is a flexible high-performance nine-multiplier array VLSI circuit which can execute a cascadeable 9-tap FIR filter, a cascadeable 4 x 2 or 3 x 3-pixel image convolution, or a 3 x 3 color space conversion. All configurations offer throughput at up to the maximum guaranteed 40MHz clock rate with 12-bit data and 10-bit coefficients. All inputs and outputs are registered on the rising edges of the clock.

The 3 x 3 matrix multiply or color conversion configuration can perform video standards conversion (YIQ or YUV to RGB, etc.) or three-dimensional perspective translation at real-time video rates.

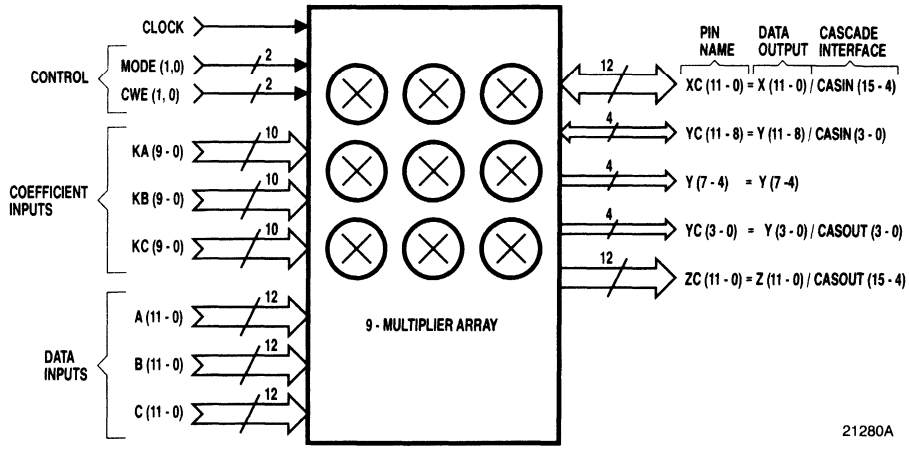
The 9-tap FIR filter configuration, useful in Video, Telecommunications, and Signal Processing, features a 16-bit cascade input to allow construction of longer filters.

The cascadeable 3 x 3 and 4 x 2-pixel image convolver functions allow the user to perform numerous image processing functions, including static filters and edge detectors. The 16-bit cascade input port facilitates two-chip 40MHz cubic convolution (4 x 4-pixel kernel).

The TMC2250 is fabricated in TRW's OMICRON-C™ one-micron CMOS process and operates at clock speeds of up to 40MHz over the full commercial (0°C to 70°C) temperature and supply voltage ranges. It is available in a 121 pin plastic pin grid array (PPGA) package. All input and output signals are TTL compatible.

H

Logic Symbol



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Printed in the U.S.A.

Features

- Four User-Selectable Filtering And Transformation Functions:
  - Triple Dot Product (3 x 3) Matrix Multiply
  - Cascadeable 9-Tap Systolic FIR Filter
  - Cascadeable 3 x 3-Pixel Image Convolver
  - Cascadeable 4 x 2-Pixel Image Convolver
- 40MHz (25ns) Pipelined Throughput
- 12-Bit Input And Output Data, 10-Bit Coefficients
- 16-Bit Cascade Input And Output Ports In All Filter Modes
- Onboard Coefficient Storage, With Three-Cycle Updating Of All Nine Coefficients

Applications

- Image Filtering And Manipulation
- Video Effects Generation
- Video Standards Conversion And Encoding/Decoding
- Three-Dimensional Image Manipulation
- Medical Image Processing
- Edge Detection For Object Recognition
- FIR Filtering For Communications Systems

Functional Description

General Information

The TMC2250 is a nine-multiplier array with the internal bus structure and summing adders needed to implement a 3 x 3 matrix multiplier (triple dot product) or cascadeable 9-tap FIR filter, 3 x 3-pixel convolver, or 4 x 2-pixel convolver, all in one monolithic circuit. With a 30MHz guaranteed maximum clock rate, this device offers video and imaging system designers a single-chip solution to numerous common image and signal-processing problems.

The three data input ports (A, B, C) accept 12-bit two's complement integer data, which is also the format for the output ports (X, Y, Z) in the matrix multiply mode (Mode 00). In the filter configurations (Modes 01, 10, and 11), the cascade ports assume 12-bit integer, 4-bit fractional two's complement data on both input and output. The coefficient input ports (KA, KB, KC) are always 10-bit two's complement fractional. ***Table 1*** details the bit weighting of the input and output data in all configurations.

Operating Modes

The TMC2250 can implement four different digital filter architectures. Upon selection of the desired function by the user ($MODE_{1-0}$), the device reconfigures its internal data paths and input and output buses appropriately. The output ports (XC, YC, and ZC) are configured in all filter modes as 16-bit Cascade In and Cascade Out ports so that multiple devices can be connected to build larger filters. These modes are described individually below. The I/O pin-function configurations for all four modes are shown in ***Table 1***.

Definitions

The calculations performed by the TMC2250 in each mode are also shown below, utilizing the following notation:

A(1), B(5), C(2), CASIN(3)	Indicates the data word presented to that input port during the specified clock rising edge (x). Applies to all input ports A_{11-0}, B_{11-0}, C_{11-0}, and $CASIN_{15-0}$.
KA1(1), KB3(4)	Indicates coefficient data stored in the specified one of the nine onboard coefficient registers KA1 through KC3, as shown in the block diagram for that mode, input during or before the specified clock rising edge (x).
X(1), Y(4), Z(6), CASOUT(6)	Indicates data available at that output port t_{DO} after the specified clock rising edge (x). Applies to all output ports X_{11-0}, Y_{11-0}, Z_{11-0}, and $CASOUT_{15-0}$.

Table 1. Data Port Formatting by Mode

Mode	Inputs						Inputs/Outputs		Outputs		
	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC_{9-0}	XC_{11-0}	YC_{11-8}	Y_{7-4}	YC_{3-0}	ZC_{11-0}
00	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC_{9-0}	X_{11-0}	Y_{11-8}	Y_{7-4}	Y_{3-0}	Z_{11-0}
01	A_{11-0}	A_{11-0}	NC	KA_{9-0}	KB_{9-0}	KC_{9-0}	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$
10	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC_{9-0}	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$
11	A_{11-0}	B_{11-0}	NC	KA_{9-0}	KB_{9-0}	KC_{9-0}	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$

Numeric Format

Table 2 shows the binary weightings of the input and output ports of the TMC2250. Although the internal sums of products could grow to 23 bits, in the matrix multiply mode (Mode 00) the outputs X, Y, and Z are truncated to yield 12-bit integer words. Thus the output format is identical to the input data format. In the filter configurations (Modes 01, 10, and 11) the cascade output is always half-LSB rounded to 16 bits, specifically 12 integer bits and 4 fractional guard bits, with no overflow "headroom." The user is of course free to half-LSB round the output word to any size less than 16 bits by forcing a 1 into the bit position of the cascade input immediately below the desired LSB. In all modes, bit weighting is easily adjusted if desired by applying the same scaling correction factor to both input and output data words. If the coefficients are rescaled, the relative weightings of the CASIN and CASOUT ports will differ accordingly.

Data Overflow

As shown in *Table 2*, the TMC2250's matched input and output data formats accommodate 0 dB (unity) gain. Therefore, the user must be aware of input conditions that could lead to numeric overflow. Maximum input data and coefficient word sizes must be taken into account with the specific algorithm performed to ensure that no overflow occurs.

Signal Definitions

Power

V_{DD}, GND — The TMC2250 operates from a single +5V supply. All pins must be connected.

Clock

CLK — The TMC2250 operates from a single system clock input. All timing specifications are referenced to the rising edge of clock.

Table 2. Bit Weightings For Input and Output Data Words

Bit Weights	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}
Inputs																						
All Modes Data A, B, C	$-I_{11}$	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	.									
Coefficients KA, KB, KC												$-K_9$	.	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0
Modes 01, 10, 11 CASIN	$-CI_{15}$	CI_{14}	CI_{13}	CI_{12}	CI_{11}	CI_{10}	CI_9	CI_8	CI_7	CI_6	CI_5	CI_4	.	CI_3	CI_2	CI_1	CI_0					
Internal Sum	X_{20}	X_{19}	X_{18}	X_{17}	X_{16}	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	.	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
Outputs																						
Mode 00 X, Y, Z	$-O_{11}$	O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	.									
Modes 01, 10, 11 CASOUT	$-CO_{15}$	CO_{14}	CO_{13}	CO_{12}	CO_{11}	CO_{10}	CO_9	CO_8	CO_7	CO_6	CO_5	CO_4	.	CO_3	CO_2	CO_1	CO_0					

Note: 1. A minus sign indicates a two's complement sign bit.

3 x 3 Matrix Multplier (Mode 00)

This mode utilizes all six input and output ports in the basic configuration to realize a "triple dot product," in which each output is the sum of all three input words in that column multiplied by the appropriate stored coefficients. The three corresponding sums of products are available at the outputs five clock cycles after the input data are latched, and three new data words truncated to 12 bits are then available every clock cycle. See *Table 6* and the *Applications Discussion* section regarding encoded video standard conversion matrices.

$$X(5) = A(1)KA1(1) + B(1)KB1(1) + C(1)KC1(1)$$
$$Y(5) = A(1)KA2(1) + B(1)KB2(1) + C(1)KC2(1)$$
$$Z(5) = A(1)KA3(1) + B(1)KB3(1) + C(1)KC3(1)$$

Figure 1. 3 x 3 Matrix Multiplier Impulse Response (Mode 00)

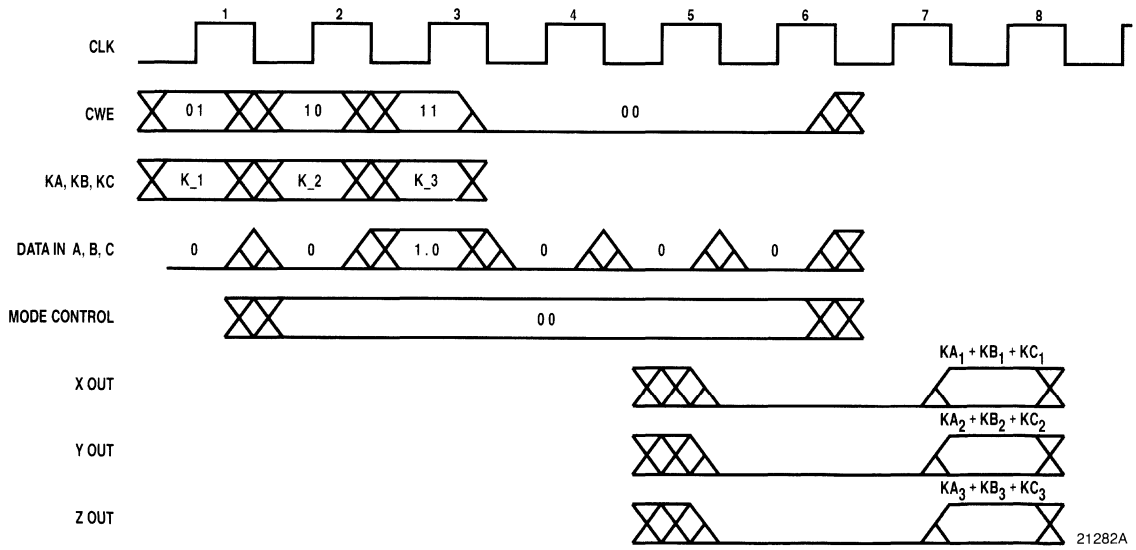
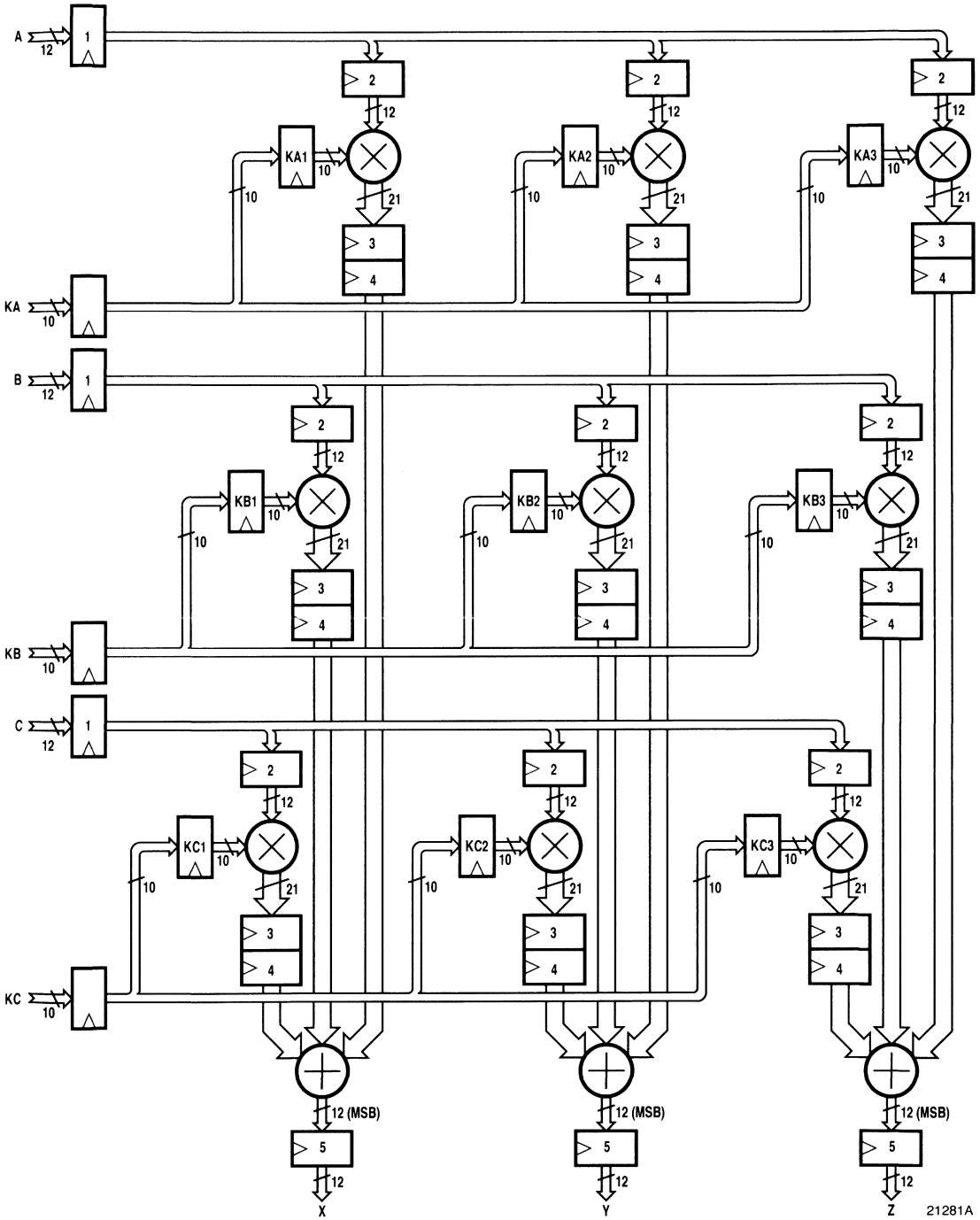


Figure 2. 3 x 3 Matrix Multiplier Configuration (Mode 00)



9-Tap FIR Filter (Mode 01)

The architecture for this configuration is shown in *Figure 3*. The user loads the desired coefficient set, presents input data to ports A and B simultaneously (most applications will wire the A and B inputs together), and receives the resulting 9-sample response, half-LSB rounded to 16 bits, 5 to 13 clock cycles later. A new output data word is available every clock cycle. The figure shows that the input data are automatically right-shifted one location through the row of multiplier input registers on every clock in anticipation of a new input data word.

$$\begin{aligned}\text{CASOUT}(13) = {} & A(9)KA3(9) + A(8)KA2(8) + A(7)KA1(7) \\ & + B(6)KB3(9) + B(5)KB2(8) + B(4)KB1(7) \\ & + B(3)KC3(9) + B(2)KC2(8) + B(1)KC1(7) \\ & + \text{CASIN}(10)\end{aligned}$$

Latency: Impulse in to center of 9-tap response = 9 registers. Cascade In to Cascade Out = 4 registers.

Figure 3. 9-Tap FIR Filter Impulse Response (Mode 01)

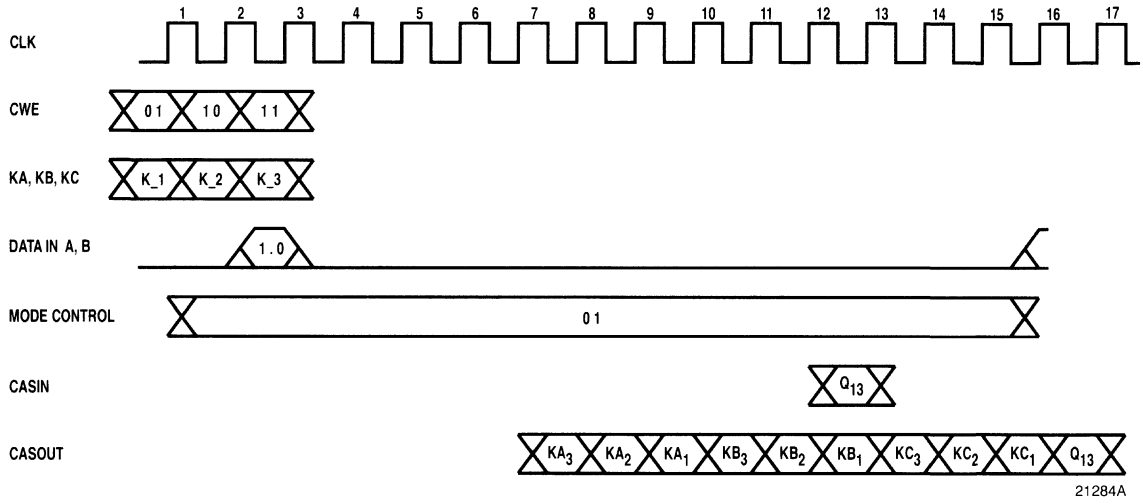
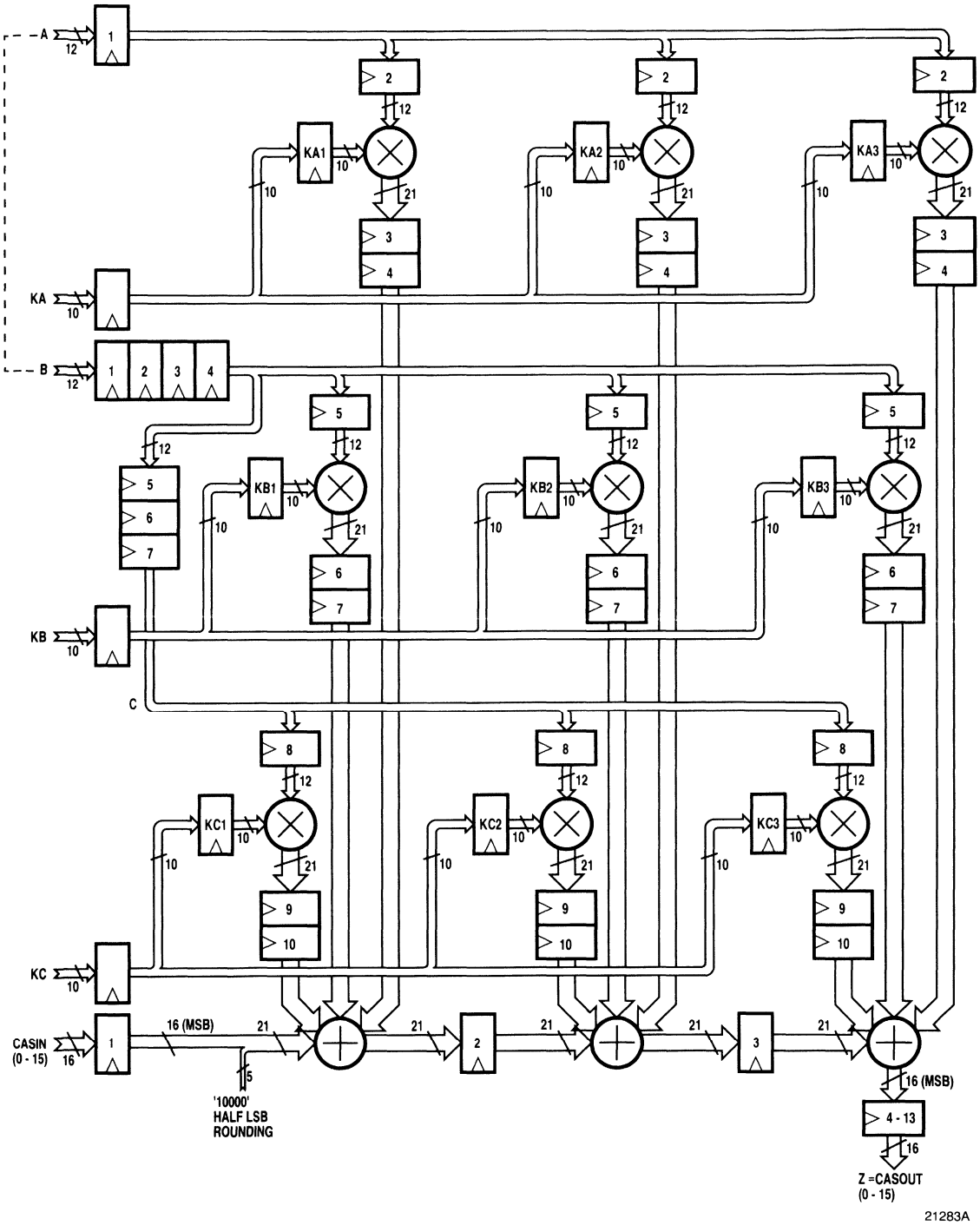


Figure 4. 9-Tap FIR Filter Configuration (Mode 01)



3 x 3-Pixel Convolver (Mode 10)

This filter configuration accepts a 3-pixel-square neighborhood, side-loaded three pixels at a time through input ports A, B, and C, and multiplies the 9 most recent pixel values by the coefficient set currently stored in the registers. These products are summed with the data presented to the cascade input, and a new 3-cycle impulse response, rounded to 16 bits, is available at the output port 5-7 clocks later, with a new output available on every clock cycle. The input pixel data are automatically shifted one location to the right through the three rows of multiplier input registers on every clock in anticipation of three new input data words, effectively sliding the convolutional window over one column in an image plane.

$$\begin{aligned}CASOUT(7) = {} & A(3)KA3(3) + A(2)KA2(2) + A(1)KA1(1) \\ & + B(3)KB3(3) + B(2)KB2(2) + B(1)KB1(1) \\ & + C(3)KC3(3) + C(2)KC2(2) + C(1)KC1(1) \\ & + CASIN(4)\end{aligned}$$

Latency: Impulse in to center of 3-tap response = 6 registers. Cascade In to Cascade Out = 4 registers.

Figure 5. 3 x 3-Pixel Convolver Impulse Response (Mode 10)

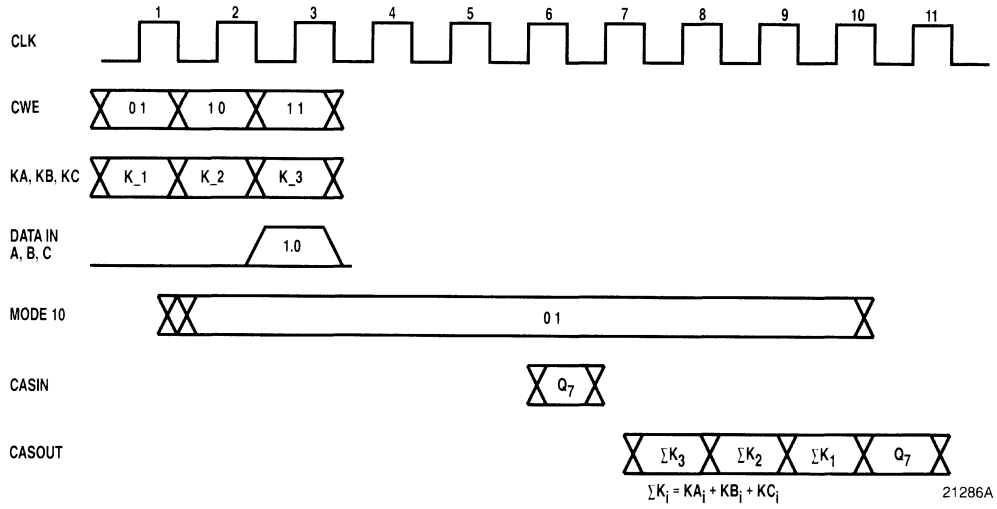
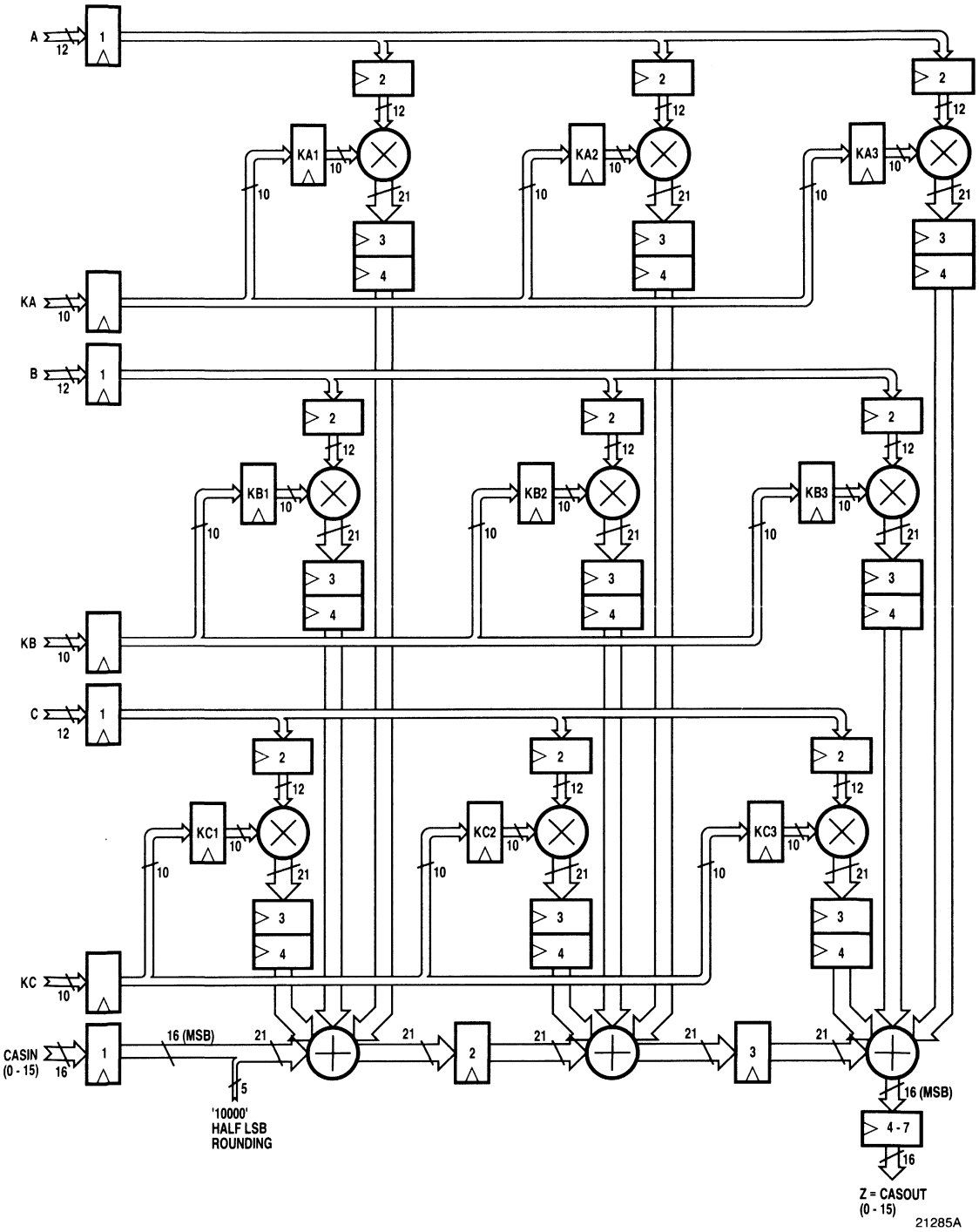


Figure 6. 3 x 3-Pixel Convolver Configuration (Mode 10)



4 x 2-Pixel Cascadeable Convolver (Mode 11)

Similar to Mode 10, the 4 x 2-pixel convolver allows the user to perform full-speed cubic convolution with only two TMC2250 devices and the TMC2111 Pipeline Delay Register to synchronize the cascade ports (see the *Applications Discussion* section). Pixel data are side-loaded into ports A and B, multiplied by the onboard coefficients, summed with the cascade input, and half-LSB rounded to 16 bits. The four-cycle impulse response emerges at the cascade output port 5 to 8 clock cycles later. A new output word is available on every clock cycle. Note that Multiplier KC2 is not used in this mode and that its stored coefficient is ignored. As shown below, the column of input pixel data is automatically shifted one location to the right through the two rows of multiplier input registers on every clock in anticipation of two new input data words, effectively sliding the convolutional window over one column in an image plane.

$$\begin{aligned}CASOUT(8) = {} & A(4)KA3(4) + A(3)KA2(3) + A(2)KA1(2) \\ & + A(1)KB3(4) + B(4)KB3(4) + B(3)KB2(3) \\ & + B(2)KB1(2) + B(1)KC1(2) + CASIN(5)\end{aligned}$$

Figure 7. 4 x 2-Pixel Convolver Impulse Response (Mode 11)

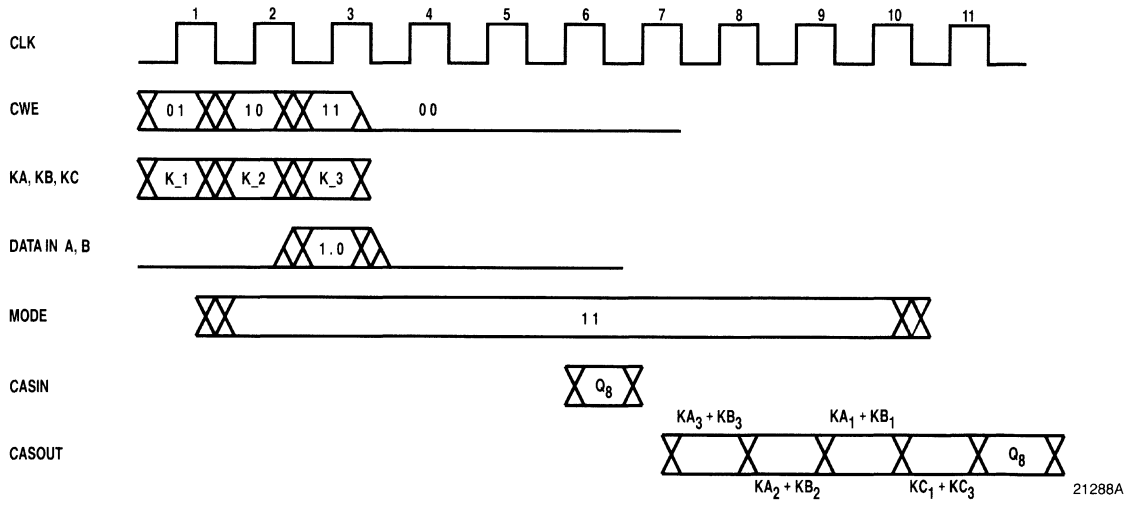
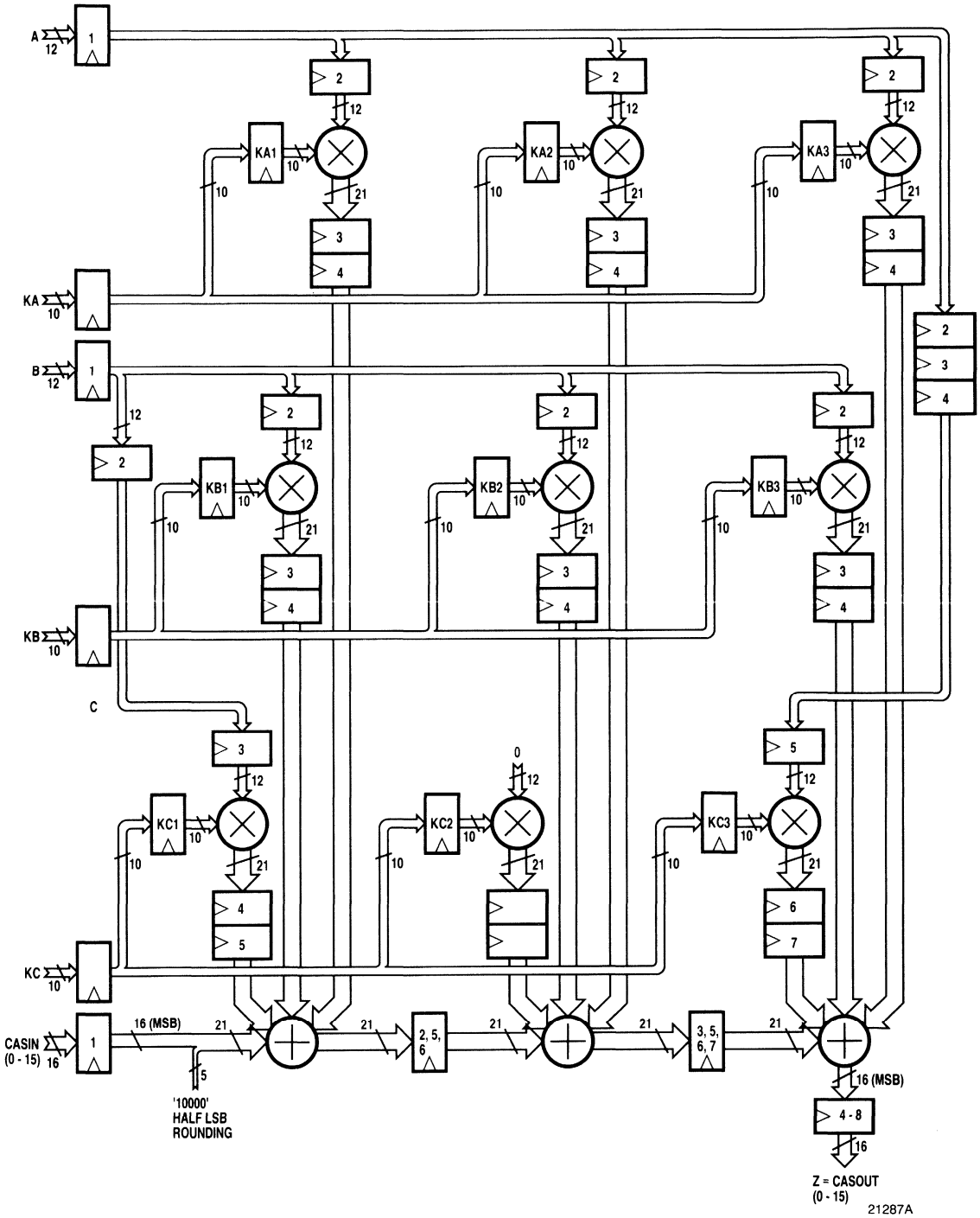


Figure 8. 4 x 2-Pixel Convolver Configuration (Mode 11)



Signal Definitions (cont.)

Controls

$MODE_{1,0}$ The TMC2250 will switch to the configuration selected by the user (as shown in *Table 3*) on the next clock. This registered control is usually static; however, should the user wish to switch between modes, the internal pipeline latencies of the device must be taken into account. Valid data will not be available at the outputs in the new configuration until enough clocks in the new mode have passed to flush the internal registers.

Table 3. Configuration Mode Word

$MODE_{1,0}$	Configuration Mode
00	3 x 3 Matrix Multiply
01	9-Tap One-Dimensional FIR
10	3 x 3-Pixel Convolver
11	4 x 2-Pixel Convolver

$CWE_{1,0}$ Data presented to the coefficient input ports (KA, KB, and KC) will update three of the internal coefficient storage registers, as indicated by the simultaneous Coefficient Write Enable select, on the next clock. See *Table 4* and the *Functional Block Diagram*.

Table 4. Coefficient Write Enable Word

$CWE_{1,0}$	Coefficient Set Selected
00	Hold all registers
01	Update KA1, KB1, KC1
10	Update KA2, KB2, KC2
11	Update KA3, KB3, KC3

Table 5. Coefficient Input Ports

Input Port	Registers Available
KA	KA1, KA2, KA3
KB	KB1, KB2, KB3
KC	KC1, KC2, KC3

Inputs And Outputs

A_{11-0}, B_{11-0}, C_{11-0} Data presented to the 10-bit registered data input ports A, B, and C are latched into the multiplier input registers for the currently selected configuration (*Table 3*). In all modes except Mode 00, new data are internally right-shifted to the next filter tap on each rising edge of CLK.

KA_{9-0}, KB_{9-0}, KC_{9-0} Data presented to the 10-bit registered coefficient input ports KA, KB, and KC are latched three at a time into the internal coefficient storage register set indicated by the Coefficient Write Enable $CWE_{1,0}$ on the next clock, as shown in *Table 4*.

$CASIN_{15-0}$ In all modes except Mode 00, the x port and four bits of the Y output port are reconfigured as the 16-bit registered Cascade Input port $CASIN_{15-0}$. Data presented to this input will be added to the weighted sums of the data words which were presented to the input ports (A, B, and C).

X_{11-0}, Y_{11-0}, Z_{11-0} In the matrix multiply mode, data are available at the 12-bit registered output ports X, Y, and Z t_{DO} after every clock. These ports are reconfigured in the filtering modes as 16-bit Cascade Input and Output ports.

NOTE: The output ports X, Y, Z and CASOUT, and the input port CASIN are internally reconfigured by the device as required for each mode of the device. The multiple-function pins have names which are combinations of these titles, as appropriate.

$CASOUT_{15-0}$ In all modes except Mode 00, the Z port and four bits of the Y output port are reconfigured as the 16-bit registered Cascade Output port $CASOUT_{15-0}$.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins
Power	V_{DD}	Supply Voltage	F3, H3, L7, C8, C4
	GND	Ground	E3, G3, J3, L4, L6, H11, C7, C5
Clock	CLK	System Clock	D11
Controls	$MODE_{1,0}$	Mode Control	B5, A4
	$CWE_{1,0}$	Coefficient Write Enable	J12, J13
Input/Output	A_{11-0}	Data Input A	E11, D13, E12, E13, F11, F12, F13, G13, G11, G12, H13, H12
	B_{11-0}	Data Input B	B10, A11, B11, C10, A12, B12, C11, A13, C12, B13, C13, D12
	C_{11-0}	Data Input C	A5, C6, B6, A6, A7, B7, A8, B8, A9, B9, A10, C9
	KA_{9-0}	Coefficient Input A1, A2, A3	K13, J11, K12, L13, L12, K11, M13, M12, L11, N13
	KB_{9-0}	Coefficient Input B1, B2, B3	M11, L10, N12, N11, M10, L9, N10, M9, N9, L8
	KC_{9-0}	Coefficient Input C1, C2, C3	M8, N8, N7, M7, N6, M6, N5, M5, N4, L5
	XC_{11-0}	$CASIN_{15-4}$/Output X	B4, A3, A2, B3, A1, C3, B2, B1, D3, C2, C1, D2
	YC_{11-8}	$CASIN_{3-0}$/Output Y_{11-0}	D1, E2, E1, F2
	Y_{7-4}	Output Y_{7-4} Only	F1, G2, G1, H1
	YC_{3-0}	$CASOUT_{3-0}$/Output Y_{3-0}	K1, J2, J1, H2
	ZC_{11-0}	$CASOUT_{15-4}$/Output Z_{11-0}	M4, N3, M3, N2, M2, L3, N1, L2, K3, M1, L1, K2

Figure 9. Input/Output Timing Diagram

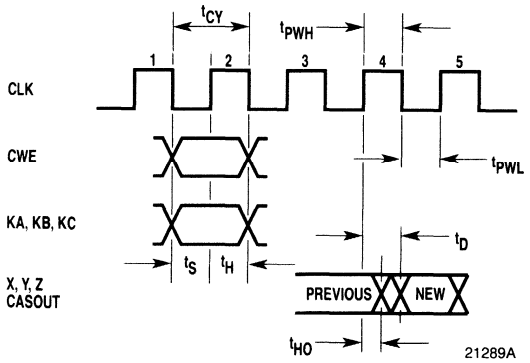


Figure 10. Equivalent Input Circuit

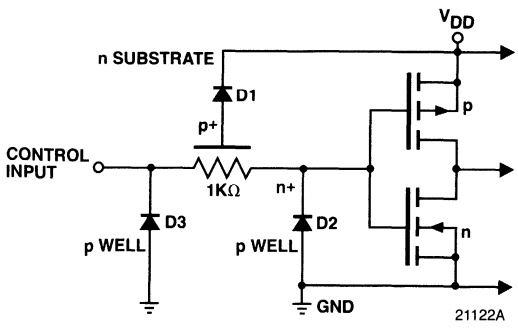
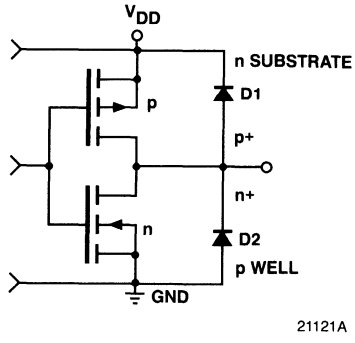


Figure 11. Equivalent Output Circuit



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD}+5.0)V

Output

Applied voltage ..... −0.5 to (V_{DD}+5.0)V [2]

Forced current ..... −6.0 to 6.0mA [3,4]

Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −60 to +130°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to 150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
	CLK Only			0.8			0.6	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
t_{CY}	Cycle Time							
	TMC2250	33			33			ns
	TMC2250-1	27.7			27.7			ns
	TMC2250-2	25						ns
t_{PWL}	Clock Pulse Width, LOW							
	TMC2250	15			15			ns
	TMC2250-1	12			12			ns
	TMC2250-2	10						ns
t_{PWH}	Clock Pulse Width, HIGH	10			10			ns
t_S	Input Setup Time							
	TMC2250	8			8			ns
	TMC2250-1	7			7			ns
	TMC2250-2	6						ns
t_H	Input Hold Time							
	TMC2250	3			3			ns
	TMC2250-1	3			3			ns
	TMC2250-2	2						ns
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		12		12	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz		160		160	mA
I_{IL}	Input Current, Logic LOW [2]	V_{DD} = Max, V_{IN} = 0V		−10		−10	μA
I_{IH}	Input Current, Logic HIGH [2]	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
I_{OIL}	Input Current, Logic LOW [3]	V_{DD} = Max, V_{IN} = 0V		−40		−40	μA
I_{OIH}	Input Current, Logic HIGH [3]	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = 4mA		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = −2mA	2.4		2.4		V
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to to ground, one second duration max.	−20	−80	−20	−80	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Notes:
1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Except pins XC_{11-0}, YC_{11-8}.
3. Pins XC_{11-0}, YC_{11-8} only.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 25pF					
	TMC2250			18		20	ns
	TMC2250-1			17		18	ns
	TMC2250-2			16			ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 25pF					
	TMC2250			4		4	ns
	TMC2250-1			3		3	ns
	TMC2250-2			3			ns

Applications Discussion

Converting Video Data from RGB to YIQ or YUV

The TMC2250 simplifies the task of converting encoded color video data between the RGB (color component) format and the YIQ (quadrature encoded chrominance) or YUV (color difference) format. Beginning with RGB component data, the standard relationships, with 8-bit quantization, are:

$$Y = (77R + 150G + 29B)/256$$
$$I = (153R - 71G - 82B)/256 + 128$$
$$Q = (54R - 134G + 80B)/256 + 128$$

and

$$Y = (77R + 150G + 29B)/256$$
$$U = (131R - 110G - 21B)/256 + 128$$
$$V = (-44R - 87G + 131B)/256 + 128$$

In digital systems, I and Q or U and V are sometimes renormalized to:

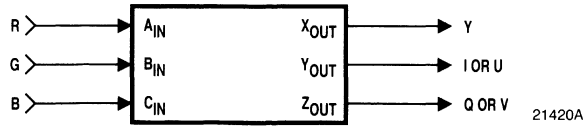
$$I = (128R - 59G - 69B)/256$$
$$Q = (52R - 128G + 76B)/256$$
$$U = (128R - 107G - 21B)/256$$
$$V = (-43R - 85G + 128B)/256$$

With each coefficient expressed as a fraction of 256, these numbers are easily converted to binary for loading into the coefficient storage of the TMC2250. The half-scale (80_{hex}) offsets included in the chrominance and color-difference terms can easily be added to the appropriate sums after the matrix multiplication, if desired. ***Table 6*** contains the 10-bit two's complement coefficients to be loaded into the TMC2250 to perform the desired conversion from RGB format. Once these factors are in place the user can continuously convert encoded data at real-time video rates, with three new encoded outputs available on every clock cycle.

Table 6. Colorspace Conversion Coefficients [1, 2]

Conversion	KA1	KA2	KA3	KB1	KB2	KB3	KC1	KC2	KC3
RGB to YIQ	04D	099	036	096	3B9	37A	01D	3AE	050
RGB to YIQ[3]	04D	080	034	096	3C5	380	01D	3BB	04C
RGB to YUV	04D	083	3D4	096	392	3A9	01D	3EB	083
RGB to YUV[3]	04D	080	3D5	096	395	3AB	01D	3EB	080

Notes:
1. All entries are given in 10-bit two's complement hexadecimal, such that all entries beginning in "2" or "3" are negative.
2. This table assumes the following bus assignments:



3. Second and fourth entries are renormalized such that largest coefficient = .5 (080_{hex}).

Converting Video Data from YIQ or YUV to RGB

With a different set of coefficients, the TMC2250 can perform the inverse conversions, whose governing equations are:

$$R = (256Y + 243I + 159Q)/256 \quad \text{and} \quad R = (256Y + 0U + 292V)/256$$
$$G = (256Y - 72I - 164Q)/256 \qquad G = (256Y - 101U - 149V)/256$$
$$B = (256Y - 284I + 443Q)/256 \qquad B = (256Y + 520U + 0V)/256$$

The values corresponding to digital normalization (see *Converting Video Data from RGB to YIQ or YUV*) are:

$$R = 256Y + 292I + 167Q)/256 \quad \text{and} \quad R = (256Y + 0U + 359V)/256$$
$$G = (256Y - 86I - 172Q)/256 \qquad G = (256Y - 88U - 183V)/256$$
$$B = (256I - 341I + 456Q)/256 \qquad B = (256Y + 453U + 0V)/256$$

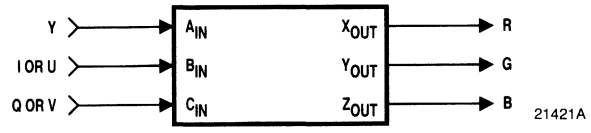
Since the first YUV to RGB equation set includes the coefficient "520," which won't fit into a 10-bit two's complement integer format, we must either divide all coefficients by 2, degrading precision by one bit, or by 520/511. In ***Table 7***, the 520/511 correction factor was selected.

H

Table 7. Colorspace Conversion Coefficients [1, 2]

Conversion	KA1	KA2	KA3	KB1	KB2	KB3	KC1	KC2	KC3
YIQ to RGB	100	100	100	0F3	3B8	3E4	09F	35C	1BB
YIQ to RGB[3]	100	100	100	124	3AA	2AB	0A7	354	101
YUV to RGB	0FC	0FC	0FC	000	39D	1FF	11F	36E	000
YUV to RGB[3]	100	100	100	000	3A8	125	167	349	000

Notes:
1. All entries are given in 10-bit two's complement hexadecimal, such that all entries beginning in "2" or "3" are negative.
2. This table assumes the following bus assignments:

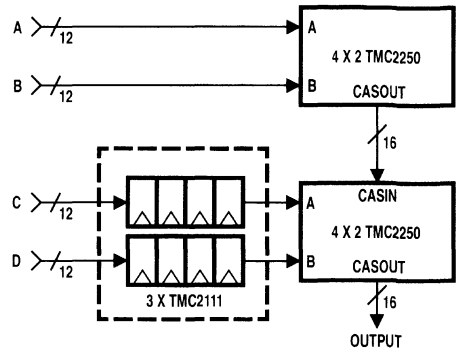


3. Second and fourth entries are renormalized such that largest coefficient = .5 (080_{hex}).

Performing Large-Kernel Pixel Interpolation

The Cascade Input and Output Ports of the TMC2250 allow the user to stack multiple devices to perform larger interpolation kernels with no decrease in pixel throughput. *Figure 12* illustrates a basic application utilizing Mode 11 to realize a 4 x 4-pixel kernel, also called Cubic Convolution. This example utilizes the TMC2011 Variable-Length Shift Register to compensate for the internal latency of each TMC2250. Alternatively, some applications may utilize RAM, FIFOs, or other methods to store multiple-line pixel data. In these cases the user may compensate for latency by simply offsetting the access sequencing of the storage devices.

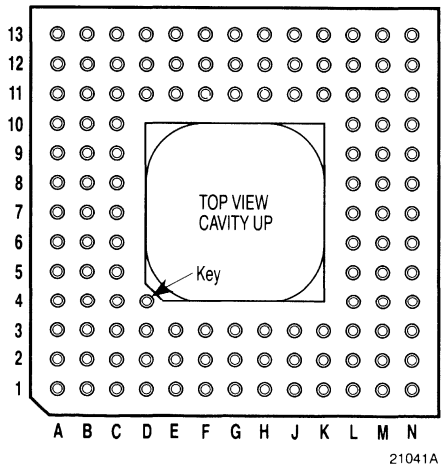
Figure 12. Performing Cubic Convolution with Two TMC2250s



Pin Assignments – 121 Pin Plastic (H5) or Ceramic (G1) Pin Grid Array

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	XC_7	B3	XC_8	C5	GND	E1	YC_9	G11	A_3	K1	YC_3	L10	KB_8	M12	KA_2
A2	XC_9	B4	XC_{11}	C6	C_{10}	E2	YC_{10}	G12	A_2	K2	ZC_0	L11	KA_1	M13	KA_3
A3	XC_{10}	B5	$MODE_1$	C7	GND	E3	GND	G13	A_4	K3	ZC_3	L12	KA_5	N1	ZC_5
A4	$MODE_0$	B6	C_9	C8	V_{DD}	E11	A_{11}	H1	Y_4	K11	KA_4	L13	KA_6	N2	ZC_8
A5	C_{11}	B7	C_6	C9	C_0	E12	A_9	H2	YC_0	K12	KA_7	M1	ZC_2	N3	ZC_{10}
A6	C_8	B8	C_4	C10	B_8	E13	A_8	H3	V_{DD}	K13	KA_9	M2	ZC_7	N4	KC_1
A7	C_7	B9	C_2	C11	B_5	F1	Y_7	H11	GND	L1	ZC_1	M3	ZC_9	N5	KC_3
A8	C_5	B10	B_{11}	C12	B_3	F2	YC_8	H12	A_0	L2	ZC_4	M4	ZC_{11}	N6	KC_5
A9	C_3	B11	B_9	C13	B_1	F3	V_{DD}	H13	A_1	L3	ZC_6	M5	KC_2	N7	KC_7
A10	C_1	B12	B_6	D1	YC_{11}	F11	A_7	J1	YC_1	L4	GND	M6	KC_4	N8	KC_8
A11	B_{10}	B13	B_2	D2	XC_0	F12	A_6	J2	YC_2	L5	KC_0	M7	KC_6	N9	KB_1
A12	B_7	C1	XC_1	D3	XC_3	F13	A_5	J3	GND	L6	GND	M8	KC_9	N10	KB_3
A13	B_4	C2	XC_2	D11	CLK	G1	Y_5	J11	KA_8	L7	V_{DD}	M9	KB_2	N11	KB_6
B1	XC_4	C3	XC_6	D12	B_0	G2	Y_6	J12	CWE_1	L8	KB_0	M10	KB_5	N12	KB_7
B2	XC_5	C4	V_{DD}	D13	A_{10}	G3	GND	J13	CWE_0	L9	KB_4	M11	KB_9	N13	KA_0

D4 Index Pin (Unconnected)



Ordering Information

Product Number	Speed (MHz)	Temperature Range	Screening	Package	Package Marking
TMC2250H5C	30	STD – T_A = 0°C to 70°C	Commercial	121 Pin Plastic Pin Grid Array	2250H5C
TMC2250H5C-1	36	STD – T_A = 0°C to 70°C	Commercial	121 Pin Plastic Pin Grid Array	2250H5C-1
TMC2250H5C-2	40	STD – T_A = 0°C to 70°C	Commercial	121 Pin Plastic Pin Grid Array	2250H5C-2
TMC2250G1V	30	MIL – T_C = −55°C to 125°C	MIL-STD-883	121 Pin Ceramic Pin Grid Array	2250G1V
TMC2250G1V1	36	MIL – T_C = −55°C to 125°C	MIL-STD-883	121 Pin Ceramic Pin Grid Array	2250G1V1

TMC2255

CMOS 3x3, 5x5 Image Convolver
8 x 8 Bits, 12MHz Data Rate

Like the faster TMC2250, the low cost TMC2255 can perform a triple 3x1 matrix-vector multiplication or a 3x3 convolution. It can also perform a 5x5 convolution with bidimensionally symmetrical coefficients. The on-chip coefficient memory stores four sets of nine 8-bit two's complement coefficients. Two of the TMC2255's five 8-bit data input ports are also used to load instructions and coefficients, which can be updated during operation. The device accepts the unsigned and/or two's complement data at 1/3 of the applied clock rate.

The 3(3x1) matrix multiply mode supports various 3-space numerical operations, such as video standards conversion (e.g. YIQ to RGB) or three-dimensional perspective transformation. Three input ports accept the 8-bit two's complement and/or unsigned magnitude data. The two remaining input ports can be loaded with coefficients and/or device control parameters "on-the-fly." In this mode, an output is generated on every clock cycle.

The 3x3 and 5x5 pixel image convolver modes support numerous functions, including static filtering and edge detection. On every third clock cycle, the TMC2255 accepts three (3x3 mode) or five (5x5 mode) data inputs. In the 5x5 mode, the coefficient kernel must be symmetric both horizontally and vertically. Outputs from the device are generated on every third clock cycle, matching the input pixel data rate, and can be limited ("clipped") to 8, 9 or 12 bits.

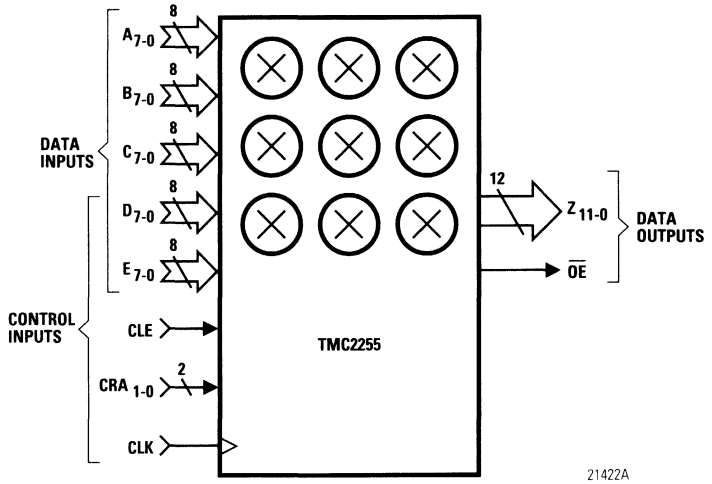
Fabricated in TRW's OMICRON-C™ one-micron CMOS process, the TMC2255 will operate at clock rates of 0 to 30MHz over the full commercial temperature (0°C to 70°C) and supply voltage ranges.

Features

- 8-Bit Data And Coefficient Input Precision
- Triple 3x1 Matrix-Vector Multiplication Mode
- 3x3 And 5x5 Two Dimensional Convolution Modes
- TTL-Compatible I/O With Three-State Output Bus
- Offered In 68-Contact Plastic Chip Carrier (PLCC)
- Built-In 8-, 9-, Or 12-Bit Arithmetic Limiter
- Two's Complement, Unsigned, Or Mixed Data Formats

H

Logic Symbol



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Applications

- RGB To/From YUV/YIQ Color Space Conversion
- 3x3 Or 5x5 Two Dimensional FIR Filtering
- Edge Enhancement And General Image Processing
- Robotics And Image Recognition
- Electronic Darkroom
- Desktop Publishing

Associated Products

- TMC2011 Variable Length Shift Register
- TMC2302 Image Manipulation Sequencer

Functional Description

The TMC2255 contains an array of multipliers and adders, four 9x8-bit coefficient "pages" and a global control block, all of which can be initialized or reconfigured through ports D and E when $\overline{CLE}$ is LOW. Device parameters include matrix coefficients, internal device configuration (mode), rounding precision, and input/output data formats (two's complement, unsigned, or mixed). After the control parameters have been loaded, device operation commences with the next clock rising edge on which $\overline{CLE}$ returns HIGH. Depending on the mode selected, three or five data are input in parallel and proceed through a sequence of operations: Input, Preaddition, Multiply-Accumulation, Rounding, Limiting and Output (*Figures 1-4*).

Input Stage

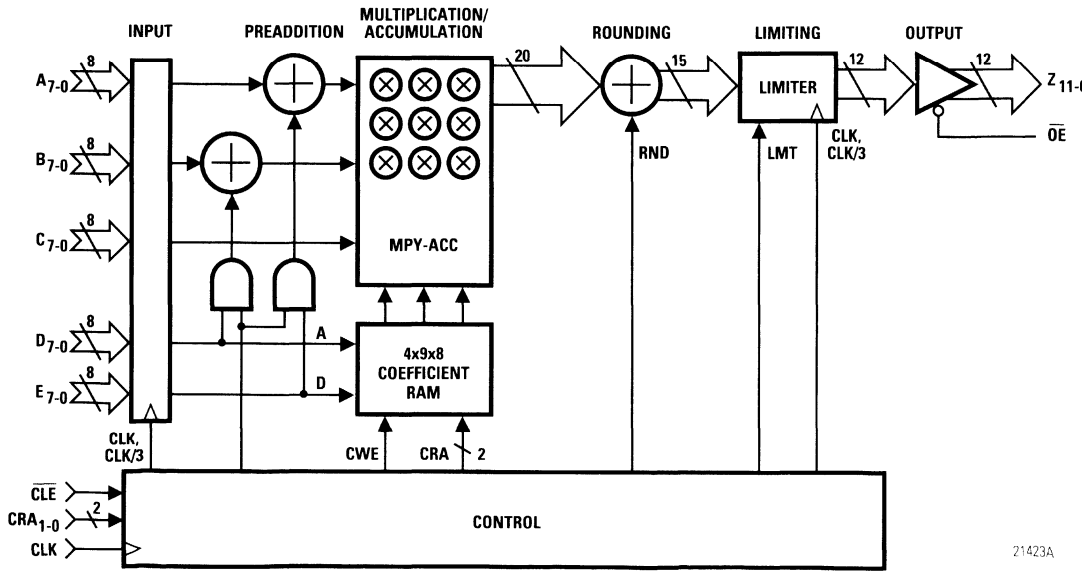
Inputs are supplied to ports A through C in all operating modes on every third clock cycle, beginning with the clock rising edge that contains the most recent $\overline{CLE}$ LOW to HIGH transition. Control and/or coefficient parameters can be input through ports D and E during any of the three master clock cycles that make up each data cycle. In the 5x5 convolution mode data enter the device through ports A-E. Control and/or coefficients may be updated through ports D and E on the remaining two cycles of each clock triplet.

Input data formats may be unsigned and/or two's complement, as identified in the mode select field of port E.

Preaddition

In and only in 5x5 convolution, the horizontal and vertical symmetry of the coefficients permits nine multipliers to do the work of 25. To facilitate this, the data input to ports A and E are pre-added before multiplication, as are the B and D inputs (*Figure 4*, the *5x5 Block Diagram*).

Figure 1. Structural Block Diagram



Coefficient Memory

The TMC2255 contains enough memory to store four "pages" of nine 8-bit two's complement coefficients each. When $\overline{CLE}$ is LOW, a new coefficient is written through port E to the page and location address identified on port D. On every third clock cycle, the coefficient page to be read and used in the immediate 3-cycle computation set is selected by CRA_0 and CRA_1. Of the nine coefficients per page, K1, i (i=1 to 3) process the port A (and E) data; K2, i, the port B (and D) data; and K3, i, the port C data.

Multiplication and Accumulation

The device computes nine products during every three clock cycles, accumulating them internally to full precision.

Rounding

Accumulated sums of products are rounded before the last 5 or 6 bits are truncated. Rounding is performed by adding "010000" or "100000" to the emerging data stream, according to the desired precision of the output results. When $\overline{CLE}$=0 and D=0XXX1111, pin E_6 sets the chip's rounding position, viz: E_6=0: add .010000 and use Z_0 as least significant bit; E_6=1: add .100000 and use Z_1 as least significant bit, ignoring Z_0.

Output Limiting

The device provides programmable output limiting in unsigned (UN) and/or two's complement (TC) format and for 8, 9, or 12 bits of output precision (including Z_0). In 3(3x1) mode, for an RGB to YIQ transformation, the device can limit Z_1 (Y) to 9 bits unsigned while limiting Z_3 (I) and Z_3 (Q) to 9 bits two's complement.

Outputs

Output is through the 12-bit Z port, which provides 1/2 or 1 LSB precision, relative to the input format. In the 3(3x1) mode three outputs will appear consecutively at the Z port during each triple clock cycle; for data input on clock rising edge 0, these results will emerge t_{DO} after clock rising edges 7, 8, and 9. In both convolution modes the results are output at 1/3 the device master clock rate, with the first point of the impulse response emerging after clock rising edge 9. To facilitate connection to a bus, the output buffers are enabled and disabled (placed in high-impedance state) by asynchronous control $\overline{OE}$.

Figure 2. Functional Block Diagram, 3(3x1) Mode

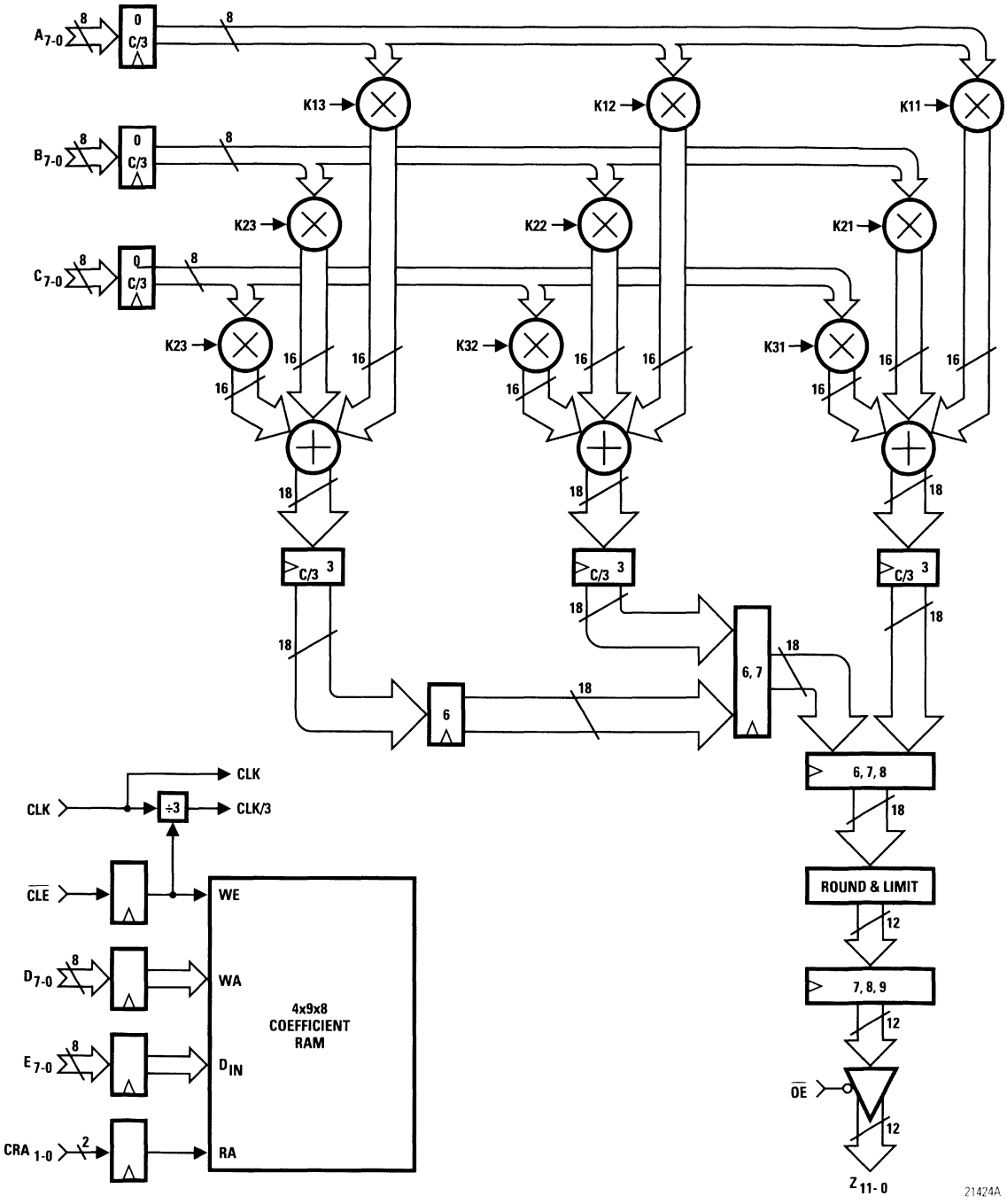


Figure 3. Functional Block Diagram, 3x3 Mode

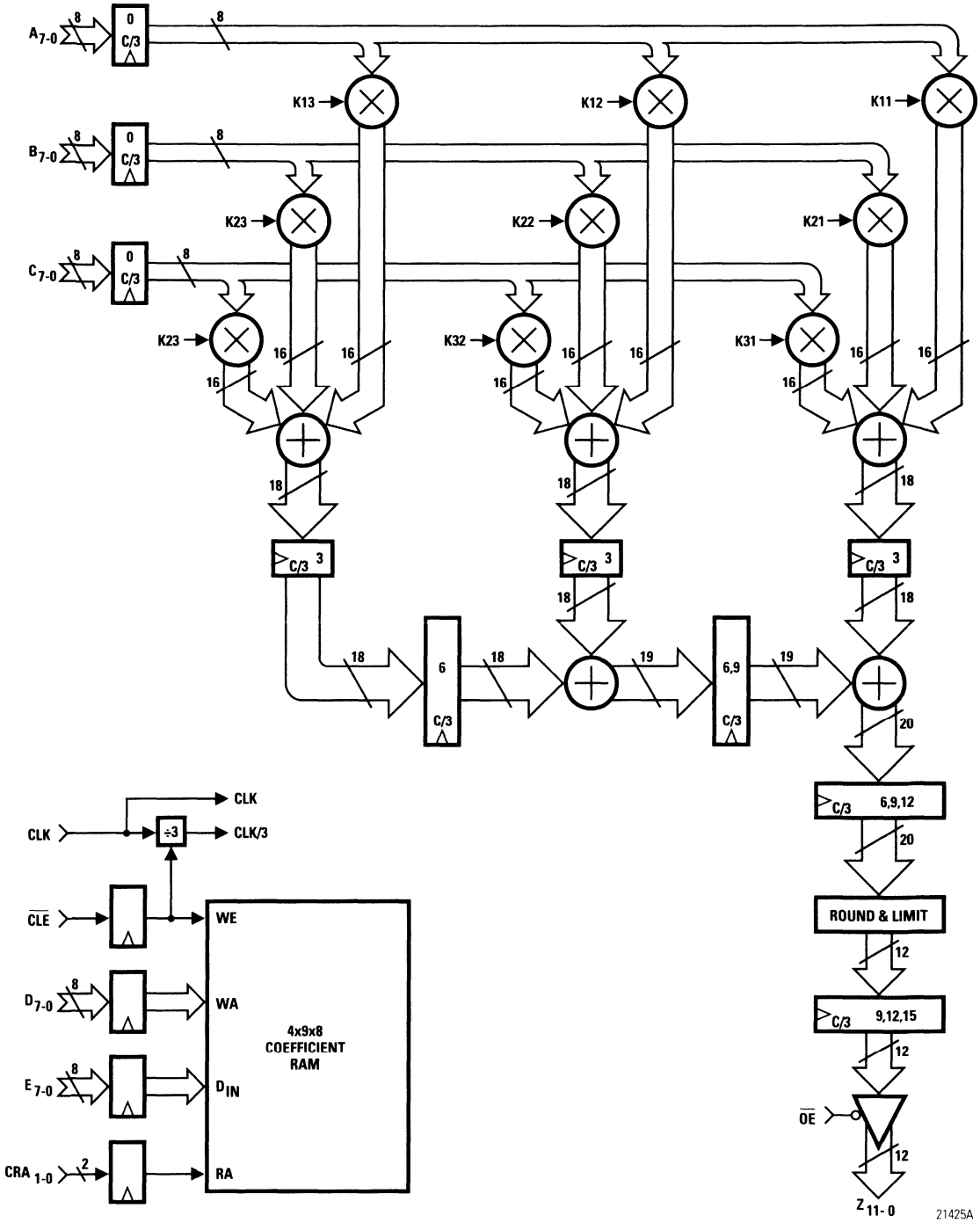
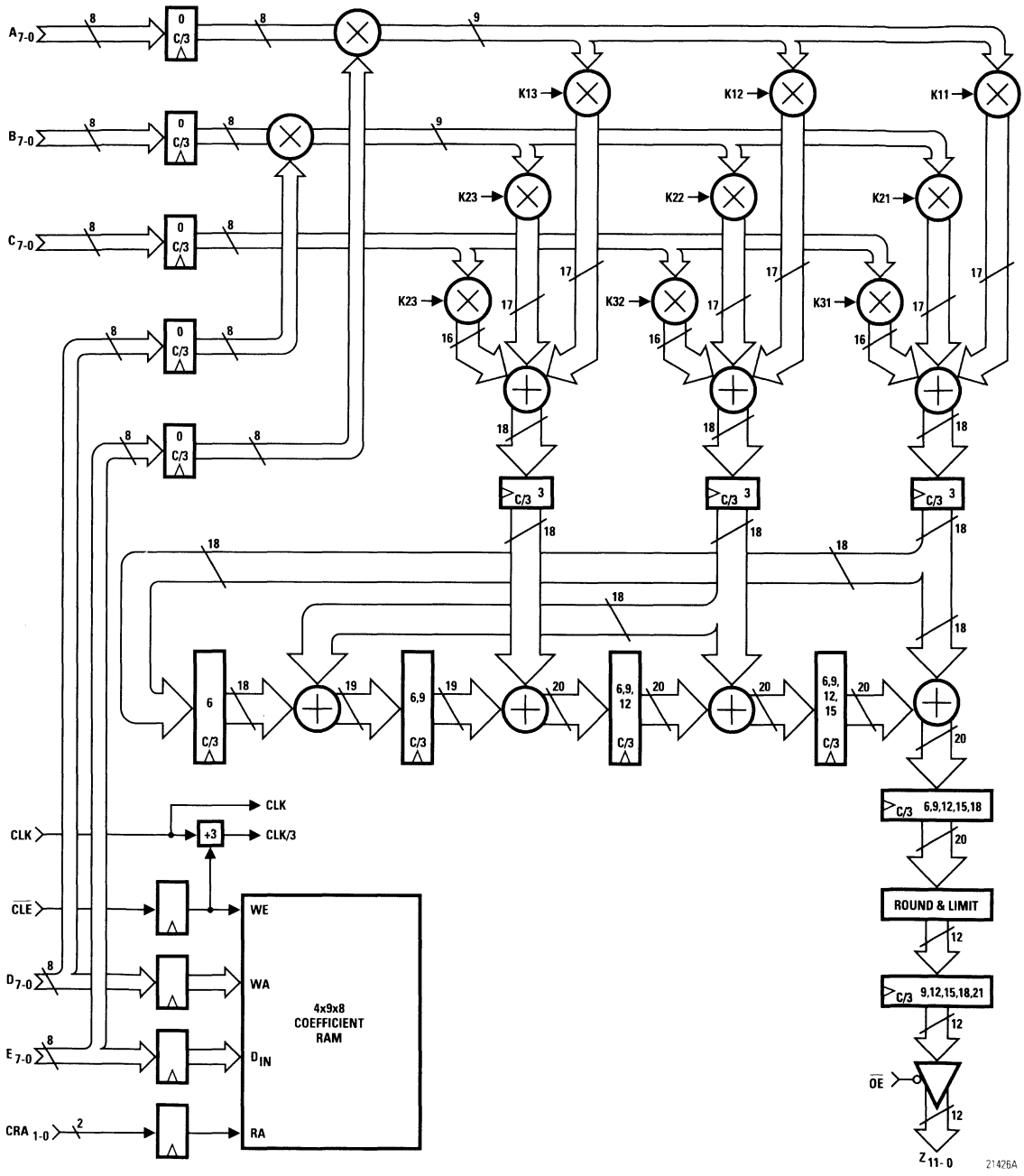


Figure 4. Functional Block Diagram, 5x5 Mode



Signal Definitions

Inputs

CLK — Master chip clock, 0 to 30MHz. All operations are referenced to the rising edges of CLK.

DATA INPUTS — Of the device's five 8-bit data input ports, A, B, and C are used exclusively as data inputs, whereas D and E are also used to program the device (see description of $\overline{CLE}$ pin). For 5x5 convolution, all five ports accept incoming data. In the other modes, only Ports A-C accept incoming data, leaving D and E dedicated to control and coefficient values, which may be updated at any time. In all modes, data are loaded on every third rising edge of CLOCK, beginning on a clock rising edge for which $\overline{CLE}$ makes a 0-to-1 transition. Bits A7, B7, ... are the two's complement sign bits or most significant unsigned bits; bits A_0, B_0, ... are the least significant bits (LSBs).

$\overline{CLE}$ — Active-LOW coefficient and control load enable. When $\overline{CLE}$ is LOW, E becomes the input port for the coefficients, and D becomes the coefficient write address and control port. When $\overline{CLE}$ is HIGH, all coefficients are held unchanged. A LOW to HIGH transition at $\overline{CLE}$ also synchronizes the TMC2255, ushering in a new data input.

CRA_0, CRA_1 — Coefficient read address. The chip can hold four "pages" of nine coefficients each. These two pins determine which of the four coefficient sets is to be used with the data entering during that cycle.

The timing of coefficient selection by CRA is mode dependent. In the 3(3x1) mode, CRA influences all coefficients simultaneously. In the 3x3 and 5x5 convolution modes, however, CRA selects the coefficients for each multiplier column individually, i.e., three per clock cycle from left to right (Block Diagram - 3x3 Mode). CRA should be changed only on "data input" clock cycles to avoid corrupting 3x3 or 3x(3x1) work in progress. CRA should not be updated during a 5x5 operation whose result is needed.

When updating coefficients on-the-fly the user should not set CRA_{1-0} and D5:4 to the same page, but should read from one page while writing to another.

$\overline{OE}$ — Asynchronous, active-LOW output enable. When $\overline{OE}$ is LOW, the output drivers are enabled. When $\overline{OE}$ is HIGH, they are disabled (high-impedance).

Outputs

DATA OUTPUTS — Outputs available on the Z Port are enabled by $\overline{OE}$. Z_{11} is the unsigned MSB or two's complement MSB/sign bit; Z_1 is the integer LSB ("ones' digit"). Z_0 is the 1/2 (fractional) digit. In the 3(3x1) mode (E=XXXXX0XX), a new valid result will emerge t_{DO} after every rising edge of CLOCK. In the other modes (E=XXXXX1XX), a result emerges after every third rising edge of CLOCK. When 9-bit limiting is used, bits Z_{11} through Z_8 will be identical.

Operation and Timing

Before operation, the TMC2255 must be initialized, i.e. loaded with coefficients and set to the desired operating mode, data format, and rounding precision. The chip is programmed via ports D and E, which double as data input ports in 5X5 mode.

Initialization

Chip Select

This control is accessed through bit 7 of port D. When $\overline{CLE}$ is LOW, D_7 must be LOW to allow the coefficient/control information to be updated. If D_7 is HIGH when $\overline{CLE}$ is forced LOW, the device will not allow the coefficient or control information to be updated, and device execution will begin or continue as commanded on the previous LOW to HIGH transition of $\overline{CLE}$. Holding D_7 HIGH (at least when $\overline{CLE}$ is LOW) permits the system to resynchronize the chip without changing any coefficients or configuration parameters.

Coefficient Loading

When $\overline{CLE}$ and D_7 are LOW, the coefficient values presented to port 6 are loaded into the coefficient position and page registers selected by port D, as shown below.

When D_{7-0} =	Update From E_{7-0}: Coef	Page
0XYY0000	1, 1	YY
0XYY0001	1, 2	YY
0XYY0010	1, 3	YY
0XYY0100	2, 1	YY
0XYY0101	2, 2	YY
0XYY0110	2, 3	YY
0XYY1000	3, 1	YY
0XYY1001	3, 2	YY
0XYY1010	3, 3	YY
0XXX0X11	Hold all Coefficients	
0XXXX011	Hold all Coefficients	
0XXX110X	Hold all Coefficients	
0XXX11X0	Hold all Coefficients	
0XXX1111	Control Information	
1XXXXXX	Hold all Coefficients	

X = Don't Care

Each of the four "pages" YY comprises a full set of nine coefficients (one per filter tap).

Mode Selection

When $\overline{CLE}$=0 and D=0XXX1111, pins E_{2-0} select the chip's operating MODE and input data formats, viz:

When E_{7-0} =	Mode =	Data Formats= A B C
0XXXX000	3(3x1)mat mpy	TC TC TC
0XXXX001	3(3x1)mat mpy	UN TC TC
0XXXX010	<Reserved – DO NOT USE>	
0XXXX011	3(3x1)mat mpy	UN UN UN
Z1 = A*K1,1 + B*K2,1 + C*K3,1		first of 3 results
Z2 = A*K1,2 + B*K2,2 + C*K3,2		
Z3 = A*K1,3 + B*K2,3 + C*K3,3		last of 3 results
0XXXX100	3x3 convolution	TC TC TC
0XXXX101	3x3 convolution	UN UN UN
Z = A1*K1,1 + B1*K2,1 + C1*K3,1 + A2*K1,2 + B2*K2,2 + C2*K3,2 + A3*K1,3 + B3*K2,3 + C3*K3,3		
0XXXX110	5x5 convolution	TC TC TC
0XXXX111	5x5 convolution	UN UN UN
Z = A1*K1,3 + B1*K2,3 + C1*K3,3 + D1*K2,3 + E1*K1,3 + A2*K1,2 + B2*K2,2 + C2*K3,2 + D2*K2,2 + E2*K1,2 + A3*K1,1 + B3*K2,1 + C3*K3,1 + D3*K2,1 + E3*K1,1 + A4*K1,2 + B4*K2,2 + C4*K3,2 + D4*K2,2 + E4*K1,2 + A5*K1,3 + B5*K2,3 + C5*K3,3 + D5*K2,3 + E5*K1,3		
1XXXXXXX	[Unchanged from previous setting]	

[Coefficients are always 8-bit two's complement.]

Rounding

All computuations are rounded internally following the final accumulation of products. Rounding position depends on the output format. If the user desires outputs with 1/2 LSB precision (relative to the inputs) then rounding is performed into Z_{-1}, just to the right of the LSB of the output port, Z_0. For 1 LSB precision, rounding is into Z_0, and the output is on pins Z_{11-1} only.

When E_{7-0} =	Outputs are,	Rounded at:
00XXXXXX	Z_{11}-Z_0 (12 bits)	Z_{-1}
01XXXXXX	Z_{11}-Z_1 (11 bits)	Z_{-0}
1XXXXXXX	Unchanged from previous setting	

Output Limiting

When $\overline{CLE}$=0 and D=0XXX1111, pins E_{5-3} tell the chip to which numerical format(s) to limit the emerging results. Unsigned (UN), two's complement (TC), and mixed data formats of 8, 9, or 12 bits (including Z_0) are supported, as follows. Limit "Z" applies to 3x3 and 5x5 convolutional modes; limits Z1, Z2, Z3 apply to 3(3x1) mode.

E_{7-0} =	Limit Z1 or Z	Limit Z2	Limit Z3	Range (RND=0)
0X000XXX	<Limiter Disabled>			
0X001XXX	UN9	UN9	UN9	0,255.5
0X010XXX	TC12	TC12	TC12	–1024,1023.5
0X011XXX	UN12	UN12	UN12	0,2047.5
0X100XXX	TC9	TC9	TC9	–128,127.5
0X101XXX	UN9	TC9	TC9	(mixed)
0X110XXX	<Reserved; Do Not Use>			
0X111XXX	UN8	UN8	UN8	0,127.5
1XXXXXX	Unchanged from previous setting			

Prior to output, the limiter (if enabled) tests the leading bits of the emerging result. In the unsigned limit modes, if the MSB=1, denoting a negative value, the output is forced to 0; if the MSB=0 but any other bit above the 8, 9 or 12 bit output field = 1, the output is forced to 11111111111.1 In the TC9 limit mode, values above 127.5 (00001111111.1) are forced to 00001111111.1 and values below –128 become 11110000000.0. In the TC12 limit mode, values above 1023.5 (01111111111.1) are forced to 01111111111.1, and values below –1024 become 10000000000.0. If full LSB rounding (E_6=1) is used, output bit Z_0 is ignored, each data format is correspondingly 1 bit narrower than shown in the table, and the .5 fractions disappear from the range limits.

Timing

Result Latency

Device operating mode affects when valid results will be available at the output port $Z_{11:0}$. The three results of a 3x1 triple dot product whose inputs enter on clock rising edge 0 will be available t_{D0} after clock rising edges 7, 8, and 9. In a 3 x 3 and 5 x 5 convolution, the first three impulse response points will emerge after clock rising edges 9, 12, and 15. The last two points of a 5-point response (5x5 mode) will follow after rising edges 18 and 21.

Instructions, Inputs, and Synchronization

Each rising edge of CLK which bears a $\overline{CLE}$ LOW to HIGH transistion resynchronizes the device. If $\overline{CLE}$ goes from LOW to HIGH on clock rising edge N, then the chip will resynchronize, starting a new 3-cycle sequence on that edge. It will look for incoming data at clock rising edges N+3i, where i = 1, 2, ... (*Timing Diagrams, Figures 5* through *11*). If $\overline{CLE}$ is brought LOW while an operation is already in progress (e.g., to update coefficients), it should be brought HIGH only on a regular data input clock cycle (N+3i), to avoid corrupting pending results.

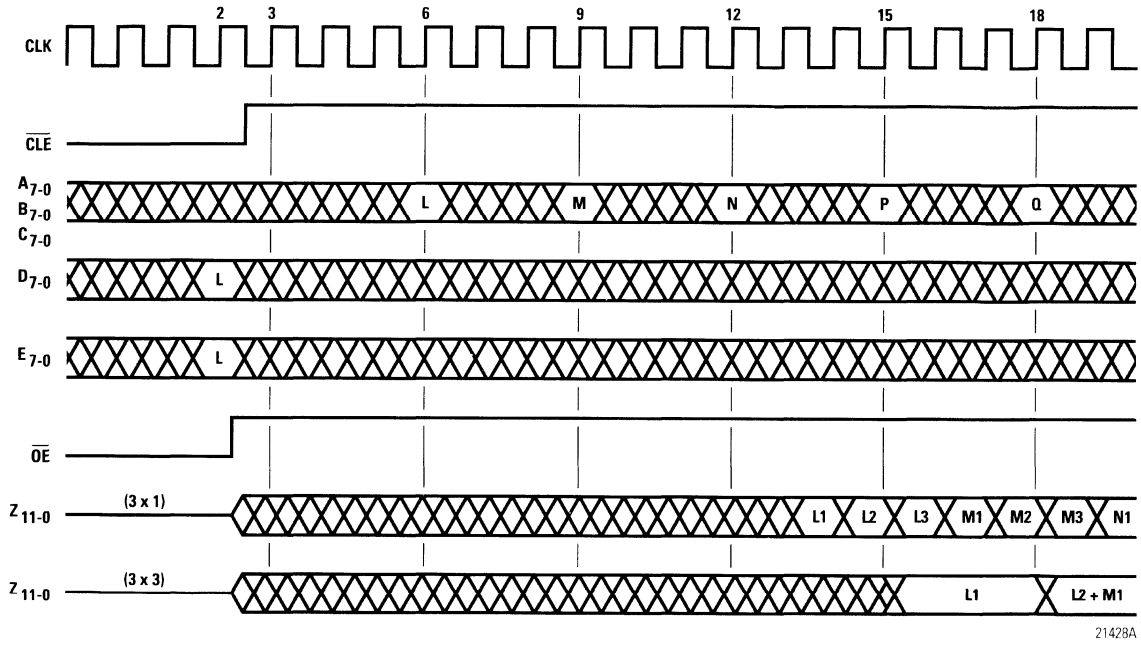
If $\overline{CLE}$ is LOW, control and/or coefficient information entering on a rising edge of CLK will affect all subsequent data inputs until the control parameters are again updated. Internal pipelining of the controls ensures that "in progress" operations on data previously input to the device will continue unaffected, as long as $\overline{CLE}$ is brought HIGH only on data input clock edges.

System Timing

Because the TMC2255's data throughput rate is 1/3 of its incoming clock rate, the user must synchronize the data inputs with the chip's control inputs and internal operation. *Figures 5* through *8* illustrate four ways to use rising edges of $\overline{CLE}$ to align data inputs in the 3(3x1) and 3x3 modes, whereas *Figures 9* through *11* show how to use $\overline{CLE}$ in the 5x5 mode.

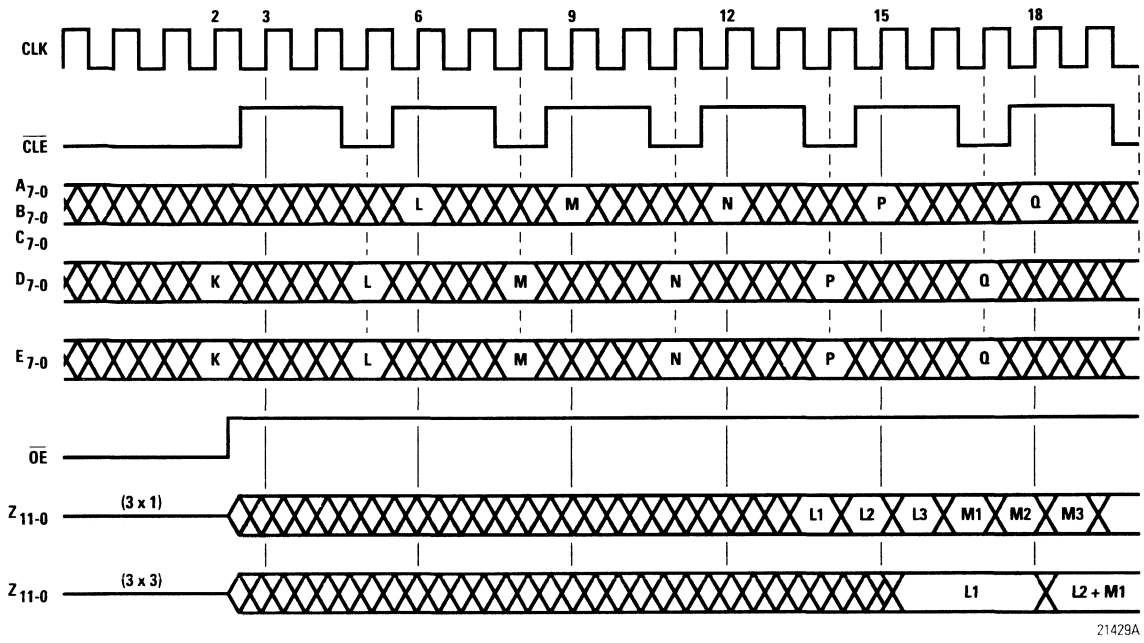
In *Figure 5*, the $\overline{CLE}$ 0 to 1 transition on CLK rising edge 3("t = 3") initializes the chip. The final configuration and coefficient values are loaded through ports D and E at t = 2 and the first incoming data enter ports A, B, and C on rising edge 6. In 3(3x1) mode, the three results from the t = 6 input data emerge after t = 13, 14, and 15. In 3x3 mode, the first result from the edge 6 input data appears after edge 15 and remains until t = 18, when the second result using t = 6 inputs (which is the first result using t = 9 inputs) emerges. After t = 18, the convolution of the t = 6, t = 9, and t = 12 inputs, the last output involving the t = 6 input, appears. The part operates continuousy, with inputs read on every third rising clock edge and a new output available t_{DO} after each rising clock edge (3(3x1) mode) or every third rising edge (3x3 mode).

Figure 5. 3(3x1), 3x3 Timing Diagram, Single $\overline{CLE}$ Rising Edge



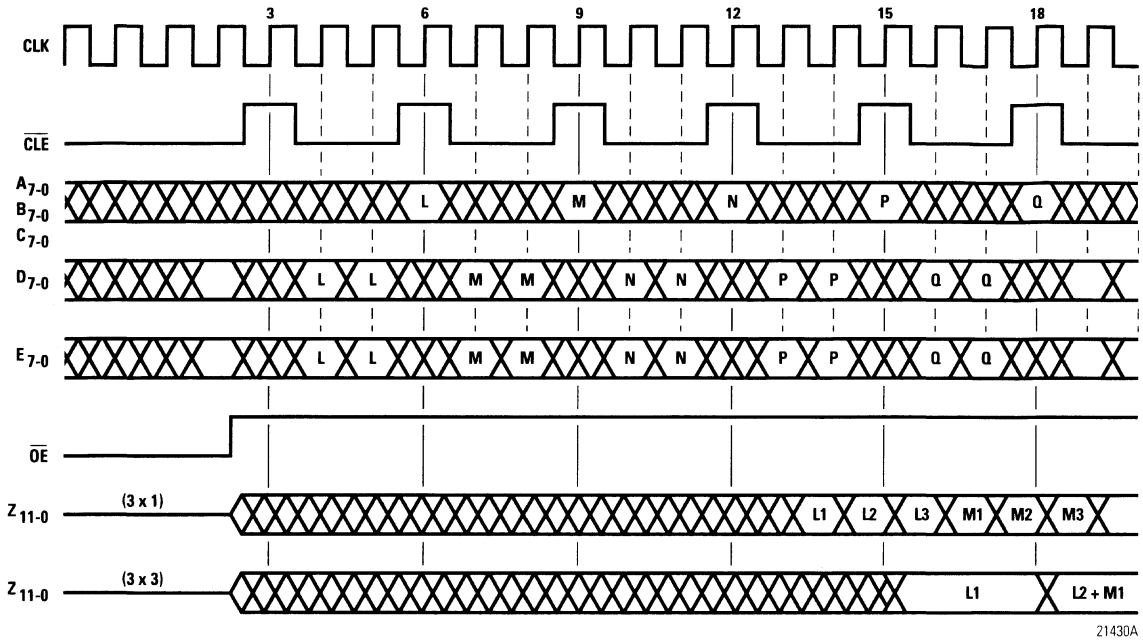
In *Figure 6*, CLK rising edges at t = 3, 6, 9, ... resynchronize the chip, with configuration or coefficient updates at t = 2, 5, 8, ... Data input/output timing is unchanged from *Figure 4*.

Figure 6. 3xX Modes, Periodic Long $\overline{CLE}$ Pulses



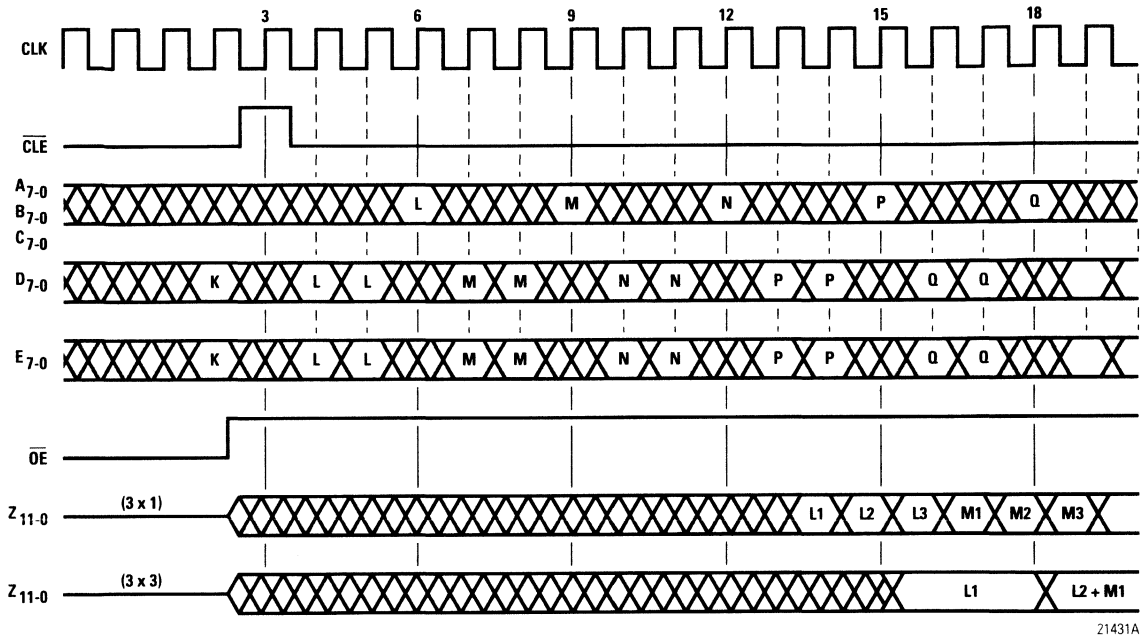
In *Figure 7*, CLK rising edges at t = 3, 6, 9, ... again resynchronize the chip, but configuration and coefficients may be changed twice as often, at t = 1, 2, 4, 5, 7, 8, ...

Figure 7. 3xX Modes, Periodic Short $\overline{CLE}$ Pulses



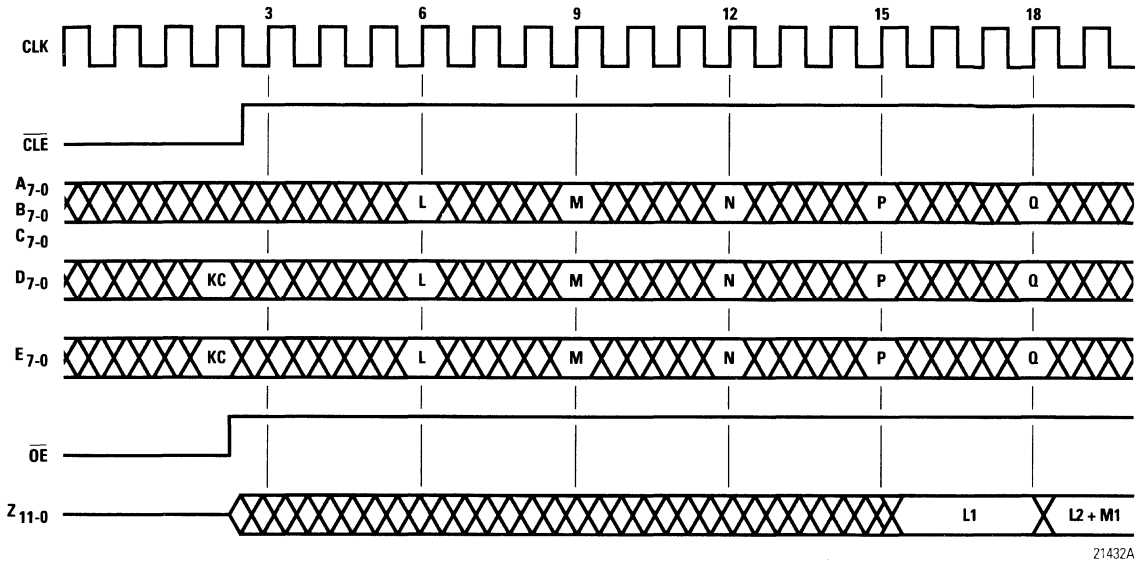
In *Figure 8*, data timing is the same as that of *Figure 5*. However, since $\overline{CLE}$ is left LOW after the one-cycle initialization pulse, instructions and coefficients may be updated on every clock cycle, or three times per data input. Instructions entering between data values, e.g. at t = 4 or t = 5, affect the next data value (i.e., that entering at t = 6). Instructions entering with a given data value (e.g., t = 6) affect the next data input (i.e., at t = 9).

Figure 8. 3xX Modes, Single $\overline{CLE}$ Rising Edge



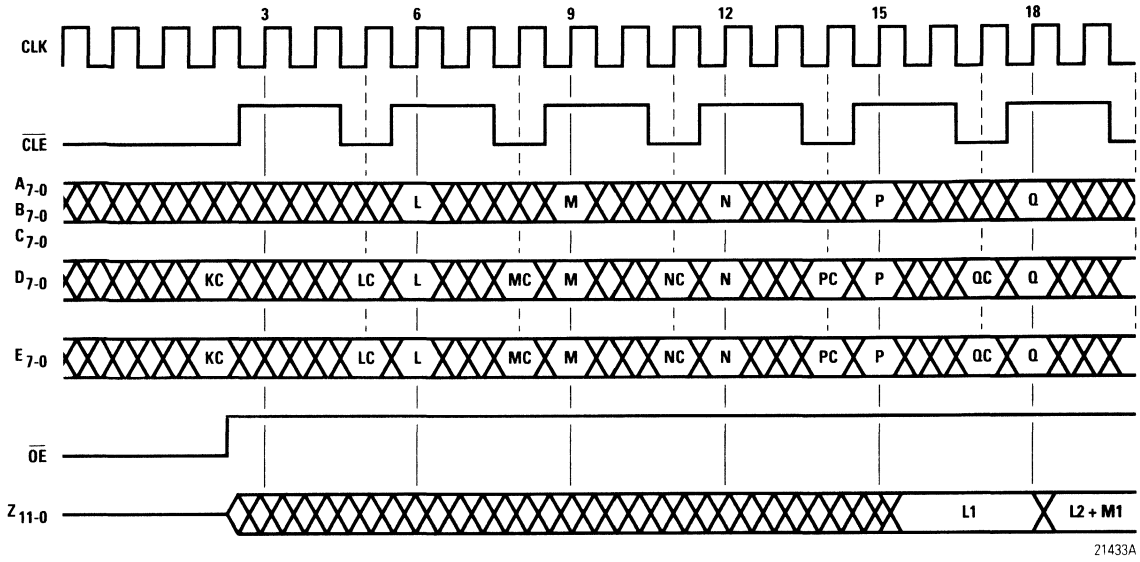
In *Figure 9*, the CLK rising edge at t = 3 synchronizes the operation. The final configuration and coefficient values are loaded through ports D and E at t = 2 and the first incoming data enter ports A through E at t = 6. The first result using the t = 6 input appears after t = 15 and remains until t = 18. The last result using the t = 6 input emerges after t = 27 and remains until t = 30. The part operates continuously, with data inputs read on every third rising edge of CLK and a new output available t_{DO} after every third rising edge of CLK.

Figure 9. 5x5 Convolution, Single $\overline{CLE}$ Rising Edge



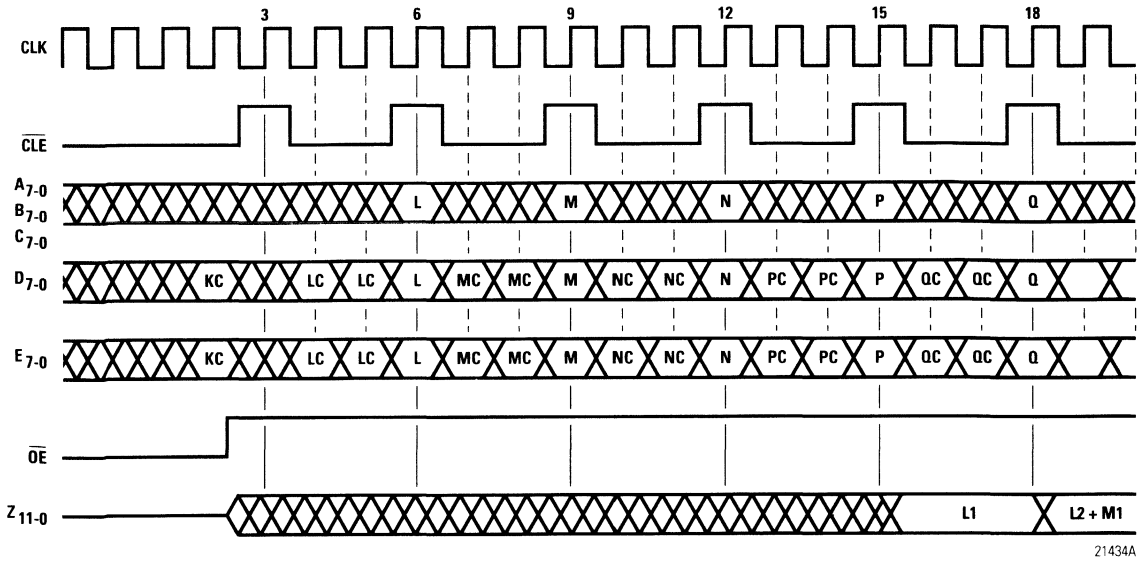
In *Figure 10*, one new coefficient or configuration value can be input for every data input, at t = 5, 8, 11, ...

Figure 10. 5x5 Convolution, Periodic Long $\overline{CLE}$ Pulse



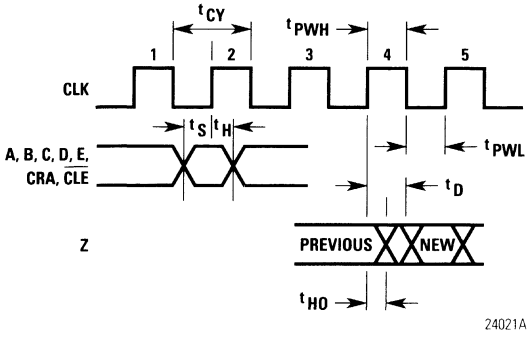
In *Figure 11*, two new coefficients or configuration values can be loaded for every incoming data point, at t = 4, 5, 7, 8, 10, 11, ...

Figure 11. 5x5 Convolution, Periodic Short $\overline{CLE}$ Pulse



In 5x5 mode, $\overline{CLE}$ should not be left LOW continuously, since ports D and E must serve as data inputs on every third clock cycle. If $\overline{CLE}$ is LOW on a data input cycle, the chip will interpret the current D and E inputs as both data and instructrions/coefficients.

Figure 12. I/O Timing Diagram



Power-Up Sequence

To ensure proper operation, the TMC2255 should receive at least two clock rising edges soon after power-up, with $\overline{CLE}$ making a 0-to-1 transition on edge 4, 5, or 6. Otherwise, some of the internal multiplexers will power up in disallowed states and draw excessive power.

Data Formats

Figure 13 summarizes the TMC2255's data and coefficient formats for all operating modes. Although integer weighting of input data is shown, the binary point may be moved anywhere to the left, as long as the binary point of the output is moved the same distance. Likewise, the coefficient binary point can be moved, as long as the output binary point is moved equally or the data input binary point is moved in the opposite direction. In all coefficients and in all two's complement data, the most significant bit carries a negative weighting.

Figure 13. Data Formats and Bit Alignment

	2^{10}	...	2^{7}	...	2^{2}	2^{1}	2^{0}.	2^{-1}	2^{-2}	...	2^{-6}
Data at Input Ports:			A_7	...	A_2	A_1	A_0.				
Coefficients:						K_7	K_6.	K_5	K_4	...	K_0
Internally Accumulated Products:	P_{16}	...	P_{13}	...	P_8	P_7	P_6.	P_5	P_4	...	P_0
Data at Output Port (Round = 0):	Z_{11}	...	Z_8	...	Z_3	Z_2	Z_1.	Z_0			
Data at Output Port (Round = 1):	Z_{11}	...	Z_8	...	Z_3	Z_2	Z_1.	(Ignore Z_0)			

Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage	−0.5 to (V_{DD} + 0.5)V[2]
Forced current	−6.0 to 6.0mA[3,4]
Short-circuit duration	
(single output in HIGH state to ground)	1 sec
Temperature	
Operating case	−60 to +130°C
junction	175°C
Lead soldering (10 seconds)	300°C
Storage	−65 to 150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{DD}	Supply Voltage	4.75	5.0	5.25	V
V_{IL}	Input Voltage LOW			0.8	V
V_{IH}	Input Voltage HIGH	2.0			V
I_{OL}	Output Current LOW			4.0	mA
I_{OH}	Output Current HIGH			−2.0	mA
t_{CY}	Cycle Time				
	TMC2255	33			ns
	TMC2255-1	27			ns
t_{PWL}	Clock Pulse Width LOW				
	TMC2255	16			ns
	TMC2255-1	14			ns
t_{PWH}	Clock Pulse With HIGH				
	TMC2255	13			ns
	TMC2255-1	10			ns
t_S	Input Setup Time				
	TMC2255	8			ns
	TMC2255-1	6			ns
t_H	Input Hold Time	0			ns
t_A	Ambient Temperature	0	25	70	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Temperature Range: Standard Max	Units
I_{DDQ}	Supply Current, Quiesc	V_{DD}=Max, V_{IN}=0	15	mA	
I_{DDU}	Supply Current, No Load	V_{DD}=Max, t_{CY}=50ns	100	mA	
I_{IL}	Input Current, LOW		−10	µA	
I_{IH}	Input Current, HIGH		10	µA	
V_{OL}	Output Voltage, LOW		0.4	V	
V_{OH}	Output Voltage, HIGH		2.0		V
I_{OS}	Short-Circuit Out Current		−100	uA	
C_I	Input Capacitance		10	pF	
C_O	Output Capacitance		10	pF	

Note: Actual test conditions may vary from those shown, but guarantee operation as specified.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Temperature Range: Standard Max	Units
t_D	Output Delay	V_{DD}=Min, C_L=25pF			
	TMC2255			22	ns
	TMC2255-1			19	ns
t_{HO}	Output Hold	V_{DD}=Max, C_L=25pF		6	ns
t_{ENA}	Output Enable	V_{DD}=Min, C_L=25pF			
	TMC2255			18	ns
	TMC2255-1			15	ns
t_{DIS}	Output Disable	V_{DD}=min, C_L=25pF			
	TMC2255			21	ns
	TMC2255-1			20	ns

Figure 14. Equivalent Input Circuit

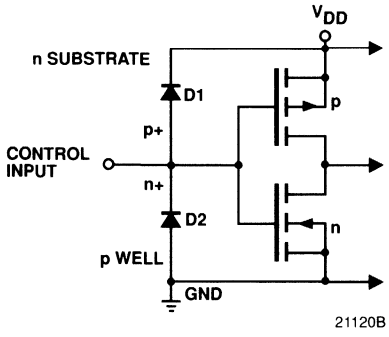


Figure 15. Equivalent Output Circuit

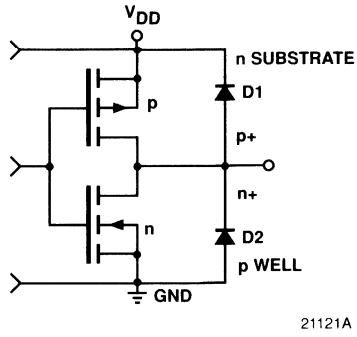
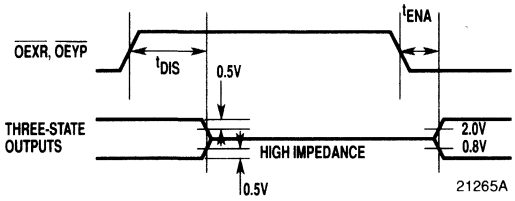


Figure 16. Transition Levels for Three-State Measurements



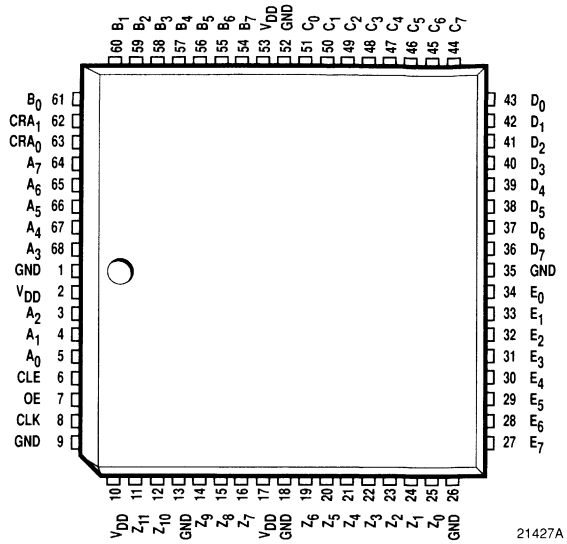
H

Package Interconnections

Signal Type	Signal Name	Function	R1 Package
Power	V_{DD}	Supply Voltage (+5)	2,10,17,53
	GND	Ground	1,9,18,26,35,52
Clock	CLK	System Clock	8
Control	$\overline{CLE}$	Coefficient Load Enable	6
	$\overline{OE}$	Output Enable	7
	CRA_{1-0}	Coefficient Read Address	62,63
Inputs	A_{7-0}	Data Input Port A	64,65,66,67,68,3,4, 5
	B_{7-0}	Data B	54,55,56,57,58,59,60,61
	C_{7-0}	Data C	44,45,46,47,48,49,50,51
	D_{7-0}	Control/Data D	36,37,38,39,40,41,42,43
	E_{7-0}	Coefficient/Data E	27,28,29,30,31,32,33,34
Outputs	Z_{11-0}	Data Outputs	11,12,14,15,16,19,20,21,22,23,24,25

Pin Assignments – 68-Lead Plastic Chip Carrier – R1 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	18	GND	35	GND	52	GND
2	V_{DD}	19	Z_6	36	D_7	53	V_{DD}
3	A_2	20	Z_5	37	D_6	54	B_7
4	A_1	21	Z_4	38	D_5	55	B_6
5	A_0	22	Z_3	39	D_4	56	B_5
6	$\overline{CLE}$	23	Z_2	40	D_3	57	B_4
7	$\overline{OE}$	24	Z_1	41	D_2	58	B_3
8	CLK	25	Z_0	42	D_1	59	B_2
9	GND	26	GND	43	D_0	60	B_1
10	V_{DD}	27	E_7	44	C_7	61	B_0
11	Z_{11}	28	E_6	45	C_6	62	CRA_1
12	Z_{10}	29	E_5	46	C_5	63	CRA_0
13	GND	30	E_4	47	C_4	64	A_7
14	Z_9	31	E_3	48	C_3	65	A_6
15	Z_8	32	E_2	49	C_2	66	A_5
16	Z_7	33	E_1	50	C_1	67	A_4
17	V_{DD}	34	E_0	51	C_0	68	A_3



21427A

Ordering Information

Product Number	Data Rate MHz	Temperature Range	Screening	Package	Package Marking
TMC2255R1C	10	STD-T_A = 0°C to 70°C	Commercial	68 Pin PLCC	2255R1C
TMC2255R1C1	12.5	STD-T_A = 0°C to 70°C	Commercial	68 Pin PLCC	2255R1C1

All parameters in this specification are guaranteed by design, characterization, sample testing ot 100% testing, as appropriate.
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Fixed-Point Arithmetic

Since the first monolithic multiplier was introduced by TRW in 1976, and multiplication was changed from something difficult to something easy, this building block has become ubiquitous in the world of signal processing. TRW continues to provide the broadest line of fixed-point multipliers, with word sizes from 8 to 16 bits, with and without embedded accumulators.

Bringing the same ease-of-application to another difficult arithmetic problem in signal processing, the TMC3211 Integer Divider produces a 32-bit quotient at 20 million operations/second. Now it is no longer necessary to avoid division in image and signal processing algorithms.

Product	Description	Size	Clock Rate [1] (MHz)	Power [1] (Watts)	Package	Grades [2]	Notes	Page
TMC208K-1	Multiplier	8 x 8	45	0.55	B5, N5 40 Pin DIP	C	Two's Complement.	I51
			50	0.55	B5 40 Pin DIP	V, SMD	Compatible with MPY008H.	
-			65	0.55	B5, N5 40 Pin DIP	C		
			70	0.55	B5 40 Pin DIP	V, SMD		
TMC28KU-1	Multiplier	8 x 8	45	0.55	B5, N5 40 Pin DIP	C	Unsigned Magnitude.	I51
			50	0.55	B5 40 Pin DIP	V, SMD	Compatible with MPY008H.	
-			65	0.55	B5, N5 40 Pin DIP	C		
			70	0.55	B5 40 Pin DIP	V, SMD		
MPY012H	Multiplier	12 x 12	115	3.7	J1 64 Pin DIP	C	24-Bit Product.	I3
			140	4.1	J1 64 Pin DIP	A		
MPY112K	Multiplier	12 x 12	50	2.4	J4 48 Pin DIP	C	16-Bit Product.	I29
			55	3.0	J4 48 Pin DIP	A		
TMC216H	Multiplier	16 x 16	145	0.37	J3 64 Pin DIP	C	32-Bit Product.	I61
			185	0.37	J3 64 Pin DIP	A		
MPY016K-1	Multiplier	16 x 16	40	4.6	J1 64 Pin DIP	C	32-Bit Product.	I15
			45	4.6	J1 64 Pin DIP	A		
-	Multiplier	16 x 16	45	4.6	J1 64 Pin DIP	C		
			50	4.6	J1 64 Pin DIP	A		
TMC2208	Multiplier-Accumulator	8 x 8	40	0.4	J4, N4 48 Pin DIP	C	Compatible with TDC1008.	I75
					R1 68 Lead PLCC	C		
			50	0.4	J4 48 Pin DIP	V		
TMC2009	Multiplier-Accumulator	12 x 12	135	0.32	J3 64 Pin DIP	C		I39
			170	0.32	J3 64 Pin DIP	V		
			170	0.32	C1 64 Contact CC	V		
TMC2210-1	Multiplier-Accumulator	16 x 16	65	0.33	N0 64 Pin DIP	C	Industry-Standard 16-Bit MAC.	I85
					G8 69 Pin PGA	C		
			80	0.33	J0 64 Pin DIP	V		
					G8 69 Pin PGA	V		
-			80	0.33	N0 64 Pin DIP	C		
					G8 69 Pin PGA	C		
			100	0.33	J0 64 Pin DIP	V		
					G8 69 Pin PGA	V		
-2			100	0.33	N0 64 Pin DIP	C		
-3			160	0.33	N0 64 Pin DIP	C		
TMC3211	Integer Divider	32-Bit	50	0.82	H5 121 Pin PPGA	C	32-Bit Dividend, Quotient	I95

Notes: 1. Guaranteed. See product specifications for test conditions.

2. A = High Reliability, $T_C = -55°C$ to $125°C$.
C = Commercial, $T_A = 0°C$ to $70°C$.
V = MIL-STD-883 Compliant, $T_C = -55°C$ to $125°C$
SMD = Available per Standardized Military Drawing, $T_C = -55°C$ to $125°C$.

MPY012H

Multiplier
12 x 12 Bit, 115ns

The MPY012H is a high-speed 12 x 12 bit parallel multiplier which operates at a 115ns cycle time (8.7MHz multiplication rate). The multiplicand and the multiplier may be independently specified as two's complement or unsigned magnitude, yielding a full-precision 24-bit product.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The MPY012H is built with TRW's 2-micron bipolar process.

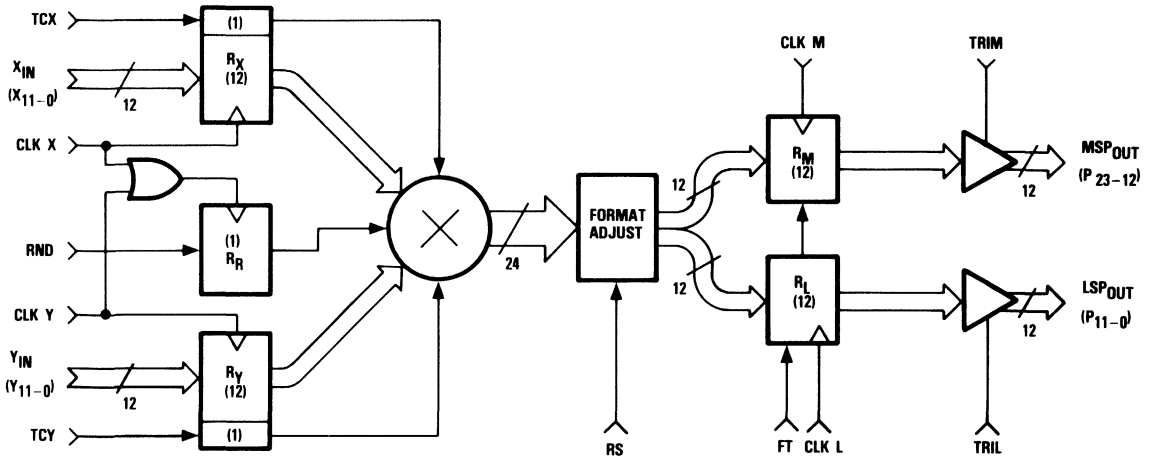
Features

- 115ns Multiply Time (Worst Case)
- 12 x 12 Bit Parallel Multiplication With 24-Bit Product Output
- Three-State Outputs
- Fully TTL Compatible
- Two's Complement, Unsigned Magnitude, And Mixed Mode Multiplication
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In A 64 Pin Ceramic DIP

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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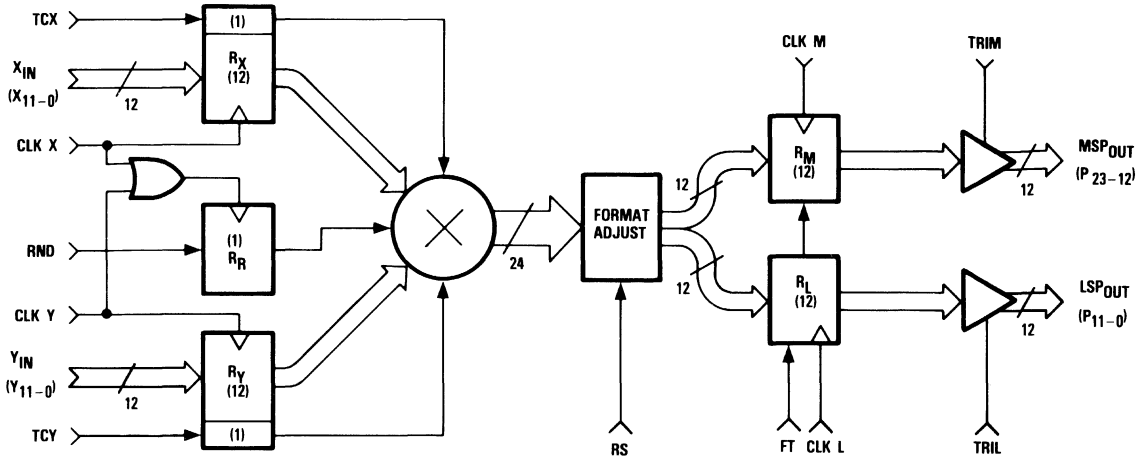
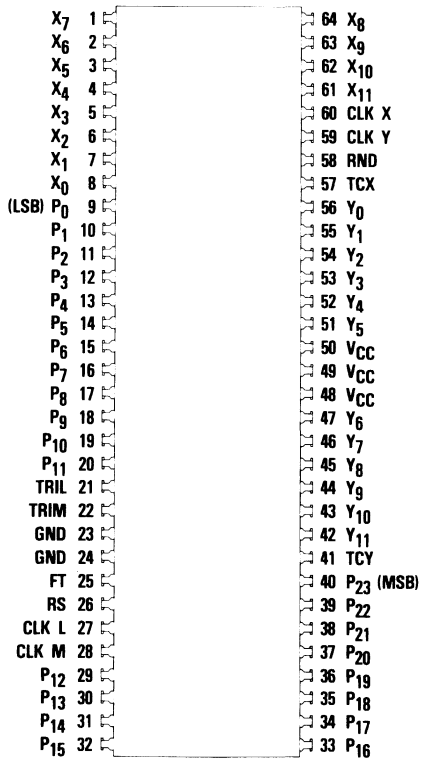
Functional Block Digram



Pin Assignments



64 Lead DIP - J1 Package

Functional Description

General Information

The MPY012H has three functional sections: input registers, an asynchronous multiplier array, and output registers. The input registers store the two 12-bit numbers which are to be multiplied and the instruction which controls the output rounding. This rounding control is used when a single-word output is desired. Each input operand is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders, designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 12-bit words, the Most Significant Product (MSP) and the Least Significant Product (LSP). Three-state output drivers allow the MPY012H to be used on a bus, or allow the least and most significant outputs to be multiplexed over the same 12-bit output lines.

Power

The MPY012H operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J1 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 48, 49, 50
GND	Ground	0.0V	Pins 23, 24

Control

The MPY012H has seven control lines:

FT — A control line which makes the output register transparent if it is HIGH.

TRIM, TRIL — Three-state enable lines for the MSP and the LSP. The output driver is in the high-impedance state when TRIM or TRIL is HIGH, and enabled when the appropriate control is LOW.

RS — RS is an output format control. A HIGH level on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, and two's complement integer operations.

RND — When RND is HIGH, a one is added to the MSB of the LSP. Note that this bit depends on the state of the RS control. If RS is LOW when RND is HIGH, a one will be added to the 2^{-12} bit (P_{10}). If RS is HIGH when RND is HIGH, a one will be added to the 2^{-11} bit (P_{11}). In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction; in some systems this may introduce a systematic bias.

TCX, TCY — Control how the device interprets data on the X and Y inputs. A HIGH on TCX or TCY forces the MPY012H to consider the appropriate input as a two's complement number, while a LOW forces the MPY012H to consider the appropriate input as a magnitude only number.

FT, RS, TRIM and TRIL are not registered. The TCX input is registered, and clocked in at the rising edge of the X clock signal, CLK X. The TCY input is also registered, and clocked in at the rising edge of the Y clock signal, CLK Y. The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading the RND control signal can be avoided by the use of normally LOW clocks.

Control (Cont.)

Name	Function	Value	J1 Package
RND	Round Control Bit	TTL	Pin 58
TCX	X Input, Two's Complement	TTL	Pin 57
TCY	Y Input, Two's Complement	TTL	Pin 41
FT	Output Register Feedthrough	TTL	Pin 25
RS	Output Right Shift	TTL	Pin 26
TRIM	MSP Three-State Control	TTL	Pin 22
TRIL	LSP Three-State Control	TTL	Pin 21

Data Inputs

The MPY012H has two 12-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{11} and Y_{11}, carry the sign information for the two's complement notation. The remaining bits are denoted X_0 through X_{10} and Y_0 through Y_{10} (with X_0 and Y_0 the Least Significant Bits). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6.

Name	Function	Value	J1 Package
X_{11}	X Data MSB	TTL	Pin 61
X_{10}		TTL	Pin 62
X_9		TTL	Pin 63
X_8		TTL	Pin 64
X_7		TTL	Pin 1
X_6		TTL	Pin 2
X_5		TTL	Pin 3
X_4		TTL	Pin 4
X_3		TTL	Pin 5
X_2		TTL	Pin 6
X_1		TTL	Pin 7
X_0	X Data LSB	TTL	Pin 8
Y_{11}	Y Data MSB	TTL	Pin 42
Y_{10}		TTL	Pin 43
Y_9		TTL	Pin 44
Y_8		TTL	Pin 45
Y_7		TTL	Pin 46
Y_6		TTL	Pin 47
Y_5		TTL	Pin 51
Y_4		TTL	Pin 52
Y_3		TTL	Pin 53
Y_2		TTL	Pin 54
Y_1		TTL	Pin 55
Y_0	Y Data LSB	TTL	Pin 56

Data Outputs

The MPY012H has a 24-bit two's complement or unsigned magnitude output which is the product of the two input data values. This output is divided into two 12-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP). The Most Significant Bit (MSB) of both the MSP and the LSP is the sign bit if fractional two's complement notation is used (TCX=TCY=1, RS=0). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6. For the MSP and LSP to be read, the respective TRIM and TRIL controls must be LOW. RS is an output format control. A logical "1" on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, or integer two's complement operation.

Name	Function	Value	J1 Package
P_{23}	Product MSB	TTL	Pin 40
P_{22}		TTL	Pin 39
P_{21}		TTL	Pin 38
P_{20}		TTL	Pin 37
P_{19}		TTL	Pin 36
P_{18}		TTL	Pin 35
P_{17}		TTL	Pin 34
P_{16}		TTL	Pin 33
P_{15}		TTL	Pin 32
P_{14}		TTL	Pin 31
P_{13}		TTL	Pin 30
P_{12}		TTL	Pin 29
P_{11}		TTL	Pin 20
P_{10}		TTL	Pin 19
P_{9}		TTL	Pin 18
P_{8}		TTL	Pin 17
P_{7}		TTL	Pin 16
P_{6}		TTL	Pin 15
P_{5}		TTL	Pin 14
P_{4}		TTL	Pin 13
P_{3}		TTL	Pin 12
P_{2}		TTL	Pin 11
P_{1}		TTL	Pin 10
P_{0}	Product LSB	TTL	Pin 9

Clocks

The MPY012H has four clock lines, one for each of the input registers and one for each product register. Data and two's complement instructions present at the inputs of these registers are loaded into the registers at the rising edge of the appropriate clock. The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading this control signal can be avoided by the use of normally LOW clocks.

Name	Function	Value	J1 Package
CLK X	Clock Input Data X	TTL	Pin 60
CLK Y	Clock Input Data Y	TTL	Pin 59
CLK L	Clock LSP Register	TTL	Pin 27
CLK M	Clock MSP Register	TTL	Pin 28

Figure 1. Fractional Two's Complement Notation

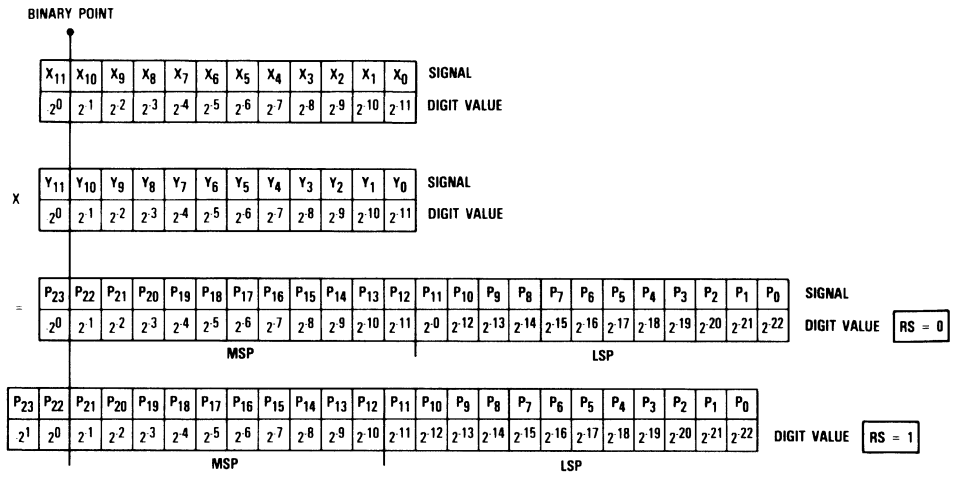


Figure 2. Fractional Unsigned Magnitude Notation

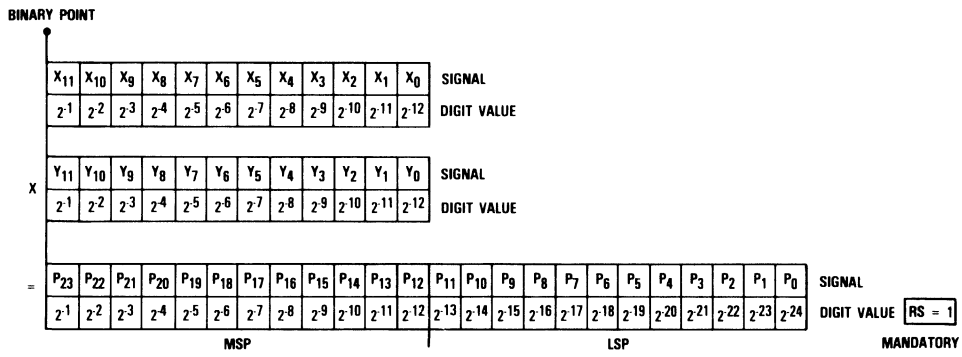


Figure 3. Fractional Mixed Mode Notation

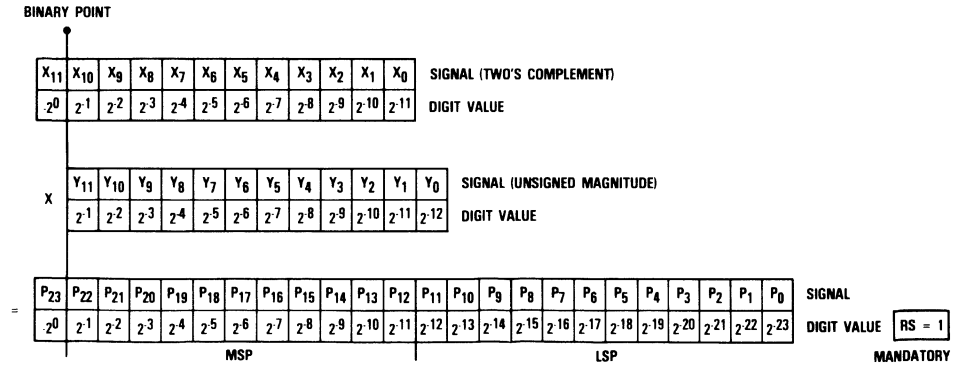


Figure 4. Integer Two's Complement Notation

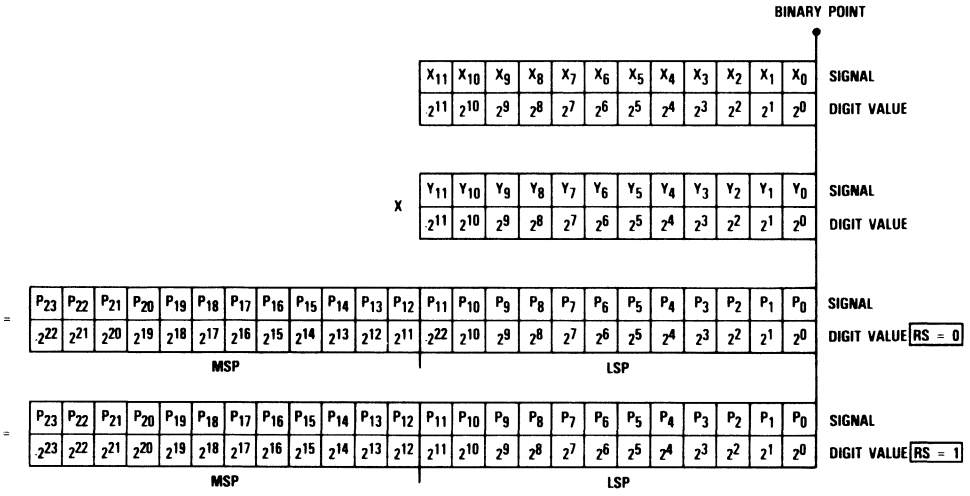


Figure 5. Integer Unsigned Magnitude Notation

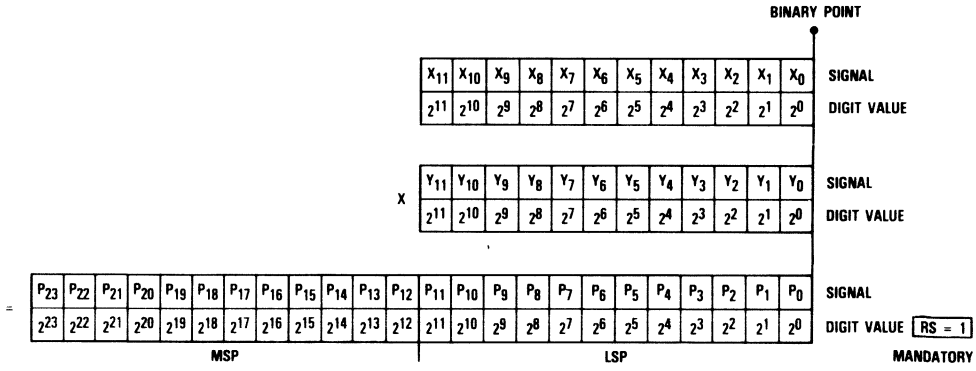


Figure 6. Integer Mixed Mode Notation

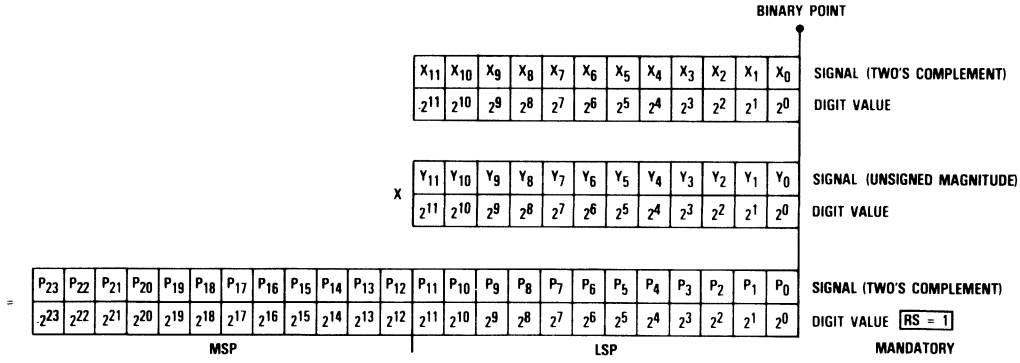


Figure 7. Timing Diagram

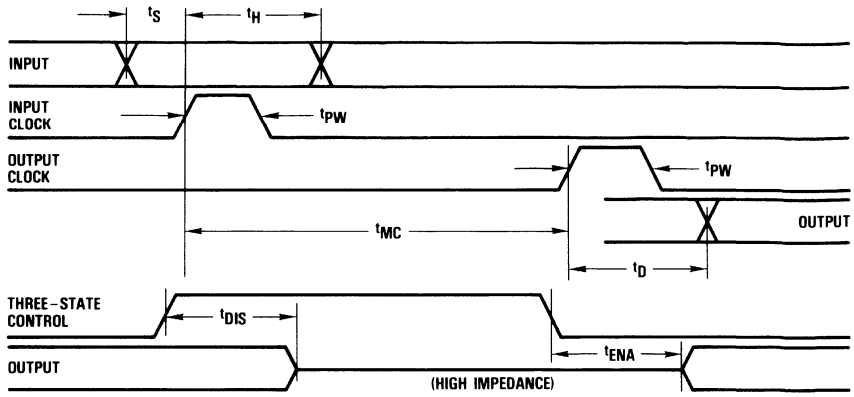


Figure 8. Timing Diagram, Unclocked Mode

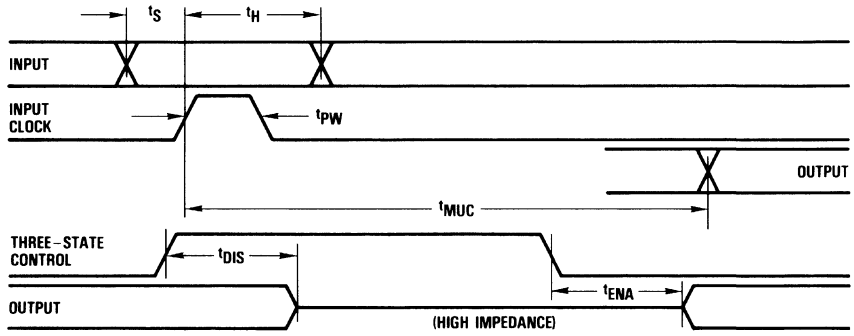
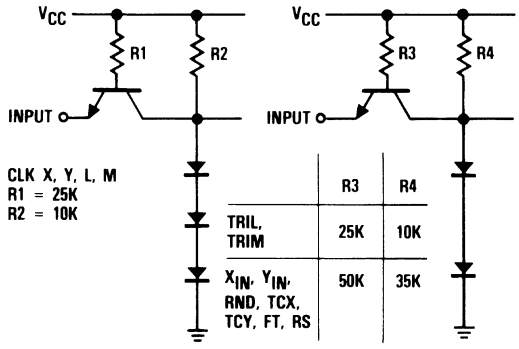


Figure 9. Equivalent Input Circuit



	R3	R4
TRIL, TRIM	25K	10K
X_{IN}, Y_{IN}, RND, TCX, TCY, FT, RS	50K	35K

Figure 10. Equivalent Output Circuit

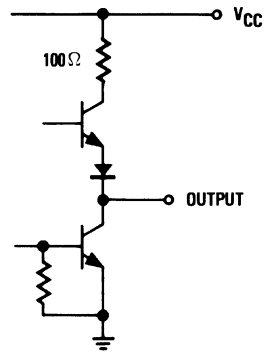


Figure 11. Test Load

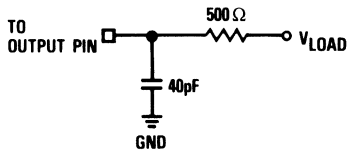
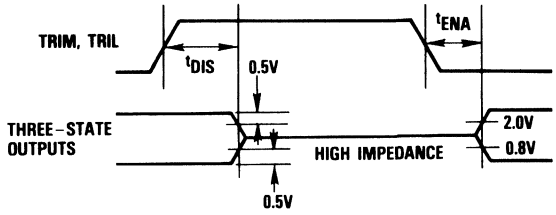


Figure 12. Three-State Delay Test Load



Application Notes

Mixed Mode Multiplication

There are several applications in which mixed mode multiplication may be advantageous. For example, inputs to a digital signal processor are often generated as unsigned magnitude numbers (e.g., data from an analog-to-digital converter). These numbers are effectively all positive values. In contrast, filter coefficients must often be negative. As a result, either the unsigned magnitude data must be converted to two's complement notation (which requires an additional bit), or the multiplier must be capable of mixed mode operation. The MPY012H provides this capability by independently specifying the mode of the multiplicand (X) and the multiplier (Y) on the TCX and TCY pins. No additional circuitry is required and the resulting product is in two's complement notation.

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the selected register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the MPY012H does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design.

Because common design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 6.

Register Shift (RS) Control

In two's complement notation, the acceptable range of values for a given word size is not the same for positive and negative numbers. The largest negative number is one LSB larger than the largest positive number. This is true for either fractional or integer notation. A problem can arise when the largest representable negative number is multiplied by itself. This should give a positive number of the same magnitude. However, the largest representable positive number is one LSB less than this value. As a result, this product cannot be correctly represented without using one additional output bit.

The MPY012H has a Register Shift (RS) control that permits shifting of the result to provide a correct answer for every two's complement multiplication. When RS is active, the value of all bits in the MSP is doubled (i.e., shifted left one position), which provides the capability to represent the largest possible product. The MSB of the Least Significant Product is changed from a duplicate of the sign bit to the necessary bit to fill in the output word. The effects of this control are illustrated in Figures 1 and 4. Note that for unsigned magnitude operation, the RS control must be HIGH.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage		−0.5 to +7.0V
Input		
	Applied voltage	−0.5 to +5.5V [2]
	Forced current	−6.0 to +6.0mA
Output		
	Applied voltage	−0.5 to +5.5V [2]
	Forced current	−1.0 to +6.0mA [3,4]
	Short-circuit duration (single output in high state to ground)	1 sec
Temperature		
	Operating, case	−55 to +125°C
	junction	175°C
	Lead, soldering (10 seconds)	300°C
	Storage	−65 to 150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width	25			30			ns
t_S	Input Register Setup Time	25			30			ns
t_H	Input Register Hold Time	0			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			-400			-400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				-55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX, Static [1]		700		750	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		X_{IN}, Y_{IN}, RND, FT		-0.4		-0.4	mA
		TCX, TCY, RS		-0.8		-0.8	mA
		CLK L, M, X, and Y; TRIM, TRIL		-1.0		-1.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		X_{IN}, Y_{IN}, RND, FT		75		100	μA
		TCX, TCY, RS		75		100	μA
		CLK L, M, X, and Y; TRIM, TRIL		75		100	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V		-40		-40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX, one pin to ground, one second duration max, output HIGH		-50		-50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. All inputs and outputs LOW.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MC}	Multiply Time, Clocked	V_{CC} = Min		115		140	ns
t_{MUC}	Multiply Time, Unclocked	V_{CC} = Min		155		185	ns
t_D	Output Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		40		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = Min, Test Load: V_{LOAD} = 1.8V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.6V (t_{DIS0}) [2] V_{LOAD} = 0.0V (t_{DIS1}) [2]		40		45	ns

Notes:
1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 12.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
MPY012HJ1C	STD – T_A = 0°C to 70°C	Commercial	64 Pin Ceramic DIP	012HJ1C
MPY012HJ1A	EXT – T_C = –55°C to 125°C	High Reliability	64 Pin Ceramic DIP	012HJ1A

MPY016K

VLSI Multiplier
16 x 16 Bit, 40ns

The TRW MPY016K is a video-speed 16 x 16 bit parallel multiplier which operates at a 40ns cycle time (25MHz multiplication rate). The multiplicand and the multiplier may be independently specified as two's complement or unsigned magnitude, yielding a full precision 32-bit product.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The Most Significant Product (MSP) and Least Significant Product (LSP) can be multiplexed through a dedicated output port, or the LSP can share a bidirectional port with the Y input. All outputs are three-state.

Built with TRW's OMICRON-B™ 1-micron bipolar process, the MPY016K is pin compatible with the industry standard MPY016H and operates with three times the speed at comparable power dissipation. The MPY016K is the industry's first true video-speed 16-bit multiplier.

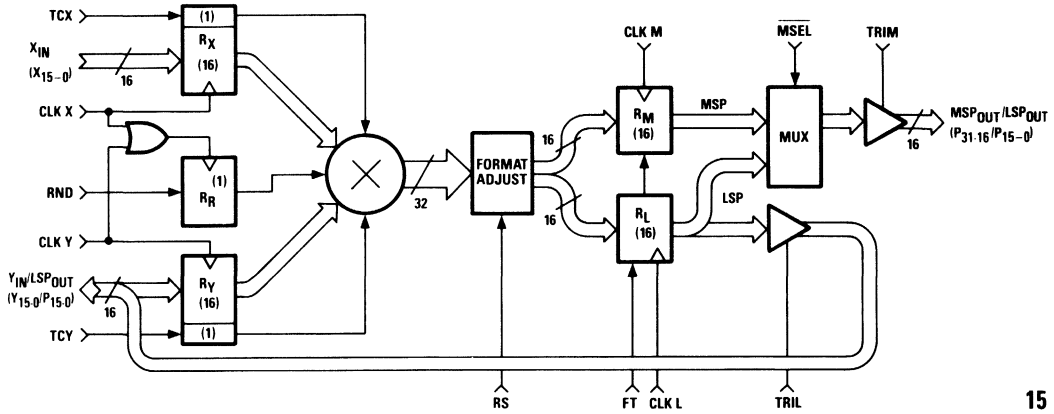
Features

- 40ns Multiply Time: MPY016K-1 (Worst Case)
- 45ns Multiply Time: MPY016K (Worst Case)
- Pin Compatible With TRW MPY016H
- 16 x 16 Bit Parallel Multiplication With 32-Bit Output
- Two Least Significant Product Output Modes: Multiplexed With Most Significant Product Or Multiplexed With Y Input
- Output Registers Can Be Made Transparent
- Three-State TTL Output
- Two's Complement, Unsigned Magnitude, Or Mixed Mode Multiplication
- Fully TTL Compatible
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In A 64 Pin Ceramic DIP

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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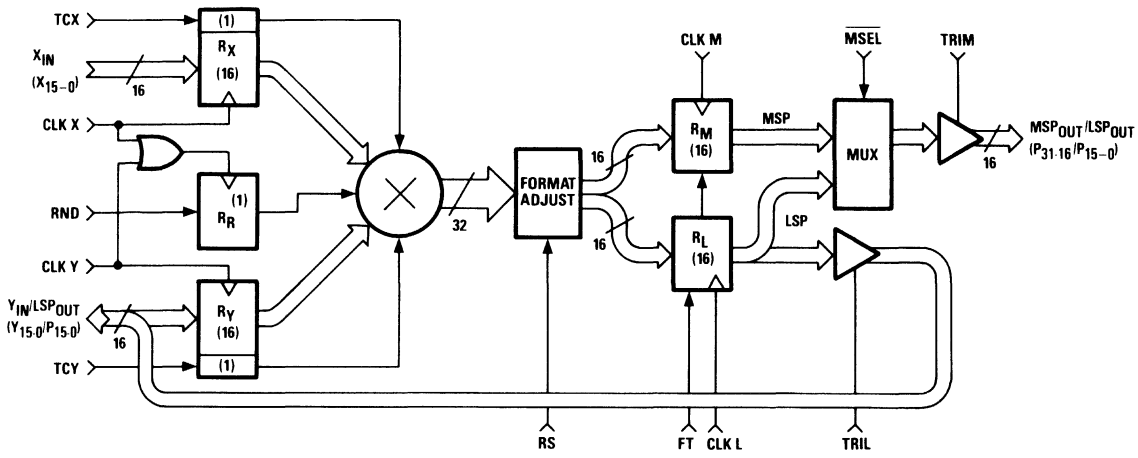
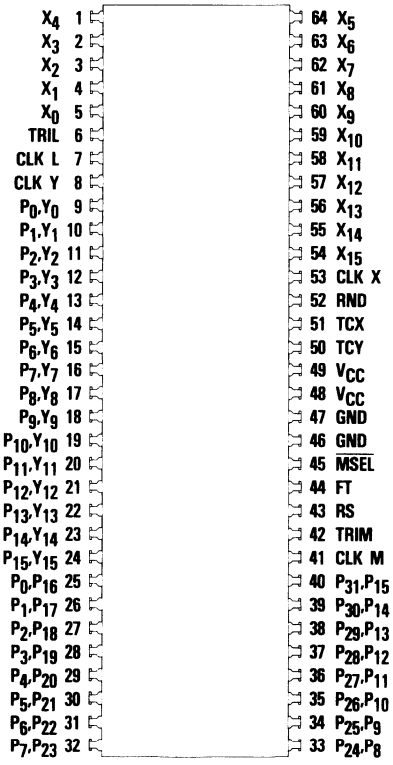
Functional Block Diagram



Pin Assignments



64 Lead DIP - J1 Package

Functional Description

General Information

The MPY016K has three functional sections: Input registers, an asynchronous multiplier array, and output registers. The input registers store the two 16-bit numbers which are to be multiplied and the instruction which controls the output rounding. The rounding control is used when a single-word output is desired. Each input operand is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders, designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 16-bit words, the Most Significant Product (MSP) and the Least Significant Product (LSP). Three-state output drivers allow the MPY016K to be used on a bus, or allow the least and most significant outputs to be multiplexed over the same 16-bit output lines. The Least Significant Product (LSP) is multiplexed with the Y input.

Power

The MPY016K operates from a single +5.0V supply. All power and ground lines must be connected. Note that the device is pin-compatible with the MPY016H, which has an additional ground pin; this is a control lead in the MPY016K. A ground on this pin (which must exist in all MPY016H applications) will cause the MPY016K to function like an MPY016H.

Name	Function	Value	J1 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 48, 49
GND	Ground	0.0V	Pins 46, 47

Data Inputs

The MPY016K has two 16-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{15} and Y_{15}, carry the sign information for the two's complement notation. The remaining bits are denoted X_0 through X_{14} and Y_0 through Y_{14} (with X_0 and Y_0 the Least Significant Bits). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6, respectively. The Y inputs are multiplexed with the LSP outputs, and hence can only be used when the TRIL control is in a HIGH state. This is true whether or not the LSP is also multiplexed out through the MSP output port.

Name	Function	Value	J1 Package
X_{15}	X Data MSB	TTL	Pin 54
X_{14}		TTL	Pin 55
X_{13}		TTL	Pin 56
X_{12}		TTL	Pin 57
X_{11}		TTL	Pin 58
X_{10}		TTL	Pin 59
X_9		TTL	Pin 60
X_8		TTL	Pin 61
X_7		TTL	Pin 62
X_6		TTL	Pin 63
X_5		TTL	Pin 64
X_4		TTL	Pin 1
X_3		TTL	Pin 2
X_2		TTL	Pin 3
X_1		TTL	Pin 4
X_0	X Data LSB	TTL	Pin 5

Data Inputs (Cont.)

Name	Function	Value	J1 Package
Y_{15}	Y Data MSB	TTL	Pin 24
Y_{14}		TTL	Pin 23
Y_{13}		TTL	Pin 22
Y_{12}		TTL	Pin 21
Y_{11}		TTL	Pin 20
Y_{10}		TTL	Pin 19
Y_9		TTL	Pin 18
Y_8		TTL	Pin 17
Y_7		TTL	Pin 16
Y_6		TTL	Pin 15
Y_5		TTL	Pin 14
Y_4		TTL	Pin 13
Y_3		TTL	Pin 12
Y_2		TTL	Pin 11
Y_1		TTL	Pin 10
Y_0	Y Data LSB	TTL	Pin 9

Data Outputs

The MPY016K has a 32-bit two's complement or unsigned magnitude output which is the product of the two input data values. This output is divided into two 16-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP). The Most Significant Bit (MSB) of both the MSP and the LSP is the sign bit if fractional two's complement notation is used (TCX = TCY = 1, RS = 0). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6, respectively.

If $\overline{\text{MSEL}}$ is LOW, the LSP output can be taken from the Y input pins only when TRIL is LOW. Care must be taken to enable these shared input lines only at the proper time. If $\overline{\text{MSEL}}$ is HIGH, the LSP output is made available at the MSP lines, as well as at the Y input pins. For an output from the MSP lines to be read, the TRIM control must be active.

RS is an output format control. A HIGH on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, or integer two's complement operation.

Name	Function	Value	J1 Package
P_{31}	Product MSB	TTL	Pin 40
P_{30}		TTL	Pin 39
P_{29}		TTL	Pin 38
P_{28}		TTL	Pin 37
P_{27}		TTL	Pin 36
P_{26}		TTL	Pin 35
P_{25}		TTL	Pin 34
P_{24}		TTL	Pin 33
P_{23}		TTL	Pin 32
P_{22}		TTL	Pin 31
P_{21}		TTL	Pin 30
P_{20}		TTL	Pin 29
P_{19}		TTL	Pin 28
P_{18}		TTL	Pin 27
P_{17}		TTL	Pin 26
P_{16}		TTL	Pin 25

Data Outputs (Cont.)

Name	Function	Value	J1 Package
			MUXED
			Input/Ouput
P_{15}		TTL	Pin 24/Pin 40
P_{14}		TTL	Pin 23/Pin 39
P_{13}		TTL	Pin 22/Pin 38
P_{12}		TTL	Pin 21/Pin 37
P_{11}		TTL	Pin 20/Pin 36
P_{10}		TTL	Pin 19/Pin 35
P_9		TTL	Pin 18/Pin 34
P_8		TTL	Pin 17/Pin 33
P_7		TTL	Pin 16/Pin 32
P_6		TTL	Pin 15/Pin 31
P_5		TTL	Pin 14/Pin 30
P_4		TTL	Pin 13/Pin 29
P_3		TTL	Pin 12/Pin 28
P_2		TTL	Pin 11/Pin 27
P_1		TTL	Pin 10/Pin 26
P_0	Product LSB	TTL	Pin 9/Pin 25

Clocks

The MPY016K has four clock lines, one for each input register and one for each product register. Data and two's complement instructions present at the inputs of these registers are loaded into the registers at the rising edge of the appropriate clock. The RND input is registered, clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading this control signal can be avoided by the use of normally LOW clocks.

Name	Function	Value	J1 Package
CLK X	Clock Input Data X	TTL	Pin 53
CLK Y	Clock Input Data Y	TTL	Pin 8
CLK L	Clock LSP Register	TTL	Pin 7
CLK M	Clock MSP Register	TTL	Pin 41

Controls

The MPY016K has eight control lines.

FT — A control line which makes the output register transparent if it is HIGH.

TRIM, TRIL — Three-state enable lines for the MSP and the LSP. The output driver is in the high-impedance state when TRIM or TRIL is HIGH, and enabled when the appropriate control is LOW.

RS — RS is an output format control. A HIGH level on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, and two's complement integer operations.

$\overline{\text{MSEL}}$ — $\overline{\text{MSEL}}$ is an output multiplex control. When $\overline{\text{MSEL}}$ is LOW, the MSP is available to the output three-state drivers at the MSP port, and the LSP is available to the output three-state drivers at the LSP/Y input port. When $\overline{\text{MSEL}}$ is HIGH, the LSP is available to both three-state drivers and the MSP is not available.

RND — When RND is HIGH, a one is added to the MSB of the LSP. Note that this bit depends on the state of the RS control. If RS is LOW when RND is HIGH, a one will be added to the 2^{-16} bit (P_{14}). If RS is HIGH when RND is HIGH, a one will be added to the 2^{-15} bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction; in some systems this may introduce a systematic bias.

TCX, TCY — Control how the device interprets data on the X and Y inputs. A HIGH on TCX or TCY makes the appropriate input a two's complement input, while a LOW makes the appropriate input a magnitude only input.

FT, RS, $\overline{\text{MSEL}}$, TRIM, and TRIL are not registered. The TCX input is registered, and clocked in at the rising edge of the X clock signal, CLK X. The TCY input is also registered, and clocked in at the rising edge of the Y clock signal, CLK Y. The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention is required if normally HIGH clock signals are used. Problems with loading of these control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J1 Package
RND	Round Control Bit	TTL	Pin 52
TCX	X Input Two's Complement	TTL	Pin 51
TCY	Y Input Two's Complement	TTL	Pin 50
FT	Output Register Feedthrough	TTL	Pin 44
RS	Output Register Shift	TTL	Pin 43
MSEL	Output Select	TTL	Pin 45
TRIM	MSP Three-State Control	TTL	Pin 42
TRIL	LSP Three-State Control	TTL	Pin 6

Figure 1. Fractional Two's Complement Notation

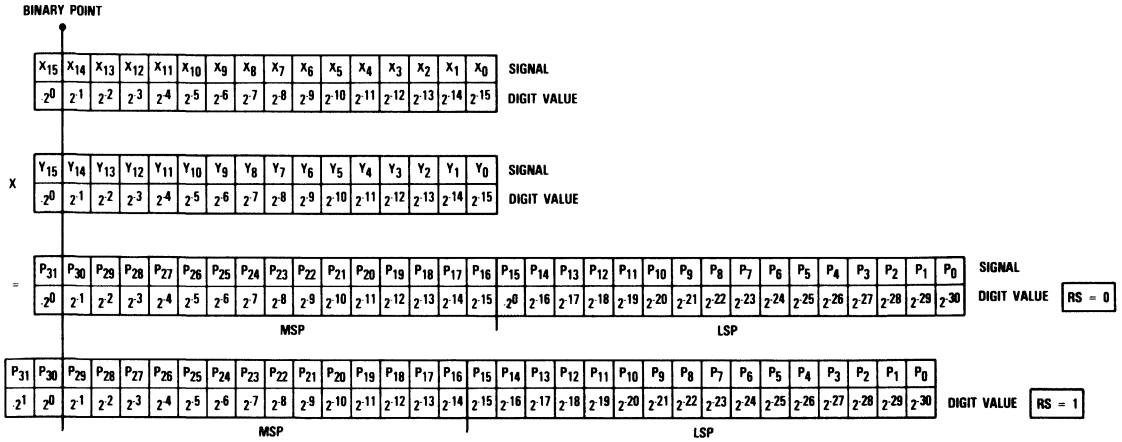


Figure 2. Fractional Unsigned Magnitude Notation

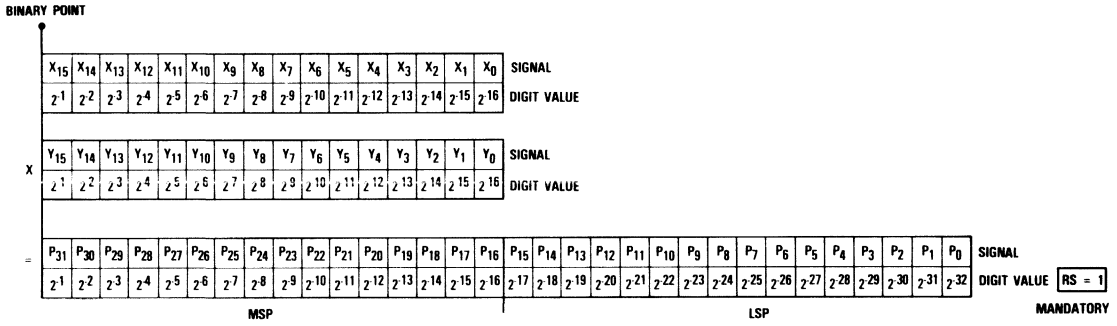


Figure 3. Fractional Mixed Mode Notation

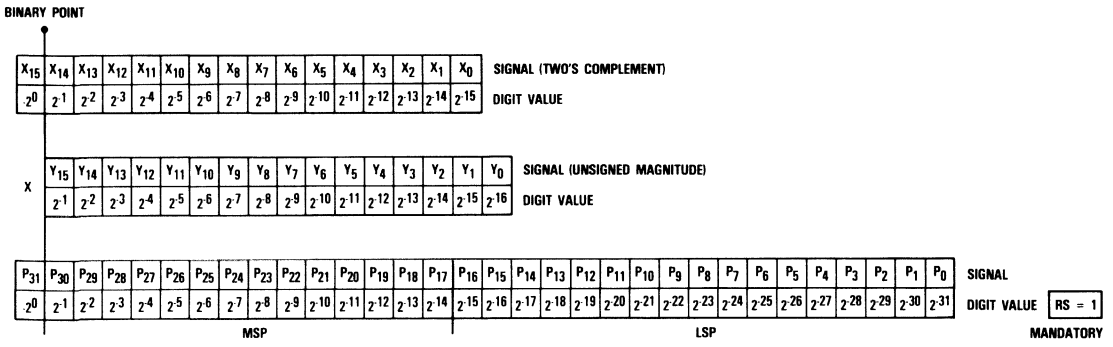


Figure 4. Integer Two's Complement Notation

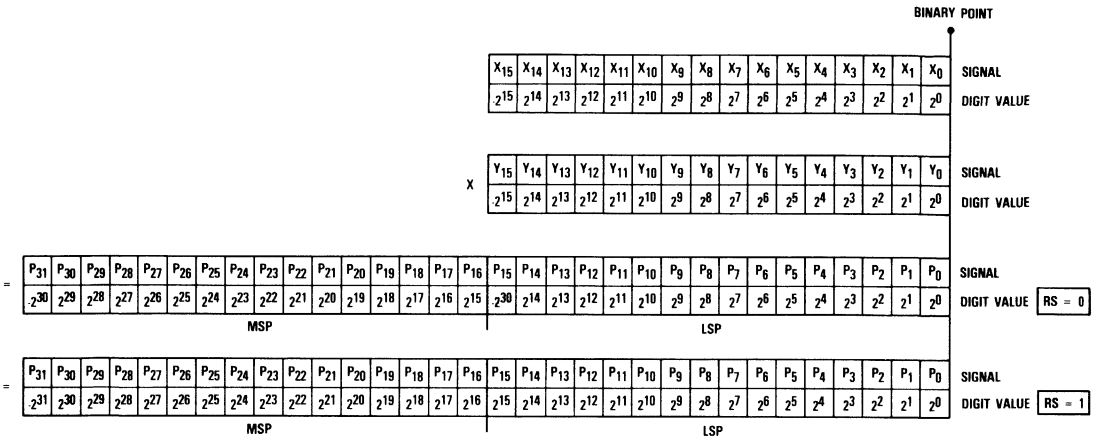


Figure 5. Integer Unsigned Magnitude Notation

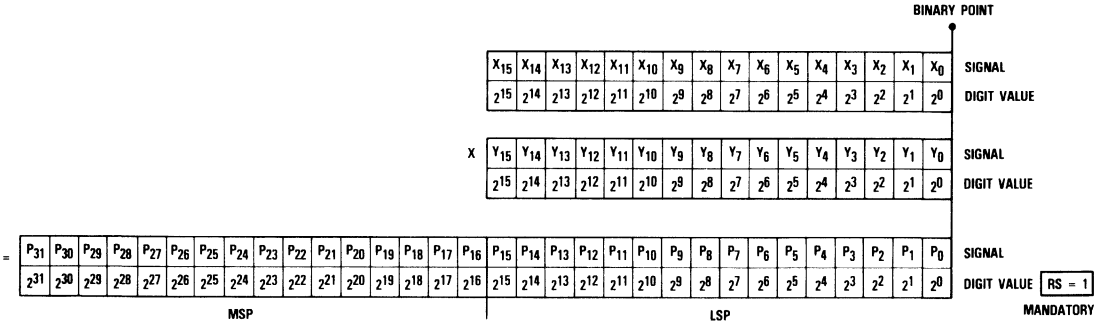


Figure 6. Integer Mixed Mode Notation

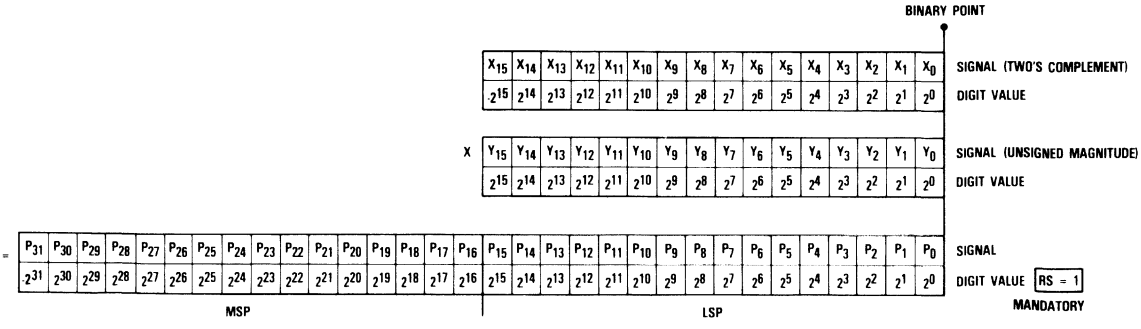


Figure 7. Timing Diagram, Non-Multiplexed Output

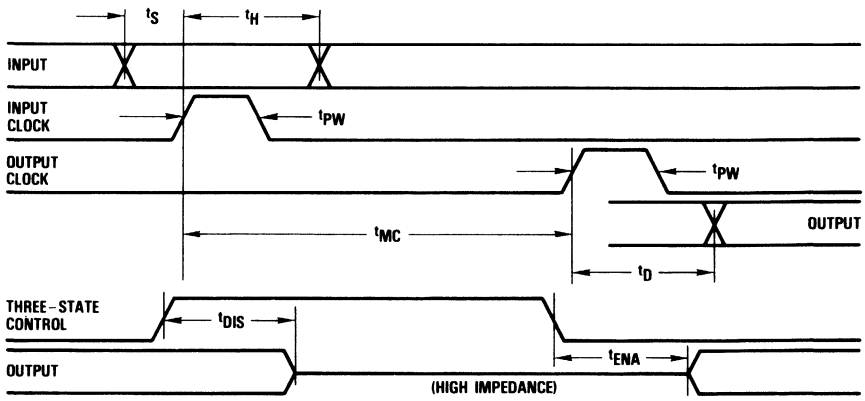


Figure 8. Timing Diagram, Unclocked Mode, Non-Multiplexed Output

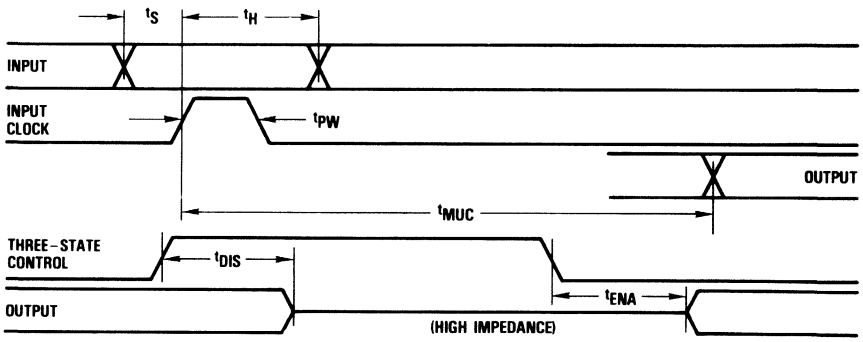


Figure 9. Timing Diagram, Multiplexed Output

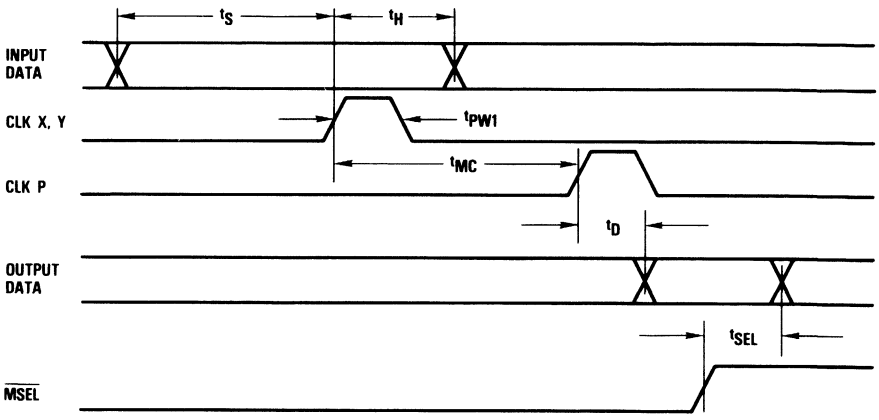
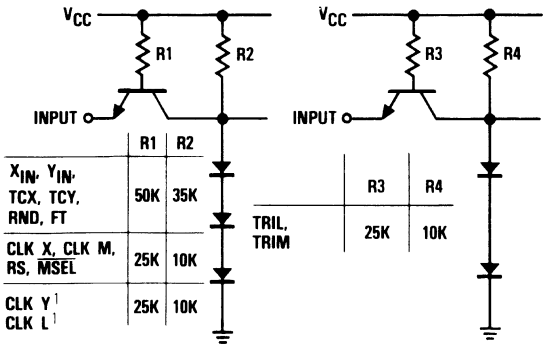


Figure 10. Equivalent Input Circuit



	R1	R2
X_{IN}, Y_{IN}, TCX, TCY, RND, FT	50K	35K
CLK X, CLK M, RS, $\overline{MSEL}$	25K	10K
CLK Y[1] CLK L[1]	25K	10K

	R3	R4
TRIL, TRIM	25K	10K

Note: 1. CLK Y and CLK L each drive two equivalent inputs.

Figure 11. Equivalent Output Circuit

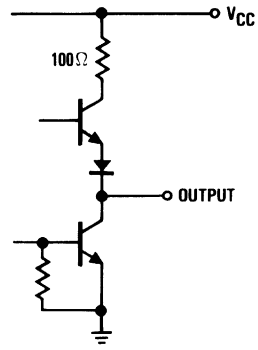


Figure 12. Test Load

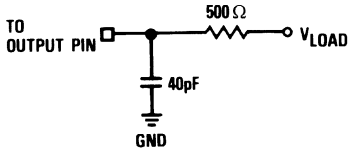
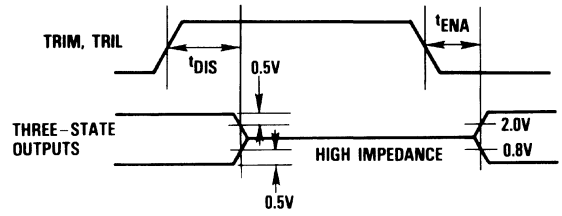


Figure 13. Transition Levels For Three-State Measurements



Application Notes

Mixed Mode Multiplication

There are several applications in which mixed mode multiplication may be advantageous. For example, inputs to a digital signal processor are often generated as unsigned magnitude numbers (e.g., data from an analog-to-digital converter). These numbers are effectively all positive values. In contrast, filter coefficients must often be negative. As a result, either the data must be converted to two's complement notation (which requires an additional bit), or the multiplier must be capable of mixed mode operation. The MPY016K provides this capability by independently specifying the mode of the multiplicand (X) and the multiplier (Y) on the TCX and TCY pins. No additional circuitry is required and the resulting product is in two's complement notation.

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the desired register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the MPY016K does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 6.

Register Shift (RS) Control

In two's complement notation, the acceptable range of values for a given word size is not the same for positive and negative numbers. The largest negative number is one LSB larger than the largest positive number. This is true for either fractional or integer notation. A problem can arise when the largest representable negative number is multiplied by itself. This should give a positive number of the same magnitude. However, the largest representable positive number is one LSB less than this value. As a result, this product cannot be correctly represented without using one additional output bit. The MPY016K has a Register Shift (RS) control that permits shifting of the result to provide a correct answer for every two's complement multiplication. When RS is active, the value of all bits in the MSP is doubled (i.e. shifted left one position), which provides the capability to represent the largest possible product. The MSB of the Least Significant Product is changed from a duplicate of the sign bit to the necessary bit to fill in the output word. The effects of this control are illustrated in Figures 1 and 4. Note that for unsigned magnitude operation, the RS control must be HIGH.

Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−0.1 to +6.0mA [3,4]
Short-circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−60 to +140°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	15			22			ns
t_{PWH}	Clock Pulse Width, HIGH	15			22			ns
t_S	Input Setup Time (MPY016K)	20			25			ns
	(MPY016K-1)	20			20			ns
t_H	Input Hold Time	0			2			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX, Static [1]					
		T_A = 0°C to 70°C		875			mA
		T_A > 25°C [2]		860			mA
		T_C = −55°C to +125°C				1050	mA
		T_C > 35°C				960	mA
		V_{CC} = 5.0V					
		T_A > 25°C		840			mA
		T_C > 35°C				920	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		$\overline{X_{IN}}$, $\overline{Y_{IN}}$, TCY, TCX, FT, RND		−0.2		−0.2	mA
		CLK Y, CLK L		−1.2		−1.2	mA
		CLK X, CLK M, $\overline{MSEL}$, TRIM, TRIL, RS		−0.6		−0.6	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		$\overline{X_{IN}}$, $\overline{Y_{IN}}$, TCY, TCX, FT, RND		50		50	μA
		CLK Y, CLK L		100		100	μA
		CLK X, CLK M, $\overline{MSEL}$, TRIM, TRIL, RS		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MAX, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V					
		Non-Shared Pins		−40		−50	μA
		Shared Pins		−200		−200	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V					
		Non-Shared Pins		40		50	μA
		Shared Pins		50		50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, One pin to ground, one second duration, output HIGH.	−4	−50	−4	−50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		10		10	pF

Notes:

1. Worst case, all inputs and outputs LOW.
2. Part has a negative temperature coefficient, i.e., power consumption falls as temperature increases.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MC}	Multiply Time, Clocked	V_{CC} = Min,					
		MPY016K		45		50	ns
		MPY016K-1		40		45	ns
t_{MUC}	Multiply Time, Unclocked	V_{CC} = Min					
		MPY016K		75		85	ns
		MPY016K-1		70		75	ns
t_D	Output Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V					
		MPY016K		30		35	ns
		MPY016K-1		30		30	ns
t_{SEL}	Output Multiplex Select Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		20		25	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = Min, Test Load: V_{LOAD} = 1.8V		30		35	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.6V (t_{DIS0}) [2] V_{LOAD} = 0.0V (t_{DIS1}) [2]		30		35	ns

Notes:
1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 13.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
MPY016KJ1C	STD – T_A = 0°C to 70°C	Commercial	64 Pin Ceramic DIP	016KJ1C
MPY016KJ1C1	STD – T_A = 0°C to 70°C	Commercial	64 Pin Ceramic DIP	016KJ1C1
MPY016KJ1A	EXT – T_C = –55°C to 125°C	High Reliability	64 Pin Ceramic DIP	016KJ1A
MPY016KJ1A1	EXT – T_C = –55°C to 125°C	High Reliability	64 Pin Ceramic DIP	016KJ1A1

MPY112K

Multiplier
12 x 12 Bit, 50ns

The MPY112K is a video-speed 12 x 12 bit parallel multiplier which operates at a 50ns cycle time (20MHz multiplication rate). The multiplicand and the multiplier may be specified together as two's complement or unsigned magnitude, yielding a 16-bit result. Mixed mode operation is not available on this device.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The most significant 16 bits of the product are available at the output register. The output is a single three-state port.

Built with TRW's OMICRON-B™ 1-micron bipolar process, the MPY112K is similar to the industry standard MPY012H but operates with more than twice the speed at about three-quarters of the power dissipation. The MPY112K is the industry's first true video-speed 12-bit multiplier.

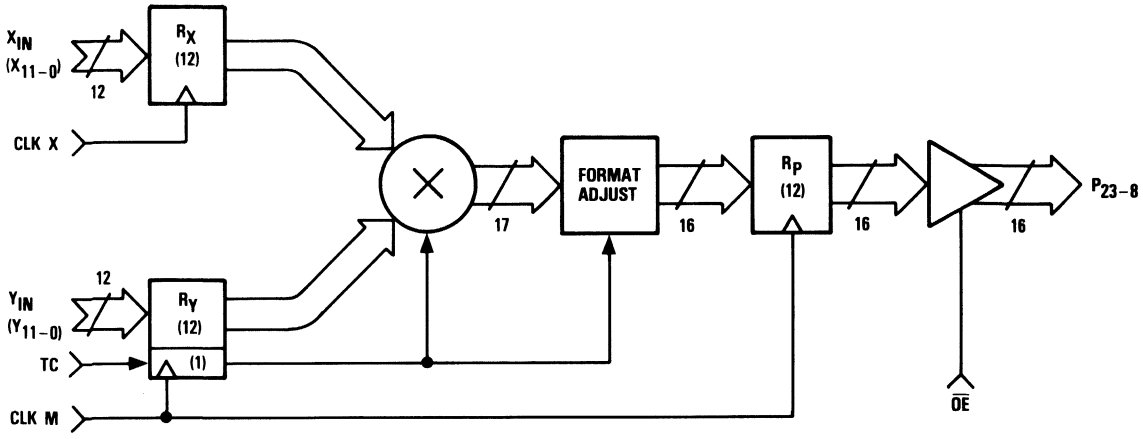
Features

- 50ns Multiply Time (Worst Case)
- 12 x 12 Bit Parallel Multiplication With 16-Bit Product Output
- Fully TTL Compatible
- Three-State Outputs
- Two's Complement Or Unsigned Magnitude Multiplication
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In A 48 Pin Ceramic DIP

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



TRW LSI Products Inc.
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La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

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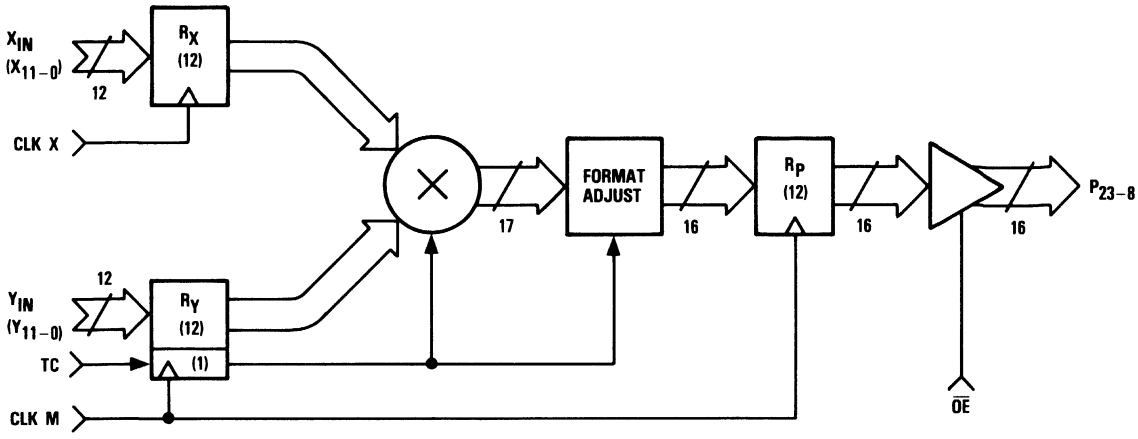
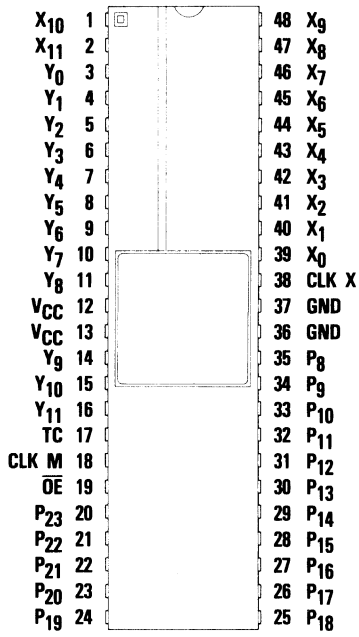
Printed in the U.S.A.

Functional Block Diagram



Pin Assignments



48 Lead DIP – J4 Package

Functional Description

General Information

The MPY112K has three functional sections: input registers, an asynchronous multiplier array, and output registers. The input registers store the two 12-bit numbers which are to be multiplied and the instruction which controls whether the inputs are to be considered as two's complement or unsigned magnitude numbers. Each input operand is stored independently, simplifying multiplication by a constant; however, since the product and the Y input share a common clock, any constant should be stored in the X register. The asynchronous multiplier array is a network of AND gates and adders which have been designed to handle two's complement or unsigned magnitude numbers. The output register holds the most significant 16 bits of the product. Three-state output drivers allow the MPY112K to be used on a bus.

Power

The MPY112K operates from a single +5 Volt supply. Note that the maximum voltage for proper operation over the extended temperature range is 5.25 Volts. All power and ground lines must be connected.

Name	Function	Value	J4 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pins 12, 13
GND	Ground	0.0V	Pins 36, 37

Data Inputs

The MPY112K has two 12-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{11} and Y_{11}, carry the sign information for the two's complement notation. The rest of the bits are denoted X_0 through X_{10} and Y_0 through Y_{10} (with X_0 and Y_0 the Least Significant Bits). The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J4 Package
X_{11}	X Data MSB	TTL	Pin 2
X_{10}		TTL	Pin 1
X_9		TTL	Pin 48
X_8		TTL	Pin 47
X_7		TTL	Pin 46
X_6		TTL	Pin 45
X_5		TTL	Pin 44
X_4		TTL	Pin 43
X_3		TTL	Pin 42
X_2		TTL	Pin 41
X_1		TTL	Pin 40
X_0	X Data LSB	TTL	Pin 39

Data Inputs (Cont.)

Name	Function	Value	J4 Package
Y_{11}	Y Data MSB	TTL	Pin 16
Y_{10}		TTL	Pin 15
Y_9		TTL	Pin 14
Y_8		TTL	Pin 11
Y_7		TTL	Pin 10
Y_6		TTL	Pin 9
Y_5		TTL	Pin 8
Y_4		TTL	Pin 7
Y_3		TTL	Pin 6
Y_2		TTL	Pin 5
Y_1		TTL	Pin 4
Y_0	Y Data LSB	TTL	Pin 3

Data Outputs

The MPY112K has a 16-bit two's complement or unsigned magnitude output which is the product of the two input data values. This output is the most significant 16 bits of the complete product. The output is truncated to this length, not rounded. The Most Significant Bit (MSB) of the product is the sign bit if two's complement notation is used (TC=1). The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively. The output driver is in the high-impedance state when $\overline{OE}$ is HIGH, and enabled when $\overline{OE}$ is LOW.

Name	Function	Value	J4 Package
P_{23}	Product MSB	TTL	Pin 20
P_{22}		TTL	Pin 21
P_{21}		TTL	Pin 22
P_{20}		TTL	Pin 23
P_{19}		TTL	Pin 24
P_{18}		TTL	Pin 25
P_{17}		TTL	Pin 26
P_{16}		TTL	Pin 27
P_{15}		TTL	Pin 28
P_{14}		TTL	Pin 29
P_{13}		TTL	Pin 30
P_{12}		TTL	Pin 31
P_{11}		TTL	Pin 32
P_{10}		TTL	Pin 33
P_9		TTL	Pin 34
P_8		TTL	Pin 35

Clocks

The MPY112K has two clock lines, one for the X input register and one for both the Y input register and the product register. Data present at the X input are loaded into the registers at the rising edge of CLK X. Data present at the Y input, the two's complement instruction, and the product present at the output of the asynchronous multiplier array are loaded into the appropriate registers at the rising edge of CLK M.

Name	Function	Value	J4 Package
CLK X	Clock Input Data X	TTL	Pin 38
CLK M	Master Clock	TTL	Pin 18

Controls

The MPY112K has two control lines. $\overline{OE}$ is a three-state enable line for the output. The output drivers are in the high-impedance state when $\overline{OE}$ is HIGH, and enabled when $\overline{OE}$ is LOW. The device will interpret data as two's complement when TC is HIGH, and as unsigned magnitude when TC is LOW. $\overline{OE}$ is not registered. TC is registered and clocked in at the rising edge of CLK M.

Name	Function	Value	J4 Package
TC	Two's Complement	TTL	Pin 17
$\overline{OE}$	Three-State Control	TTL	Pin 19

Figure 1. Fractional Two's Complement Notation

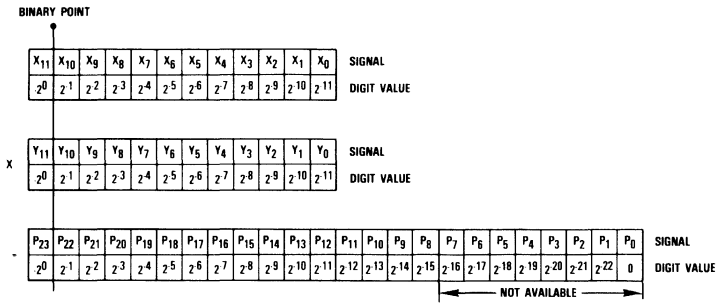


Figure 2. Fractional Unsigned Magnitude Notation

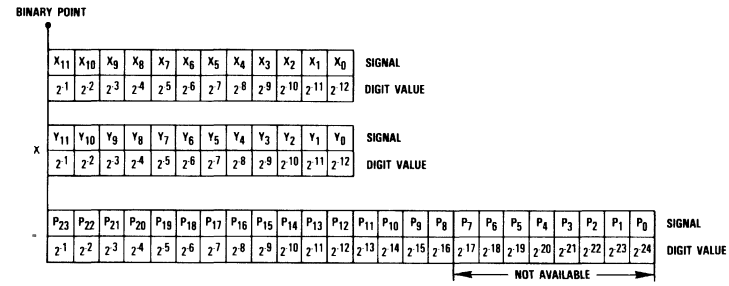


Figure 3. Integer Two's Complement Notation

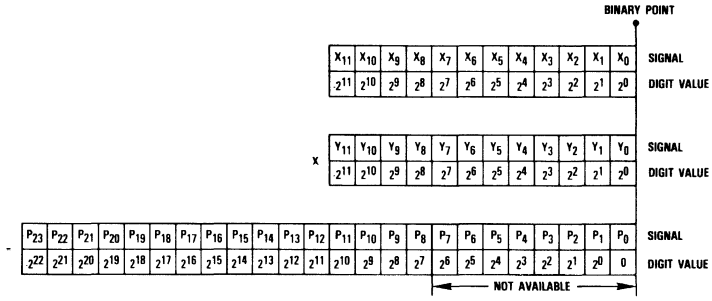


Figure 4. Integer Unsigned Magnitude Notation

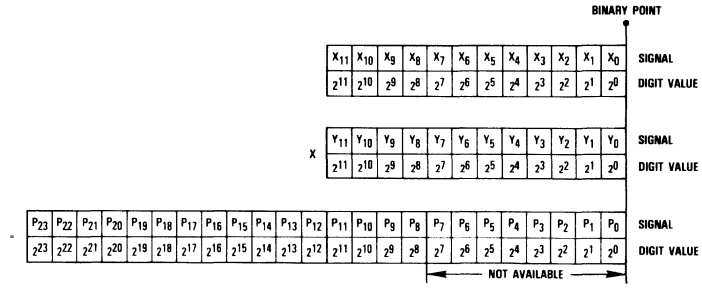


Figure 5. Timing Diagram

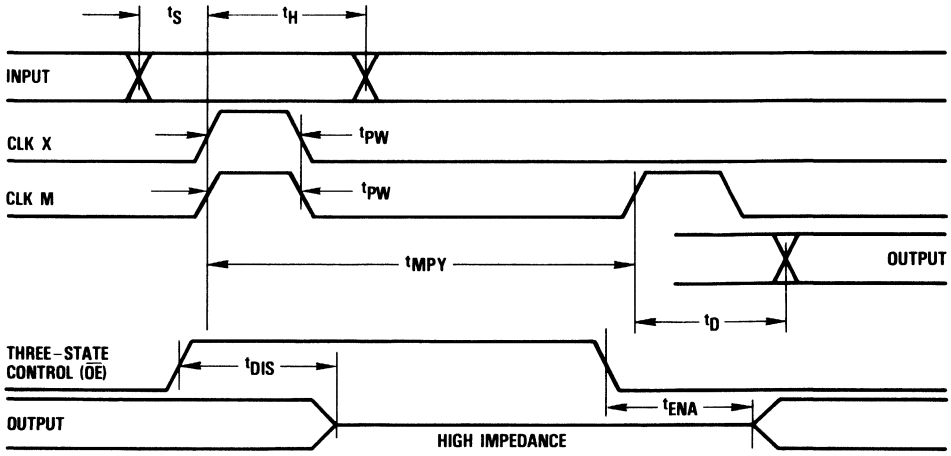


Figure 6. Equivalent Input Circuit

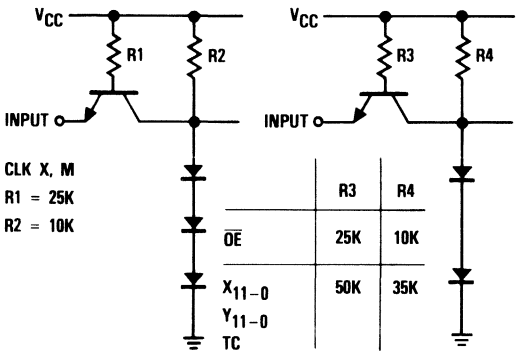


Figure 7. Equivalent Output Circuit

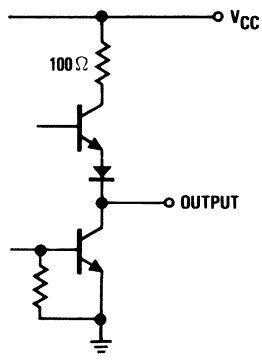


Figure 8. Test Load

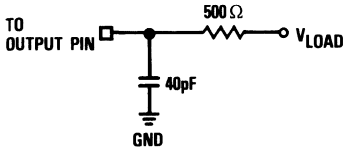
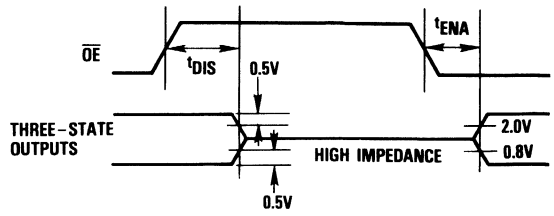


Figure 9. Transition Levels For Three-State Measurements



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−1.0 to +6.0mA [3,4]
Short-circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−55 to +125°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to 150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.25	V
t_{PWL}	Clock Pulse Width, LOW	20			25			ns
t_{PWH}	Clock Pulse Width, HIGH	20			25			ns
t_S	Input Setup Time	25			30			ns
t_H	Input Hold Time	5			10			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			2.5	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = MAX, Static		450		550	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.4V					
		Data Inputs, TC		−0.2		−0.3	mA
		CLK X, $\overline{OE}$		−0.6		−0.75	mA
		CLK M		−1.2		−1.5	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V					
		Data Inputs, TC		50		50	μA
		CLK X, $\overline{OE}$		50		50	μA
		CLK M		100		100	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MAX, I_{OL} = MAX		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{CC} = MAX, V_I = 0.4V	−40	40	−40	40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{CC} = MAX, V_I = 2.4V	−40	40	−40	40	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = MAX, Output HIGH, one pin to ground, one second duration max		−50		−50	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MPY}	Multiply Time	V_{CC} = MIN		50		55	ns
t_D	Output Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.2V		35		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 1.8V		30		45	ns
t_{DIS}	Three-State Output Enable Delay	V_{CC} = MIN, Test Load: V_{LOAD} = 2.6V t_{DIS0}, 0.0V for t_{DIS1} [2]		30		45	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 9.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Application Notes

Mixed-Mode Multiplication

There are several applications in which it may be advantageous to perform mixed-mode multiplication. Video data are often generated as unsigned magnitude numbers (e.g., data from an analog-to-digital converter). These numbers are effectively all positive values. In contrast, filter coefficients must often be negative. As a result, either the video data must be converted to two's complement notation (which requires an additional bit), or the multiplier must be capable of mixed-mode operation. The MPY112K can only provide this capability by making the MSB of the unsigned magnitude number a zero, thus reducing its precision to eleven bits. No additional circuitry is required.

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and that the register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register. Due to the sharing of the CLK M pin by the Y input register and the output register, all constants should be kept in the X register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the MPY112K does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 4.

Exceptional Case

The most negative number which can be represented in two's complement notation is greater in magnitude than the largest representable positive number by one LSB. This is only a problem when the full-scale negative number is squared. If fractional notation is used, this means that $(-1) \times (-1)$ with the MPY112K will yield the (incorrect) result (-1). In the full-precision series of multipliers the correct result can be obtained by the use of the RS control, which was not included on the MPY112K due to pin count limitations.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
MPY112KJ4C	STD–T_A = 0°C to 70°C	Commercial	48 Pin Ceramic DIP	112KJ4C
MPY112KJ4A	EXT–T_C = –55°C to 125°C	High Reliability	48 Pin Ceramic DIP	112KJ4A

TMC2009

CMOS Multiplier-Accumulator

12 x 12 Bit, 135ns

The TMC2009 is a high-speed 12 x 12 bit parallel multiplier-accumulator which operates at a 135ns cycle time (7.4MHz multiply-accumulate rate). The input data may be specified as two's complement or unsigned magnitude, yielding a full-precision 24-bit product. Products may be accumulated to a 27-bit result.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit eXTended Product (XTP), a 12-bit Most Significant Product (MSP), and a 12-bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP, the MSP, and the LSP. The output register can be preloaded directly via the output ports.

Built with TRW's 2-micron CMOS process, the TMC2009 is pin and function compatible with the industry standard TDC1009 and operates with the same speed at one-fifth or less power dissipation.

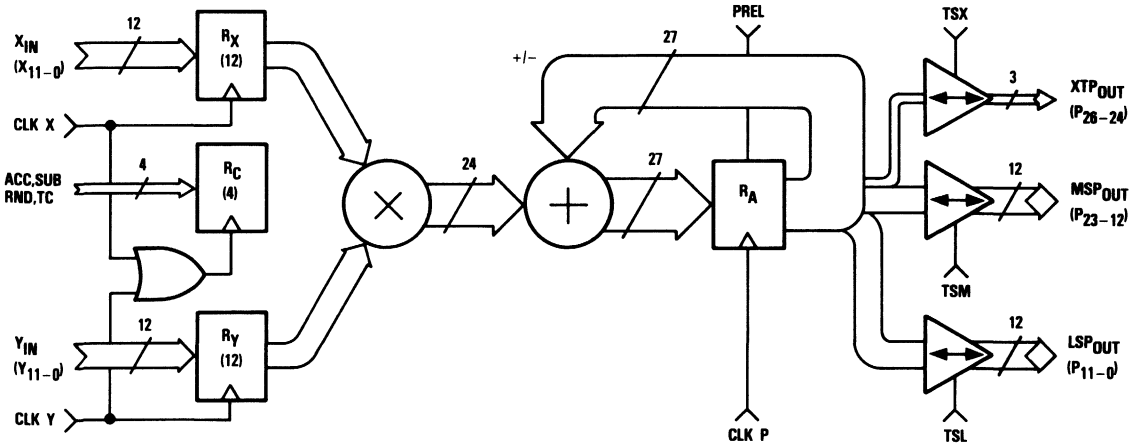
Features

- Low Power Consumption CMOS Process
- Pin And Function Compatible With TRW TDC1009
- 135ns Multiply-Accumulate Time (Worst Case)
- 12 x 12 Bit Parallel Multiplication With Accumulation To 27-Bit Result
- Selectable Accumulation, Subtraction, Rounding, And Preloading
- All Inputs And Outputs Are Registered TTL Compatible
- Three-State Output
- Two's Complement Or Unsigned Magnitude Operation
- Single +5V Power Supply
- Available In 64 Pin Hermetic Ceramic DIP

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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FAX: (619) 455-6314

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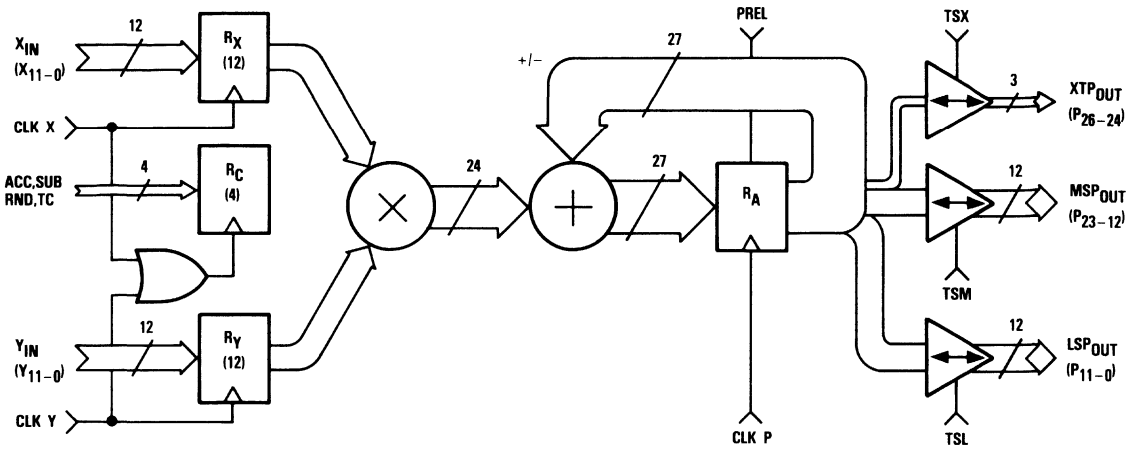
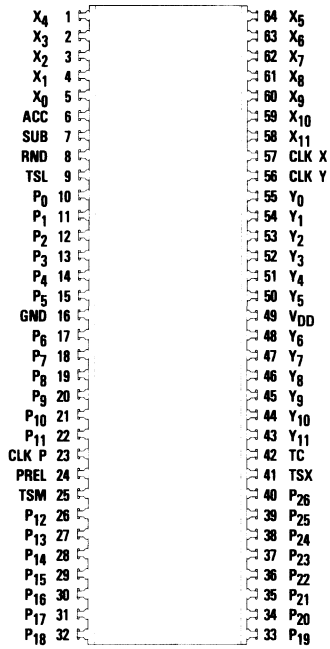
Functional Block Diagram



Pin Assignments



64 Lead DIP – J3 Package

Functional Description

General Information

The TMC2009 consists of four functional sections: Input registers, an asynchronous multiplier array, an adder, and output registers. The input registers store the two 12-bit operands which are to be multiplied, and the control lines which control the input numerical format (two's complement or unsigned magnitude), output rounding, accumulation, and subtraction. The round control is used when a single-word output is desired. Each number is independently stored, simplifying multiplication by a constant. The output registers can be preloaded with a constant to provide the sum of products plus a constant. The asynchronous multiplier array is a network of AND gates and adders, which has been designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 12-bit words and one 3-bit word: the Most Significant Product (MSP), the Least Significant Product (LSP), and the eXTended Product (XTP). Three-state output drivers permit the TMC2009 to be used on a bus, or allow the outputs to be multiplexed over the same 12-bit output lines.

Power

The TMC2009 operates from a single +5 Volt supply. All power and ground lines must be connected.

Name	Function	Value	J3 Package
V_{DD}	Positive Supply Voltage	+5.0V	Pin 49
GND	Ground	0.0V	Pin 16

Data Inputs

The TMC2009 has two 12-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), X_{11} and Y_{11}, carry the sign information for the two's complement notation. The remaining bits are denoted X_{10} through X_0 and Y_{10} through Y_0 (with X_0 and Y_0 the Least Significant Bits). Data present at the X and Y inputs are clocked into the input registers at the rising edge of the appropriate clock. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J3 Package
X_{11}	X Data MSB	TTL	Pin 58
X_{10}		TTL	Pin 59
X_9		TTL	Pin 60
X_8		TTL	Pin 61
X_7		TTL	Pin 62
X_6		TTL	Pin 63
X_5		TTL	Pin 64
X_4		TTL	Pin 1
X_3		TTL	Pin 2
X_2		TTL	Pin 3
X_1		TTL	Pin 4
X_0	X Data LSB	TTL	Pin 5

Data Inputs (Cont.)

Name	Function	Value	J3 Package
Y_{11}	Y Data MSB	TTL	Pin 43
Y_{10}		TTL	Pin 44
Y_9		TTL	Pin 45
Y_8		TTL	Pin 46
Y_7		TTL	Pin 47
Y_6		TTL	Pin 48
Y_5		TTL	Pin 50
Y_4		TTL	Pin 51
Y_3		TTL	Pin 52
Y_2		TTL	Pin 53
Y_1		TTL	Pin 54
Y_0	Y Data LSB	TTL	Pin 55

Data Outputs

The TMC2009 has a 27-bit two's complement or unsigned magnitude result that is the sum of the products of the two input data values and the previous products which have been accumulated. This output is divided into two 12-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP), and one 3-bit output word, the eXTended Product (XTP). The Most Significant Bit (MSB) of the XTP is the sign bit if two's complement notation is used. The input and output formats for fractional two's complement notation, fractional unsigned magnitude notation, integer two's complement notation, and integer unsigned magnitude notation are shown in Figures 1 through 4, respectively.

Name	Function	Value	J3 Package
P_{26}	Product MSB	TTL	Pin 40
P_{25}		TTL	Pin 39
P_{24}		TTL	Pin 38
P_{23}		TTL	Pin 37
P_{22}		TTL	Pin 36
P_{21}		TTL	Pin 35
P_{20}		TTL	Pin 34
P_{19}		TTL	Pin 33
P_{18}		TTL	Pin 32
P_{17}		TTL	Pin 31
P_{16}		TTL	Pin 30
P_{15}		TTL	Pin 29
P_{14}		TTL	Pin 28
P_{13}		TTL	Pin 27
P_{12}		TTL	Pin 26

Data Outputs (Cont.)

Name	Function	Value	J3 Package
P_{11}		TTL	Pin 22
P_{10}		TTL	Pin 21
P_9		TTL	Pin 20
P_8		TTL	Pin 19
P_7		TTL	Pin 18
P_6		TTL	Pin 17
P_5		TTL	Pin 15
P_4		TTL	Pin 14
P_3		TTL	Pin 13
P_2		TTL	Pin 12
P_1		TTL	Pin 11
P_0	Product LSB	TTL	Pin 10

Clocks

The TMC2009 has three clock lines, one for each of the input registers and one for the product register. Data present at the inputs of these registers are loaded into the registers at the rising edge of the appropriate clock. The RouND (RND), Two's Complement (TC), ACCumulate (ACC) and SUBtract (SUB) inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J3 Package
CLK X	Clock Input Data X	TTL	Pin 57
CLK Y	Clock Input Data Y	TTL	Pin 56
CLK P	Clock Product Register	TTL	Pin 23

Controls

The TMC2009 has eight control lines. TSX, TSM, and TSL are three-state enable lines for the XTP, the MSP, and the LSP, respectively. The output driver is in the high-impedance state when TSX, TSM, or TSL is HIGH, and enabled when the appropriate control is LOW.

PRELoad (PREL) is an active-HIGH control which has several effects when active (see Table 1). First, all output buffers are forced into the high-impedance state. Second, when any or all of TSX, TSM, and TSL are also HIGH, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX, TSM, TSL), and to the data being preloaded. These setup and hold times are with respect to the rising edge of CLK P.

RouND (RND) controls the addition of a 1 to the MSB of the LSP for rounding. When RND is high, a 1 is added to the MSB of the LSP for rounding the product in the MSP and XTP (if appropriate) rather than truncating them.

Two's Complement (TC) controls how the device interprets data on the X and Y inputs. TC HIGH makes both inputs two's complement inputs, while TC LOW makes both inputs unsigned magnitude only inputs.

When ACCumulate (ACC) is HIGH, the content of the output register is added to or subtracted from the next product generated, and the result is stored back into the output registers at the next rising edge of CLK P. When ACC is LOW, multiplication without accumulation is performed, and the next product generated is stored into the output registers directly. This operation is used for the first term in a summation to eliminate the need for a separate "clear" operation.

The SUBtract (SUB) control is used in conjunction with the ACC control. When both the ACC and SUB controls are HIGH, the content of the output register is subtracted from the next product generated and the difference is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

Controls (Cont.)

The RND, TC, ACC, and SUB inputs are registered, with all four bits clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J3 Package
TSX	XTP Three-State Control	TTL	Pin 41
TSM	MSP Three-State Control	TTL	Pin 25
TSL	LSP Three-State Control	TTL	Pin 9
PREL	Preload Control	TTL	Pin 2
RND	Round Control Bit	TTL	Pin 8
TC	Two's Complement Control	TTL	Pin 42
ACC	Accumulate Control	TTL	Pin 6
SUB	Subtract Control	TTL	Pin 7

Preload Truth Table 1

PREL[1]	TSX[1]	TSM[1]	TSL[1]	XTP	MSP	LSP
L	L	L	L	Register → Output pin	Register → Output pin	Register → Output pin
L	L	L	H	Register → Output pin	Register → Output pin	Hi-Z
L	L	H	L	Register → Output pin	Hi-Z	Register → Output pin
L	L	H	H	Register → Output pin	Hi-Z	Hi-Z
L	H	L	L	Hi-Z	Register → Output pin	Register → Output pin
L	H	L	H	Hi-Z	Register → Output pin	Hi-Z
L	H	H	L	Hi-Z	Hi-Z	Register → Output pin
L	H	H	H	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	L	Hi-Z	Hi-Z	Hi-Z
H[2]	L	L	H	Hi-Z	Hi-Z	Hi-Z Preload
H[2]	L	H	L	Hi-Z	Hi-Z Preload	Hi-Z
H[2]	L	H	H	Hi-Z	Hi-Z Preload	Hi-Z Preload
H[2]	H	L	L	Hi-Z Preload	Hi-Z	Hi-Z
H[2]	H	L	H	Hi-Z Preload	Hi-Z	Hi-Z Preload
H[2]	H	H	L	Hi-Z Preload	Hi-Z Preload	Hi-Z
H[2]	H	H	H	Hi-Z Preload	Hi-Z Preload	Hi-Z Preload

Notes:

1. PREL, TSX, TSM, and TSL are not registered.
2. PREL Hi inhibits any change of output register for those outputs in which the three-state control is LOW.

Figure 1. Fractional Two's Complement Notation

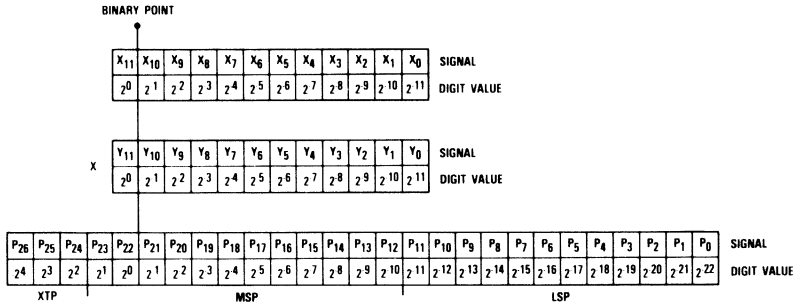


Figure 2. Fractional Unsigned Magnitude Notation

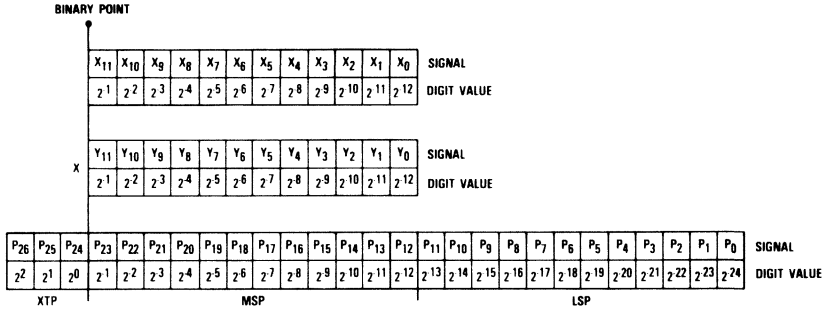


Figure 3. Integer Two's Complement Notation

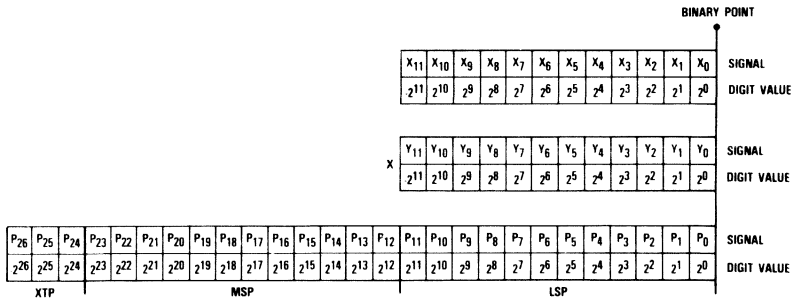
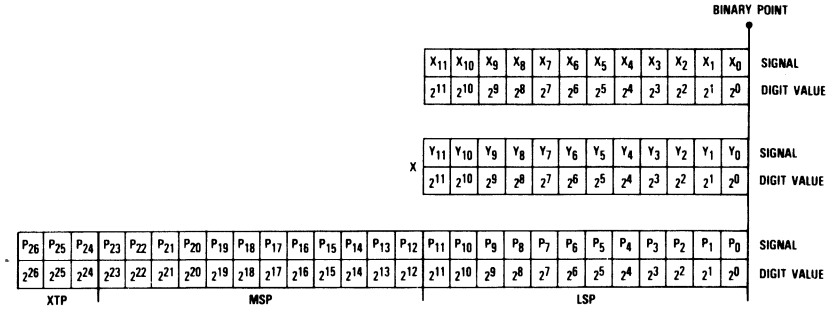


Figure 4. Integer Unsigned Magnitude Notation



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	-0.5 to +7.0V
Input Voltage	-0.5 to (V_{DD} +0.5V)
Output	
Applied voltage	-0.5 to (V_{DD} +0.5V)[2]
Forced current	-1.0 to +6.0mA[3,4]
Short-circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	-60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	-65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	25			35			ns
t_{PWH}	Clock Pulse Width, HIGH	25			35			ns
t_S	Input Setup Time	25			30			ns
t_H	Input Hold Time	3			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			-2.0			-2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				-55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = MAX, V_{IN} = 0V TSL, TSM, TSX = 5.0V		5		10	mA
I_{DDU}	Supply Current, Unloaded [1]	V_{DD} = MAX, F = 7.4MHz TSL, TSM, TSX = 5.0V		60		60	mA
I_{DDL}	Supply Current, Loaded [1, 2]	V_{DD} = MAX, F = 7.4MHz TSL, TSM, TSX = 0V Test Load: V_{LOAD} = V_{DD} MAX		150		170	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = MAX, V_I = 0.0V	-10	+10	-10	+10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = MAX, V_I = V_{DD}	-10	+10	-10	+10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = MIN, I_{OL} = MAX		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = MAX, V_I = 0.0V	-40	+40	-40	+40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = MAX, V_I = V_{DD}	-40	+40	-40	+40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = MAX, Output HIGH, one pin to ground, one second duration max		-100		-100	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Notes:

1. Guaranteed to maximum clock rate, tested at 2MHz.
2. Worst case, all inputs and outputs toggling at maximum rate.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MA}	Multiply-Accumulate Time	V_{DD} = MIN		135		170	ns
t_D	Output Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 2.2V		40		45	ns
t_{ENA}	Three-State Output Enable Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 1.5V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1} [2]		35		40	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in figure 9.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Figure 5. Timing Diagram

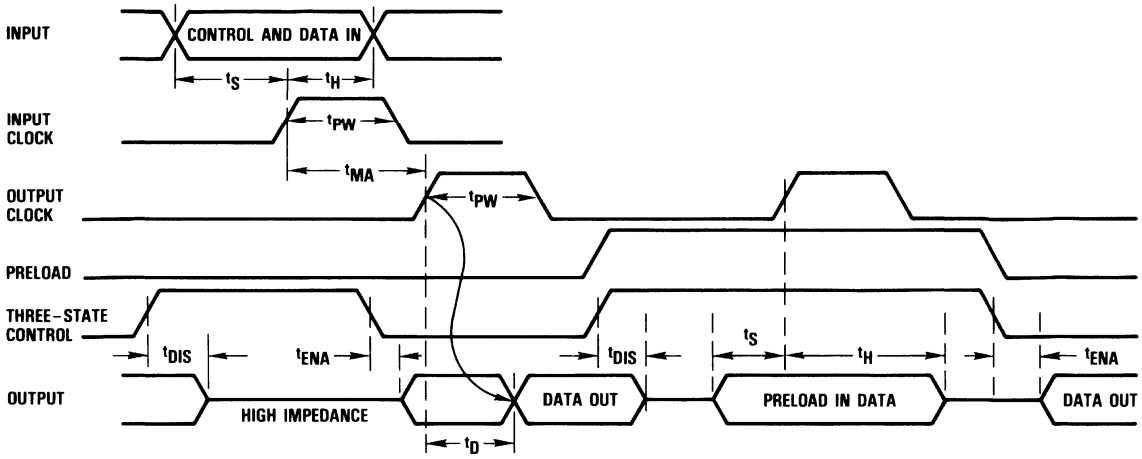


Figure 6. Equivalent Input Circuit

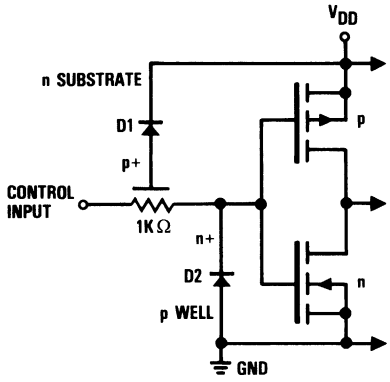


Figure 7. Equivalent Output Circuit

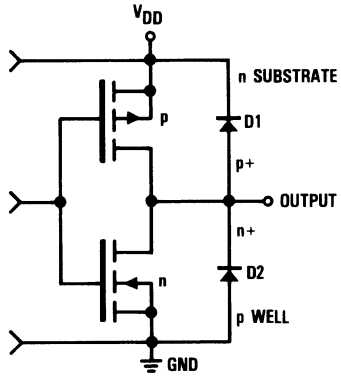


Figure 8. Test Load

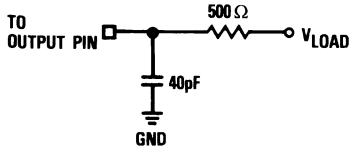
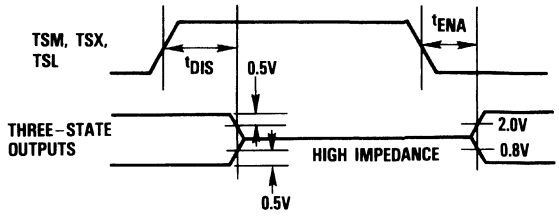


Figure 9. Transition Levels For Three-State Measurements



Application Notes

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and the register not be loaded again until a new constant is required. The multiply cycle then consists of loading new data into the remaining input register and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed and fractional notation in system design is only conceptual. For example, the TMC2009 does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 4.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2009J3C	STD – T_A = 0°C to 70°C	Commercial	64 Pin Hermetic Ceramic DIP	2009J3C
TMC2009J3V	EXT – T_C = –55°C to 125°C	MIL-STD-883	64 Pin Hermetic Ceramic DIP	2009J3V
TMC2009C1V	EXT – T_C = –55°C to 125°C	MIL-STD-883	64 Contact Hermetic Ceramic Chip Carrier	2009C1V

TMC208K, TMC28KU

CMOS Multiplier

8 x 8 Bit, 45ns, 65ns

The TMC208K and TMC28KU are high-speed 8 x 8 bit parallel multipliers which operate at a 45 or 65ns cycle time (22.2 or 15.3MHz multiplication rate). The multiplicand and multiplier are both two's complement numbers in the TMC208K and unsigned magnitude numbers in the TMC28KU, yielding a full precision 16-bit product.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are constructed using positive-edge-triggered D-type flip-flops. Built with TRW's OMICRON-C™ CMOS process, the TMC208K and TMC28KU are pin and function compatible with the MPY008H and MPY08HU yet operate with greater speeds at much less power dissipation.

Features

- 45 or 65ns Multiply Time
- 8 x 8 Bit Parallel Multiplication With 16-Bit Product Output
- Three-State Outputs
- Single +5V Power Supply
- TTL Compatible
- Available In A 40 Pin CERDIP Or Plastic DIP

TMC208K

- Pin Compatible With MPY008H
- Two's Complement Multiplication

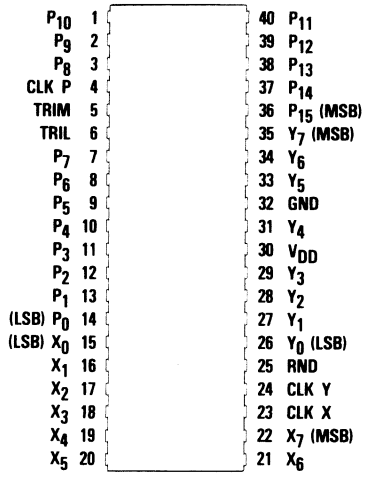
TMC28KU

- Pin Compatible With MPY08HU
- Unsigned Magnitude Multiplication

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Pin Assignments



40 Pin CERDIP – B5 Package
40 Pin Plastic DIP – N5 Package

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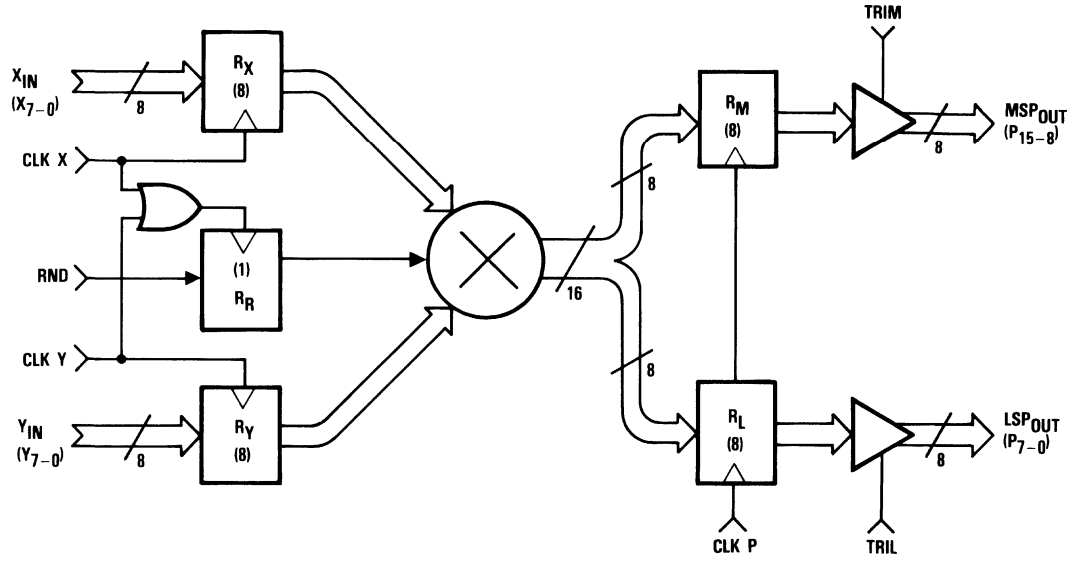
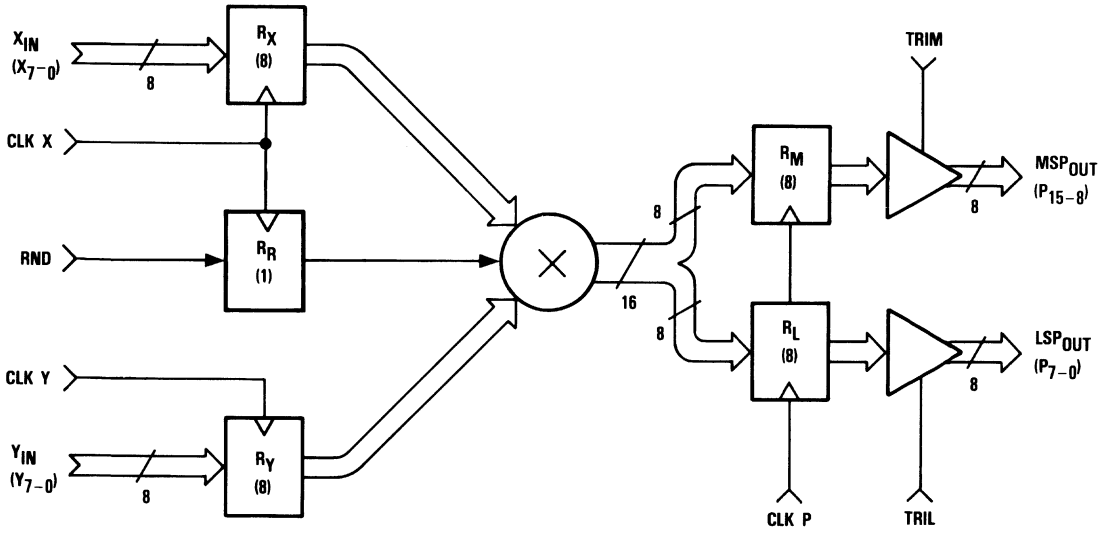
TMC208K Functional Block Diagram



TMC28KU Functional Block Diagram



Functional Description

General Information

The TMC208K and TMC28KU have three functional sections: input registers, an asynchronous multiplier array and output registers. The input registers store the two 8-bit numbers which are to be multiplied and the instruction which controls output rounding. The rounding control is used when a single-word output is desired. Each input operand is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders designed to handle two's complement numbers in the TMC208K or unsigned magnitude numbers in the TMC28KU. The output registers hold the product as two 8-bit words, the Most Significant Product (MSP) and the Least Significant Product (LSP). Three-state output drivers allow the multipliers to be used on a bus, or allow the MSP and LSP to be multiplexed over the same 8-bit output lines.

Signal Definitions

Power

V_{DD}, GND — The TMC208K and TMC28KU operate from a single +5 Volt supply. All power and ground lines must be connected.

Data Inputs

X_{7-0},Y_{7-0} — The TMC208K has two 8-bit two's complement data inputs labeled X and Y. The TMC28KU has two 8-bit unsigned magnitude data inputs labeled X and Y. The Most Significant Bits (MSBs), X_7 and Y_7, carry the sign information for the two's complement notation in the TMC208K. The remaining bits are X_{6-0} and Y_{6-0} with X_0 and Y_0 the LSBs. The input and output formats for fractional and integer two's complement, and fractional and integer unsigned magnitude notations are shown in Figures 1 through 4.

Data Outputs

P_{15-0} — The TMC208K has a 16-bit two's complement output which is the product of the two input X and Y values. The TMC28KU has a 16-bit unsigned magnitude output which is the product of the two input X and Y values. This output is divided into two 8-bit output words, the MSP and LSP. The MSB of both the MSP and the LSP is the sign bit in the TMC208K. The input and output formats for fractional and integer two's complement, and fractional and integer unsigned magnitude notations are shown in Figures 1 through 4. Note that since +1 cannot be exactly represented in fractional two's complement notation, some provision for handling the case (−1) x (−1) must be made. The TMC208K outputs a −1 in this case. As a result, external error handling provisions may be required.

Clocks

CLK X, CLK Y, CLK P — The TMC208K and TMC28KU have three clock lines, one for each input register (CLK X and CLK Y) and one for the product register (CLK P). Data present at the inputs of these registers are loaded into the registers on the rising edge of the appropriate clock. In the TMC208K, the RND input is registered and clocked in on the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading this control signal can be avoided by the use of normally LOW clocks. In the TMC28KU, the RND input is registered and clocked in on the rising edge of CLK X.

Controls

TRIM, TRIL — TRIM and TRIL are the three-state enable lines for the MSP and the LSP. The output driver is in the high-impedance state when TRIM or TRIL is HIGH, and enabled when LOW. TRIM and TRIL are not registered.

RND — When RND (Round) is HIGH, a one is added to the MSB of the LSP. A one will be added to the P_6 bit in the 208K or to the P_7 bit in the 28KU. Note that rounding always occurs in the positive direction. In some applications this may introduce a systematic bias. The RND input is registered and used when a rounded 8-bit product is desired.

Package Interconnections

Signal Type	Signal Name	Function	B5, N5 Package
Power	V_{DD}	Supply Voltage	30
	GND	Ground	32
Data Inputs	X_{7-0}	X Input Word	22-15
	Y_{7-0}	Y Input Word	35-33, 31, 29-26
Data Outputs	P_{15-8}	MSP Output	36-40, 1-3
	P_{7-0}	LSP Output	7-14
Clocks	CLK X	X Register Clock	23
	CLK Y	Y Register Clock	24
	CLK P	Product Register Clock	4
Controls	TRIM	MSP Three-State	5
	TRIL	LSP Three-State	6
	RND	Round	25

Figure 1. Fractional Two's Complement Notation (TMC208K)

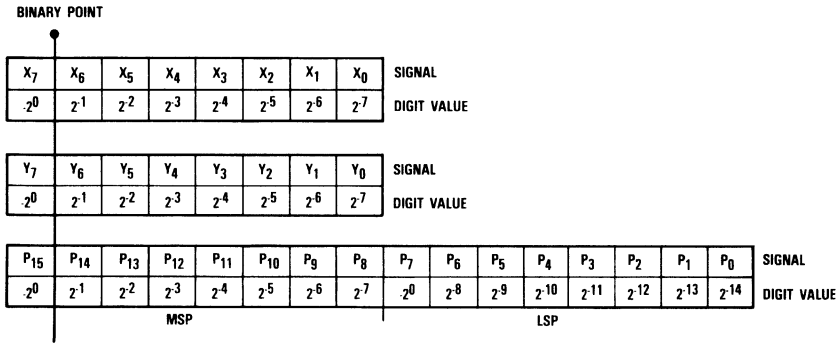


Figure 2. Integer Two's Complement Notation (TMC208K)

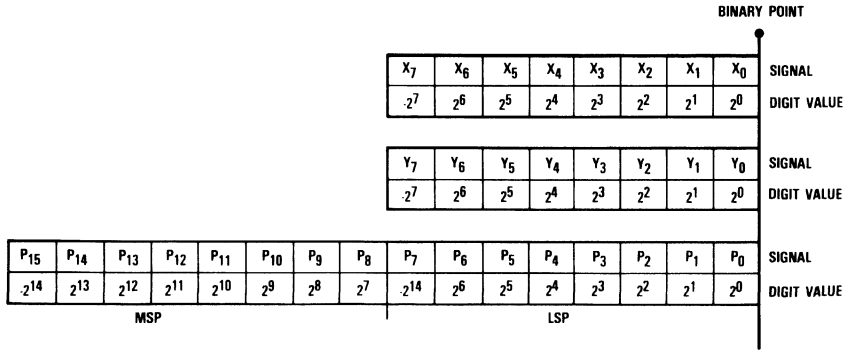


Figure 3. Fractional Unsigned Magnitude Notation (TMC28KU)

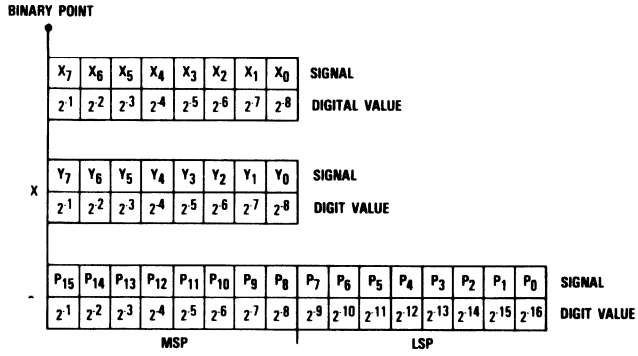


Figure 4. Integer Unsigned Magnitude Notation (TMC28KU)

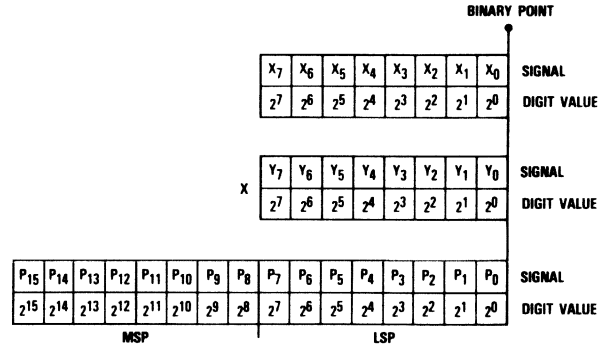


Figure 5. Timing Diagram

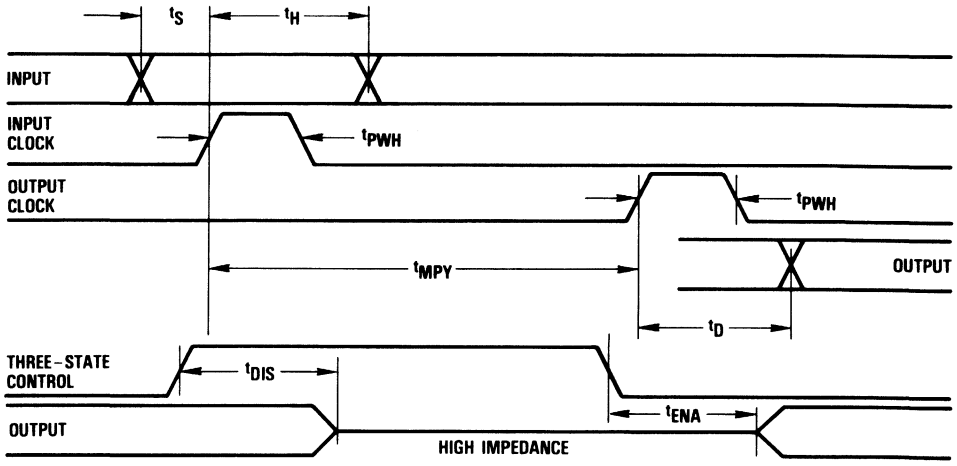


Figure 6. Equivalent Input Circuit

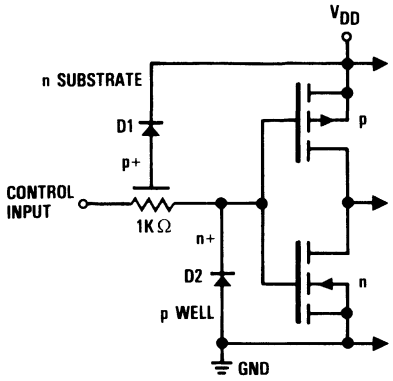


Figure 7. Equivalent Output Circuit

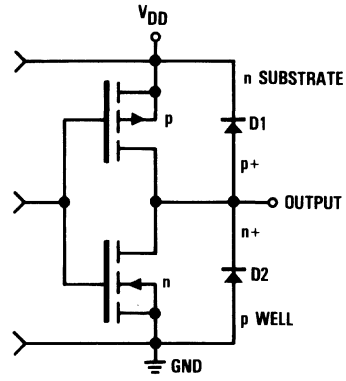
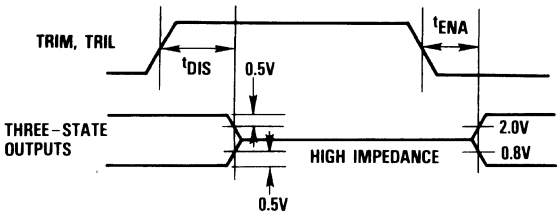


Figure 8. Threshold Levels For Three-State Measurements



Application Discussion

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register and that the register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed and fractional notation in system design is only conceptual. For example, the TMC208K and TMC28KU do not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64$$

The difference lies in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer or fractional notation. If integer notation is used, the LSBs of the multiplier, multiplicand and product all have the same value. If fractional notation is used, the MSBs of the multiplier, multiplicand and product all have the same value.

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		5		5	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, TRIM, TRIL = 5V, f = 10MHz		50		50	mA
		V_{DD} = Max, TRIM, TRIL = 5V, f = 22MHz		100		100	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		-10		-10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		-40		-40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		-100		-100	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note:
1. Actual test conditions may vary from those shown, but guarantee operation as specified.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MPY}	Multiply Time	V_{DD} = Min					
		TMC208K, TMC28KU		65		70	ns
		TMC208K-1, TMC28KU-1		45		50	ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD} = Min	15		15		ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD} = Min	15		15		ns
t_S	Input Setup Time	TMC208K, TMC28KU	25		30		ns
		TMC208K-1, TMC28KU-1	20		25		ns
t_H	Input Hold Time		0		0		ns
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF					
		TMC208K, TMC28KU		40		45	ns
		TMC208K-1, TMC28KU-1		25		30	ns
t_{ENA}	Three-State Output Enable Delay [1]	V_{DD} = Min, C_{LOAD} = 40pF					
		TMC208K, TMC28KU		40		45	ns
		TMC208K-1, TMC28KU-1		20		25	ns
t_{DIS}	Three-State Output Disable Delay [1]	V_{DD} = Min, C_{LOAD} = 40pF					
		TMC208K, TMC28KU		40		45	ns
		TMC208K-1, TMC28KU-1		20		25	ns

Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage [2]	−0.5 to (V_{DD} + 0.5)V
Forced current [3,4]	−1.0 to 6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC208KB5C	STD – T_A = 0°C to 70°C	Commercial	40 Pin CERDIP	208KB5C
TMC208KB5C1	STD – T_A = 0°C to 70°C	Commercial	40 Pin CERDIP	208KB5C1
TMC208KB5V	EXT – T_C = – 55°C to 125°C	MIL-STD-883	40 Pin CERDIP	208KB5V
TMC208KB5V1	EXT – T_C = – 55°C to 125°C	MIL-STD-883	40 Pin CERDIP	208KB5V1
TMC208KN5C	STD – T_A = 0°C to 70°C	Commercial	40 Pin Plastic DIP	208KN5C
TMC208KN5C1	STD – T_A = 0°C to 70°C	Commercial	40 Pin Plastic DIP	208KN5C1
TMC28KUB5C	STD – T_A = 0°C to 70°C	Commercial	40 Pin CERDIP	28KUB5C
TMC28KUB5C1	STD – T_A = 0°C to 70°C	Commercial	40 Pin CERDIP	28KUB5C1
TMC28KUB5V	EXT – T_C = – 55°C to 125°C	MIL-STD-833	40 Pin CERDIP	28KUB5V
TMC28KUB5V1	EXT – T_C = – 55°C to 125°C	MIL-STD-883	40 Pin CERDIP	28KUB5V1
TMC28KUN5C	STD – T_A = 0°C to 70°C	Commercial	40 Pin Plastic DIP	28KUN5C
TMC28KUN5C1	STD – T_A = 0°C to 70°C	Commercial	40 Pin Plastic DIP	28KUN5C1

TMC216H

CMOS Multiplier
16 x 16 Bit, 145ns

The TRW TMC216H is a high-speed 16 x 16 bit parallel multiplier which operates at a 145ns cycle time (6.9MHz multiplication rate). The multiplicand and the multiplier may be independently specified as two's complement or unsigned magnitude, yielding a full precision 32-bit product.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The Least Significant Product (LSP) shares a bidirectional port with the Y input. All outputs are three-state.

Built with TRW's state of the art 2-micron CMOS process, the TMC216H is pin and function compatible with the industry standard MPY016H and operates with the same speed at approximately one-fifth the power dissipation.

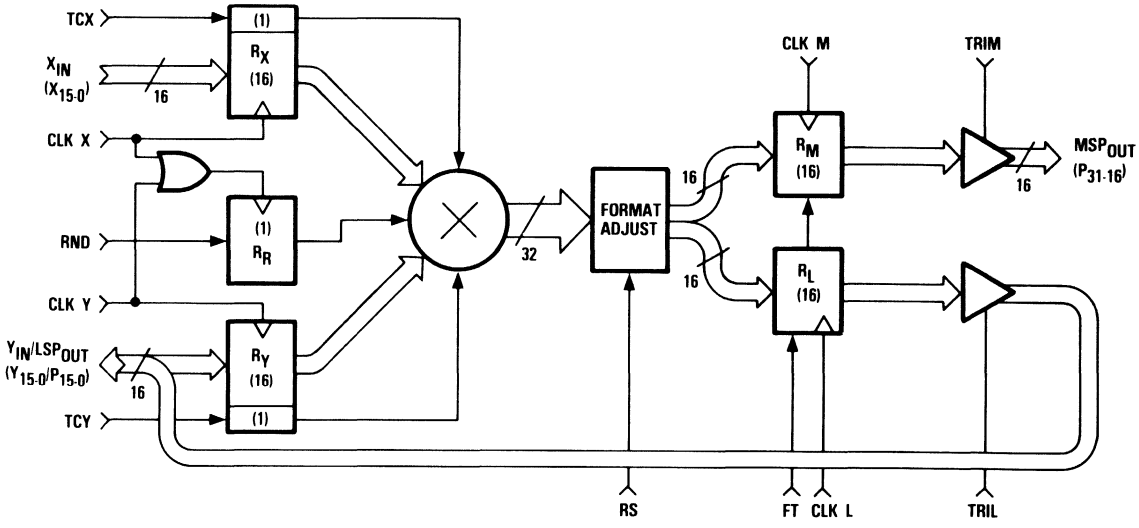
Features

- Fully TTL Compatible
- 145ns Multiply Time (Worst Case)
- Low Power CMOS Technology
- Single +5V Power Supply
- Pin And Function Compatible With TRW MPY016H
- Output Registers Can Be Made Transparent
- Three-State Outputs
- Two's Complement, Unsigned Magnitude, Or Mixed Mode Multiplication
- Available In 64 Pin Hermetic Ceramic DIP

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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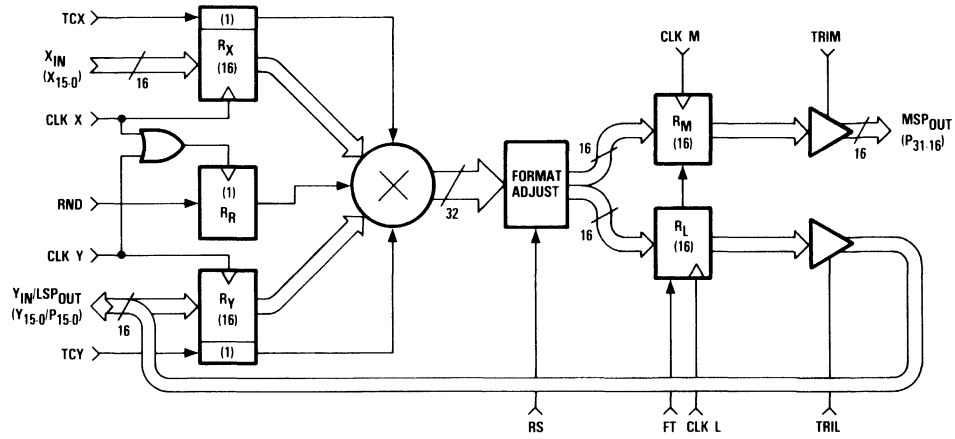
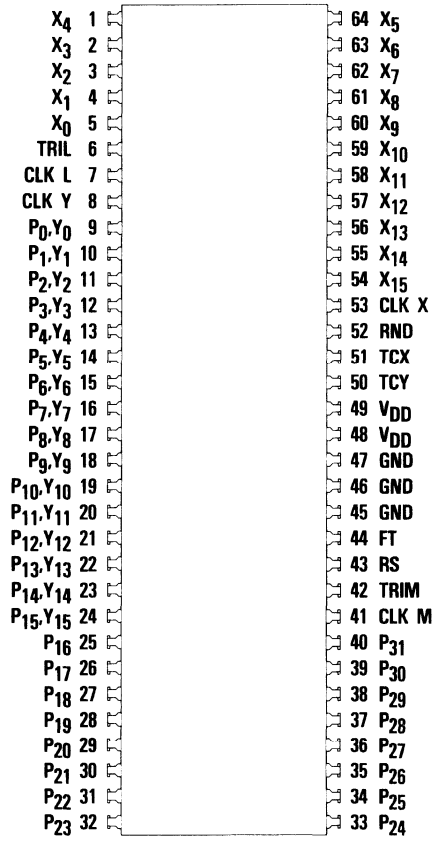
Printed in the U.S.A.

Functional Block Diagram



Pin Assignments



64 Lead DIP – J3 Package

Functional Description

General Information

The TMC216H has three functional sections: Input registers, an asynchronous multiplier array, and output registers. The input registers store the two 16-bit numbers which are to be multiplied and the instruction which controls the output rounding. The rounding control is used when a single-word output is desired. Each input operand is stored independently, simplifying multiplication by a constant. The asynchronous multiplier array is a network of AND gates and adders, designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 16-bit words, the Most Significant Product (MSP) and the Least Significant Product (LSP). Three-state output drivers allow the TMC216H to be used on a bus, or allow the Y input, least and most significant outputs to be multiplexed over the same 16-bit input/output lines. The Least Significant Product (LSP) is multiplexed with the Y input.

Power

The TMC216H operates from a single +5 Volt supply. All power and ground lines must be connected. Note that the device is pin and function compatible with the MPY016H.

Name	Function	Value	J3 Package
V_{DD}	Positive Supply Voltage	+5.0V	Pins 48, 49
GND	Ground	0.0V	Pins 45, 46, 47

Data Inputs

The TMC216H has two 16-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{15} and Y_{15}, carry the sign information for the two's complement notation. The remaining bits are denoted X_0 through X_{14} and Y_0 through Y_{14} (with X_0 and Y_0 the Least Significant Bits). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6, respectively. The Y inputs are multiplexed with the LSP outputs, and hence can only be used when the TRIL control is in a HIGH state.

Name	Function	Value	J3 Package
X_{15}	X Data MSB	TTL	Pin 54
X_{14}		TTL	Pin 55
X_{13}		TTL	Pin 56
X_{12}		TTL	Pin 57
X_{11}		TTL	Pin 58
X_{10}		TTL	Pin 59
X_9		TTL	Pin 60
X_8		TTL	Pin 61
X_7		TTL	Pin 62
X_6		TTL	Pin 63
X_5		TTL	Pin 64
X_4		TTL	Pin 1
X_3		TTL	Pin 2
X_2		TTL	Pin 3
X_1		TTL	Pin 4
X_0	X Data LSB	TTL	Pin 5

Data Inputs (Cont.)

Name	Function	Value	J3 Package
Y_{15}	Y Data MSB	TTL	Pin 24
Y_{14}		TTL	Pin 23
Y_{13}		TTL	Pin 22
Y_{12}		TTL	Pin 21
Y_{11}		TTL	Pin 20
Y_{10}		TTL	Pin 19
Y_9		TTL	Pin 18
Y_8		TTL	Pin 17
Y_7		TTL	Pin 16
Y_6		TTL	Pin 15
Y_5		TTL	Pin 14
Y_4		TTL	Pin 13
Y_3		TTL	Pin 12
Y_2		TTL	Pin 11
Y_1		TTL	Pin 10
Y_0	Y Data LSB	TTL	Pin 9

Data Outputs

The TMC216H has a 32-bit two's complement or unsigned magnitude output which is the product of the two input data values. This output is divided into two 16-bit output words, the Most Significant Product (MSP) and Least Significant Product (LSP). The Most Significant Bit (MSB) of both the MSP and the LSP is the sign bit if fractional two's complement notation is used (TCX=TCY=1, RS=0). The input and output formats for fractional two's complement, fractional unsigned magnitude, fractional mixed mode, integer two's complement, integer unsigned magnitude, and integer mixed mode notation are shown in Figures 1 through 6, respectively.

The LSP output can be taken from the Y input pins only when TRIL is LOW. Care must be taken to enable these shared input lines only at the proper time. For an output from the MSP lines to be read, the TRIM control must be LOW.

RS is an output format control. A HIGH on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, or integer two's complement operation.

Name	Function	Value	J3 Package
P_{31}	Product MSB	TTL	Pin 40
P_{30}		TTL	Pin 39
P_{29}		TTL	Pin 38
P_{28}		TTL	Pin 37
P_{27}		TTL	Pin 36
P_{26}		TTL	Pin 35
P_{25}		TTL	Pin 34
P_{24}		TTL	Pin 33
P_{23}		TTL	Pin 32
P_{22}		TTL	Pin 31
P_{21}		TTL	Pin 30
P_{20}		TTL	Pin 29
P_{19}		TTL	Pin 28
P_{18}		TTL	Pin 27
P_{17}		TTL	Pin 26
P_{16}		TTL	Pin 25

Data Outputs (Cont.)

Name	Function	Value	J3 Package
P_{15}		TTL	Pin 24
P_{14}		TTL	Pin 23
P_{13}		TTL	Pin 22
P_{12}		TTL	Pin 21
P_{11}		TTL	Pin 20
P_{10}		TTL	Pin 19
P_9		TTL	Pin 18
P_8		TTL	Pin 17
P_7		TTL	Pin 16
P_6		TTL	Pin 15
P_5		TTL	Pin 14
P_4		TTL	Pin 13
P_3		TTL	Pin 12
P_2		TTL	Pin 11
P_1		TTL	Pin 10
P_0	Product LSB	TTL	Pin 9

Clocks

The TMC216H has four clock lines, one for each input register and one for each product register. Data and two's complement instructions present at the inputs of these registers are loaded into the registers at the rising edge of the appropriate clock. The RND input is registered and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading this control signal can be avoided by the use of normally LOW clocks.

Name	Function	Value	J3 Package
CLK X	Clock Input Data X	TTL	Pin 53
CLK Y	Clock Input Data Y	TTL	Pin 8
CLK L	Clock LSP Register	TTL	Pin 7
CLK M	Clock MSP Register	TTL	Pin 41

Controls

The TMC216H has seven control lines:

FT — Feedthrough. A control line which makes the output register transparent if it is HIGH.

TRIM, TRIL — Three-state enable lines for the MSP and the LSP. The output driver is in the high-impedance state when TRIM or TRIL is HIGH, and enabled when the appropriate control is LOW.

RS — Register Shift. RS is an output format control. A HIGH level on RS deletes the sign bit from the LSP and shifts the MSP down one bit. This is mandatory for unsigned magnitude, mixed mode, and two's complement integer operations.

RND — Round. When RND is HIGH, a one is added to the MSB of the LSP. Note that this bit depends on the state of the RS control. If RS is LOW when RND is HIGH, a one will be added to the 2^{-16} bit (P_{14}). If RS is HIGH when RND is HIGH, a one will be added to the 2^{-15} bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction; in some systems this may introduce a systematic bias.

TCX, TCY — Control how the device interprets data on the X and Y inputs. A HIGH on TCX or TCY forces the TMC216H to consider the appropriate input as a two's complement number, while a LOW forces the TMC216H to consider the appropriate input as a magnitude only number.

FT, RS, TRIM, and TRIL are not registered. The TCX input is registered, and clocked in at the rising edge of the X clock signal, CLK X. The TCY input is also registered, and clocked in at the rising edge of the Y clock signal, CLK Y. The RND input is registered, and clocked in at the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems with loading these control signals can be avoided by the use of normally LOW clocks.

Name	Function	Value	J3 Package
RND	Round Control Bit	TTL	Pin 52
TCX	X Input Two's Complement	TTL	Pin 51
TCY	Y Input Two's Complement	TTL	Pin 50
FT	Output Register Feedthrough	TTL	Pin 44
RS	Output Register Shift	TTL	Pin 43
TRIM	MSP Three-State Control	TTL	Pin 42
TRIL	LSP Three-State Control	TTL	Pin 6

Figure 1. Fractional Two's Complement Notation

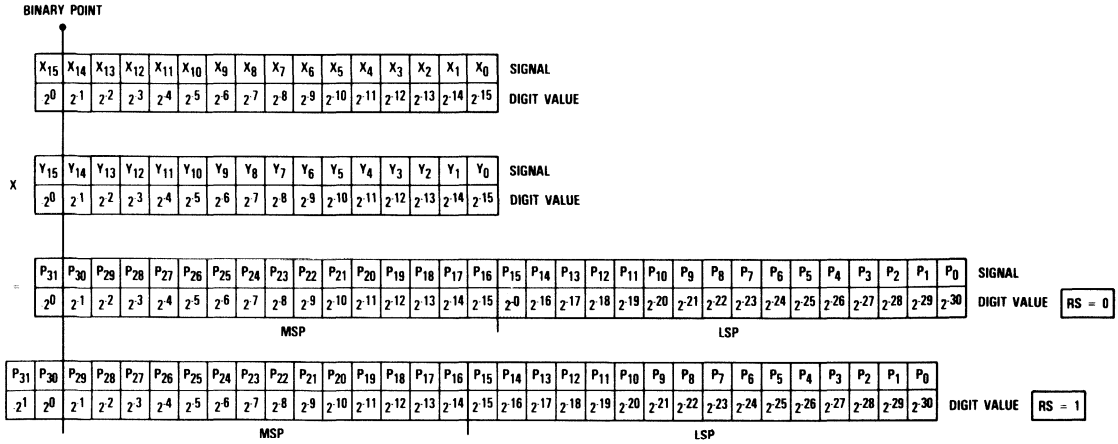


Figure 2. Fractional Unsigned Magnitude Notation

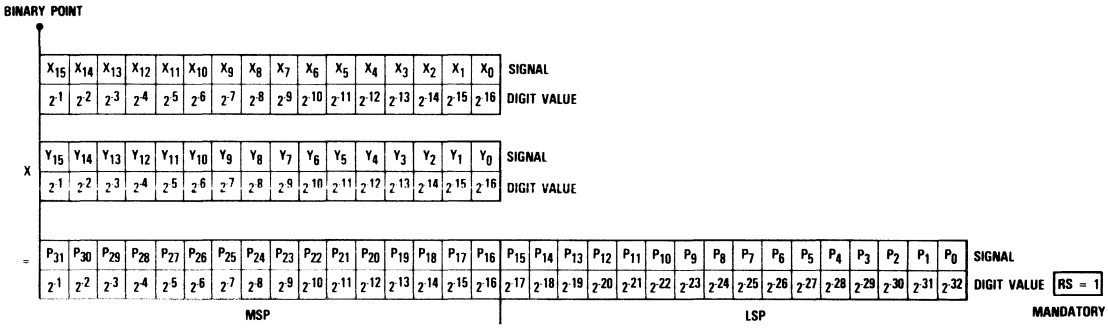


Figure 3. Fractional Mixed Notation

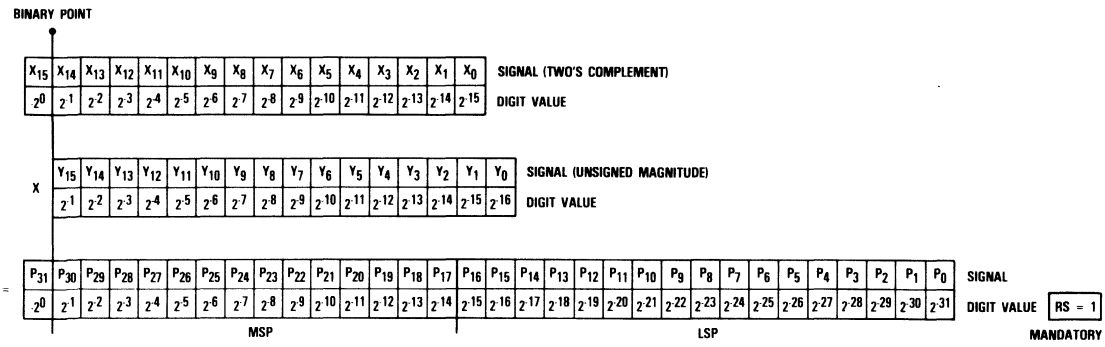


Figure 4. Integer Two's Complement Notation

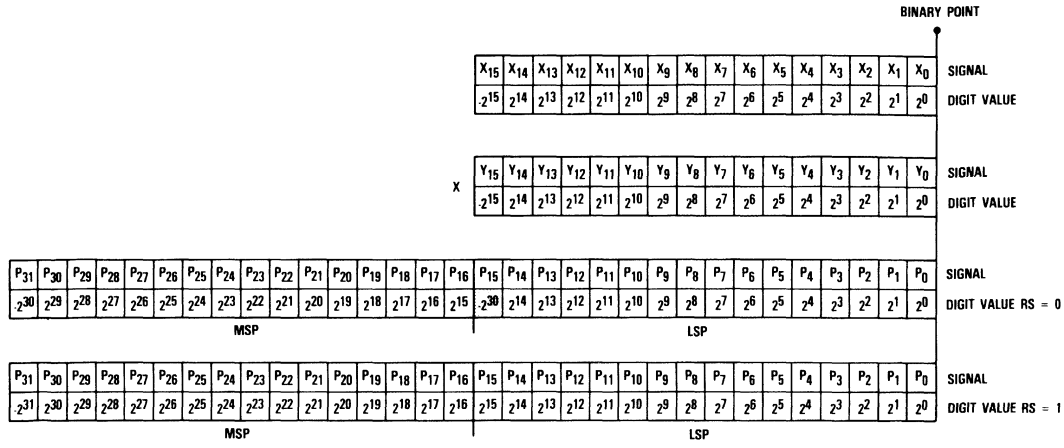


Figure 5. Integer Unsigned Magnitude Notation

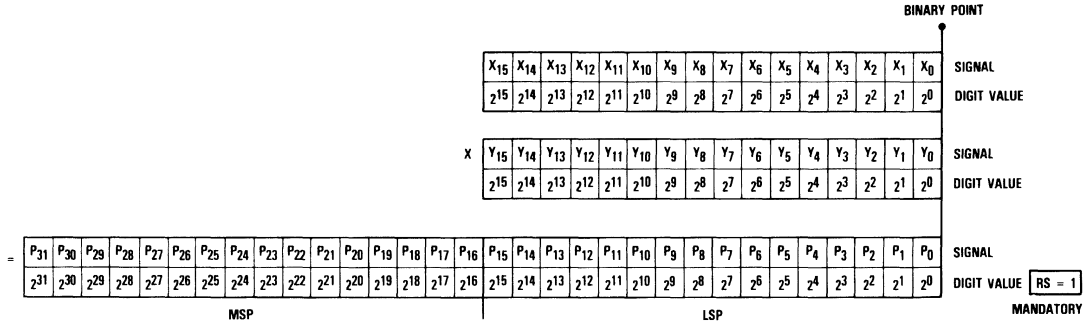


Figure 6. Integer Mixed Mode Notation

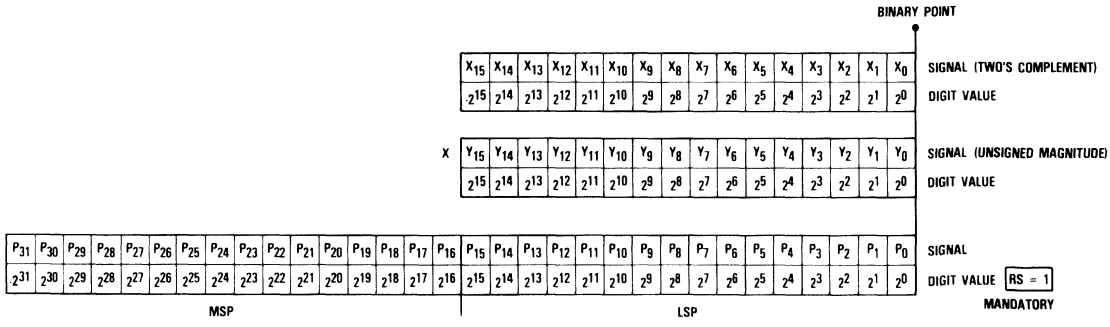


Figure 7. Timing Diagram, Clocked Mode

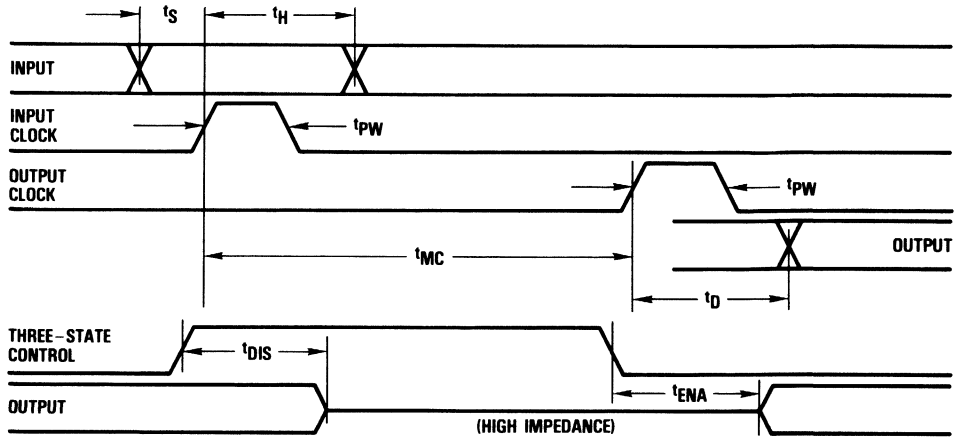


Figure 8. Timing Diagram, Unclocked Mode

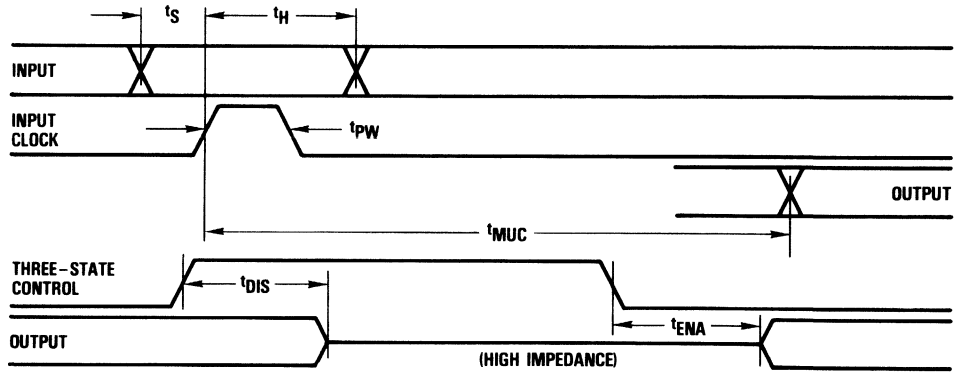


Figure 9. Equivalent Input Circuit

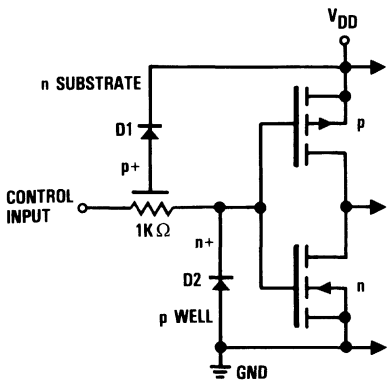


Figure 10. Equivalent Output Circuit

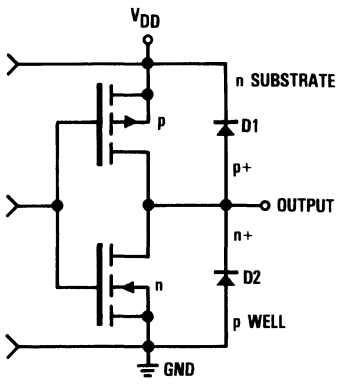


Figure 11. Test Load

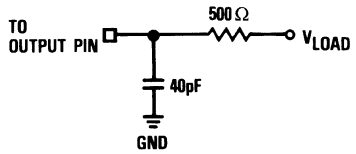
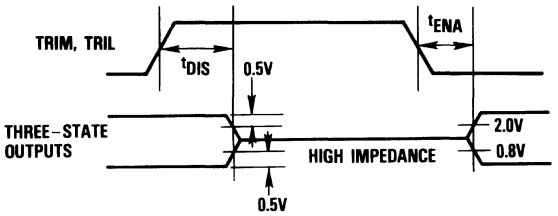


Figure 12. Transition Levels For Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD} +0.5V)

Output

Applied voltage ..... −0.5 to (V_{DD} +0.5V)[2]

Forced current ..... −1.0 to +6.0mA[3,4]

Short-circuit duration (single output in high state to ground) ..... 1 sec

Temperature

Operating, case ..... −60 to +130°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	25			30			ns
t_{PWH}	Clock Pulse Width, HIGH	25			30			ns
t_S	Input Setup Time	25			30			ns
t_H	Input Hold Time	3			3			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		+125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD} = MAX, V_{IN} = 0V TRIM, TRIL = 5.0V		5		10	mA
I_{DDU}	Supply Current, Unloaded [1]	V_{DD} = MAX, F = 6.8MHz TRIM, TRIL = 5.0V		70		70	mA
I_{DDL}	Supply Current, Loaded [1, 2]	V_{DD} = MAX, F = 6.8MHz TRIM, TRIL = 0V Test Load: V_{LOAD} = V_{DD} MAX		180		180	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = MAX, V_I = 0.4V					
		X_{IN}, Controls, Clocks	-10	+10	-10	+10	μA
		$\overline{Y_{IN}}$	-40	+40	-40	+40	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = MAX, V_I = 2.4V					
		X_{IN}, Controls, Clocks	-10	+10	-10	+10	μA
		$\overline{Y_{IN}}$	-40	+40	-40	+40	μA
I_I	Input Current, Max Input Voltage	V_{DD} = MAX, V_I = V_{DD}		+75		+75	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = MIN, I_{OL} = MAX		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = MAX, V_I = 0.4V	-40	+40	-40	+40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = MAX, V_I = 2.4V	-40	+40	-40	+40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = MAX, Output HIGH, one pin to ground, one second duration max		-80		-80	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		10		10	pF

Notes:

1. Guaranteed to maximum clock rate, tested at 2MHz.
2. Worst case, all inputs and outputs toggling at maximum rate.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Extended Min	Extended Max	Units
t_{MC}	Multiply Time, Clocked	V_{DD} = MIN		145		185	ns
t_{MUC}	Multiply Time, Unclocked	V_{DD} = MIN, Test Load: V_{LOAD} = 2.2V		185		230	ns
t_D	Output Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 2.2V		45		50	ns
t_{ENA}	Three-State Output Enable Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 1.5V		40		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{DD} = MIN, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1} [2]		40		45	ns

Notes:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in figure 12.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Application Notes

Mixed Mode Multiplication

There are several applications in which mixed mode multiplication may be advantageous. For example, inputs to a digital signal processor are often generated as unsigned magnitude numbers (e.g., data from an analog-to-digital converter). These numbers are effectively all positive values. In contrast, filter coefficients must often be negative. As a result, either the unsigned magnitude data must be converted to two's complement notation (which requires an additional bit), or the multiplier must be capable of mixed mode operation. The TMC216H provides this capability by independently specifying the mode of the multiplicand (X) and the multiplier (Y) on the TCX and TCY pins. No additional circuitry is required and the resulting product is in two's complement notation.

Multiplication by a Constant

Multiplication by a constant only requires that the constant be loaded into the desired input register, and that the selected register not be loaded again until a new constant is desired. The multiply cycle then consists simply of loading new data and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed, and fractional notation in system design is only conceptual. For example, the TMC216H does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in Figures 1 through 6.

Register Shift (RS) Control

In two's complement notation, the acceptable range of values for a given word size is not the same for positive and negative numbers. The largest negative number is one LSB larger than the largest positive number. This is true for either fractional or integer notation. A problem can arise when the largest representable negative number is multiplied by itself. This should give a positive number of the same magnitude. However, the largest representable positive number is one LSB less than this value. As a result, this product cannot be correctly represented without using one additional output bit. The TMC216H has a Register Shift (RS) control that permits shifting of the result to provide a correct answer for every two's complement multiplication. When RS is active, the value of all bits in the MSP is doubled (i.e. shifted left one position), which provides the capability to represent the largest possible product. The MSB of the Least Significant Product is changed from a duplicate of the sign bit to the necessary bit to fill in the output word. The effects of this control are illustrated in Figures 1 and 4. Note that for unsigned magnitude operation, the RS control must be HIGH.

Output Register Transparent Mode

If the FT input is HIGH, the output register is made transparent: i.e., the product will appear at the output drivers as it is generated internally. The clock for the product register (CLK P) is not required in this mode of operation. The transparent mode is rarely used as it is much slower than the registered mode. It is essentially a special-purpose mode of operation.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC216HJ3C	STD – T_A = 0°C to 70°C	Commercial	64 Pin Hermetic Ceramic DIP	216HJ3C
TMC216HJ3A	EXT – T_C = –55°C to 125°C	High Reliability	64 Pin Hermetic Ceramic DIP	216HJ3A

TMC2208

CMOS Multiplier-Accumulator

8 x 8 Bit, 40ns

The TMC2208 is a high-speed 8 x 8 bit parallel multiplier-accumulator which operates at a 40ns cycle time (25MHz multiply-accumulate rate). The input data may be specified as two's complement or unsigned magnitude, yielding a full-precision 16-bit product. Products may be accumulated to a 19-bit result.

Individually clocked input and output registers are used to provide maximum system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit eXTended Product (XTP), an 8-bit Most Significant Product (MSP), and an 8-bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP, MSP, and LSP. The output register can be preloaded directly via the output ports.

The TMC2208 is pin and function compatible with the TDC1008 in the 48 pin DIP. Built with TRW's OMICRON C™ one micron CMOS process, power consumption is greatly reduced.

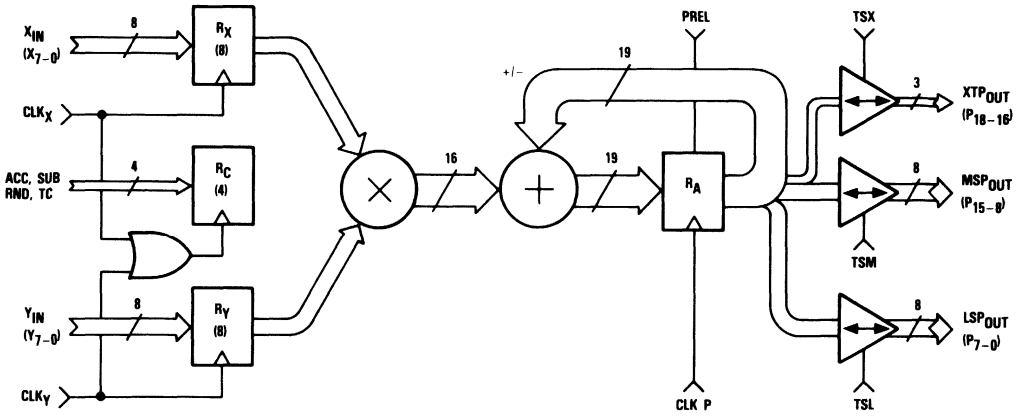
Features

- Function Compatible With The TDC1008 (Pin Compatible In 48 Pin Dip Package)
- 40ns Multiply-Accumulate Time (Worst Case Commercial)
- 8 x 8 Parallel Multiplication With Accumulation To 19-Bit Result
- Selectable Accumulation, Subtraction, Rounding, And Accumulator Preload
- All Inputs And Outputs Are Registered And TTL Compatible
- Three-State Outputs
- Two's Complement Or Unsigned Magnitude Operation
- Single +5V Power Supply
- Low Power CMOS Construction
- Available In 48 Pin Ceramic Or Plastic DIP And PLCC

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Micro/Mini-Computer

Functional Block Diagram



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FAX: (619) 455-6314

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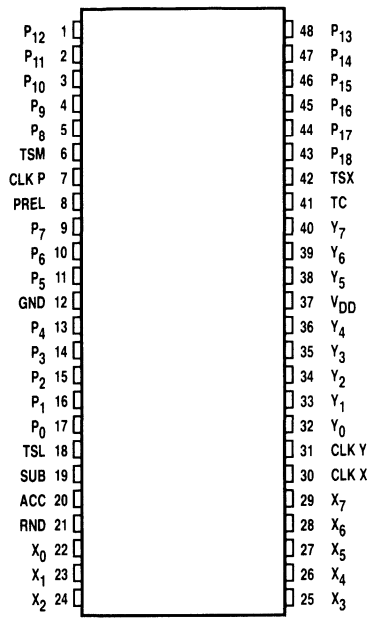
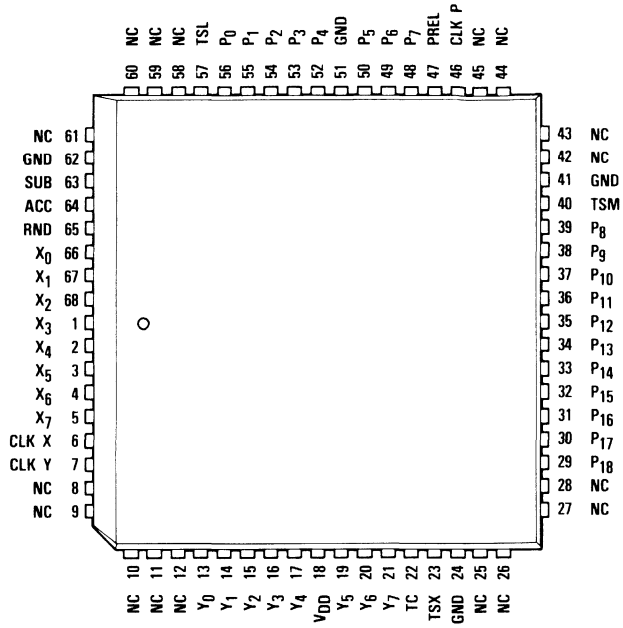
Pin Assignments



48 Pin Hermetic Ceramic DIP – J4 Package
48 Pin Ceramic DIP – N4 Package



68 Leaded Plastic Chip Carrier – R1 Package

Functional Description

General Information

The TMC2208 consists of four functional sections: input registers, an asynchronous multiplier array, an adder and output registers. The input registers store the two 8-bit numbers which are to be multiplied, and the control lines which control the input numerical format (two's complement or unsigned magnitude), output rounding, accumulation, and subtraction. The round control is used when a single-word output is desired. Each input is independently stored, simplifying multiplication by a constant. The output registers can be preloaded with a constant to provide the sum of products plus a constant. The asynchronous multiplier array is a network of AND gates and adders, which has been designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 8-bit words and one 3-bit word: the Most Significant Product (MSP), the Least Significant Product (LSP) and the eXTended Product (XTP). Three-state output drivers permit the TMC2208 to be used on a bus, or allow the outputs to be multiplexed over the same 8-bit output lines.

Signal Definitions

Power

VDD, GND — The TMC2208 operates from a single +5V supply. All power and ground lines must be connected.

Data Inputs

$X_{7\text{-}0}$ — The 8-bit two's complement or unsigned magnitude X data input. X_7 is the MSB and contains the sign information for two's complement notation. The data on the X input is clocked into the input register on the rising edge of CLK X.

$Y_{7\text{-}0}$ — The 8-bit two's complement or unsigned magnitude Y data input. Y_7 is the MSB and contains the sign information for two's complement notation. The data on the Y input is clocked into the input register on the rising edge of CLK Y.

Data Outputs

P_{18-0} — P_{18-0} is the accumulated product result for the TMC2208. The 19-bit output is either the two's complement or unsigned magnitude result of the accumulated products. The output is divided into two 8-bit output words (MSP, LSP) and one 3-bit output word (XTP). P_{18} is the MSB and contains the sign information for two's complement notation. Formats for two's complement, fractional unsigned magnitude, integer two's complement and integer unsigned notation are shown in ***Figures 1 through 4***.

Clocks

CLK X, CLK Y — The rising edge of CLK X (CLK Y) loads the data lines into the appropriate input register. The RouND (RND), Two's Complement (TC), ACCumulate (ACC), and SUBtract (SUB) control inputs are registered and loaded on the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally HIGH clock signals are used. Problems can be avoided by the use of normally LOW clocks.

CLK P — CLK P is used to clock the accumulated product sum into the output register. If ACC is HIGH, the content of the output register is added to the next product generated and loaded into the output register. CLK P is also used to preload the output register from the output pins (see *Table 1*).

Controls

TSX, TSM, TSL — TSX is the three-state control for the 3-bit XTP output drivers. TSM and TSL are the three-state controls for the MSP and LSP outputs respectively. The outputs are in the high-impedance state when the control is HIGH, and enabled when the control is LOW.

PREL — PRELoad is the active-HIGH control used to directly load the output register (see *Table 1*). When PREL is HIGH, all output buffers are forced into the high-impedance state. Second, when any or all the the TSX, TSM and TSL controls is also HIGH, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX, TSM, TSL), and to the data being preloaded.

RND — The RouND input is used to control the rounding of results. When RND is HIGH, a 1 is added to the Most Significant Bit (MSB) of the LSP for rounding the product in the MSP and XTP rather than truncating it. This control is used to improve accuracy when the LSP will not be used.

TC — The Two's Complement input is used to control how the TMC2208 interprets the data on the X and Y inputs. TC HIGH makes both inputs two's complement, while TC LOW makes both inputs unsigned magnitude numbers.

ACC — When ACCumulate is HIGH, the content of the output register is added or subtracted from the next product generated, and their sum stored back into the output register on the next rising edge of CLK P. When ACC is LOW, multiplication without accumulation is performed, and the next product generated is stored into the output registers directly. This operation is used for the first term in a summation to avoid a separate "clear" operation.

SUB — SUBtract is used in conjunction with the ACC control. When both the ACC and SUB controls are HIGH, the content of the output register is subtracted from the next product generated and the difference is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

Package Interconnections

Signal Type	Signal Name	Function	J4, N4 Package Pins	R1 Package Pins
Power	V_{DD}	Supply Voltage	37	18
	GND	Ground	12	24, 41, 51, 62
Data Input	X_{7-0}	X Input Data	29, 28, 27, 26, 25, 24, 23, 22	5, 4, 3, 2, 1, 68, 67, 66
	Y_{7-0}	Y Input Data	40, 39, 38, 36, 35, 34, 33, 32	21, 20, 19, 17, 16, 15, 14, 13
Data Outputs	P_{18-0}	Product Output Data	43, 44, 45, 46, 47, 48, 1, 2, 3, 4, 5, 9, 10, 11, 13, 14, 15, 16, 17	29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 48, 49, 50, 52, 53, 54, 55, 56
Clock	CLK X	X Input Clock	30	6
	CLK Y	Y Input Clock	31	7
	CLK P	Output Register Clock	7	46
Control	TSX	XTP Three-State Control	42	23
	TSM	MSP Three-State Control	6	40
	TSL	LSP Three-State Control	18	57
	PREL	Preload Output Register	8	47
	RND	Round MSP of Product	21	65
	TC	Two's Complement Control	41	22
	ACC	Accumulate Control	20	64
	SUB	Subtract Control	19	63
No Connect	NC	Unused		8, 9, 10, 11, 12, 25, 26, 27, 28, 28, 42, 43, 44, 45, 58, 59, 60, 61

Preload Truth Table

PREL [1]	TSX [1]	TSM [1]	TSL [1]	XTP	MSP	LSP
L	L	L	L	Register → Output Pin	Register → Output Pin	Register → Output Pin
L	L	L	H	Register → Output Pin	Register → Output Pin	Hi-Z
L	L	H	L	Register → Output Pin	Hi-Z	Register → Output Pin
L	L	H	H	Register → Output Pin	Hi-Z	Hi-Z
L	H	L	L	Hi-Z	Register → Output Pin	Register → Output Pin
L	H	L	H	Hi-Z	Register → Output Pin	Hi-Z
L	H	H	L	Hi-Z	Hi-Z	Register → Output Pin
L	H	H	H	Hi-Z	Hi-Z	Hi-Z
H [2]	L	L	L	Hi-Z	Hi-Z	Hi-Z
H [2]	L	L	H	Hi-Z	Hi-Z	Hi-Z Preload
H [2]	L	H	L	Hi-Z	Hi-Z Preload	Hi-Z
H [2]	L	H	H	Hi-Z	Hi-Z Preload	Hi-Z Preload
H [2]	H	L	L	Hi-Z Preload	Hi-Z	Hi-Z
H [2]	H	L	H	Hi-Z Preload	Hi-Z	Hi-Z Preload
H [2]	H	H	L	Hi-Z Preload	Hi-Z Preload	Hi-Z
H [2]	H	H	H	Hi-Z Preload	Hi-Z Preload	Hi-Z Preload

Notes: 1. PREL, TSX, TSM and TSL are not registered.
2. PREL Hi inhibits any change of output register for those outputs in which the three-state control is LOW.

Figure 1. Fractional Two's Complement Notation

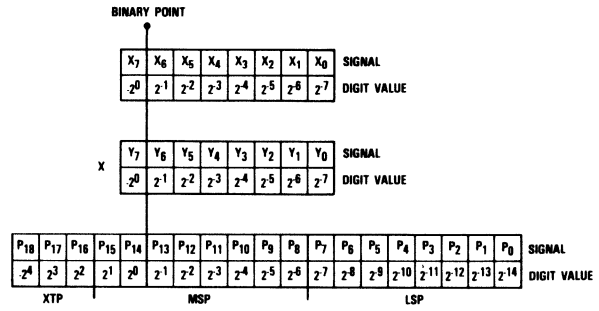


Figure 2. Fractional Unsigned Magnitude Notation

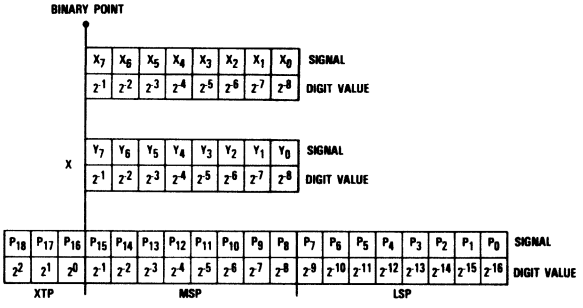


Figure 3. Integer Two's Complement Notation

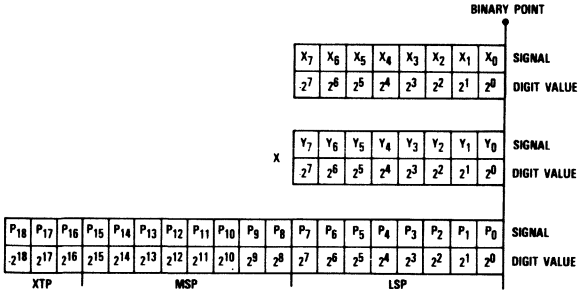
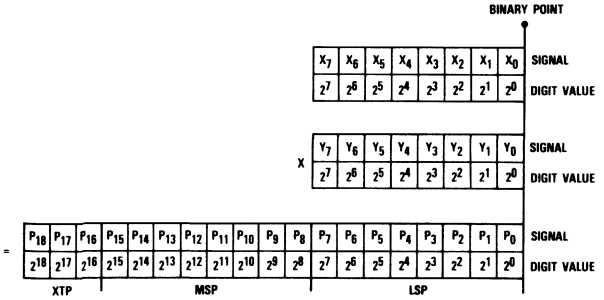


Figure 4. Integer Unsigned Magnitude Notation



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD} + 0.5)V

Output

Applied voltage [2] ..... −0.5 to (V_{DD} + 0.5)V

Forced current [3,4] ..... −1.0 to +6.0mA

Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −60 to +130°C

junction ..... +175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width HIGH	15			15			ns
t_S	Input Setup Time (Except PREL)	10			11			ns
t_S	Input Setup Time (PREL)	12			13			ns
t_H	Input Hold Time	0			2			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V TSL, TSM, TSX = 5V		5		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 25MHz TSL, TSM, TSX = 5V		30		35	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		−10		−10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = 4mA		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = −2mA	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		−40		−40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		−100		−100	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		15		15	pF

Note: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{MA}	Multiply-Accumulate Time	V_{DD} = Min		40		50	ns
t_D	Output Delay	V_{DD} = Min, Load = 40pF		23		25	ns
t_{ENA}	Three-State Output Enable Delay	V_{DD} = Min, Load = 40pF		19		21	ns
t_{DIS}	Three-State Output Disable Delay	V_{DD} = Min, Load = 40pF		16		18	ns

Notes: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Figure 5. Timing Diagram

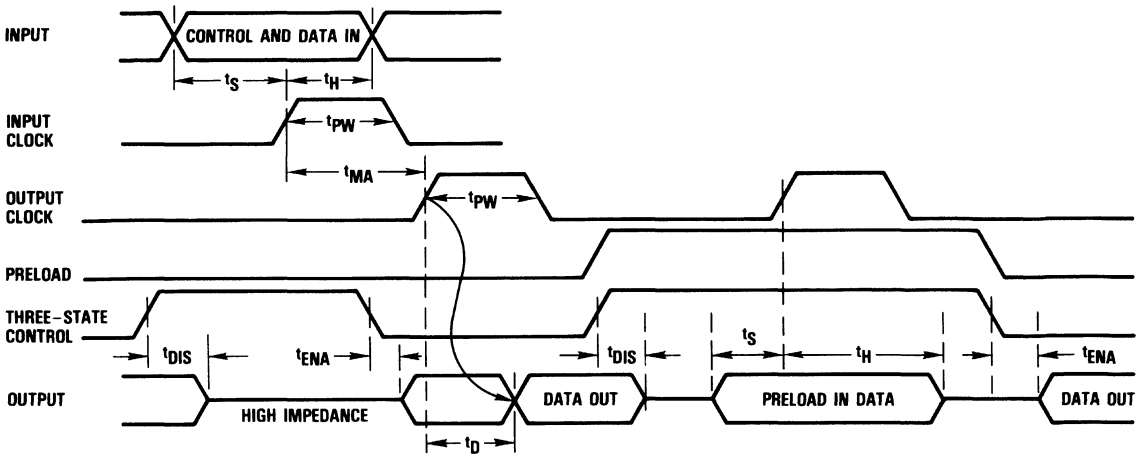


Figure 6. Equivalent Input Circuit

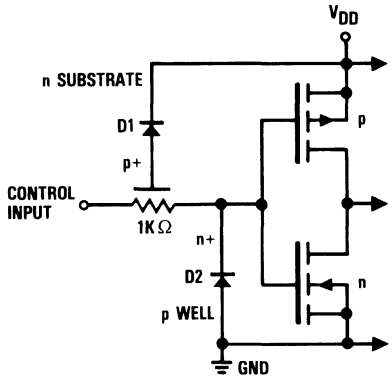
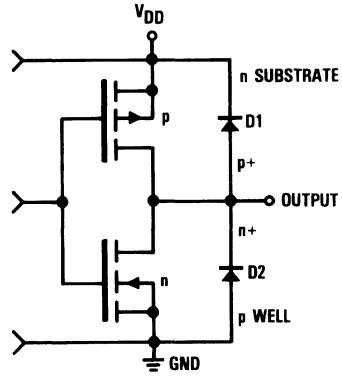


Figure 7. Equivalent Output Circuit



Application Notes

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register, and the register not be loaded again until a new constant is required. The multiply cycle then consists of loading new data into the remaining input register and strobing the output register.

Selection of Numeric Format

Essentially, the difference between integer, mixed and fractional notation in system design is only conceptual. For example, the TMC2208 does not differentiate between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the Least Significant Bits of the multiplier, multiplicand, and product all have the same value. If fractional notation is used, the Most Significant Bits of the multiplier, multiplicand, and product all have the same value. These formats are illustrated in detail in *Figures 1 through 4*.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2208J4C	STD – T_A = 0°C to 70°C	Commercial	48 Pin Hermetic Ceramic DIP	2208J4C
TMC2208J4V	EXT – T_C = –55°C to 125°C	MIL-STD-883C	48 Pin Hermetic Ceramic DIP	2208J4V
TMC2208N4C	STD – T_A = 0°C to 70°C	Commercial	48 Pin Plastic DIP	2208N4C
TMC2208R1C	STD – T_A = 0°C to 70°C	Commercial	68 Leaded Plastic Chip Carrier	2208R1C

TMC2210

CMOS Multiplier-Accumulator

16 x 16 Bit, 65, 80, 100, 160ns

The TMC2210 is a high-speed 16 x 16 bit digital multiplier-accumulator which is available in four speed bins of 65, 80, 100 or 160ns. Input data may be specified as two's complement or unsigned magnitude yielding a 32-bit product. Products may be accumulated to a 35-bit result.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are constructed using positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit Extended Product (XTP), a 16-bit Most Significant Product (MSP) and a 16-bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP and MSP. The LSP is multiplexed with the Y operand inputs. The output register can be preloaded directly via the output ports.

Built with TRW's OMICRON-C™ CMOS process, the TMC2210 is a drop in replacement for the TMC2010 and the TMC2110, and is pin and function compatible with the industry standard TDC1010 in DIP form and with the Analog Devices ADSP-1010 in the pin grid array.

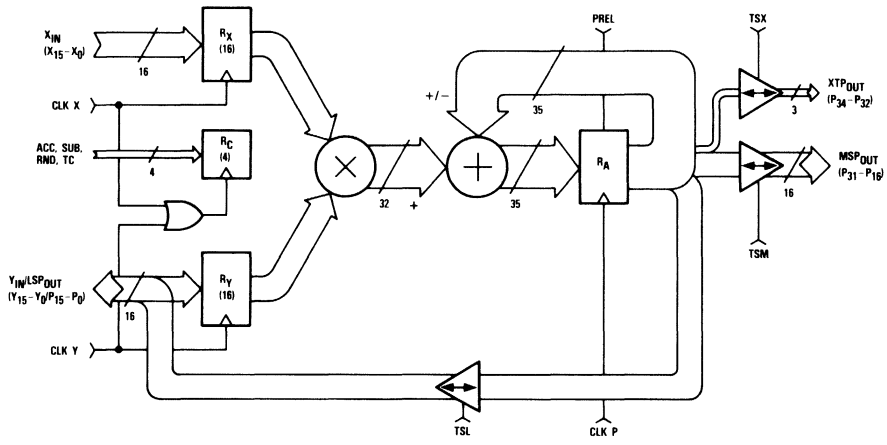
Features

- 65, 80, 100 Or 160ns Multiply-Accumulate Time
- 16 x 16 Bit Parallel Multiplication With Accumulation To 35-Bit Result
- Selectable Accumulation, Subtraction, Rounding And Preloading
- Two's Complement Or Unsigned Magnitude Operation
- All Inputs And Outputs Are Registered And TTL Compatible
- Low Power Consumption CMOS Process
- Single +5V Power Supply
- Available In A 64 Pin Ceramic Or Plastic DIP Or 68 Pin Grid Array

Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

Functional Block Diagram



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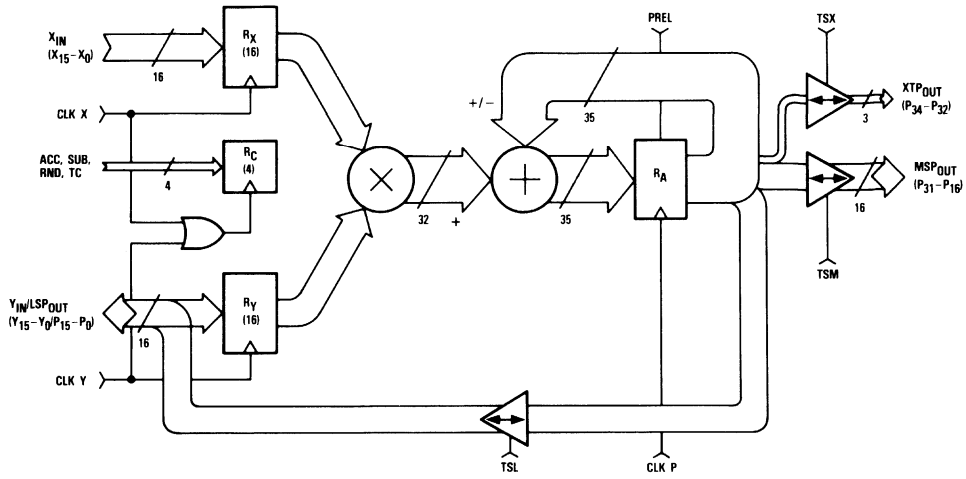
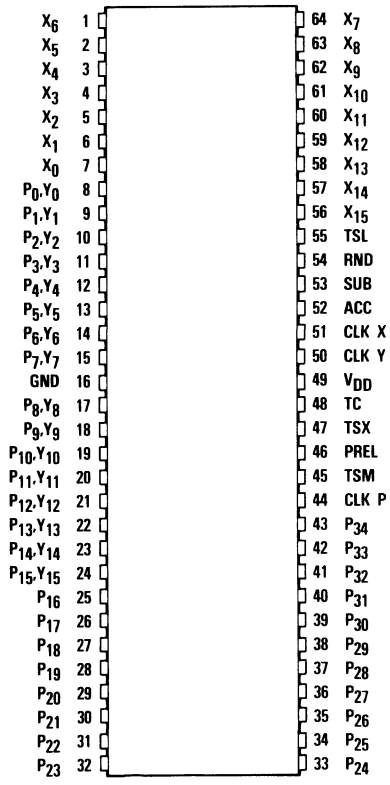
Printed in the U.S.A.

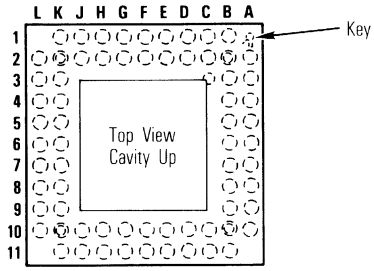
Functional Block Diagram



Pin Assignments



64 Lead DIP – J0, N0 Package



68 Pin Grid Array – G8 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B2	P_1,Y_1	K2	P_{16}	K10	P_{32}	B10	X_{14}
B1	P_2,Y_2	L2	P_{17}	K11	P_{33}	A10	X_{13}
C2	P_3,Y_3	K3	P_{18}	J10	P_{34}	B9	X_{12}
C1	P_4,Y_4	L3	P_{19}	J11	CLK P	A9	X_{11}
D2	P_5,Y_5	K4	P_{20}	H10	TSM	B8	X_{10}
D1	P_6,Y_6	L4	P_{21}	H11	PREL	A8	X_9
E2	P_7,Y_7	K5	P_{22}	G10	TSX	B7	X_8
E1	GND	L5	P_{23}	G11	TC	A7	X_7
F2	P_8,Y_8	K6	P_{24}	F10	V_{DD}	B6	X_6
F1	P_9,Y_9	L6	P_{25}	F11	CLK Y	A6	X_5
G2	P_{10},Y_{10}	K7	P_{26}	E10	CLK X	B5	X_4
G1	P_{11},Y_{11}	L7	P_{27}	E11	ACC	A5	X_3
H2	P_{12},Y_{12}	K8	P_{28}	D10	SUB	B4	X_2
H1	P_{13},Y_{13}	L8	P_{29}	D11	RND	A4	X_1
J2	P_{14},Y_{14}	K9	P_{30}	C10	TSL	B3	X_0
J1	P_{15},Y_{15}	L9	P_{31}	C11	X_{15}	A3	P_0,Y_0
K1	NC	L10	NC	B11	NC	A2	NC

Functional Description

General Information

The TMC2210 consists of four functional sections: input registers, an asynchronous multiplier array, an adder and output registers. The input registers store the two 16-bit numbers which are to be multiplied and the control lines which control the input numerical format (two's complement or unsigned magnitude), output rounding, accumulation and subtraction. The round control is used when a single-word output is desired. Each number is independently stored, simplifying multiplication by a constant. The output registers can be preloaded with a constant to provide the sum of products plus a constant. The asynchronous multiplier array uses a modified Booth's algorithm and has been designed to handle two's complement or unsigned magnitude numbers. The output registers hold the product as two 16-bit words and one 3-bit word: the MSP, the LSP and the XTP. Three-state output drivers permit the TMC2210 to be used on a bus or allow the outputs to be multiplexed over the same 16-bit output lines. The LSP is multiplexed with the Y input.

The TMC2210 has three clock lines, one for each of the input registers and one for the product register. Data present at the inputs of these registers are loaded into the registers on the rising edge of the appropriate clock. The Round (RND), Two's Complement (TC), Accumulate (ACC) and Subtract (SUB) inputs are registered and all four bits are clocked in on the rising edge of the logical OR of both CLK X and CLK Y. Problems with the loading of these four control signals can be avoided by the use of normally LOW clocks.

Signal Definitions

Power

V_{DD}, GND — The TMC2210 operates from a single +5 Volt supply. All power and ground lines must be connected.

Data Inputs

X_{15-0}, Y_{15-0} — There are two 16-bit two's complement or unsigned magnitude data inputs, labeled X and Y. The Most Significant Bits (MSBs), denoted X_{15} and Y_{15}, carry the sign information when two's complement notation is used. The remaining bits are denoted X_{14-0} and Y_{14-0} (with X_0 and Y_0 the Least Significant Bits). Data present at the X and Y inputs are clocked into the input registers on the rising edge of the appropriate clock.

Data Outputs

P_{34-0} — There is a 35-bit two's complement or unsigned magnitude result that is the sum of the products of the two input data values and the previous products which have been accumulated. The output is divided into two 16-bit output words, the MSP and LSP, and one 3-bit output word, the XTP. The MSB of the XTP is the sign bit if two's complement notation is used.

Clocks

CLK X — CLK X is the clock input for the X_{15-0} data register.

CLK Y — CLK Y is the clock input for the Y_{15-0} data register.

CLK P — CLK P is the clock input for the product register.

Controls

TSX, TSM, TSL — TSX, TSM and TSL are three-state enable lines for the XTP, the MSP and the LSP, respectively. The output driver is in the high-impedance state when TSX, TSM or TSL is HIGH and enabled when the appropriate control is LOW.

PREL — PREL (Preload) is an active HIGH control which has several effects when active. First, all output buffers are forced into the high-impedance state. Second, when any or all of TSX, TSM and TSL are also HIGH, external data present at the output pins will be preloaded into the corresponding section of the output register on the rising edge of CLK P. Normal data setup and hold times apply both to the logical AND of PREL and the relevant three-state control (TSX, TSM, TSL) and to the data being preloaded. These setup and hold times are with respect to the rising edge of CLK P.

RND — RND (Round) controls the addition of a one to the MSB of the LSP for rounding. When RND is HIGH, a one is added to the MSB of the LSP for rounding the product in the MSP and XTP (if appropriate) rather than truncating.

TC — TC (Two's Complement) controls how the device interprets data on the X and Y inputs. When TC is HIGH, both inputs are two's complement inputs. When TC is LOW, both inputs are unsigned magnitude only inputs. The necessary sign extension for negative two's complement numbers is provided internally.

ACC — When ACC (Accumulate) is HIGH, the content of the output register is added to or subtracted from the next product generated, and the result is stored back into the output registers on the next rising edge of CLK P. When ACC is LOW, multiplication without accumulation is performed, and the next product generated will be stored into the output registers directly. This operation is used for the first term in a summation to eliminate the need for a separate "clear" operation.

SUB — The SUB (Subtract) control is used in conjunction with the ACC control. When both the ACC and SUB controls are HIGH, the content of the output register is subtracted from the next product generated, and the difference is stored back into the output register. When ACC is HIGH and SUB is LOW, the content of the output register is added to the next product generated and the sum is stored back into the output register. Note that the previous output is subtracted from the product, not the product from the previous output.

No Connects

NC — The pin grid array version of the TMC2210 has four pins which are not connected internally.

Package Interconnections

Signal Type	Signal Name	Function	J0, N0 Package	G8 Package
Power	V_{DD}	Supply Voltage	49	F10
	GND	Ground	16	E1
Data Inputs	X_{15-0}	X Input Word	56-64, 1-7	C11, B10, A10, B9, A9, B8, A8, B7, A7, B6, A6, B5, A5, B4, A4, B3
	Y_{15-0}	Y Input Word	24-17, 15-8	J1, J2, H1, H2, G1, G2, F1, F2, E2, D1, D2, C1, C2, B1, B2, A3
Data Outputs	P_{34-0}	Product Output	43-17, 15-8	J10, K11, K10, L9, K9, L8, K8, L7, K7, L6, K6, L5, K5, L4, K4, L3, K3, L2, K2, J1, J2, H1, H2, G1, G2, F1, F2, E2, D1, D2, C1, C2, B1, B2, A3
Clocks	CLK X	X Register Clock	51	E10
	CLK Y	Y Register Clock	50	F11
	CLK P	P Register Clock	44	J11
Controls	TSX	XTP Three-state	47	G10
	TSM	MSP Three-state	45	H10
	TSL	LSP Three-state	55	C10
	PREL	Preload	46	H11
	RND	Round	54	D11
	TC	Two's Complement	48	G11
	ACC	Accumulate	52	E11
	SUB	Subtract	53	D10
No Connects	NC	No Connection	-	K1, L10, B11, A2

Application Discussion

Multiplication By A Constant

Multiplication by a constant requires that the constant be loaded into the desired input register and that the register not be loaded again until a new constant is desired. The multiply cycle then consists of loading new data and strobing the output register.

Selection Of Numeric Format

Essentially, the difference between integer, mixed and fractional notation in system design is only conceptual. For example, there is no differentiation between this operation:

$$6 \times 2 = 12$$

and this operation:

$$(6/8) \times (2/8) = 12/64.$$

The difference lies only in constant scale factors (in this case, a factor of 8 in the multiplier and multiplicand and a factor of 64 in the product). However, these scale factors do have implications for hardware design. Because common good design practice assigns a fixed value to any given line (and input and output signals often share the same line), the scale factors determine the connection of the output pins of any multiplier in a system. As a result, only two choices are normally made: integer and fractional notation. If integer notation is used, the LSBs of the multiplier, multiplicand and product all have the same value. If fractional notation is used, the MSBs of the multiplier, multiplicand and product all have the same value.

Figure 1. Fractional Two's Complement Notation

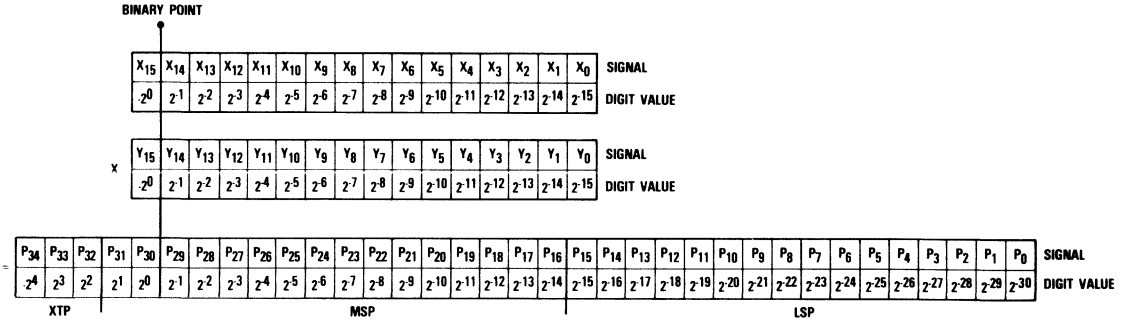


Figure 2. Fractional Unsigned Magnitude Notation

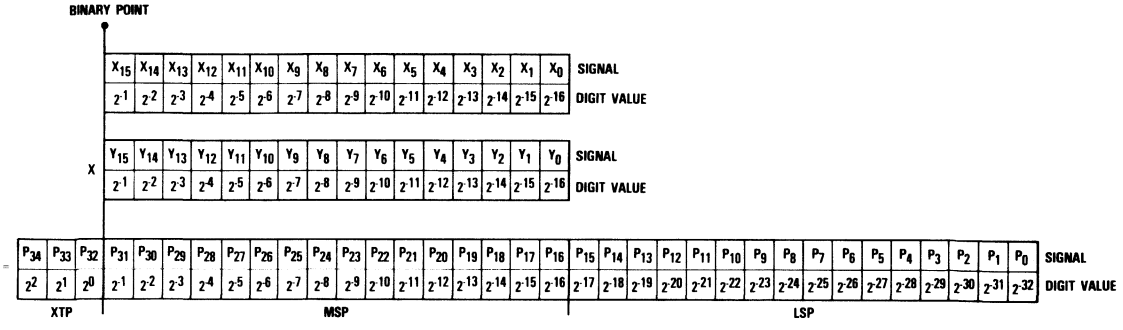


Figure 3. Integer Two's Complement Notation

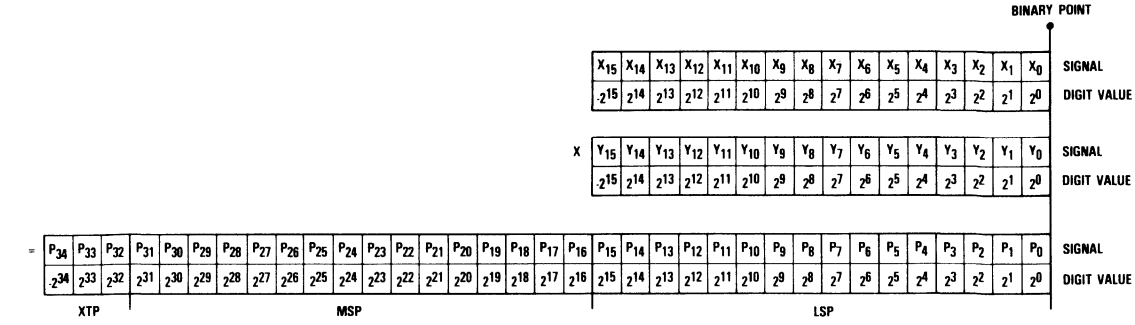


Figure 4. Integer Unsigned Magnitude Notation

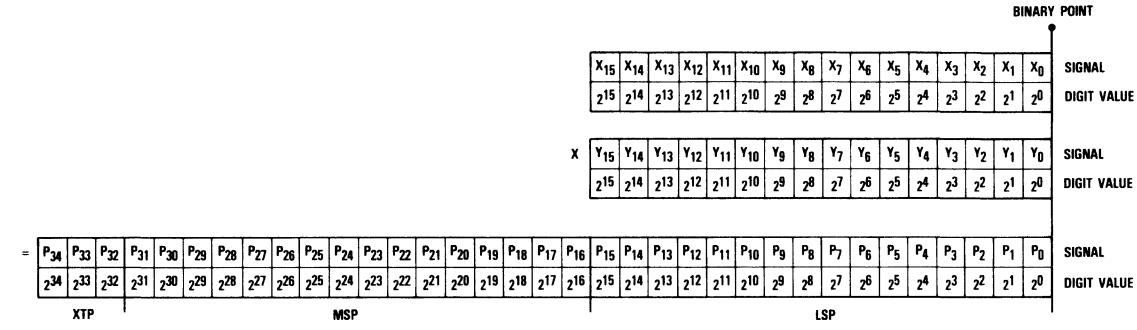
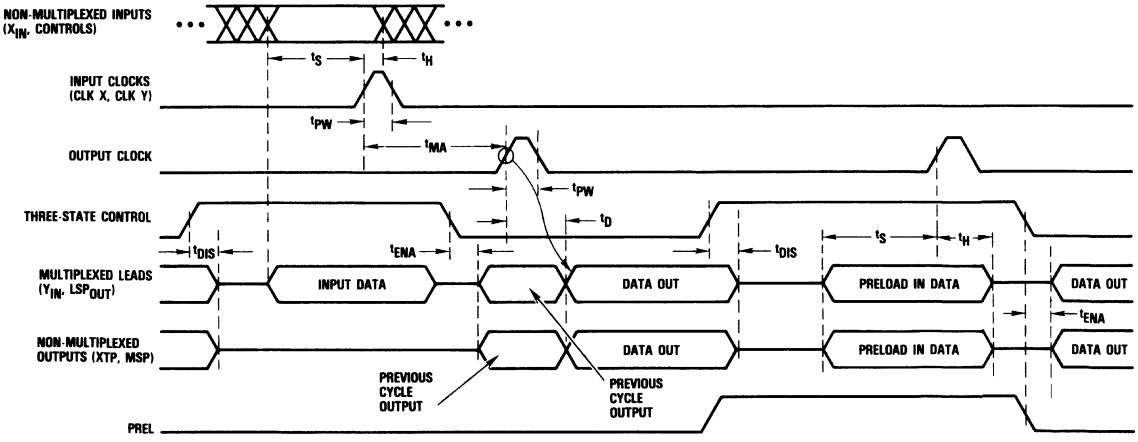


Figure 5. Timing Diagram



Note: On multiplexed leads, input data and preload in data are applied to the TMC2210, and data out is produced and driven by the TMC2210.

Figure 6. Equivalent Input Circuit

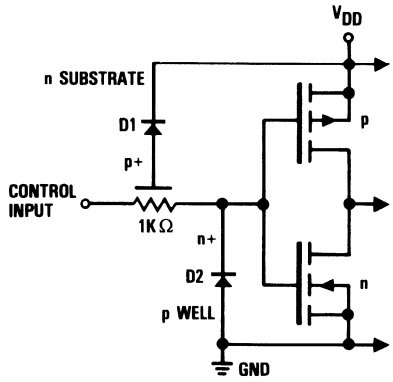


Figure 7. Equivalent Output Circuit

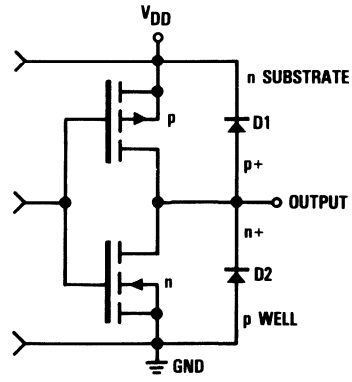
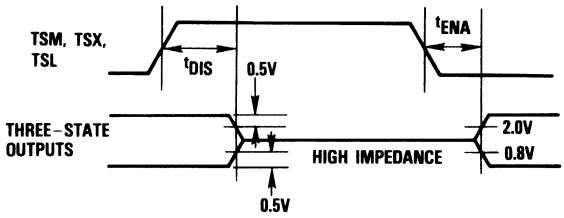


Figure 8. Threshold Levels for Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	-0.5 to +7.0V
Input Voltage	-0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage [2]	-0.5 to (V_{DD} + 0.5)V
Forced current [3,4]	-1.0 to 6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	-60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	-65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			-2.0			-2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				-55		125	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		5		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, TSL, TSM, TSX = 5V					
		f = 15MHz		75		75	mA
		f = 10MHz		50		50	mA
		f = 6.2MHz		30		30	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V					
		X_{15-0}, Controls, CLKs		-10		-10	μA
		P_{15-0}, Y_{15-0}		-40		-40	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}					
		X_{15-0}, Controls, CLKs		10		10	μA
		P_{15-0}, Y_{15-0}		40		40	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		-40		-40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		-100		-100	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note:

1. Actual test conditions may vary from those shown, but guarantee operation as specified.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range												Units
			-1								-2		-3		
			Standard		Extended		Standard		Extended		Standard		Standard		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{MA}	Multiply-Accumulate Time	V_{DD} = Min		65		80		80		100		100		160	ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD} = Min	15		15		15		15		25		25		ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD} = Min	15		15		15		15		25		25		ns
t_S	Input Setup Time	Data, ACC, SUB, RND, TC	15		20		20		20		25		25		ns
		PREL, TSL, TSM, TSX	30		30		30		30		30		30		ns
t_H	Input Hold Time	Data, ACC, SUB, RND, TC	0		0		0		0		0		3		ns
		PREL, TSL, TSM, TSX	3		3		3		3		3		3		ns
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		35		35		40		40		35		45	ns
t_{ENA}	Three-State Output Enable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF		30		35		35		40		30		40	ns
t_{DIS}	Three-State Output Disable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF		30		30		35		35		30		35	ns

Note:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Preload Truth Table

PREL [1,2]	TSX [1]	TSM [1]	TSL [1]	XTP	MSP	LSP
0	0	0	0	Register → Output Pin	Register → Output Pin	Register → Output Pin
0	0	0	1	Register → Output Pin	Register → Output Pin	Hi-Z
0	0	1	0	Register → Output Pin	Hi-Z	Register → Output Pin
0	0	1	1	Register → Output Pin	Hi-Z	Hi-Z
0	1	0	0	Hi-Z	Register → Output Pin	Register → Output Pin
0	1	0	1	Hi-Z	Register → Output Pin	Hi-Z
0	1	1	0	Hi-Z	Hi-Z	Register → Output Pin
0	1	1	1	Hi-Z	Hi-Z	Hi-Z
1	0	0	0	Hi-Z	Hi-Z	Hi-Z
1	0	0	1	Hi-Z	Hi-Z	Hi-Z Preload
1	0	1	0	Hi-Z	Hi-Z Preload	Hi-Z
1	0	1	1	Hi-Z	Hi-Z Preload	Hi-Z Preload
1	1	0	0	Hi-Z Preload	Hi-Z	Hi-Z
1	1	0	1	Hi-Z Preload	Hi-Z	Hi-Z Preload
1	1	1	0	Hi-Z Preload	Hi-Z Preload	Hi-Z
1	1	1	1	Hi-Z Preload	Hi-Z Preload	Hi-Z Preload

Notes: 1. PREL, TSX, TSM and TSL are not registered.
2. When PREL is HIGH, any change of output register (for those outputs in which the three-state control is LOW) is inhibited.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2210G8C	STD – T_A = 0°C to 70°C	Commercial	68 Pin Grid Array	2210G8C
TMC2210G8C1	STD – T_A = 0°C to 70°C	Commercial	68 Pin Grid Array	2210G8C1
TMC2210G8V	EXT – T_C = –55°C to 125°C	MIL-STD-883	68 Pin Grid Array	2210G8V
TMC2210G8V1	EXT – T_C = –55°C to 125°C	MIL-STD-883	68 Pin Grid Array	2210G8V1
TMC2210J0V	EXT – T_C = –55°C to 125°C	MIL-STD-883	64 Pin Hermetic Ceramic DIP	2210J0V
TMC2210J0V1	EXT – T_C = –55°C to 125°C	MIL-STD-883	64 Pin Hermetic Ceramic DIP	2210J0V1
TMC2210N0C	STD – T_A = 0°C to 70°C	Commercial	64 Pin Plastic DIP	2210N0C
TMC2210N0C1	STD – T_A = 0°C to 70°C	Commercial	64 Pin Plastic DIP	2210N0C1
TMC2210N0C2	STD – T_A = 0°C to 70°C	Commercial	64 Pin Plastic DIP	2210N0C2
TMC2210N0C3	STD – T_A = 0°C to 70°C	Commercial	64 Pin Plastic DIP	2210N0C3

TMC3211

Integer Divider
32-Bit, 20 MOPS

The TMC3211 is a fast monolithic two's complement integer divider which can divide a 32-bit dividend by a 16-bit divisor to produce a 32-bit quotient, with a maximum pipelined throughput of 20 MOPS (Million Operations Per Second). Data is input on separate busses, and quotients are available on a 32-bit output bus with synchronous three-state enable. All data inputs and outputs are registered and TTL compatible. All input and output signal timing is referenced to the rising edge of Clock.

The TMC3211 has a single system clock and separate load enable controls for the dividend and divisor registers. This allows the device to be used in applications requiring division by a constant. Underflow automatically produces the expected zero quotient, and dividing by zero sets a divide-by-zero output flag.

The internal architecture of the TMC3211 allows all 32-bit two's complement integer dividends and nonzero 16-bit two's complement integer divisors, without prenormalization. The output quotient format is 32-bit integer.

The TMC3211 makes a full-precision, full-speed divide function available to designers of Workstations, Image Processors, and Radar Systems who need to perform perspective extractions, matrix operations, range scaling, and other complex functions.

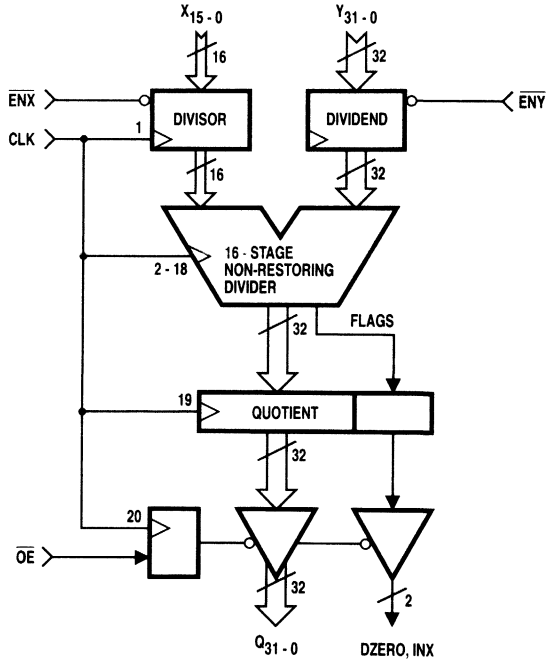
Features

- 32-Bit By 16-Bit Fixed-Point Integer Division With 32-Bit Quotient
- 20MHz Clock Rate And Pipelined Throughput Rate
- Three-Bus I/O Architecture Allows Unrestricted Throughput
- Easy System Interfacing
- Status Flags For Divide-By-Zero And Inexact Result
- All Inputs And Outputs TTL Compatible
- Low Power CMOS Technology
- Available In A 120 Pin Plastic Pin Grid Array Package

Applications

- Graphics And Image Processors
- Matrix Operations And Geometric Transforms
- Perspective Extraction
- Radar Signal Processing
- Range Scaling

Functional Block Diagram



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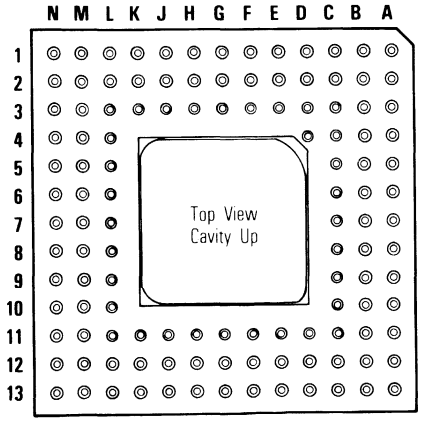
40G05579 Rev. C – 11/90
Printed in the U.S.A.

Pin Assignments

120-Pin Plastic Pin Grid Array – H5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
C3	V_{DD}	L3	GND	L11	V_{DD}	C11	GND
B2	Y_{15}	M2	X_0	M12	GND	B12	Q_7
B1	$\overline{YEN}$	N2	X_1	M13	Q_{25}	A12	Q_6
D3	GND	L4	V_{DD}	K11	V_{DD}	C10	Q_5
C2	V_{DD}	M3	X_2	L12	GND	B11	Q_4
C1	Y_{16}	N3	X_3	L13	Q_{24}	A11	Q_3
D2	Y_{17}	M4	X_4	K12	Q_{23}	B10	Q_2
E3	GND	L5	GND	J11	V_{DD}	C9	Q_1
D1	Y_{18}	N4	X_5	K13	Q_{22}	A10	Q_0
E2	Y_{19}	M5	X_6	J12	Q_{21}	B9	DZ
E1	Y_{20}	N5	X_7	J13	Q_{20}	A9	REM
F3	V_{DD}	L6	X_8	H11	GND	C8	Y_0
F2	Y_{21}	M6	X_9	H12	Q_{19}	B8	Y_1
F1	Y_{22}	N6	X_{10}	H13	Q_{18}	A8	Y_2
G2	GND	M7	X_{11}	G12	V_{DD}	B7	Y_3
G3	V_{DD}	L7	V_{DD}	G11	Q_{17}	C7	Y_4
G1	Y_{23}	N7	X_{12}	G13	Q_{16}	A7	Y_5
H1	Y_{24}	N8	X_{13}	F13	Q_{15}	A6	Y_6
H2	Y_{25}	M8	X_{14}	F12	Q_{14}	B6	Y_7
H3	GND	L8	X_{15}	F11	V_{DD}	C6	Y_8
J1	Y_{26}	N9	$\overline{XEN}$	E13	Q_{13}	A5	Y_9
J2	Y_{27}	M9	CLK	E12	Q_{12}	B5	Y_{10}
K1	Y_{28}	N10	$\overline{OEQ}$	D13	Q_{11}	A4	V_{DD}
J3	V_{DD}	L9	Q_{31}	E11	GND	C5	Y_{11}
K2	Y_{29}	M10	Q_{30}	D12	Q_{10}	B4	Y_{12}
L1	Y_{30}	N11	Q_{29}	C13	Q_9	A3	Y_{13}
M1	Y_{31}	N12	Q_{28}	B13	Q_8	A2	Y_{14}
K3	GND	L10	Q_{27}	D11	V_{DD}	C4	GND
L2	V_{DD}	M11	GND	C12	GND	B3	V_{DD}
N1	GND	N13	Q_{26}	A13	V_{DD}	A1	GND



Functional Description

General Information

The TMC3211 consists of input registers, a pipelined array divider, and output (quotient) registers. The 16-bit divisor and 32-bit dividend input registers can each be loaded independently using the two synchronous load enable controls. The divider is a 16-stage pipelined non-restoring array which produces a 32-bit quotient and condition flags which indicate an attempted division by zero, or operations which yield a non-zero remainder or inexact result. The 32-bit parallel quotient output register includes three-state output drivers with synchronous enable control, which permits multiple TMC3211s to be operated in parallel or connected directly to a system bus.

The TMC3211 requires a total of 19 clock cycles to generate a full 32-bit quotient result. Once the internal pipeline is full, a new quotient is available at the output every clock cycle.

Signal Definitions

Power

V_{DD}, GND — The TMC3211 operates on a single +5V supply. All power and ground lines must be connected.

Clock

CLK — The TMC3211 has a single Clock input. All input and output signal timing is referenced to the rising edge of Clock.

Inputs

Y_{31-0} — The 32-bit Dividend is presented through the registered Y input port. Y_{31} is the sign bit. The LSB is Y_0.

X_{15-0} — The 16-bit Divisor is presented through the registered X input port. X_{15} is the sign bit. The LSB is X_0.

Outputs

Q_{31-0} — The current Quotient is available on the registered Q output bus. Q_{31} is the sign bit. The LSB is Q_0.

Controls

$\overline{YEN}$ — Data present at the Dividend input Y_{31-0} is latched into the input registers on the rising edge of clock when the enable control $\overline{YEN}$ is LOW.

$\overline{XEN}$ — Data present at the Divisor input X_{15-0} is latched into the input registers on the rising edge of clock when the enable control $\overline{XEN}$ is LOW.

$\overline{OEQ}$ — The quotient output bus Q_{31-0} and flags DZ and REM are in the high-impedance state when the registered Output Enable $\overline{OEQ}$ is HIGH. When $\overline{OEQ}$ is LOW, they are enabled on the next clock cycle.

Flags

DZ — Whenever a zero divisor is input, the resulting invalid output quotient will be accompanied by a registered Divide-By-Zero Flag HIGH.

REM — Whenever a division operation leaves a nonzero remainder, the resulting quotient is accompanied by a registered nonzero Remainder Flag HIGH.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package
Power	V_{DD}	Supply Voltage	B3, A4, A13, D11, F11, G12, J11, K11, L11, L7, L4, L2, J3, G3, F3, C2, C3
	GND	Ground	A1, C4, C11, C12, E11, H11, L12, M12, M11, L5, L3, N1, K3, H3, G2, E3, D3
Clock	CLK	System Clock	M9
Inputs	Y_{31-0}	Dividend Data	M1, L1, K2, K1, J2, J1, H2, H1, G1, F1, F2, E1, E2, D1, D2, C1, B2, A2, A3, B4, C5, B5, A5, C6, B6, A6, A7, C7, B7, A8, B8, C8
	X_{15-0}	Divisor Data	L8, M8, N8, N7, M7, N6, M6, L6, N5, M5, N4, M4, N3, M3, N2, M2
Outputs	Q_{31-0}	Quotient Data	L9, M10, N11, N12, L10, N13, M13, L13, K12, K13, J12, J13, H12, H13, G11, G13, F13, F12, E13, E12, D13, D12, C13, B13, B12, A12, C10, B11, A11, B10, C9, A10
Controls	$\overline{YEN}$	Dividend Write Enable	B1
	$\overline{XEN}$	Divisor Write Enable	N9
	$\overline{OEQ}$	Quotient Output Enable	N10
Flags	DZ	Divide-By Zero Flag	B9
	REM	Inexact Remainder Flag	A9
No Connect		Index Pin	D4

Applications Discussion

Division Using A Constant

By utilizing the separate input data register load enable controls, the TMC3211 can perform division by a constant. The data currently held remain in the input registers until updated by the user.

Data Formats

The TMC3211 supports fixed-point two's complement data formats. By keeping track of the binary points of the input data, the user can then interpret the resulting quotient properly. Two possible binary weightings of the input and output bits are as follows:

Figure 1. Integer Data Format

Pin	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Y	-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X																	-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
Q	-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Figure 2. Fractional Data Format

Y	-2^{0}	$\bullet 2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}
X																	-2^{0}	$\bullet 2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
Q	-2^{15}	$\bullet 2^{14}$	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

where a leading minus sign indicates a sign bit.

Care must be taken when adopting fractional data formats. By observing the binary weighting applied to the input data in the dividend and divisor, the binary point of the quotient can then be correctly established. The difference lies only in constant scale factors, which must be considered in order to maintain a data format which is compatible with the bit weighting of the hardware system. The two most common choices are fractional and integer notation. If integer notation is used, the LSBs of the dividend, divisor, and quotient all have the same value. With fractional notation the MSBs are all of equal weight.

Divide by Zero

The flag DZ indicates that the divisor input for the current calculation was a zero, independent of the dividend. Dividing by zero is an undefined operation yielding a meaningless quotient. Thus, this flag must be monitored to guard against possible errors.

Inexact Results

The flag REM is provided to indicate that the current quotient left a nonzero remainder and was truncated toward zero.

Negative Full-Scale Overflow

Due to a finite data word width, a two's complement overflow error occurs under the following unique condition:

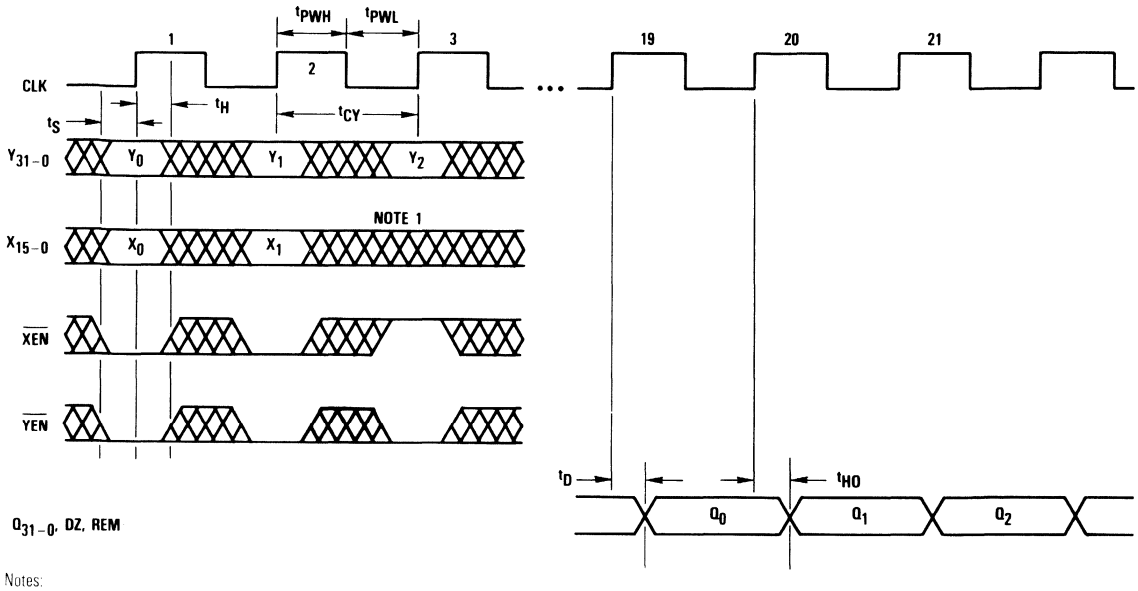
Divisor $Y = 80000000_H$ (−Full-Scale)
Dividend $X = FFFF_H$ (−1)

Result:

Quotient $Q = 80000000_H$ (−Full-Scale)

As stated above, this is due to a limitation in the number of bits available to indicate a positive full-scale quotient, and data overflows into the MSB position to indicate an incorrect sign.

Figure 3. Timing Diagram



Notes:

1. Demonstrates division by a constant, $Q_2 = Y_2/X_1$.
2. Assumes $\overline{OEQ}$ = LOW.

Figure 4. Equivalent Input Circuit

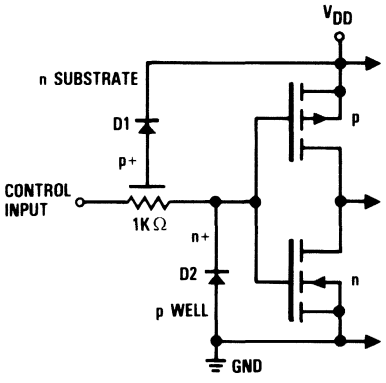
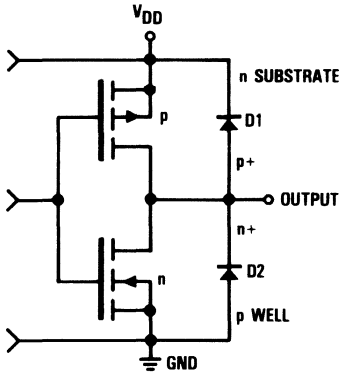


Figure 5. Equivalent Output Circuit



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage [2]	−0.5 to (V_{DD} + 0.5)V
Forced current [3,4]	−3.0 to 6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Nom	Standard Max	Units
V_{DD}	Supply Voltage		4.75	5.0	5.25	V
V_{IL}	Input Voltage, Logic LOW				0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0			V
I_{OL}	Output Current, Logic LOW				4.0	mA
I_{OH}	Output Current, Logic HIGH				−2.0	mA
t_{CY}	Cycle Time	V_{DD} = Min			50	ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD} = Min	15			ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD} = Min	15			ns
t_S	Input Setup Time		12			ns
t_H	Input Hold Time		6			ns
T_A	Ambient Temperature, Still Air		0		70	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range: Standard Min	Temperature Range: Standard Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		5	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, $\overline{OEQ}$ = 5V, f = 20MHz		150	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		−10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		−40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		−150	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10	pF

Note: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Temperature Range: Standard Max	Units
t_D	Output Delay [1]	V_{DD} = Min, C_{LOAD} = 25pF		35	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 25pF	5		ns

Note: 1. Equivalent to t_{DIS} and t_{ENA} of the three-state outputs.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC3211H5C	STD − T_A = 0°C to 70°C	Commercial	120 Pin Plastic Pin Grid Array	3211H5C

Floating-Point Arithmetic

Fixed-point digital signal processor design requires careful attention to dynamic range, limit cycles, and overflow conditions. Block floating-point is often used to extend the dynamic range, but it carries with it significant bookkeeping overhead.

TRW offers a broad line of floating point processors, designed to implement signal processing algorithms or accelerate computers doing floating-point arithmetic. These devices differ from the well-know floating-point accelerators used with standard microprocessors (ie., the 80387). The TRW products implement a limited instruction set (often no more than add, multiply, and/or divide), and execute them much faster than the generic floating-point acclerator. These chips are clearly targeted at signal processing applications.

TRW's processors comply with the IEEE 754 standard floating-point arithmetic format. Addition/ subtraction, multiplication, and division are supported. For systems requiring compliance with MIL-STD-1750 format, the TMC3202 provides addition, subtraction, and multiplication.

Floating-Point Arithmetic

Product	Description	Size	Clock Rate [1] (MHz)	Power [1] (Watts)	Package		Grades [2]	Notes	Page
TMC3032-1	Floating-Point Multiplier	32-Bit	10	0.21	J3	64 Pin DIP	C	IEEE-754 Format.	J3
					A1	68 Contact CC	C		
-			8	0.21	J3	64 Pin DIP	C, V		
					A1	68 Contact CC	C		
TMC3033-1	Floating-Point ALU	32-Bit	10	0.21	J3	64 Pin DIP	C	IEEE-754 Format.	J3
					A1	68 Contact CC	C		
-			8	0.21	J3	64 Pin DIP	C, V		
					A1	68 Contact CC	C		
TMC3200	Floating-Point Multiplier	32/34-Bit	10	0.16	G5	89 Pin PGA	C, A	IEEE-754 w/Internal Accumulate.	J3
TMC3201	Floating-Point ALU	32/34-Bit	8	0.16	G5	89 Pin PGA	C, A	IEEE-754 w/Three Port I/O.	J17
TMC3202	1750A Accelerator	32-Bit	16	0.3	L3	84 Lead CC	C, V	8MFLOP, MIL-STD-1750A.	J39
TMC3210	Floating-Point Divider	32-Bit	20	0.3	J4	48 Pin DIP	C, V	2.5MFLOP, IEEE-754 Format.	J57

Notes: 1. Guaranteed. See product specifications for test conditions.

2. A = High Reliability, $T_C = -55°C$ to $125°C$.
C = Commercial, $T_A = 0°C$ to $70°C$.
V = MIL-STD-883 Compliant, $T_C = -55°C$ to $125°C$

TMC3032/3033

Floating-Point Multiplier and ALU

32-Bit, 10 Megaflops

The TMC3032 and TMC3033 are form, fit, and function compatible with the WTL1032 and WTL1033. Since the TMC3032 and TMC3033 are built using TRW's OMICRON-C™ one micron CMOS process, power consumption is greatly reduced. Power supply considerations are also eased by the requirement for only a single (+5V) supply voltage.

The TMC3032 is a digital multiplier which provides the product of two normalized floating point numbers. These numbers are expressed in the 32-bit single-precision format of the IEEE Standard 754, Version 8.0 or 10.0. When the three internal pipeline registers are enabled, the data throughput rate of the TMC3032-1 is 10 Megaflops (Million floating point operations per second). With the pipeline registers disabled, the TMC3032-1 runs at 3 Megaflops. The TMC3032 (like the WTL1032) operates from a single clock.

The TMC3033 is an arithmetic unit which adds, subtracts, and compares floating point numbers expressed in the 32-bit single-precision format of the IEEE Standard 754. It can also convert between floating point and a 24-bit two's complement integer fixed point representation. When the three internal pipeline registers are enabled, the data throughput rate of the TMC3033-1 is 10 Megaflops. With the pipeline registers disabled, the TMC3033-1 runs at 3 Megaflops. The TMC3033 (like the WTL1033) operates from a single clock.

All data and instruction inputs are registered. Each input operand enters on a half-width bus on two successive rising edges of the clock when enabled by the LOAD controls. The synchronous UNLOAD controls enable or disable the three-state output buffers and select the most or least significant output word.

Instruction and mode registers hold data format and rounding control signals. Renormalizing, rounding, and limiting logic ensure proper handling of special cases and correct output data formatting.

Features

- Exact Replacements For WTL1032 And WTL1033
- Low-Power CMOS Construction, Single +5V Power Supply Operation
- 10 Megaflop Throughput Rate With The TMC3032-1 And TMC3033-1
- Six Additional Functional Instructions Over The WTL1033 (TMC3033)
- Complete IEEE Compare And Compare Magnitude Functions (TMC3033)
- Conforms To IEEE Standard 754 Version 8.0 Or 10.0
- Available In Commercial And Military Grades

Applications

- Matrix Operations And Geometric Transforms
- Arithmetic Section In Microprogrammed Array Processor
- Arithmetic Element In Systolic Processor
- Graphics And Image Processing
- Floating Point Digital Filters And FFTs
- Radar And Sonar Signal Processor
- Arithmetic Co-Processor
- Solids Modeling

J

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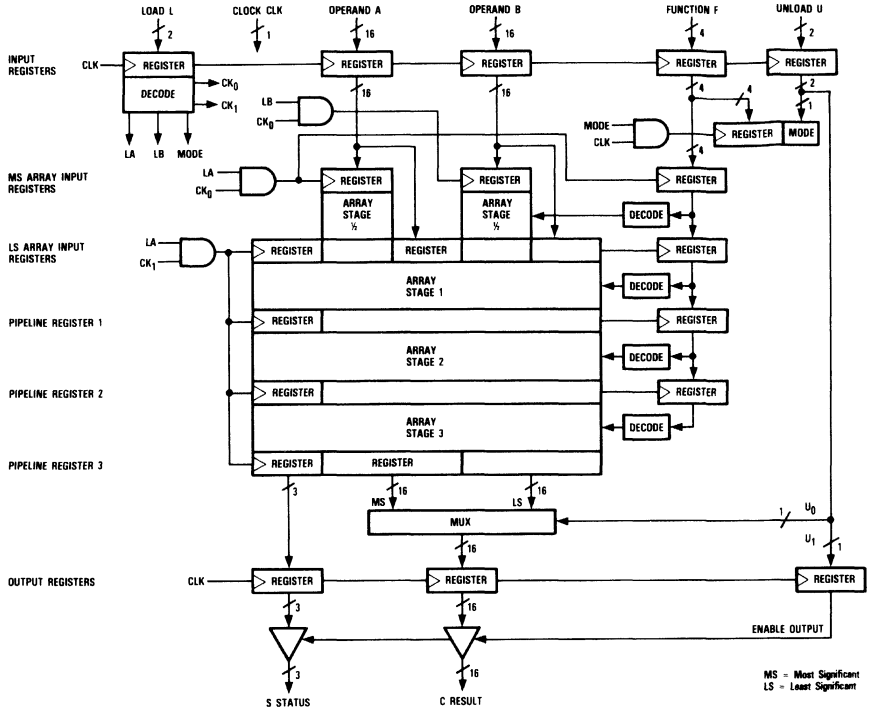
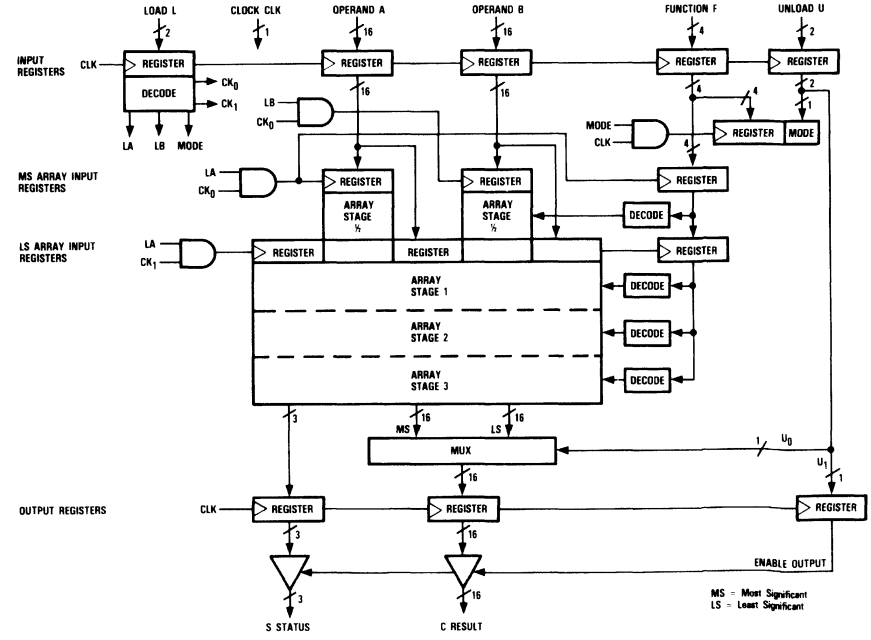
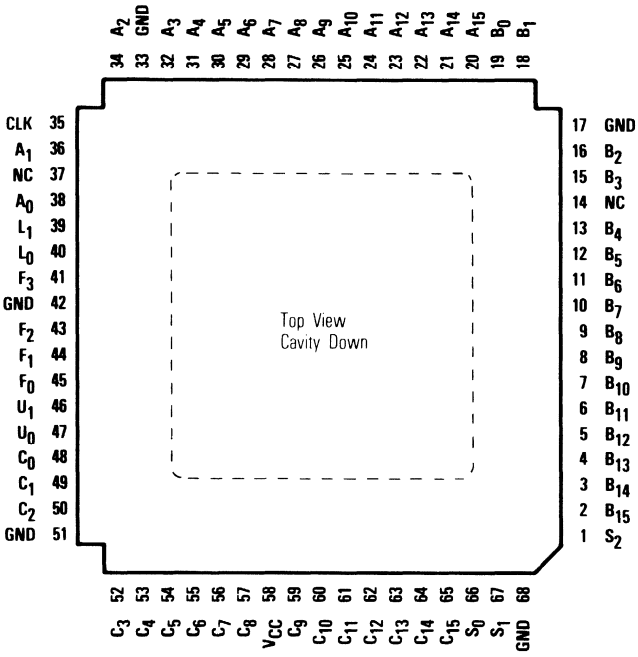
Block Diagram Pipeline Operation



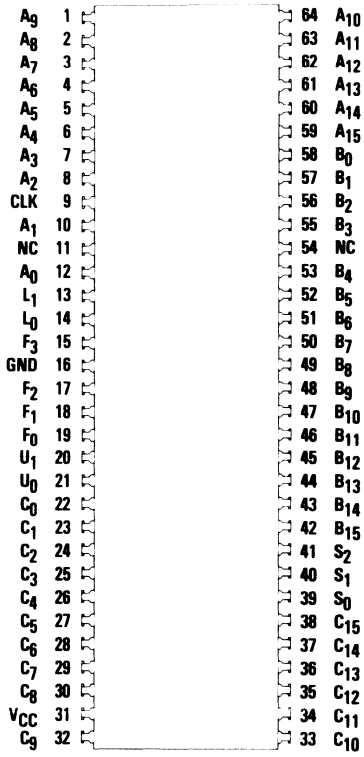
Block Diagram Flowthrough Operation



Pin Assignments



68 Contact Chip Carrier – A1 Package



64 Lead DIP – J3 Package

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Functional Description

TMC3032

The TMC3032 consists of four sections: the input stage, the significand multiplier/exponent adder, the renormalize/round/limit block and the output stage.

The input stage accepts instructions for loading data, unloading (outputting) data, and performing operations. It consists of five registers (L, A, B, F, and U) and control/sequencing logic to permit the controlled multiplexing of inputs to the proper destinations.

The multiplier/adder multiplies the significands and adds the exponents to produce a "raw" (possibly unnormalized) result.

If the significand emerging from the multiplier/adder overflows, the renormalizer right shifts the significand and increments the exponent. The rounder performs the selected rounding operation. The limiter replaces overflowing results with a properly signed infinity or maximum normalized value according to IEEE convention. In FAST mode, underflowing results are replaced with zero. In IEEE mode, they are output in wrapped format with the Underflow or Underflow/Inexact flag.

The output stage consists of registers which are loaded under the control of Unload Control U_0, and three-state output drivers which are enabled and disabled by Unload Control U_1.

TMC3033

The TMC3033 consists of five sections: the input stage, the denormalizer, the arithmetic unit, the renormalize/round/limit block and the output stage.

The input stage accepts instructions for loading data, unloading (outputting) data, and performing operations. It consists of five registers (L, A, B, F and U) and control/sequencing logic to permit the controlled multiplexing of inputs to the proper destinations.

The denormalizer shifts the smaller exponent's significand rightward. This section also executes the "UNWRAP A" and "FIX A" functions.

The arithmetic unit adds or subtracts the two significands.

The renormalize/round/limit block shifts the significand as required to produce the IEEE specified normalized or denormalized result. Rounding is then performed in this section. Finally, the results are limited according to IEEE conventions to eliminate overflow and improper handling of underflows.

The output stage consists of registers which are loaded by U_0, and three-state output drivers which are enabled and disabled by the U_1.

The TMC3033 arithmetic unit conforms to IEEE Standard 754, Version 8.0 or 10.0 data format for standard 32-bit arithmetic. The TMC3033 arithmetic unit needs two clock cycles to transfer any input or output data word, since the input and output buses are 16 bits wide.

Power

The TMC3032 and TMC3033 operate from a single +5 Volt supply. The TMC3032 and TMC3033 do not require a 3 Volt supply on the V_{DD} pins. These pins (11, 54) are not connected and permit operation in sockets wired for the WTL1032 and WTL1033.

Clock

The TMC3032 and TMC3033 operate on a single, TTL-compatible clock, CLK. All data are loaded into the appropriate registers on the rising edge of CLK as controlled by the LOAD, FUNCTION and UNLOAD commands.

Data Inputs

The TMC3032 and TMC3033 have two 16-bit multiplexed input data buses, A_{15-0} and B_{15-0}. The Most Significant Word (MSW) is loaded on the rising edge of CLK which follows the assertion of a LOAD instruction, LA or LAB. The Least Significant Word (LSW) is loaded on the next rising edge of CLK following the loading of the MSW. If the load instructions are not changed, consecutive rising edges of CLK will load alternating MSWs and LSWs continuously.

Data Outputs

The TMC3032 and TMC3033 have a single, 16-bit multiplexed output bus with three-state output drivers. The loading of the output register is controlled by the U_0 instruction. Three-state enable/disable is synchronous and is controlled by the U_1 instruction.

Controls

The load controls, L_0 and L_1, determine how data are transferred into the data input registers, A and B, and the mode control register. The load controls are read on every rising edge of CLK. All data transfers into the A, B and mode registers take place on the rising edge of CLK following the load controls commanding the data transfer. Since two consecutive clock cycles are required to load A or B operands into the data input registers, L_0 and L_1 must be valid for two consecutive clock cycles.

Unload control U_0 determines how data is transferred into the output registers. U_1 controls the enabling and disabling of the three-state output drivers. The unload controls are read on the rising edge of CLK. The state of the output drivers will change after the next rising edge of CLK following the loading of a DAB or ENB instruction on U_1. Therefore, two CLK cycles are required to enable or disable the three-state drivers.

The dual-purpose function controls F_{3-0} and U_0 select the operational mode (flow-through or pipeline), the rounding and underflow modes, and the input data formats (normalized or wrapped). The mode controls are read on the rising edge of CLK following an LMODE instruction.

Status Outputs

The TMC3032 and TMC3033 have three pins which indicate the presence of exception conditions in the result in the data output register. These flags are valid while both the MSW and the LSW are unloaded. Note that these pins are three-state under the control of the U_1 input. If the magnitude of a

TMC3033 result is smaller than the smallest normalized IEEE number, the TMC3033 produces a denormalized value (with a zero exponent). In the IEEE mode, when a TMC3032 product magnitude is smaller than the smallest normalized IEEE number, the TMC3032 produces a normalized but unrounded value with a (nonpositive) "wrapped" exponent. In this case, the UNF and UNF+INEX (underflow and underflow with inexact result) status flags can be applied to the TMC3033 along with the product to generate a properly rounded IEEE "gradual underflow" numerical representation. In FAST mode, underflowing products are flushed to zero with the UNF+INEX flag.

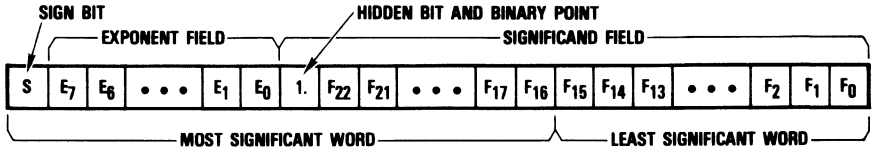
Instructions

Function codes 1010 binary through 1111 binary (listed as WTL1033 "Reserved" instructions) have been implemented as absolute value and IEEE Comparison instructions. Comparisons of infinities follow IEEE Standard 754 Version 8.0 for projective and affine modes. For IEEE Standard 754 Version 10.0, the affine infinity mode should be selected.

The FIX A instruction can be used with any user-selected type of rounding in the TMC3033, whereas the WTL1033 supports only round-toward-zero. When round-toward-zero is used, the WTL1033 and TMC3033 yield the same (correct) result.

Figure 1. Data Formats

32-bit floating point (IEEE Standard)

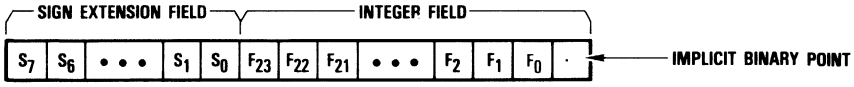


32-bit floating point values are determined by:

Exponent	Significand	Value	Name	Mnemonic
255	Not all zeros	-	Not a number	NaN
255	All zeros	$(-1)^S$	Infinity	INF
1-254	Any	$(-1)^S(1.F)2^{E-127}$	Normalized number	NRM
0	Not all zeros	$(-1)^S(0.F)2^{E-126}$	Denormalized number	DNRM
0	Zero	$(-1)^S(0.0)$	Zero	ZERO

Note: The F_{23} bit of the significand (hidden bit) is always one except for zero and denormalized numbers, when it is zero.

24-bit fixed point two's complement



Note: The 8-bit sign extension is a repeat of bit F_{23}, the sign bit of the two's complement representation. Values can range between $+2^{23}-1$ and -2^{23}.

Table 1. Load Instructions

L_{1-0}	Mnemonic	Operation
00	NOP	No loading of A, B or mode - Internal registers disabled
01	LAB	Load operands A & B into array from A & B registers
10	LA	Load only operand A into array from A register
11	LMODE	Load only MODE register from F and U registers

Table 2. Unload Instructions

U_{1-0}	Mnemonic	Operation
1X	DAB	Disable output driver (Hi-Z state)
0X	ENB	Enable output driver
X0	UMS	Load output register MSW from array
X1	ULS	Load output register LSW from array

Table 3. Mode Instructions

F_{3-0}	U_0	Mnemonic	Operation
XXXX	0	FLOW	Pipeline registers are disabled
XXXX	1	PIPE	Pipeline registers are enabled
XX00	X	RN	Round to nearest number, or nearest even number if distances are equal
XX01	X	RZ	Round toward zero (truncate product significand)
XX10	X	RP	Round toward positive infinity
XX11	X	RM	Round toward negative infinity
X0XX	X	AI	Affine infinity (sign preserved) IEEE Standard 754 Version 8.0 or 10.0
X1XX	X	PI	Projective infinity (sign ignored) IEEE Standard 754 Version 8.0
0XXX	X	IEEE	Gradual Underflow (use wrap for exponent underflow, TMC3032 only)
1XXX	X	FAST	Flush-to-zero (replace underflowing numbers with zero, TMC3032 only)

Table 4. TMC3032 Load Instructions

F_{3-0}	Mnemonic	Operation
0000	A x B	Multiply normalized A times normalized B
0001	WA x B	Multiply wrapped A times B
0010	A x WB	Multiply A times wrapped B
0011	WA x WB	Multiply wrapped A times wrapped B
01XX	-	Reserved
1XXX	-	Reserved

Table 5. Status Outputs

S_{2-0}	Mnemonic	Exceptions
000	OK	No exceptions
001	INEX	Inexact result
010	UNF	Exponent underflow
011	UNF+INEX	Exponent underflow and inexact result
100	-	Unused
101	OVF+INEX	Exponent overflow and inexact result
110	INV	Invalid operands or invalid operation
111	DIN	Denormalized operand, TMC3032

Table 6. TMC3033 Function Instructions

F_{3-0}	Mnemonic	Operation
0000	WRAP A	Convert a "gradual underflow" denormalized A operand (exponent zero) to normalized form with a negative (wrap-around) exponent. Used before multiplying a denormalized number.
0001	UNWRAP A	Convert a normalized A operand with a nonpositive (wrap-around) exponent to a denormalized number with a zero exponent. Used after an underflowing multiplication. The LSB of the B operand must contain the S_0 (inexact) bit from the multiplier STATUS word.
0010	FLOAT A	Convert a 24-bit two's complement integer at the A input to 32-bit normalized floating point.
0011	FIX A	Convert 32-bit normalized floating point number to 24-bit integer. All rounding modes usable.
0100	A+B	Add A and B in 32-bit floating point.
0101	A-B	Subtract B from A in 32-bit floating point.
0110	B-A	Subtract A from B in 32-bit floating point.
0111	(ABS A)+(ABS B)	Add the absolute values of A and B in 32-bit floating point.
1000	ABS (A-B)	Take the absolute value of the difference between A and B in 32-bit floating point.
1001	ABS (A+B)	Take the absolute value of the sum of A and B in 32-bit floating point.
1010	COMP A, B [1]	Compare A and B; result is A-B. Status flags indicate B>A, A=B, A>B.
1011	-A-B [1]	Subtract B from minus A, 32-bit floating point.
1100	COMP ABS A, ABS B [1]	Compare the absolute values of A and B; result is (ABS A)-(ABS B). Status flags indicate B>A, A=B, A>B.
1101	(ABS A)-(ABS B) [1]	Subtract the absolute value of B from the absolute value of A in 32-bit floating point.
1110	(ABS B)-(ABS A) [1]	Subtract the absolute value of A from the absolute value of B in 32-bit floating point.
1111	(-ABS A)-(ABS B) [1]	Subtract the absolute value of B from minus the absolute value of A 32-bit floating point.

Note:

1. These instructions are not implemented on the WTL1033 ALU device.

Table 7. TMC3033 Status Outputs for Comparison Operations

S_{2-0}	Mnemonic	Comparison Result
000	IOP	Invalid operation: one operand is not a number.
001	A>B	A operand greater than B operand.
010	A=B	A operand equal to B operand.
100	A<B	A operand less than B operand.

Table 8. Multiplication Exception Flags and Outputs

A Operand	B Operand				
	ZERO	DNRM	NRM/WNRM	INF	NaN
ZERO	OK, ZERO	OK, ZERO	OK, ZERO	INV, NaN	INV, NaN
DNRM	OK, ZERO	DIN [1], ZERO	DIN [1], ZERO	OK, INF	INV, NaN
NRM/WNRM	OK, ZERO	DIN [1], ZERO	See Note 2	OK, INF	INV, NaN
INF	INV, NaN	OK, INF	OK, INF	OK, INF	INV, NaN
NaN	INV, NaN	INV, NaN	INV, NaN	INV, NaN	INV, NaN

Notes: 1. In FAST mode, DIN becomes OK.

2. In the case of NRM.WNRM x NRM.WNRM

OVF: Output is OVF, -NRM.MAX if (RM,RZ) and TRESULT > NRM.MAX
OVF, NRM.MAX if (RP,RZ) and TRESULT < NRM.MAX
OVF, -INF if (RN,RP) and TRESULT > NRM.MAX
OVF, INF if (RN,RM) and TRESULT < NRM.MAX

UNF: Output is zero with UNF or UNF.INEX if |TRESULT| < NRM.MIN (FAST mode)
Output is WNRM with UNF or UNF.INEX if |TRESULT| < NRM.MIN (IEEE mode)

ELSE: Output is OK or INEX with normalized value
NRM.MIN ≤ |TRESULT| ≤ NRM.MAX

3. Terms used in this table include:

OK = No exceptions raised
NRM = Normalized number
DNRM = Denormalized number
WNRM = Wrapped number
INEX = Inexact result, output differs from infinite precision value
TRESULT = Normalized, rounded, true result before limiting
NRM.MAX = Maximum allowable positive normalized number, $2-2^{-128}\cdot 2^{104}$
NRM.MIN = Minimum allowable positive normalized number, 2^{-126}

Table 9. Conversion of 32-bit Floating Point to 24-bit Fixed Point

32-Bit Floating Point Operand	24-Bit Result	Status
$+1.XXX...XXX \times 2^{+128}$ (NaN OR INF)	0111...111	OVF
•	•	•
•	•	•
•	•	•
$+1.XXX...XXX \times 2^{+23}$	0111...111	OVF
$+1.111...111 \times 2^{+22}$	0111...111	INEX
$+1.111...110 \times 2^{+22}$	0111...111	OK
•	•	•
•	•	•
•	•	•
$+1.000...000 \times 2^{0}$	000...0001	OK
•	•	•
•	•	•
•	•	•
$+1.000...000 \times 2^{-126}$	000...0000	INEX
•	•	•
•	•	•
•	•	•
$+0.000...001 \times 2^{-126}$ (DNRM)	000...0000	INEX
$+0.000...000 \times 2^{-126}$ (ZERO)	000...0000	OK
$-0.000...000 \times 2^{-126}$ (ZERO)	000...0000	OK
•	•	•
•	•	•
•	•	•
$-0.111...111 \times 2^{-126}$ (DNRM)	000...0000	INEX
$-1.000...000 \times 2^{-126}$	000...0000	INEX
•	•	•
•	•	•
•	•	•
$-1.000...000 \times 2^{0}$	1111...111	OK
•	•	•
•	•	•
•	•	•
$-1.111...110 \times 2^{+22}$	1000...001	OK
$-1.111...111 \times 2^{+22}$	1000...001	INEX
$-1.000...000 \times 2^{+23}$ Note 1	1000...000	OVF
•	•	•
•	•	•
•	•	•
$-1.000...010 \times 2^{+23}$	1000...000	OVF
$-1.XXX...XXX \times 2^{+128}$ (NaN or INF)	1000...000	OVF

Note:

1. The indicated operation causes the OVF flag but is actually OK.

DNRM and WNRM represent numbers in which the fraction is normalized and the exponent is allowed to wrap through the biased exponent value of zero.

The multiplier accepts wrapped inputs from the ALU over the WNRM range. The smallest positive WNRM is $2^{-126} \times 2^{-23} = 2^{-149}$. The multiplier outputs wrapped numbers over the DNRM range. The smallest positive result is $2^{-149} \times 2^{-149} = 2^{-298}$.

Table 10. DNRM and WNRM Floating Point Numbers (IEEE Mode)

Exponent	Biased Value	Unbiased Value
0	0	127
255	1	128
•	•	•
•	•	•
•	•	•
234	22	149
232	23	150
•	•	•
•	•	•
•	•	•
85	171	298

WNRM

DNRM

Package Interconnections

Signal Type	Signal Name	Function	J3 Package	A1 Package
Power	V_{CC}	Positive Supply Voltage	31	58
Ground	GND	Ground	16	17, 33, 42, 51, 68
Data Inputs	A_{15-0}	A Operand Input Bus	59-64, 1-8, 10, 12	20-32, 34, 36, 38
	B_{15-0}	B Operand Input Bus	42-53, 55-58	2-13, 15, 16, 18, 19
Data Outputs	C_{15-0}	Result Output Bus	38-32, 30-22	65-59, 57-52, 50-48
Clock	CLK	Timing Reference	9	35
Controls	L_{1-0}	Load Instructions	13, 14	39, 40
	U_{1-0}	Unload Instructions	20, 21	46, 47
	F_{3-0}	Mode/Format Select	15, 17-19	41, 43-45
Flags	S_{2-0}	Status Outputs	41-39	1, 67, 66
No Connection	NC	None	11, 54	14, 37

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Figure 2. Input and Output Timing

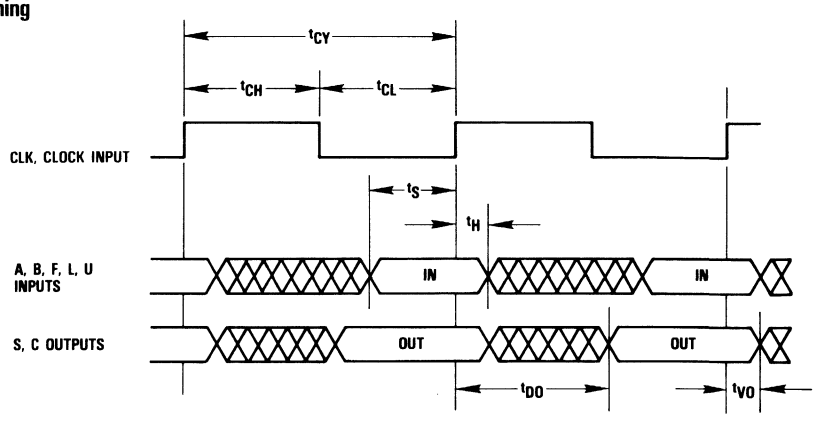


Figure 3. Flowthrough Mode Timing

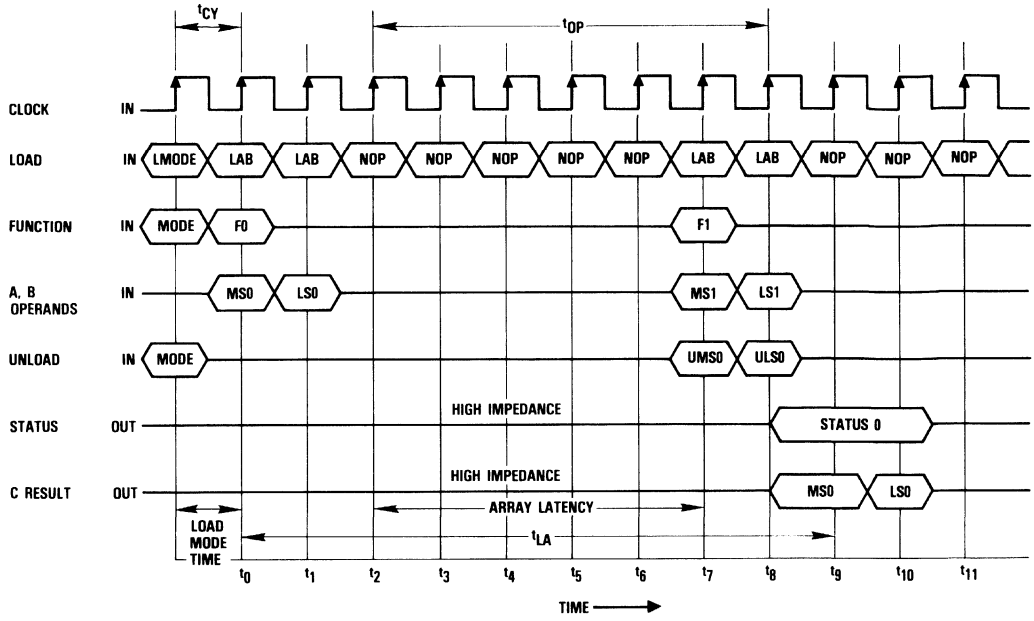


Figure 4. Pipeline Mode Timing

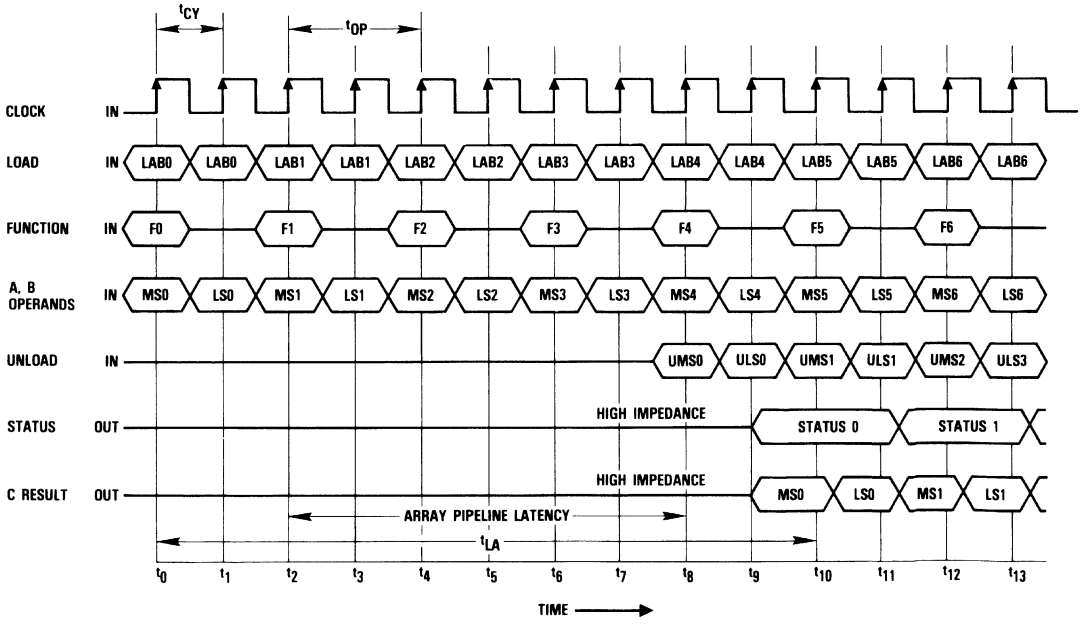


Figure 5. Equivalent Input Circuit

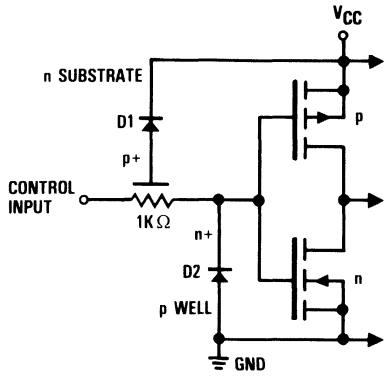
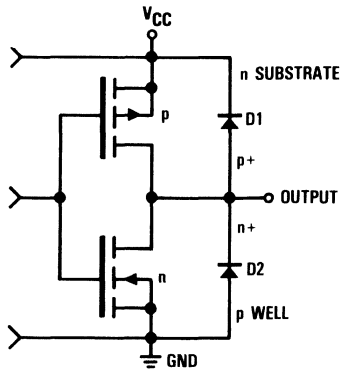


Figure 6. Equivalent Output Circuit



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{CC} + 5.5V)
Output	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−1.0 to 6.0mA [3,4]
Short-circuit duration (single output in HIGH state to ground)	1 Second
Temperature	
Operating, case	−55 to 125°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Military Min	Military Nom	Military Max	Units
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.5	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range								Units
			Standard				Military [2]				
			3032/3033		3032-1/3033-1		3032		3033		
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	Input Voltage, Logic HIGH		2.0		2.0		2.5		2.5		V
V_{IL}	Input Voltage, Logic LOW			0.8		0.8		0.8		0.8	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = −2mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = 4mA		0.4		0.4		0.5		0.5	V
I_{LI}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0 to 5V		10		10		10		10	μA
I_{LO}	Output Leakage Current (Outputs Disabled)	V_{CC} = Max, V_{OUT} = 0 to 5V		40		40		40		40	μA
C_{IN}	Input Capacitance	V_{CC} = Max, V_{IN} = 0 to 5V		15		15		15		15	pF
C_{OUT}	Output Capacitance (Outputs Disabled)	V_{CC} = Max, V_{IN} = 0 to 5V		15		15		15		15	pF
I_{CCQ}	Supply Current, Quiescent	V_{CC} = Max, V_{IN} = 0V		10		10		10		10	mA
I_{CCU}	Supply Current, Unloaded	V_{CC} = Max, f = 10MHz		40		40		50		40	mA

Notes:
1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Contact factory for final values.

AC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range								Units
			Standard				Military [2]				
			3032/3033		3032-1/3033-1		3032		3033		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CY}	Clock Cycle Time	V_{CC} = Min	62.5		50		60		60		ns
t_{CH}	Clock HIGH Time	V_{IH} = 2.4V	30		20		25		25		ns
t_{CL}	Clock LOW Time	V_{IL} = 0.8V	30		20		25		25		ns
t_S	Input Setup Time	V_{OH} = 2.8V, I_{OH} = −1mA	25		15		25		25		ns
t_H	Input Hold Time	V_{OL} = 0.4V, I_{OL} = 5mA	0		0		2		2		ns
t_{DO}	Output Delay Time	C_{LOAD} = 50pF		35		35		40		40	ns
t_{VO}	Output Valid Time	See Figure 2	10		10		8		8		ns
t_{OP}	Flowthrough Operation Time	See Figure 3		375		300		360		360	ns
t_{LA}	Total Flowthrough Latency			565		450		540		540	ns
t_{OP}	Pipelined Time Per Stage	See Figure 4		125		100		120		120	ns
t_{LA}	Total Pipeline Latency			625		500		600		600	ns

Notes:
1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Contact factory for final values.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC3032J3C	STD – T_A = 0°C to 70°C	Commercial	64 Pin Hermetic Ceramic DIP	3032J3C
TMC3032J3C1	STD – T_A = 0°C to 70°C	Commercial	64 Pin Hermetic Ceramic DIP	3032J3C1
TMC3032J3V[1]	MIL – T_C = –55°C to 125°C	MIL-STD-883	64 Pin Hermetic Ceramic DIP	3032J3V
TMC3033J3C	STD – T_A = 0°C to 70°C	Commercial	64 Pin Hermetic Ceramic DIP	3033J3C
TMC3033J3C1	STD – T_A = 0°C to 70°C	Commercial	64 Pin Hermetic Ceramic DIP	3033J3C1
TMC3033J3V[1]	MIL – T_C = –55°C to 125°C	MIL-STD-883	64 Pin Hermetic Ceramic DIP	3033J3V
TMC3032A1C	STD – T_A = 0°C to 70°C	Commercial	68 Contact Chip Carrier	3032A1C
TMC3032A1C1	STD – T_A = 0°C to 70°C	Commercial	68 Contact Chip Carrier	3032A1C1
TMC3033A1C	STD – T_A = 0°C to 70°C	Commercial	68 Contact Chip Carrier	3033A1C
TMC3033A1C1	STD – T_A = 0°C to 70°C	Commercial	68 Contact Chip Carrier	3033A1C1

Note: 1. Contact factory for availability.

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TMC3200, TMC3201

CMOS Floating-Point Arithmetic Unit and Multiplier

32/34 Bits

The TMC3200, an arithmetic unit, adds and subtracts floating-point numbers expressed in IEEE 32-bit single-precision format or extended-range 34-bit format. Conversions between floating-point and 24-bit two's-complement integer fixed-point representations are provided. Also, an internal accumulate path enhances performance in high-speed systems. The TMC3201, the multiplier compatible with the TMC3200, generates a product of two normalized floating-point numbers. These devices meet the floating-point format and operations described in Version 10.0 of IEEE Standard 754. The TMC3200 and TMC3201 are built using TRW's OMICRON-C™ one-micron CMOS process.

All data and instruction inputs to the TMC3200 and TMC3201 are registered. The input operands of the TMC3200 are selected from the input bus, zero or the accumulate path. Each input operand enters on a half-width bus on two consecutive rising edges of the clock. Controls are provided to determine the operand selection, the arithmetic operation, the data format and the rounding mode. Renormalizing, rounding and limiting functions are provided on both the TMC3200 and TMC3201 to ensure proper handling of special cases and to correct output data formatting. Results are output as two words on successive clock cycles and emerge through a three-state output port.

Features

- IEEE Standard 754 Version 10.0 32-Bit Or Extended-Range 34-Bit Floating-Point Data Format
- IEEE Default Unbiased Round-To-Nearest And Round-Toward-Zero Modes
- Three-Bus Architecture For High Throughput
- Automatic Limiting For Overflow/Underflow Cases
- Selectable Pipelining
- All Inputs And Outputs Are Registered And TTL Compatible
- Low Power CMOS Construction
- Standard/Extended Temperature Range
- Available In An 88 Pin Grid Array Package

TMC3200

- 10 Megaflop Throughput Rate (100ns Pipelined Cycle Time)
- Internal Accumulator Feedback Path
- Integer Two's-Complement 24-Bit Fixed-Point Data Format Conversions
- Full Conversion Between All Data Formats
- Flexible Data Source Selection
- Direct User-Transparent Handling Of Denormalized Operands
- Input Traps For Infinity And Not-A-Number

TMC3201

- 8 Megaflop Throughput Rate (125ns Pipelined Cycle Time)
- Input Traps For Infinity, Zero, Not-A-Number And Denormalized Numbers

Applications

- Matrix Operations And Geometric Transforms
- Arithmetic Element In Microprogrammed Array Processors
- Graphics And Image Processors
- Floating-Point Digital Filters
- Fast Fourier Transforms
- Radar And Sonar Signal Processors
- Solids Modeling

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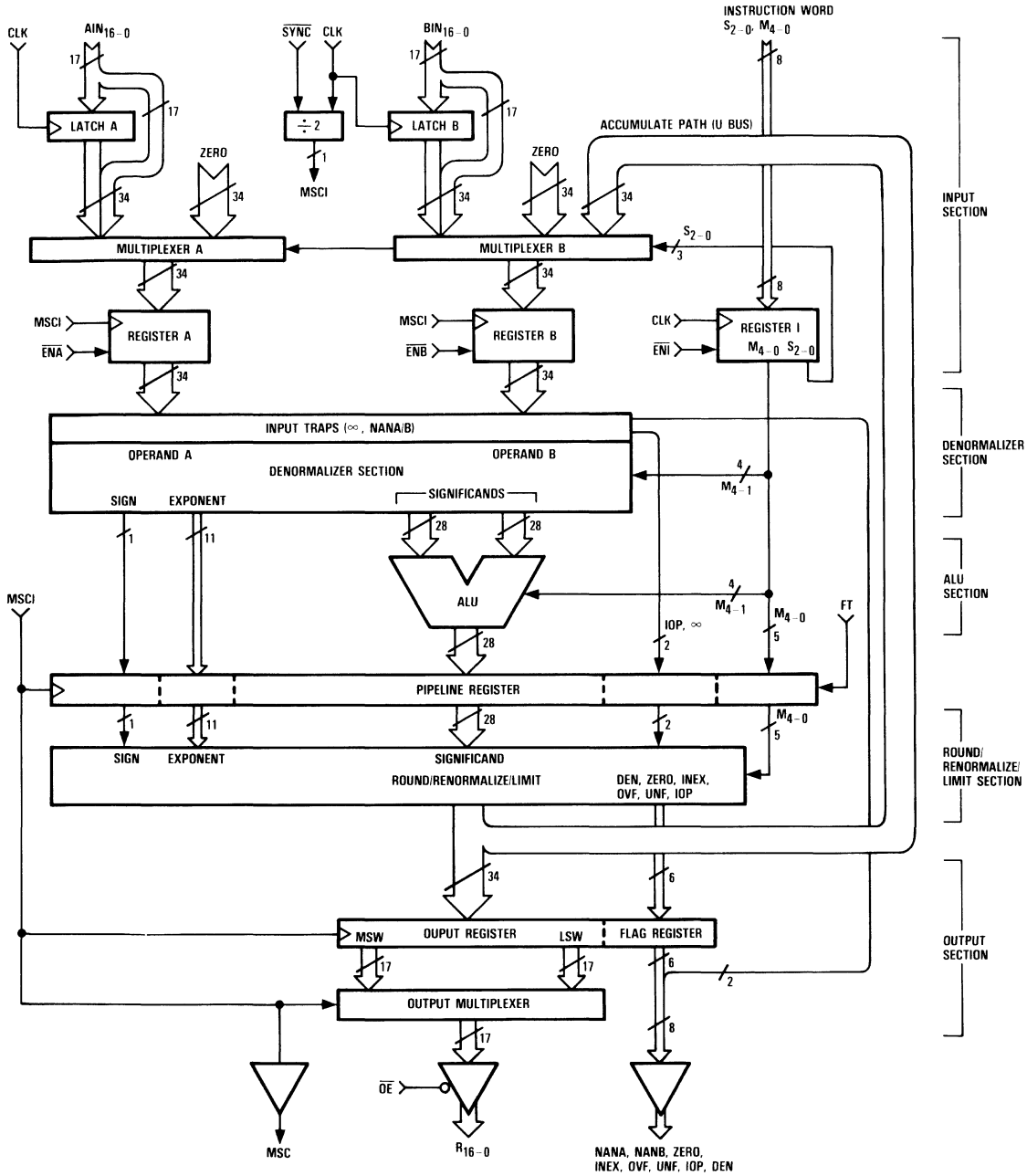
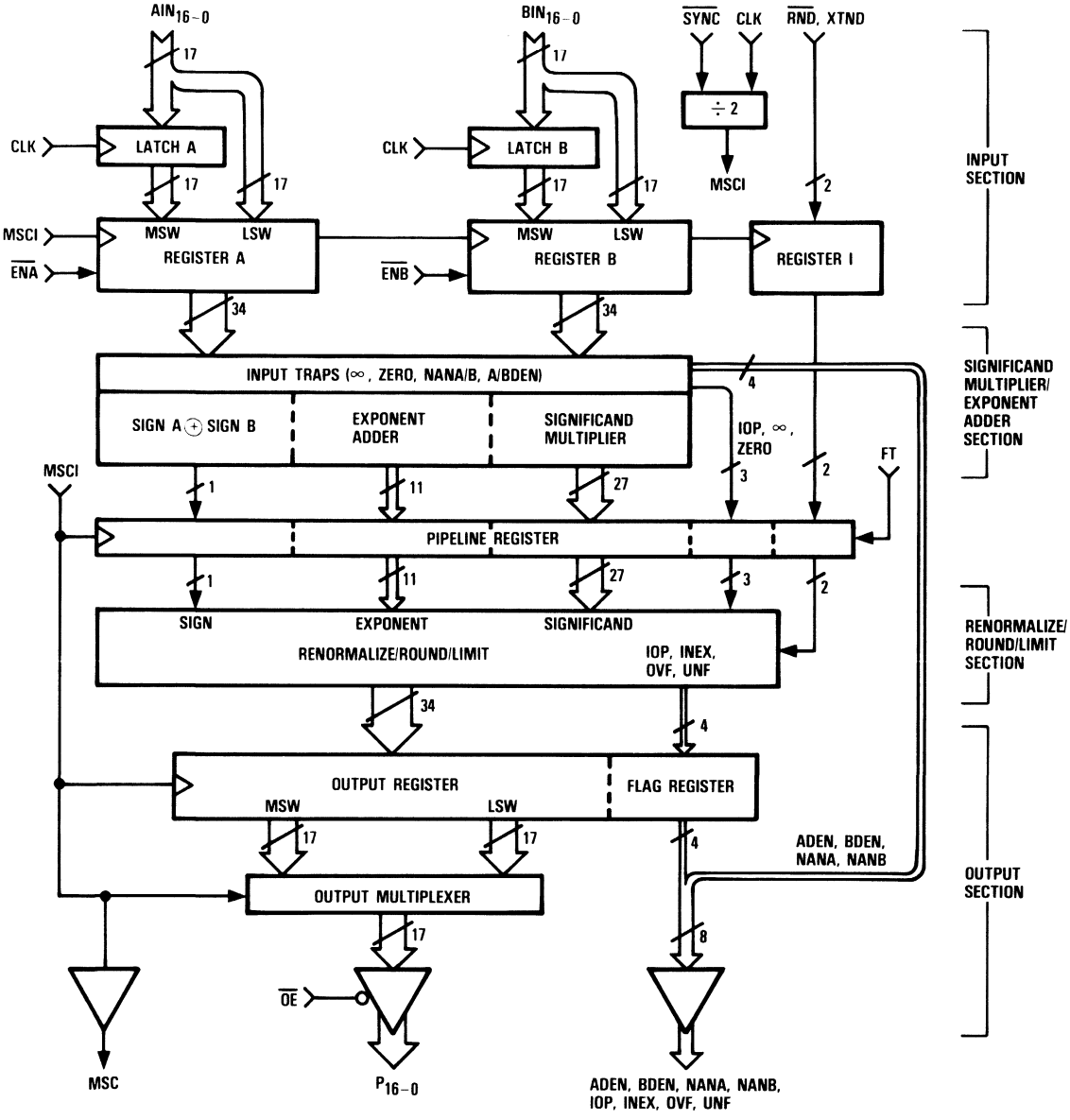
TMC3200 Functional Block Diagram



TMC3201 Functional Block Diagram



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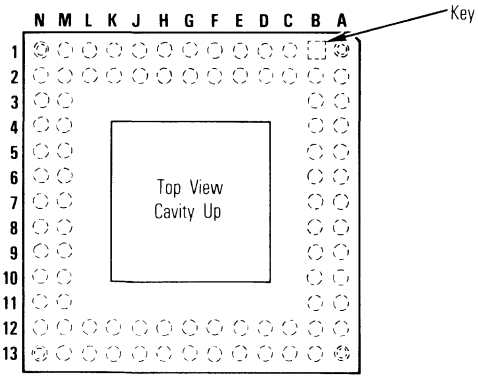
TMC3200 Pin Assignments

88 Pin Grid Array – G5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B1	AIN_8	N2	V_{DD}	M13	NC	A12	BIN_9
C2	AIN_9	M3	DEN	L12	V_{DD}	B11	BIN_{10}
C1	AIN_{10}	N3	NANA	L13	V_{DD}	A11	BIN_{11}
D2	AIN_{11}	M4	NANB	K12	R_6	B10	BIN_{12}
D1	AIN_{12}	N4	MSC	K13	R_5	A10	BIN_{13}
E2	AIN_{13}	M5	IOP	J12	R_4	B9	BIN_{14}
E1	AIN_{14}	N5	OVF	J13	R_3	A9	BIN_{15}
F2	AIN_{15}	M6	UNF	H12	R_2	B8	BIN_{16}
F1	AIN_{16}	N6	INEX	H13	R_1	A8	$\overline{ENB}$
G1	FT	N7	ZERO	G13	R_0	A7	$\overline{SYNC}$
G2	GND	M7	GND	G12	V_{DD}	B7	V_{DD}
H1	V_{DD}	N8	V_{DD}	F13	GND	A6	GND
H2	S_2	M8	R_{16}	F12	$\overline{OE}$	B6	CLK
J1	S_1	N9	R_{15}	E13	BIN_0	A5	$\overline{ENA}$
J2	S_0	M9	R_{14}	E12	BIN_1	B5	AIN_0
K1	M_2	N10	R_{13}	D13	BIN_2	A4	AIN_1
K2	M_0	M10	R_{12}	D12	BIN_3	B4	AIN_2
L1	M_1	N11	R_{11}	C13	BIN_4	A3	AIN_3
L2	M_4	M11	R_{10}	C12	BIN_5	B3	AIN_4
M1	M_3	N12	R_9	B13	BIN_6	A2	AIN_5
N1	$\overline{ENI}$	N13	R_8	A13	BIN_7	A1	AIN_6
M2	GND	M12	R_7	B12	BIN_8	B2	AIN_7



TMC3200 Functional Description

The TMC3200 consists of five sections: the input multiplexers and registers, the denormalizer, the arithmetic logic unit (ALU) and pipeline register, the round/renormalize/limit block, and the output registers and drivers.

TMC3201 Pin Assignments

88 Pin Grid Array – G5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B1	AIN_8	N2	V_{DD}	M13	NC	A12	BIN_9
C2	AIN_9	M3	GND	L12	V_{DD}	B11	BIN_{10}
C1	AIN_{10}	N3	NANA	L13	V_{DD}	A11	BIN_{11}
D2	AIN_{11}	M4	NANB	K12	P_6	B10	BIN_{12}
D1	AIN_{12}	N4	MSC	K13	P_5	A10	BIN_{13}
E2	AIN_{13}	M5	IOP	J12	P_4	B9	BIN_{14}
E1	AIN_{14}	N5	OVF	J13	P_3	A9	BIN_{15}
F2	AIN_{15}	M6	UNF	H12	P_2	B8	BIN_{16}
F1	AIN_{16}	N6	INEX	H13	P_1	A8	$\overline{ENB}$
G1	FT	N7	V_{DD}	G13	P_0	A7	$\overline{SYNC}$
G2	GND	M7	GND	G12	V_{DD}	B7	V_{DD}
H1	V_{DD}	N8	NC	F13	GND	A6	GND
H2	GND	M8	P_{16}	F12	$\overline{OE}$	B6	CLK
J1	GND	N9	P_{15}	E13	BIN_0	A5	$\overline{ENA}$
J2	V_{DD}	M9	P_{14}	E12	BIN_1	B5	AIN_0
K1	XTND	N10	P_{13}	D13	BIN_2	A4	AIN_1
K2	$\overline{RND}$	M10	P_{12}	D12	BIN_3	B4	AIN_2
L1	GND	N11	P_{11}	C13	BIN_4	A3	AIN_3
L2	V_{DD}	M11	P_{10}	C12	BIN_5	B3	AIN_4
M1	ADEN	N12	P_9	B13	BIN_6	A2	AIN_5
N1	BDEN	N13	P_8	A13	BIN_7	A1	AIN_6
M2	NC	M12	P_7	B12	BIN_8	B2	AIN_7

Input Multiplexers And Registers

The input section accepts the AIN and BIN operands along with the 8-bit instruction word which determines the A and B source multiplexer action, the arithmetic section operation, the rounding mode and data format of the operands. The clock (CLK) is divided by two generating the Most Significant Word Clock (MSCI) which is used internally for I/O multiplexing and is also available as an output, the MSC flag.

The AIN and BIN operands each enter on their respective 17-bit half-width input buses. Input preload registers latch in the data on the input buses on the rising edge of CLK. When the enable controls ($\overline{ENA}$ and $\overline{ENB}$) for the operand registers are LOW and AIN and BIN are selected by MUX A and MUX B, the data present in the preload registers and the data present on the input bus are simultaneously loaded into the operand registers on the rising edge of internal MSCI. The Most Significant Word (MSW) must be present on the rising edge of CLK which generates the falling edge of MSCI, and the Least Significant Word (LSW) must be present on the rising edge of CLK which generates the rising edge of MSCI. The

synchronization control ($\overline{SYNC}$) allows the user to align the MSCI signal with the desired phase of CLK. Initially, $\overline{SYNC}$ must be LOW to align the falling edge of MSCI with the rising edge of CLK and HIGH to align the rising edge of MSCI with CLK. After initial synchronization, alignment of CLK and MSCI will remain set as long as $\overline{SYNC}$ is held HIGH. The pipeline register contents are loaded into the operand register B on the rising edge of MSCI when $\overline{ENB}$ is LOW and the feedback accumulate path is selected.

The 8-bit instruction is loaded into the instruction register on the rising edge of CLK and must be input at the same time as the MSW of the operands with which it is associated. The instruction word must be held through both load cycles (MSW and LSW input) of the data to which it applies. The instruction word is divided into four fields: one to control the operand source multiplexers (S_{2-0}), one to select the data format (M_{2-1}), one to control the arithmetic operation performed (M_{4-3}) and one to control the rounding method (M_0). Operand A can be selected from two possible sources: AIN or zero. The B operand can be selected from three possible sources: BIN, the accumulate path or zero. The input and output data formats may differ and be selected from 32-bit floating-point, 34-bit floating-point or 24-bit integer fixed-point formats. The arithmetic operation performed is selected from A + B, A - B, B - A, -A - B, and CONVB (Convert B to a different data format). The rounding method is either IEEE round-to-nearest (which gives an unbiased error over a sequence of operations) or IEEE round-toward-zero, also known as truncation.

The input traps test AIN and BIN for the special cases of infinity and Not-A-Number (NAN). Internal flags which identify these cases are generated. If NAN is found, the NANA or NANB flag is set immediately and the output will be NAN with the Invalid Operation (IOP) flag. Infinity minus infinity produces a NAN output and sets the IOP flag.

Table 1. Multiplexer A And Multiplexer B Control

S_{2-0}	A Operand	B Operand
000	AIN	BIN
001	AIN	U
010	0	BIN
011	AIN	0
100	Magnitude (AIN)	Magnitude (BIN)
101	Magnitude (AIN)	Magnitude (U)
110	0	Magnitude (BIN)
111	Magnitude (AIN)	0

Note: 1. The Magnitude function turns off the sign bit and applies to floating-point operands only.

Denormalizer

This section prepares the operands by denormalizing (right-shifting) the smaller exponent's significand. This section outputs the larger incoming exponent, the sign and the input trap status flags.

Arithmetic Block

The ALU adds or subtracts the two significands which were output from the denormalizer section. The ALU output, exponent, sign and IOP flag are transferred to the pipeline register on the rising edge of internal MSCI if the Feedthrough (FT) control is LOW. When FT is HIGH, the pipeline register is transparent.

Round/Renormalize/Limit Block

The TMC3200 supports the IEEE default "unbiased round-to-nearest" when M_0 (round) is LOW. When M_0 is HIGH, the device implements "round-toward-zero" which truncates the result. The rounding adder operates on the output generated from the arithmetic section and outputs the result to the renormalizer.

The renormalizer shifts the rounded significand as necessary and adjusts the exponent. The resulting exponent is examined for overflow or underflow of the output data format. The renormalizer is disabled when converting from floating-point to integer and when converting from 34-bit to 32-bit IEEE denormalized "gradual underflow" format.

The limiter replaces overflowing results with a signed infinity (full-scale positive or negative integer in fixed mode). If the output is not in the "gradual underflow" mode, underflowing numbers are replaced with zero. A NAN output is triggered whenever an illegal operation (infinity minus infinity or NAN plus any number) is executed. In all other cases, the limiter will pass the result unchanged. The output from the round/renormalize/limit section is connected to the output register and also may be the input to register B through the accumulate path (U bus), a 34-bit feedback path.

Output Register And Drivers

The output section contains a 34-bit output result register, a 6-bit output flag register, the output multiplexer and the output drivers.

The output registers are clocked by internal MSCI. The contents of the registers are the 34-bit output from the limit section and the output flags. NANA and NANB are set when their particular input operand is NAN and will remain set until

a new legal operand is loaded. The arithmetic section results that are flushed to NANs set the IOP flag but not the NAN flags. The remaining flags become valid with their corresponding results and remain as long as the associated result is in the output register. The flag outputs are always enabled independent of the Output Enable ($\overline{OE}$) control.

The output multiplexer passes either the MSW or LSW of the result to the output drivers. The output multiplexer selects the MSW when MSC is HIGH and the LSW when MSC is LOW. The output drivers are enabled when $\overline{OE}$ is LOW and in the high-impedance state when $\overline{OE}$ is HIGH.

Table 2. Instruction Decoding

Instruction Select M_{4-3}	Mode, Round Select M_{2-0}							
	000	001	010	011	100	101	110	111
00	A+B $F_2 \rightarrow F_2$ Round	A+B $F_2 \rightarrow F_2$ Trunc	A+B $F_4 \rightarrow F_2$ Round	A+B $F_4 \rightarrow F_2$ Trunc	A+B $F_4 \rightarrow F_4$ Round	A+B $F_4 \rightarrow F_4$ Trunc	A+B $F_2 \rightarrow F_4$ Round	A+B $F_2 \rightarrow F_4$ Trunc
01	A-B $F_2 \rightarrow F_2$ Round	A-B $F_2 \rightarrow F_2$ Trunc	CONVB $F_2 \rightarrow F_4$ x	CONVB $F_2 \rightarrow F_4$ x	A-B $F_4 \rightarrow F_4$ Round	A-B $F_4 \rightarrow F_4$ Trunc	CONVB $F_4 \rightarrow F_2$ Round	CONVB $F_4 \rightarrow F_2$ Trunc
10	B-A $F_2 \rightarrow F_2$ Round	B-A $F_2 \rightarrow F_2$ Trunc	CONVB $I \rightarrow F_2$ x	CONVB $I \rightarrow F_2$ x	B-A $F_4 \rightarrow F_4$ Round	B-A $F_4 \rightarrow F_4$ Trunc	CONVB $I \rightarrow F_4$ x	CONVB $I \rightarrow F_4$ x
11	-A-B $F_2 \rightarrow F_2$ Round	-A-B $F_2 \rightarrow F_2$ Trunc	CONVB $F_2 \rightarrow I$ Trunc	CONVB $F_2 \rightarrow I$ Trunc	-A-B $F_4 \rightarrow F_4$ Round	-A-B $F_4 \rightarrow F_4$ Trunc	CONVB $F_4 \rightarrow I$ Trunc	CONVB $F_4 \rightarrow I$ Trunc

Notes:

1. M_0 = Round
   M_1 = Convert
   M_2 = 34-bit
   M_3 = Negate B
   M_4 = Negate A
2. For floating-point to fixed point conversions round-toward-zero is implemented.
3. F_2 and F_4 are 32-bit and 34-bit floating-point formats respectively.
4. I = Integers (fixed-point).
5. x = Don't care.
6. Round = Round-to-nearest.
7. Trunc = Round-toward-zero.
8. For all CONVB (convert B) instructions, the A operand field is ignored.

TMC3201 Functional Description

The TMC3201 consists of four sections: the input registers, the significand multiplier/exponent adder and pipeline register, the renormalize/round/limit block, and the output registers and drivers.

Input Section

The input section accepts the AIN and BIN operands along with a 2-bit instruction word which determines the data format of the operands and the rounding mode. CLK is divided by two generating MSCI which is used internally for I/O multiplexing and is also available as an output, the MSC flag.

The AIN and BIN operands each enter on their respective 17-bit half-width input buses. Input preload registers latch in the data on the input buses on the rising edge of CLK. When the enable controls ($\overline{ENA}$ and $\overline{ENB}$) for the operand registers are LOW, the data present in the preload registers and the data present on the input bus are simultaneously loaded into the operand registers on the rising edge of internal MSCI. The MSW must be present on the rising edge of CLK which generates the falling edge of MSCI, and the LSW must be present on the rising edge of CLK which generates the rising edge of MSCI. $\overline{SYNC}$ allows the user to align the MSCI signal with the desired phase of CLK. Initially, $\overline{SYNC}$ must be LOW to align the falling edge of MSCI with the rising edge of CLK and HIGH to align the rising edge of MSCI with CLK. After initial synchronization, alignment of CLK and MSCI will remain set as long as $\overline{SYNC}$ is held HIGH.

The 2-bit instruction is loaded into the instruction register on the rising edge of CLK and must be input at the same time as the MSW of the operands with which it is associated. The instruction word must be held through both load cycles (MSW and LSW input) of the data to which it applies. The Extended-Range control (XTND) selects the data format and Round ($\overline{RND}$) controls whether round-to-nearest or IEEE round-toward-zero is used.

The input traps test AIN and BIN for the special cases of infinity, zero, NAN and denormalized numbers. If NAN is found, the NANA or NANB flag is set immediately and the product output will be the product NAN with the IOP flag. Multiplication of zero times infinity also produces a NAN output and sets the IOP flag. The TMC3201 is not able to process denormalized operands and will set the appropriate ADEN or BDEN flag. The product output in this case will be zero corresponding to the "fast" implementation of IEEE Standard 754.

Significand Multiplier/Exponent Adder

Floating-point multiplication consists of multiplying the fraction fields and adding the exponent fields. Since the TMC3201 operates only on normalized numbers, the 23 bits of each input fraction field are input to the multiplier array with the implicit "hidden bit" (which is always a one) added. This output is latched by the pipeline register which follows the multiplier array.

The A and B exponent fields are added generating a two's-complement product exponent. The result is passed through the pipeline registers and the exponent adjust section performs further processing before final output.

The significand product, the exponent sum, the instructions, the IOP flag and the product sign are latched into the pipeline register on the rising edge of internal MSCI if FT is LOW.

Renormalize/Round/Limit Section

The significand is renormalized and passed to the rounding adder. If $\overline{RND}$ is LOW, the TMC3201 will round-to-nearest according to the IEEE default standard. If $\overline{RND}$ is HIGH, the significand is truncated (IEEE round-toward-zero).

The product exponent is checked for overflow or values greater than or equal to 255 for IEEE 32-bit format or 511 for extended-range 34-bit format. Underflow has occurred if the exponent is less than or equal to zero in 32-bit format or -512 in extended-range 34-bit format.

The limiter forces the significand and exponent fields to appropriate signed infinities, zero or NAN. Overflow cases are forced to signed infinities, underflow and zero cases are forced to a signed zero, and illegal operation cases are forced to NAN. Also, the two status flags Overflow (OVF) and Underflow (UNF) are generated for output in this section. The output of this section is a 34-bit field, interpreted as either IEEE 32-bit or extended-range 34-bit data.

Output Register And Drivers

The output section contains a 34-bit output product register, a 4-bit output flag register, the output multiplexer and the output drivers.

The output registers are clocked by internal MSCI. The contents of the registers are the 34-bit output from the limit section along with the output flags. The flags are valid while the result is held in the output register except for the NANA, NANB, ADEN and BDEN flags. These operand trap flags are set when their particular input operand is a NAN or a denormalized number and will remain set until a new legal operand is loaded. The flags are always enabled independent of the $\overline{OE}$ control.

The output multiplexer passes either the MSW or LSW to the output drivers. The output multiplexer selects the MSW when MSC is HIGH and the LSW when MSC is LOW. The output drivers are enabled when $\overline{OE}$ is LOW and in the high-impedance state when $\overline{OE}$ is HIGH.

J

Signal Definitions

Power

V_{DD}, GND — The TMC3200 and TMC3201 operate from a single +5 Volt supply. All power and ground lines must be connected.

Data Inputs

AIN_{16-0}, BIN_{16-0} — AIN and BIN are the 17-bit input ports. AIN_{16} and BIN_{16} are the extension bits for 34-bit floating-point operation.

Data Outputs

R_{16-0} — R_{16-0} is the 17-bit result output port of the TMC3200. R_{16} is the extension bit for 34-bit floating-point operation.

P_{16-0} — P_{16-0} is the 17-bit product output port of the TMC3201. P_{16} is the extension bit for 34-bit floating-point operation.

Clock

CLK — The CLK frequency is twice the data throughput rate to allow for data multiplexing. All operations are with respect to the rising edge of CLK. CLK is internally divided by two to generate internal MSCI. The rising edge of MSCI is coincident with every other rising edge of CLK.

Controls

$\overline{ENA}$, $\overline{ENB}$ — Enable A (Enable B) enables register A (B) when LOW. Register A (B) is then loaded with the output of Multiplexer A (Multiplexer B) on the rising edge of internal MSCI.

$\overline{SYNC}$ — $\overline{SYNC}$ causes the falling edge of MSCI to be coincident with the rising edge of CLK when LOW for t_S before the rising edge of CLK. This signal must go HIGH for the device to operate properly. Bringing $\overline{SYNC}$ LOW with the incoming MSW and then HIGH during the LSW will initialize the device.

$\overline{OE}$ — Output Enable controls the three-state outputs. When $\overline{OE}$ is LOW, the output drivers are enabled. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state. $\overline{OE}$ does not affect the flag outputs and must be held LOW for two CLK cycles to obtain a complete output result.

FT — Feedthrough controls the pipeline register. When FT is LOW, the pipeline register is enabled. When FT is HIGH, the pipeline register is transparent. FT is a DC control.

$\overline{ENI}$ — Enable Instruction enables register I when LOW for t_S before the rising edge of CLK. Register I is then loaded with an instruction M_{4-0} and S_{2-0}. If $\overline{ENI}$ is held LOW, the instruction words must be valid for two cycles of CLK for a valid operation. (TMC3200)

S_{2-0} — Source decoding selects the A and B operands of the TMC3200 by controlling Multiplexer A and Multiplexer B.

M_{4-0} — These controls (instruction, mode, round select) define the various ways the TMC3200 operates. When M_0 is LOW, the result will round-to-nearest (round). When M_0 is HIGH, the result will round-toward-zero (truncate). M_2 selects 32 or 34-bit formats. When M_1 is LOW, M_4 and M_3 control the A and B operands.

XTND — Extended-range 34-bit data format is in effect when XTND is HIGH. This control signal is loaded on every rising edge of CLK. (TMC3201)

$\overline{RND}$ — When Round is LOW, the result will round-to-nearest. When HIGH, the result will round-toward-zero or truncate. This control signal is loaded on every rising edge of CLK. (TMC3201)

Flags

MSC — Most Significant Word Clock output synchronizes the data output. When the output is enabled and MSC is HIGH, the MSW result is present at the output. When the output is enabled and MSC is LOW, the LSW result is present at the output.

OVF — Overflow will go HIGH when a floating-point result exponent exceeds the maximum allowed or when a full-scale integer result is available at the output.

UNF — Underflow will go HIGH when a nonzero result is too small to be a normalized floating-point number and is available at the output.

INEX — Inexact Result will go HIGH when a result fractional part is not exactly equal to the results of an infinitely precise calculation and the result is available at the output.

NANA, NANB — Not-A-Number A and B flags will go HIGH when the A and B operand registers contain non-valid IEEE Standard 754 numbers.

IOP — Invalid Operation flag will go HIGH when an operation is requested which cannot be properly executed for any reason.

ZERO — All operations which result in zero cause this flag to go HIGH when the result is available at the output. (TMC3200)

DEN — Denormalize will go HIGH when any result with zero exponent and nonzero fraction is available at the output. (TMC3200)

ADEN, BDEN — A and B Operand Denormalized will go HIGH when the contents of the respective operand register is not a normalized IEEE Standard 754 number. (TMC3201)

No Connects

NC — The pin grid array version of the TMC3200 has one pin which is not connected internally. The pin grid array version of the TMC3201 has three pins which are not connected internally.

TMC3200 Package Interconnections

Signal Type	Signal Name	Function	G5 Package
Power	V_{DD}	Supply Voltage	H1, N2, N8, L12, L13, G12, B7
	GND	Ground	G2, M2, M7, F13, A6
Data Input	AIN_{16-0}	A Input Data	F1, F2, E1, E2, D1, D2, C1, C2, B1, B2, A1, A2, B3, A3, B4, A4, B2
	BIN_{16-0}	B Input Data	B8, A9, B9, A10, B10, A11, B11, A12, B12 A13, B13, C12, C13, D12, D13, E12, E13
Data Output	R_{16-0}	Result Output Data	M8, N9, M9, N10, M10, N11, M11, N12, N13 M12, K12, K13, J12, J13, H12, H13, G13
Clock	CLK	Clock	B6
Controls	$\overline{ENA}$	Enable A Register	A5
	$\overline{ENB}$	Enable B Register	A8
	$\overline{ENI}$	Enable I Register	N1
	$\overline{SYNC}$	Synchronize ALU	A7
	S_{2-0}	Operand Source	H2, J1, J2
	M_{4-3}	Instruction Select	L2, M1
	M_{2-1}	Mode Select	K1, L1
	M_0	Round	K2
	$\overline{OE}$	Output Enable	F12
	FT	Feedthrough	G1
Flags	MSC	MSW Clock	N4
	ZERO	Zero Result	N7
	DEN	Denormalized Result	M3
	OVF	Overflow	N5
	UNF	Underflow	M6
	INEX	Inexact Result	N6
	NANA	Not-A-Number A	N3
	NANB	Not-A-Number B	M4
	IOP	Invalid Operation	M5
No Connection	NC	None	M13

TMC3201 Package Interconnections

Signal Type	Signal Name	Function	G5 Package
Power	V_{DD}	Supply Voltage	H1, J2, L2, N2, N7, L12, L13, G12, B7
	GND	Ground	G2, H2, J1, L1, M3, M7, F13, A6
Data Input	AIN_{16-0}	A Input Data	F1, F2, E1, E2, D1, D2, C1, C2, B1, B2, A1, A2, B3, A3, B4, A4, B5
	BIN_{16-0}	B Input Data	B8, A9, B9, A10, B10, A11, B11, A12, B12, A13, B13, C12, C13, D12, D13, E12, E13
Data Output	P_{16-0}	Product Output Data	M8, N9, M9, N10, M10, N11, M11, N12, N13 M12, K12, K13, J12, J13, H12, H13, G13
Clock	CLK	Clock	B6
Controls	$\overline{ENA}$	Enable A Register	A5
	$\overline{ENB}$	Enable B Register	A8
	$\overline{SYNC}$	Synchronization	A7
	XTND	Extended Precision	K1
	$\overline{RND}$	Round	K2
	$\overline{OE}$	Output Enable	F12
	FT	Feedthrough	G1
Flags	MSC	MSW Clock	N4
	ADEN	A Denormalized	M1
	BDEN	B Denormalized	N1
	OVF	Overflow	N5
	UNF	Underflow	M6
	INEX	Inexact	N6
	NANA	Not-A-Number A	N3
	NANB	Not-A-Number B	M4
	IOP	Invalid Operation	M5
No Connection	NC	None	M2, N8, M13

Data Format

The TMC3200 arithmetic unit and TMC3201 multiplier conform to IEEE Standard 754, Version 10.0 data format for 32-bit arithmetic. These devices also have an extended-range 34-bit floating-point format. The two additional bits of the extended format are appended to the exponent field. Any two legal 32-bit operands can be added without generating an overflow if the 34-bit extended format is used for output. The ALU accumulate path uses the 34-bit extended format. For both data formats the arithmetic unit needs only two clock cycles to transfer a data word since the input and output buses are 17-bit wide.

Standard IEEE 32-Bit Floating-Point Format

The IEEE Standard 754, Version 10.0 specifies a 32-bit data format for floating-point arithmetic. In this format the MSB (bit 31) is the sign bit, the next eight bits (bits 30-23) are the exponent field, and the 23 LSBs are the fractional significand field (bits 22-0). The "hidden bit" completes the 24-bit significand.

Sign Bit

The MSB carries the sign information. A HIGH for a sign bit indicates a negative number and a LOW indicates a positive number.

Exponent Field

The 8-bit exponent field determines whether the floating-point number is a signed infinity, a NAN, a zero, a denormalized number or a normalized floating-point number.

The exponent values 0 and 255 are special. If the exponent field is all ones (1111 1111, 255_{10}) and the fraction (bits 22-0) is zero, the number is evaluated as infinity x $(-1)^S$ with S being the sign bit. Any exponent of 255 with a nonzero fraction is a NAN. NANs are generally used to communicate error information and have no numerical value.

When the exponent field is all zeros (0000 0000) and the fraction is also zero, the number is a true floating-point zero. Note that this data format allows both positive and negative zeros which are computationally treated identically. When the exponent is zero and the fraction is nonzero, the number is a denormalized floating-point number evaluated as:

$$\text{Number} = (-1)^S \times 2^{E-126} \times (0.F)$$

where S is the sign bit, E is the value of the exponent field (base 10), and F is the value of the fractional field.

If the exponent field is neither all zeros nor all ones, the floating-point number is normalized and evaluated as:

$$\text{Number} = (-1)^S \times 2^{E-127} \times (1.F)$$

Note that the exponent bias has changed from 126 to 127 and that 1.0 has been added to the fractional field. The exponent can assume values which run from -126 to +127 (0 to 254 biased by 127). Note that both exponent fields of zero and one map onto the exponent value of -126. These provisions ensure a smooth transition from normalized numbers through gradual underflow into the denormalized numbers.

Fractional Field

Bits 22-0 comprise the fractional field (mantissa). There is a binary point assumed between bit 22 and the implied "hidden" bit 23. For a nonzero exponent, the hidden bit assumes a value of "1." For a zero exponent, the hidden bit has a value of "0." Bit 22 carries a binary weighting of 2^{-1}. The following bits carry decreasing binary weights down to the LSB (bit 0) which carries the weight of 2^{-23}. This is identical to treating the fractional part (bits 22-0) like an integer F multiplied by 2^{-23}. The fractional part of the floating-point number is either 0 + F (in the case of a zero exponent), or 1 + F (in the case of a nonzero exponent).

The difference between the smallest normalized number (exponent = 1, fractional part = 0) and the largest denormalized number (exponent = 0, fractional part= all ones) is one LSB. The smallest normalized number is: exponent = -126, significand = 1.00...00. The largest denormalized number is: exponent = -126, significand = 0.11...11.

Extended 34-Bit Floating-Point Format

The 34-bit extended-data format is a superset of the IEEE 32-bit floating-point format because every number represented in the IEEE 32-bit format can be represented in the 34-bit format. The MSB (bit 33) is the sign bit; the next ten bits (bits 32-23) are the exponent field; and the 23 LSBs are the fractional field.

Sign Bit

The sign bit (bit 33) signifies the sign of the floating-point number. If the sign bit is HIGH, the number is negative. If the sign bit is LOW, the number is positive.

Exponent Field

As in the 32-bit format, the extreme exponents are special. The exponent field is interpreted as a 10-bit two's-complement integer which can vary from 10 0000 0000 (-512_{10}) to 01 1111 1111 (511_{10}). If the fraction is zero with an exponent of 511, the floating-point number is a signed infinity. A nonzero fraction with an exponent of 511 means that the number is a NAN.

If the exponent is -512, a fraction of zero signifies a true floating-point zero. As in the 32-bit format, there are both positive and negative zeros. A nonzero fraction with a -512 exponent signifies a denormalized number.

If the exponent is any value other than -512 or 511, the exponent value is the 10-bit two's-complement number minus a bias of 127 and the number is evaluated as:

$$\text{Number} = (-1)^S \times 2^{E-127} \times (1.F)$$

where S is the sign bit, E is the exponent and F is the fraction to which the hidden bit of 1 is added. Note that the exponents can be in the range of -638 (-511-127) to 383 (510-127).

Two's-Complement 24-Bit Integer Format

The TMC3200 converts data between the floating-point formats and a 24-bit two's-complement integer format which is sign-extended to 32 bits.

Sign Bit

In the integer format, the bit occupying the position of the exponent LSB (E_0) is the two's-complement MSB/sign bit whose weighting is -2^{23}. When an integer is output, the sign extends this bit through the normal 32-bit floating-point sign and exponent fields. The nine MSBs will be all ones for negative numbers and zeros for positive numbers.

Fraction Field

The 23-bit floating-point fraction field becomes the magnitude portion of the two's-complement integer. The weighting is shifted giving the LSB a weighting of one. The numerical interpretation of an integer is:

$$I = E_0 \times (-2^{23}) + \sum_{n=0}^{22} F_n \times (2^n)$$

where F_n is the 23 fraction bits and E_0 is the exponent LSB. For integer input, the device ignores the 8 MSBs (floating point sign and seven highest exponent bits) plus the 34-bit extension bit.

Application Discussion (TMC3200)

Comparisons

One function required of arithmetic systems is the comparison of two quantities. The device can perform this function by subtracting one IEEE or extended-range number from another (the rounding mode is not important for this function). The ZERO flag and sign output will reflect the results of the comparison of the operands. Normalized and denormalized numbers and infinities can be compared. The results will be correct in all meaningful cases: two normalized or denormalized numbers in any combination, a normalized or denormalized number and +/-infinity, and even +infinity compared to -infinity. The IOP flag will be HIGH when there is no mathematically meaningful order to the inputs. Note that magnitudes (absolute values) can be compared by using the magnitude function of the source select segment of the instruction.

Table 3. Flags For Comparison Results (Operation A – B)

Operand A	Operand B	Order	IOP	ZERO	Sign
Norm/Denorm	Norm/Denorm	A > B	0	0	0
Norm/Denorm	Norm/Denorm	A = B	0	1	X
Norm/Denorm	Norm/Denorm	A < B	0	0	1
+∞	Norm/Denorm		0	0	0
Norm/Denorm	+∞		0	0	1
+∞	-∞		0	0	0
-∞	+∞		0	0	1
+∞	+∞		1	0	X
-∞	-∞		1	0	X

Table 4. Flag Interpretation

IOP	ZERO	Sign	Interpretation
0	0	0	A > B
0	0	1	A < B
0	1	X	A = B
1	X	X	no mathematical order to inputs, e.g. comparison of two negative infinities.

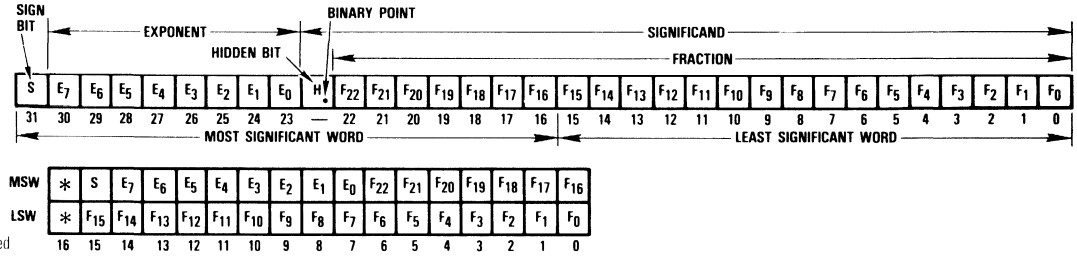
Reduced Microcode

The control signals are encoded to lower the device pin count. Because this encoding is relatively light, applications that do not require the full functionality of the TMC3200 can permanently connect many of the control signals resulting in a reduced microcode set.

The IEEE default round-to-nearest mode can be permanently selected by connecting M_0 to a logic LOW. If the 34-bit extended-range mode is not used for inputs or outputs (which would be the situation in IEEE standard systems), M_2 can be permanently connected to a logic LOW. Note that internal accumulation is always extended range. If a 32-bit output format is selected by the operation and mode controls, the flags and outputs are proper for the IEEE standard, but internally accumulated results are more accurate than those obtained by reducing the sum to 32 bits. This treatment can eliminate overflow or underflow errors in long accumulations. If magnitude operations are not required, then S_2 can be permanently connected to a logic LOW.

These suggestions enable the designer to reduce the number of instruction bits with little loss in functionality.

Figure 1. IEEE 32-Bit Format



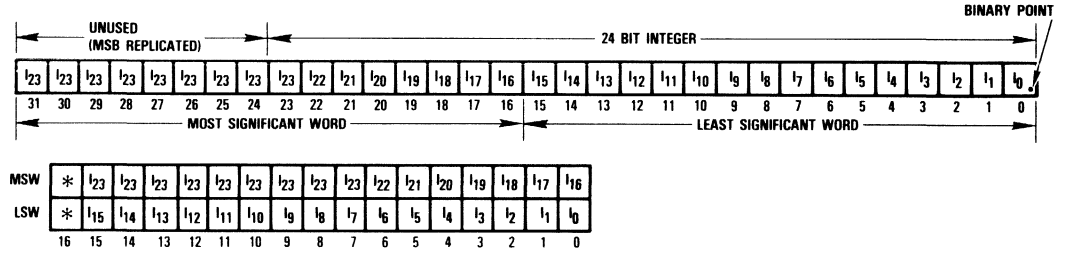
*Not Used

Exponent	Fraction	Value	Name
255	Not all zeros	--	Not-A-Number
255	All zeros	$(-1)^S \times \infty$	Signed Infinity
1 through 254	Any	$(-1)^S \times (1.F) \times 2^{E-127}$	Normalized Number
0	Not all zeros	$(-1)^S \times (0.F) \times 2^{E-126}$	Denormalized Number
0	All zeros	$(-1)^S \times 0.0$	Zero

Notes:

1. If an illegal operation generates a NAN, then F = 200000_H in the TMC3200 and F = 400000_H in the TMC3201.
2. H, the hidden bit, is one except for zero and denormalized numbers when it is zero.
3. E and F are magnitude representations.

Figure 2. 24-Bit Integer Format



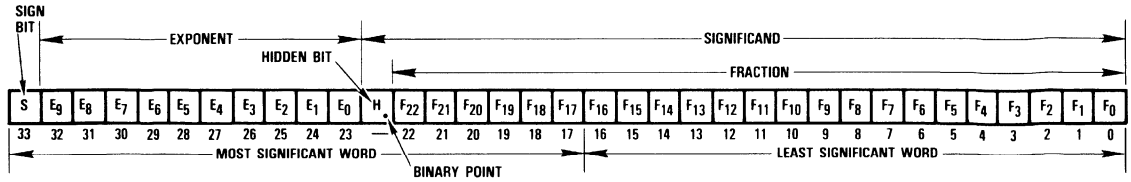
*Not Used

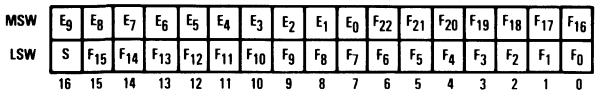
Notes:

1. $I = -2^{23} I_{23} + \sum_{i=0}^{22} 2^i I_i$
2. For fixed-point inputs, the sign bit is bit 23, and bits 31-24 are don't care.
3. For fixed-point outputs, the sign bit is replicated through bits 31-23.

J

Figure 3. Extended 34-Bit Format





Exponent	Fraction	Value	Name
511	Not all zeros	--	Not-A-Number
511	All zeros	$(-1)^S \times \infty$	Signed Infinity
-511 through 510	Any	$(-1)^S \times (1.F) \times 2^{E-127}$	Normalized Number
-512	Not all zeros	$(-1)^S \times (0.F) \times 2^{E-126}$	Denormalized Number
-512	All zeros	$(-1)^S \times 0.0$	Zero

Notes:

1. If an illegal operation generates a NAN, then $F = 200000_H$ in the TMC3200 and $F = 400000_H$ in the TMC3201.
2. $E = -2^9 E_9 + \sum_{i=0}^{8} 2^i E_i$ (true exponent = E-127 as in IEEE Format)

$$\text{Significand} = 2^0 + \sum_{i=0}^{22} 2^{i-23} F_i \quad \text{if } E > -512$$

$$\text{Significand} = \sum_{i=0}^{22} 2^{i-23} F_i \quad \text{if } E = -512$$

3. H, the hidden bit, is one except for zero and denormalized numbers, when it is zero.
4. F is a magnitude number.
5. E is a 10-bit two's-complement number. Note that the IEEE exponent is a subset of the extended-range exponent.
6. S, the sign bit, is in the LSW's MSB position.

Figure 4. Synchronization Timing Diagram

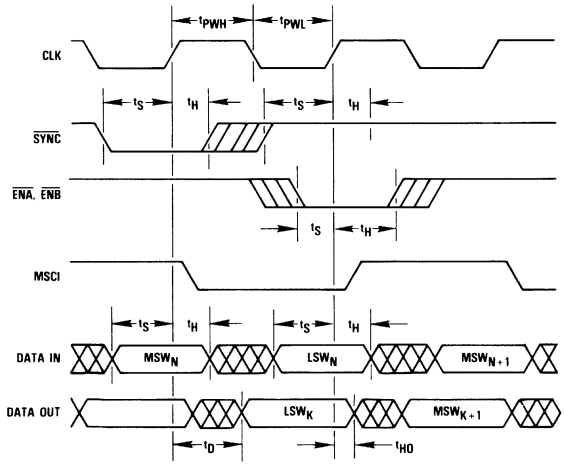


Figure 5. TMC3200 Non-Accumulate Mode Without Pipelining Timing Diagram

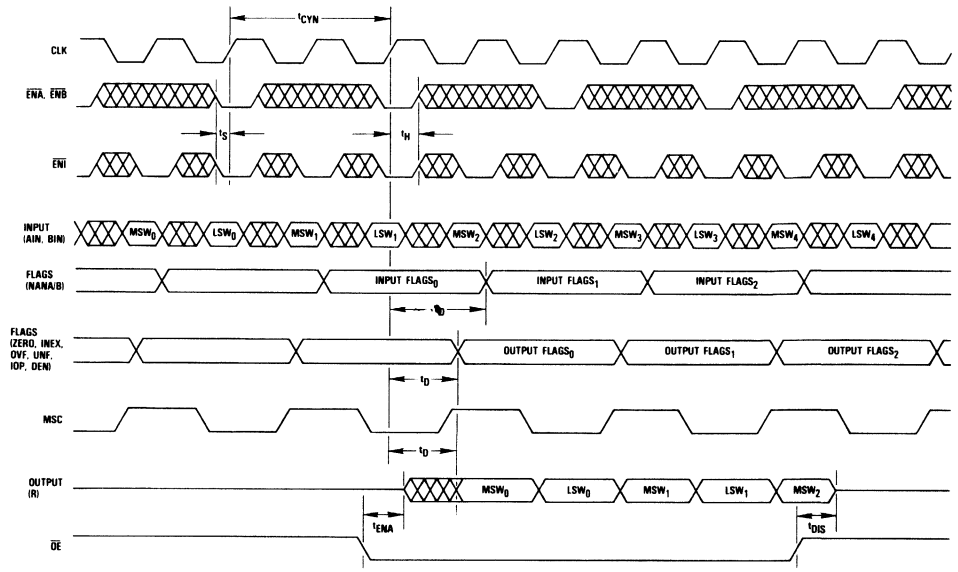


Figure 6. TMC3200 Non-Accumulate Mode With Pipelining Timing Diagram

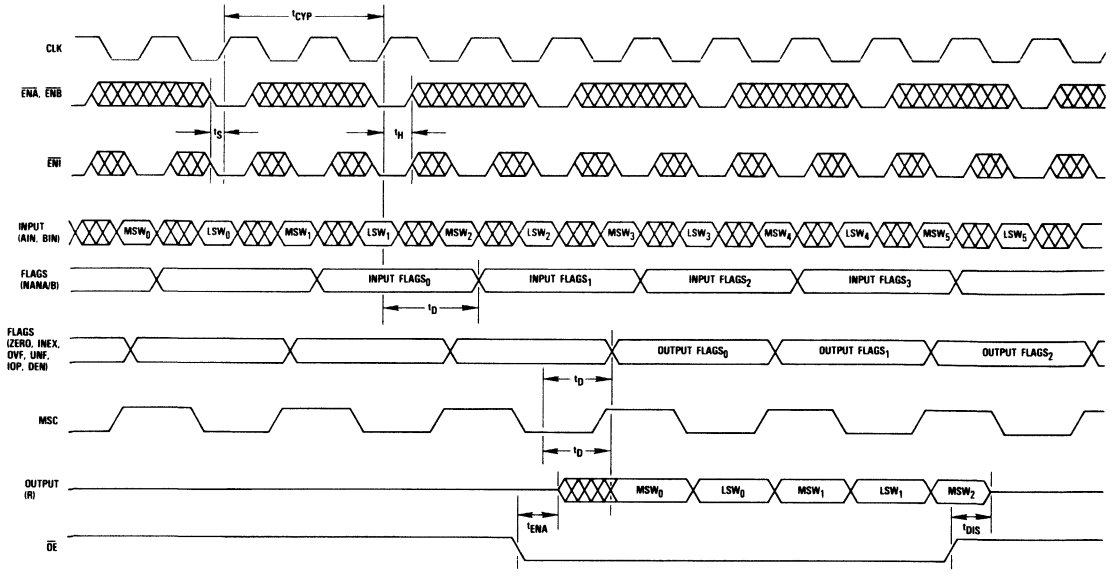


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Figure 7. TMC3200 Accumulate Mode Without Pipelining Timing Diagram

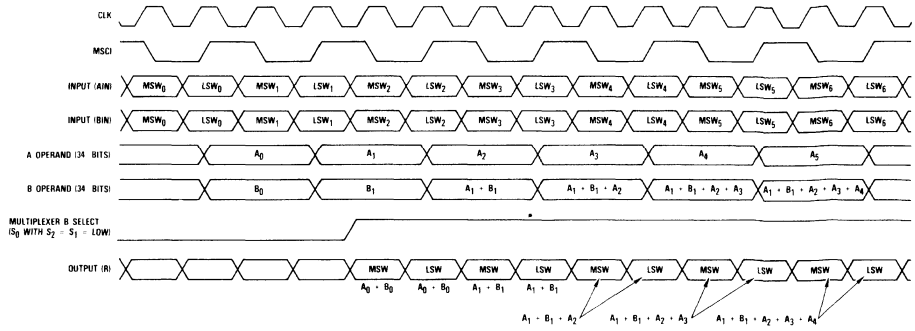


Figure 8. TMC3200 Accumulate Mode With Pipelining Timing Diagram

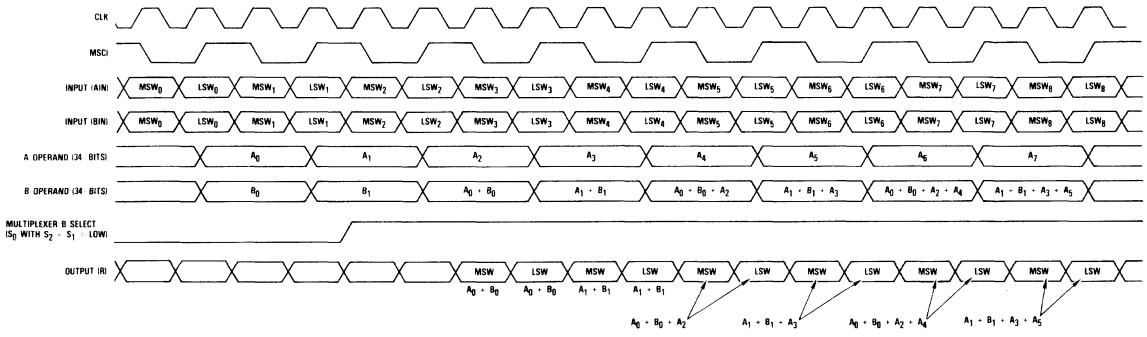


Figure 9. TMC3201 Multiplication Mode Without Pipelining Timing Diagram

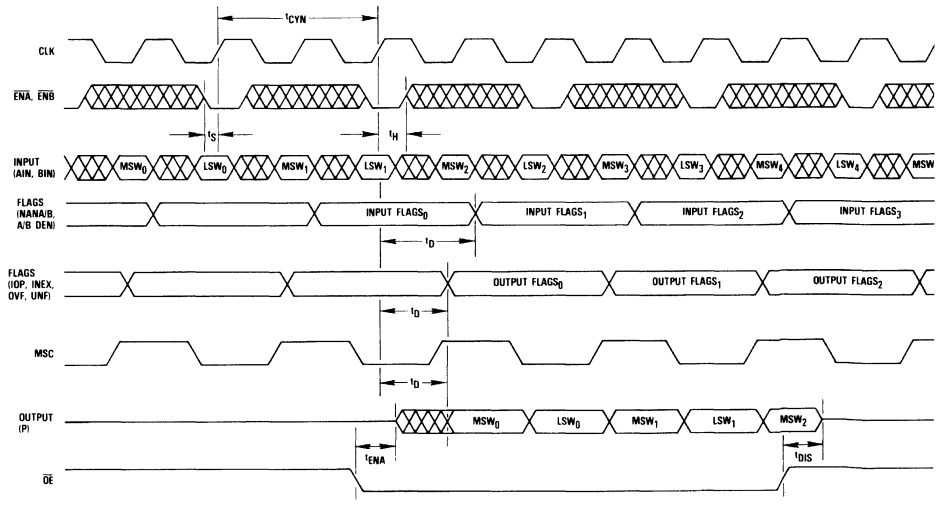


Figure 10. TMC3201 Multiplication Mode With Pipelining Timing Diagram

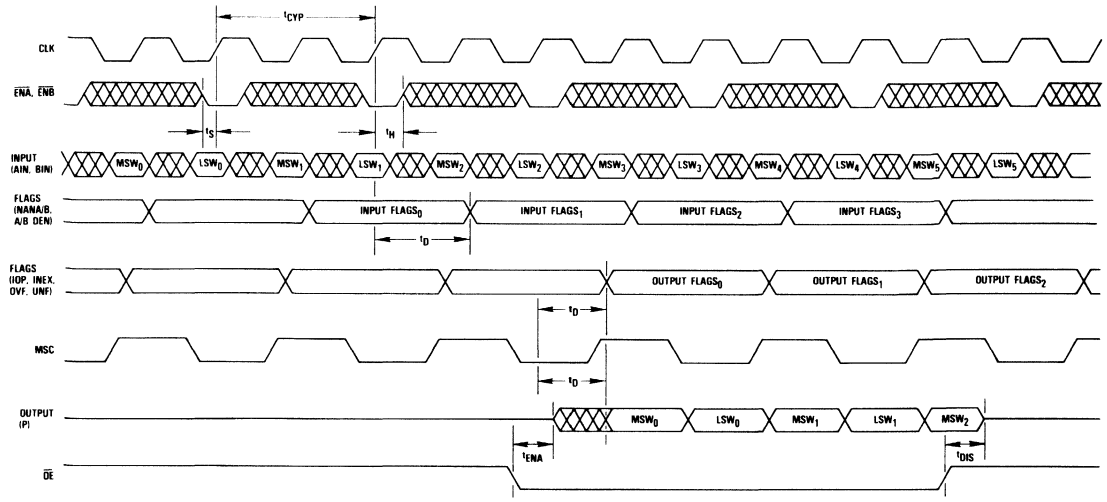


Figure 11. Equivalent Input Circuit

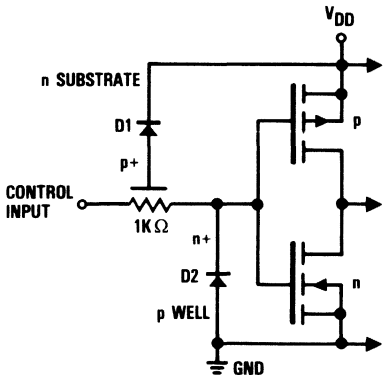


Figure 12. Equivalent Output Circuit

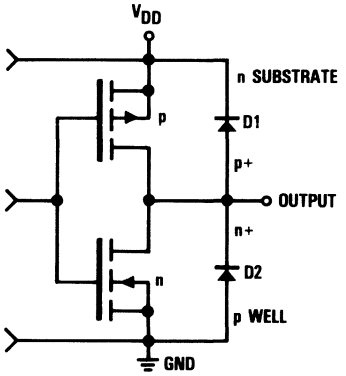
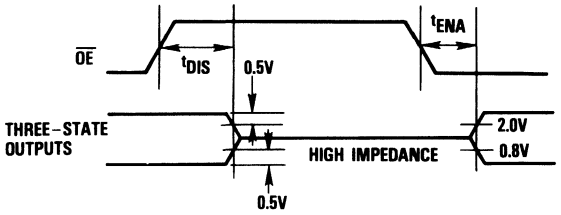


Figure 13. Threshold Levels For Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage [2]	−0.5 to (V_{DD} + 0.5)V
Forced current [3,4]	−1.0 to 6.0mA
Short circuit duration (single output in HIGH state to ground)	1 second
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

DC characteristics within specified operating conditions [1]

Parameter	Test Conditions	Temperature Range				Units
		Standard		Extended		
		Min	Max	Min	Max	
I_{DDQ} Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V, $\overline{OE}$ = 5V		20		20	mA
I_{DDU} Supply Current, Unloaded	V_{DD} = Max, f = 16MHz, $\overline{OE}$ = 5V		30		30	mA
I_{DDL} Supply Current, Loaded [2]	V_{DD} = Max, f = 16MHz, $\overline{OE}$ = 0V, C_{LOAD} = 40pF		50		50	mA
I_{IL} Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		-10		-10	μA
I_{IH} Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
V_{IL} Input Voltage, Logic LOW			0.8		0.8	V
V_{IH} Input Voltage, Logic HIGH	TMC3200	2.1		2.1		V
	TMC3201, (Except CLK)	2.2		2.2		V
	(CLK)	2.4		2.5		V
V_{OL} Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = 4mA		0.4		0.4	V
V_{OH} Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = -2mA	2.4		2.4		V
I_{OZL} Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		-40		-40	μA
I_{OZH} Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
I_{OS} Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		-100		-100	mA
C_I Input Capacitance	T_A = 25°C, f = 1MHz		15		15	pF
C_O Output Capacitance	T_A = 25°C, f = 1MHz		15		15	pF

Notes:

1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Worst case, all inputs and outputs toggling at specified rate.

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AC characteristics within specified operating conditions

Parameter	Test Conditions	Temperature Range				Units
		Standard		Extended		
		Min	Max	Min	Max	
t_{CYP} Cycle Time, Pipelined	TMC3200, V_{DD} = Min		100		100	ns
	TMC3201, V_{DD} = Min		125		135	ns
t_{CYN} Cycle Time, Non-Pipelined	TMC3200, V_{DD} = Min		200		200	ns
	TMC3201, V_{DD} = Min		250		270	ns
t_{PWL} Clock Pulse Width, LOW	V_{DD} = Min	20		20		ns
t_{PWH} Clock Pulse Width, HIGH	V_{DD} = Min	20		20		ns
t_S Input Setup Time	TMC3200, (Except $\overline{ENI}$, $\overline{ENA}$, $\overline{ENB}$)	15		20		ns
	($\overline{ENA}$, $\overline{ENB}$)	0		0		ns
	($\overline{ENI}$)	5		5		ns
	TMC3201, (Except $\overline{ENA}$, $\overline{ENB}$)	15		20		ns
	($\overline{ENA}$, $\overline{ENB}$)	0		0		ns
t_H Input Hold Time	TMC3200, (Except $\overline{ENI}$, $\overline{ENA}$, $\overline{ENB}$)	0		0		ns
	($\overline{ENI}$, $\overline{ENA}$, $\overline{ENB}$)	15		15		ns
	TMC3201, (Except $\overline{ENA}$, $\overline{ENB}$)	3		3		ns
	($\overline{ENA}$, $\overline{ENB}$)	15		15		ns
t_D Output Delay	V_{DD} = Min, C_{LOAD} = 40pF					
	TMC3200, (Except NANA, NANB)		45		50	ns
	(NANA, NANB)		65		80	ns
	TMC3201, (Except ADEN, BDEN, NANA, NANB)		45		50	ns
	(ADEN, BDEN, NANA, NANB)		100		100	ns
t_{HO} Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF	10		10		ns
t_{ENA} Three-State Output Enable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF					
	TMC3200		25		25	ns
	TMC3201		40		50	ns
t_{DIS} Three-State Output Disable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF					
	TMC3200		25		25	ns
	TMC3201		30		30	ns

Note:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC3200G5C	STD – T_A = 0°C to 70°C	Commercial	88 Pin Grid Array	3200G5C
TMC3200G5A	EXT – T_C = – 55°C to 125°C	High Reliability	88 Pin Grid Array	3200G5A
TMC3201G5C	STD – T_A = 0°C to 70°C	Commercial	88 Pin Grid Array	3201G5C
TMC3201G5A	EXT – T_C = – 55°C to 125°C	High Reliability	88 Pin Grid Array	3201G5A

TMC3202

MIL-STD-1750A Floating/Fixed-Point Accelerator

32-Bit, 10MFLOPS

The TMC3202 is a floating-point arithmetic unit and multiplier which adds, subtracts or multiplies floating-point numbers expressed in the single-precision (32-bit) MIL-STD-1750A format. The TMC3202 also supports single-precision (16-bit) integer multiplication (two's complement and unsigned) as well as conversion between fixed and floating-point formats. The TMC3202 can perform at a throughput rate of up to 10MFLOPS (Million Floating-Point Operations Per Second) in pipelined mode. In feedthrough mode (pipeline registers transparent), it will operate at a rate of up to 5MFLOPS.

All data and instruction inputs are registered. The 32-bit operands are loaded using 16-bit, half-word input buses. The input stage consists of preload registers to permit user controlled loading of the operands. The operands and controls can be loaded on the rising or falling edge of the system clock. Separate enable controls are provided to control independently the loading of AIN and BIN operands, pipeline modes and output registers. The 32-bit result is output on a 16-bit output bus as two consecutive words using synchronous and asynchronous word select and three-state controls. Three status flags are included to indicate zero, positive or negative results. Three pending interrupt flags are included to indicate floating-point overflow, floating-point underflow and fixed-point overflow. For diagnostic purposes, the internal pipeline register can be configured into a serial scan path for off-line scan testing. The TMC3202 is built using TRW's OMICRON-C™ one-micron CMOS process.

The TMC3202 floating-point arithmetic unit enhances the speed of MIL-STD-1750A processors by performing high-speed floating and fixed-point operations. Many digital signal processing algorithms such as vector operations, matrix arithmetic and Fourier Transforms, in systems which require large dynamic range and low signal-to-noise ratios, will benefit from the TMC3202.

Features

- MIL-STD-1750A 32-Bit Floating-Point Addition And Multiplication, 16-Bit Fixed-Point Multiplication
- Conversion Between 32-Bit Floating-Point And 16-Bit Integer Fixed-Point Formats
- 10MFLOPS Pipelined Throughput Rate, 5MFLOPS Feedthrough Rate
- Three-Bus Architecture For High Throughput
- Selectable Pipelining With One, Two Or Three Register Latency
- Serial Scan Mode For Diagnostics (Pipeline Register)
- Selectable Positive Edge Or Two-Phase I/O Clocking
- All Inputs And Outputs Registered And TTL Compatible
- Low Power CMOS Construction
- Available In An 84 Leaded Ceramic Chip Carrier

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Applications

- Matrix Operations And Geometric Transforms
- Arithmetic Element In Microprogrammed Array Processors
- Floating-Point Digital Filters
- Fast Fourier Transforms
- Radar And Sonar Signal Processors
- Co-Processor To 1750A Microprocessors

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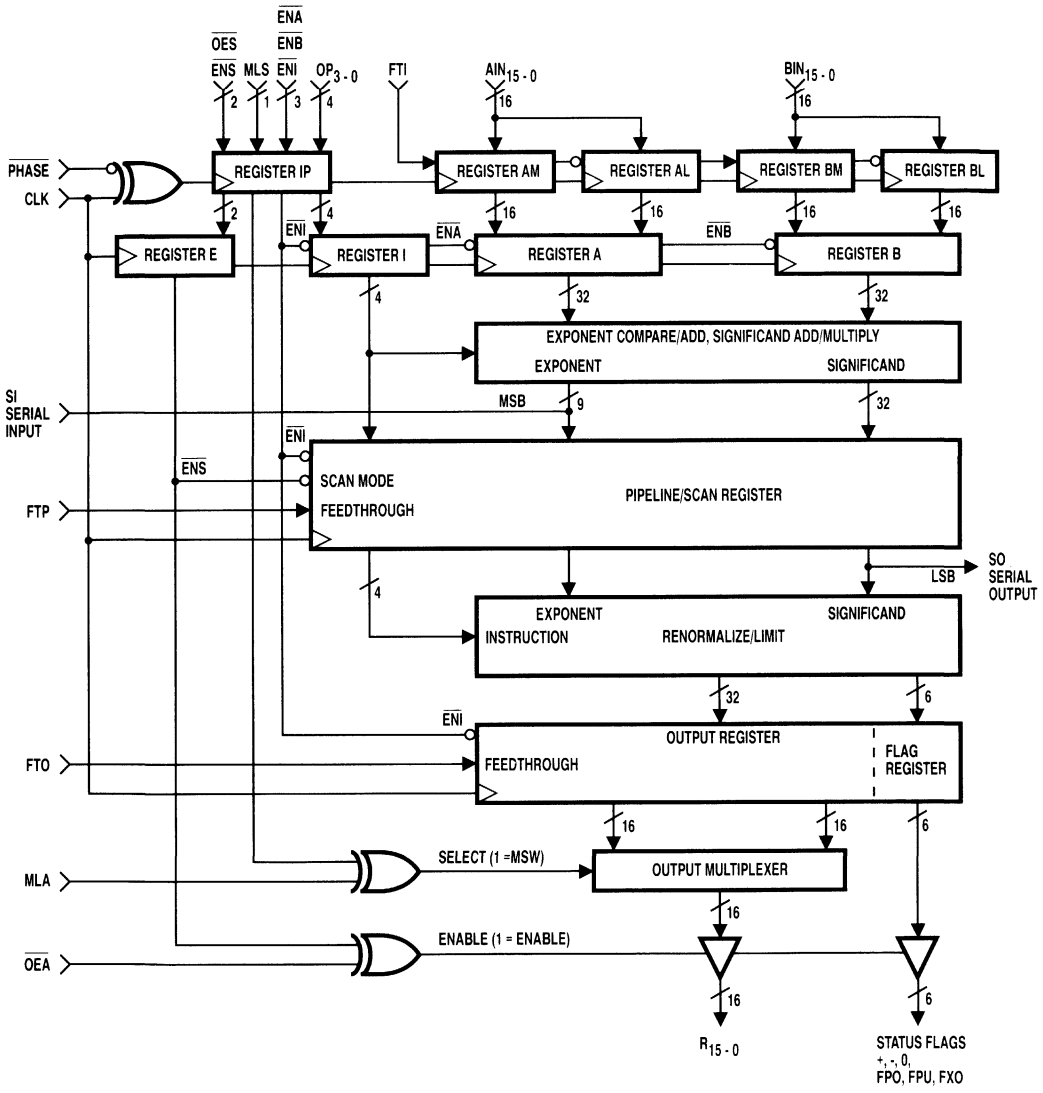
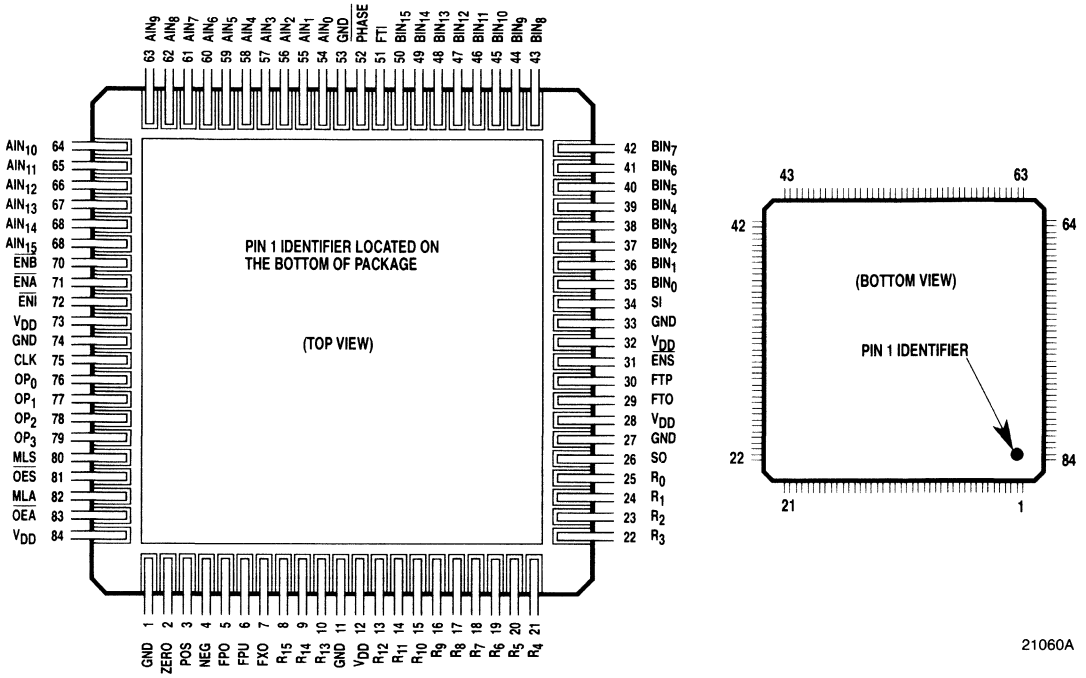
FAX: (619) 455-6314

40G02177 Rev. D – 11/90
Printed in the U.S.A.

Functional Block Diagram



Pin Assignments – 84 Leaded Ceramic Chip Carrier, L3 Package



Functional Description

General Information

The TMC3202 consists of five sections: input registers, arithmetic block, pipeline/scan register, renormalize/limit section and the output register/multiplexer.

Input Section

The input section consists of the operand and instruction/control preload registers, main registers, and the clock phase control.

The input section loads the operands, the enables and the 4-bit instruction word. All operands and synchronous controls are loaded into preload registers before being transferred to the main instruction and operand registers on the subsequent rising edge of CLK. The 32-bit A and B operands are input on 16-bit wide buses. Operand loading is controlled by the enables ($\overline{ENA}$, $\overline{ENB}$), the input feedthrough (FTI) and the clock phase ($\overline{PHASE}$) controls.

The $\overline{PHASE}$ input allows the user to load the preload registers on either the rising edge or falling edge of the system clock. When the $\overline{PHASE}$ input is HIGH, the preload clock and the system clock are "in phase" and preload registers are loaded on the rising edge of CLK. $\overline{PHASE}$ = LOW causes the preload registers to be loaded on the falling edge of CLK (preload clock becomes $\overline{CLK}$). This control allows the user to input full 32-bit operands during one clock period (see *Timing*).

The input feedthrough control (FTI) determines the loading sequence for the A and B operands (MSW or LSW first), while the register enables ($\overline{ENA}$, $\overline{ENB}$) control the loading of the 32-bit A and B operands into the main registers. To load Register A/B, the first 16 bits are loaded into the preload register (MSW or LSW), with $\overline{ENA}$/$\overline{ENB}$ set LOW. The second half of the operand is then placed on the AIN and BIN input bus.

Input Section (cont.)

The following rising edge of CLK causes the data in the preload register and the data on the AIN (BIN) bus to be strobed into the 32-bit main operand register.

Preload registers are also included for the instruction (OP_{3-0}), synchronous output controls ($\overline{OES}$, MLS) and the scan enable ($\overline{ENS}$). The Op Code register is used to align instructions with data. Loading is controlled by the instruction enable ($\overline{ENI}$). When $\overline{ENI}$ is LOW, the instruction register is loaded on the next rising edge of CLK and all pipeline registers are enabled. When $\overline{ENI}$ is HIGH, loading of the instruction and pipeline registers is disabled for the next clock rising edge, allowing execution to be suspended. The $\overline{ENS}$ and $\overline{OES}$ inputs are always loaded on the rising edge of CLK.

Table 1. Preload Register Operation

Inputs			Preload Register Action		
CLK	$\overline{PHASE}$	FTI	AM, BM	AL, BL	IP (Instruction)
⌝⌞	0	0	load	pass	load
⌝⌞	0	1	pass	load	load
⌝⌞	1	0	hold	pass	hold
⌝⌞	1	1	pass	hold	hold
⌞⌜	1	0	load	pass	load
⌞⌜	1	1	pass	load	load
⌞⌜	0	0	hold	pass	hold
⌞⌜	0	1	pass	hold	hold

Table 2. Main Register Operation

Inputs				Register Operation		
CLK	$\overline{ENI}$	$\overline{ENA}$	$\overline{ENB}$	Reg I	Reg A	Reg B
⌞⌜	0	1	1	load	hold	hold
⌞⌜	1	0	1	hold	load	hold
⌞⌜	1	1	0	hold	hold	load
⌞⌜	1	1	1	hold	hold	hold
⌝⌞	x	x	x	hold	hold	hold

Other controls are provided for selection of pipelining and serial scan modes. The internal pipeline register and the output register can each be set for pipelined or feedthrough modes. Setting FTP HIGH makes the internal pipeline register transparent and a HIGH on FTO causes the output register to be transparent. A LOW on either of the inputs enables the respective register. These controls allow the user to select one, two or three register delay operation. Changing the feedthrough controls (FTI, FTP, FTO) during operation is not recommended. Doing so may cause undefined operation and results.

The $\overline{ENS}$ control is used to select the scan mode for the internal pipeline register. When $\overline{ENS}$ is LOW, the parallel pipeline register becomes a serial shift register for test and diagnostics. Detailed operation and formats are discussed under the *Pipeline/Scan Register* section.

Arithmetic Block

The arithmetic block performs the operation defined by the instruction Op Code (OP_{3-0}). For multiply operations the exponents of the A and B operands are added and the significands multiplied together before being passed to the pipeline register.

For addition and subtraction, the operand with the smaller exponent will have its significand right shifted and its exponent incremented until the two exponents match. Once the significands are aligned they are added/subtracted and the result passes to the pipeline register.

Detailed operation of each instruction is described in *Table 3*.

Table 3. TMC3202 Instruction Operation

OP_{3-0}	Function	A-Data	B-Data	Result	Operation
0000	A + B	FP	FP	FP	Floating-point addition. Result truncated towards negative infinity (per MIL-STD-1750A).
0001	A x B	TC	TC	TC	Multiply 16-bit two's complement integers (uses MSW data fields), with 32-bit two's complement result.
0010	A x B	TC	TC	TC [1]	Multiply 16-bit two's complement integers (MSW data field), with 16-bit TC result. Fixed-point overflow for products less than 8000_H or greater than $7FFF_H$.
0011	A x B	FP	FP	FP	Floating-point multiply.
0100	A − B	FP	FP	FP	Subtract B from A in floating-point, truncate result towards negative infinity (per MIL-STD-1750A).
0101	A x B	TC	UM	TC	Mixed mode integer multiplication with 32-bit two's complement result.
0110	FLOAT B	X	TC	FP	Convert 16-bit fixed-point B to a 32-bit floating-point value with truncation towards 0 (per MIL-STD-1750A).
0111	ABS B	X	FP	FP	Absolute value of B. Positive numbers passed, negative numbers two's complemented. ABS value of $(800000\ 7F)_H$ is $(7FFFFF\ 7F)_H$ with FPO flag set.
1000	−A + B	FP	FP	FP	Subtract A from B in floating-point, truncate result towards negative infinity (per MIL-STD-1750A).
1001	A x B	UM	TC	TC	Mixed mode integer multiplication with 32-bit two's complement result.
1010	DEN B	FP	FP	FP	Right shift (with sign extension) the significand of B according to (Exp A—Exp B), truncating towards negative infinity.
1011	NEG B	X	FP	FP	Two's complement B operand. $(800000\ 7F_H \rightarrow 7FFFFF\ 7F_H$ with floating-point overflow, $400000\ 80_H \rightarrow 000000\ 00_H$ with floating-point underflow).
1100	COMP(A, B)	FP	FP	X	Subtract B from A in floating-point and update flags. (Note: R_{15-0} Output is undefined.)
1101	A x B	UM	UM	UM	Unsigned integer multiplication with 32-bit unsigned magnitude result.
1110	FIX B	X	FP	TC	Convert floating-point B to 16-bit two's complement integer, truncating towards 0 (per MIL-STD-1750A). FXO flag set for EXP B>15.
1111	NORM B	X	FP	FP	Normalize floating-point B operand. Normalized numbers are passed unchanged, denormalized numbers are normalized before being output.

ZERO	POS	NEG	Result
0	1	0	A>B
0	0	1	A<B
1	0	0	A = B

Notes:
1. Integer multiplication with the least-significant 16-bits of the product output on the MSW cycle of R_{15-0}.
2. Abbreviations: FP — 32-bit floating-point numbers represented in MIL-STD-1750A format.
   TC — 16-bit fixed-point, two's complement numbers (MIL-STD-1750A) input on MSW (LSW ignored).
   UM — 16-bit fixed-point, unsigned magnitude numbers input on MSW.
   X — Don't Care.

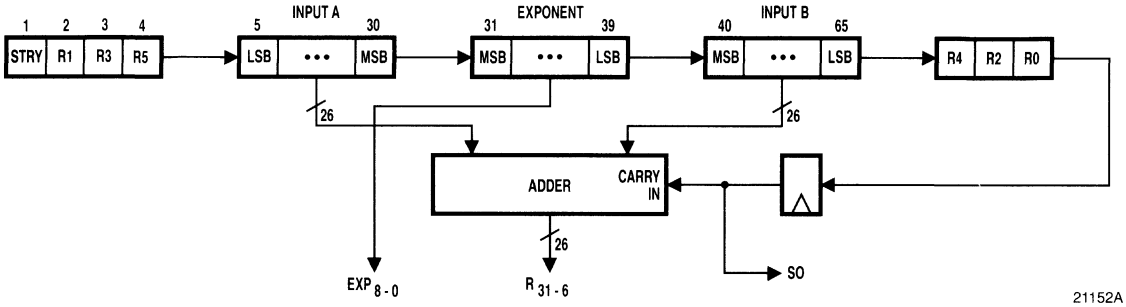
Pipeline/Scan Register

The pipeline/scan register is used to store the partial product of the arithmetic block and for serial scan testing. This register can be made transparent (feed-through operation) by setting FTP HIGH. When FTP is LOW, the register is enabled. In pipelined mode, the data will hold when $\overline{ENI}$ is HIGH and be updated on the rising edge of CLK when $\overline{ENI}$ is LOW.

Setting $\overline{ENS}$ LOW converts the data portion of the pipeline register into a serial shift (SCAN) register. The instruction portion of the register (OP_{3-0}) remains in parallel mode. This feature allows the user to shift out the current pipeline register contents and shift in/out arbitrary bit patterns for test and device verification.

The pipeline/scan register is a 69-bit register with the format shown in *Figure 1*. Serial inputs are loaded through the SI input with the appropriate setup and hold time requirements while the serial output of the register is available on the SO output. The user may load inputs through the normal operand registers and shift out the current contents of the scan register or may load diagnostic values into the register and read the output of the TMC3202 to verify logic. Values shifted into the register are used to form the result output as shown by *Figure 1*.

Figure 1. Scan Register Format



Renormalize/Limit Section

The renormalize/limit section normalizes the significand of the result, detects and generates flags for exception conditions, and sets the result to maximum or minimum values for overflow and underflow respectively. To normalize floating-point results, the significand is shifted left and the exponent decremented by one for each position shift until the first two bits of the significand differ. If the exponent reaches its minimum value before the significand is normalized, underflow occurs, both the significand and exponent are set to zero, the ZERO and floating-point underflow flags (FPU) are set HIGH.

Floating-point results which have exponents of greater than $7F_H$ set the floating-point overflow flag (FPO) HIGH and then force the result to 7FFFFF $7F_H$ for positive overflow and 800000 $7F_H$ for negative overflow.

Fixed-point multiplication with a 32-bit result can never cause an overflow. A fixed-point overflow (FXO) will occur, however, in integer multiplication with a 16-bit result when the product exceeds $7FFF_H$ for positive or 8000_H for negative results. Fixed-point overflows may also occur as a result of the DENormalize instruction when Exp B > Exp A, or the FIX instruction when Exp B > 15.

Output Multiplexer, Registers and Drivers

The 32-bit output register and 6-bit flag register are clocked by the rising edge of CLK and enabled by $\overline{ENI}$. The result is output through the three-state 16-bit output port. This port uses a 2-to-1 output multiplexer to select between the MSW or LSW. Selection of MSW or LSW is done using either the synchronous (MLS) or asynchronous (MLA) mux select controls. The data and status flags are enabled and disabled using the synchronous and asynchronous output enable controls $\overline{OES}$ and $\overline{OEA}$.

Output Multiplexer, Registers and Drivers (cont.)

The output register can be made transparent for feedthrough operation using the Feedthrough Output (FTO) control (FTO = HIGH). In pipelined mode (FTO = LOW), the output register is clocked on the rising edge of CLK if the enable ($\overline{ENI}$) was LOW during the previous preload clock. It holds if $\overline{ENI}$ was HIGH.

Signal Definitions

Power

V_{DD}, GND — The TMC3202 operates from a single +5V supply. All power and ground lines must be connected.

Data Inputs

AIN_{15-0} — AIN is the 16-bit input bus for the A operand. Both the MSW and LSW of the operand are loaded through this bus.

BIN_{15-0} — BIN is the 16-bit input bus for the B operand. Both the MSW and LSW of the operand are loaded through this bus.

SI — Serial input to the pipeline register. This input allows data to be serially loaded into the pipeline register for test and diagnostics. Data is shifted in on the rising edge of CLK.

Data Outputs

R_{15-0} — The three-state R-bus is used to output results from the TMC3202. The output multiplexer selects between MSW and LSW outputs and the three-state controls are used to activate the bus.

SO — Serial output data. SO is the value shifted out of the pipeline register when in serial mode ($\overline{ENS}$ = LOW). Data are shifted out on the rising edge of CLK. This output is always active.

Clock

CLK — The TMC3202 is operated using a single, TTL compatible clock for all internal operations. Data are loaded into preload registers on the rising or falling edge of CLK. All other internal operations are referenced to the rising edge. When $\overline{PHASE}$ is set LOW, the preload registers are loaded on the falling edge of CLK.

Controls

$\overline{PHASE}$ — $\overline{PHASE}$ determines the clock edge for the preload registers. If $\overline{PHASE}$ is HIGH, the preload registers are loaded on the rising edge of CLK. If $\overline{PHASE}$ is LOW, the preload registers are loaded on the falling edge of CLK. Setting $\overline{PHASE}$ LOW allows 32-bit operands to be loaded in a single clock cycle (16-bit loading on each rising and falling edge).

$\overline{ENA}$ — $\overline{ENA}$ is a registered enable for register A. This input is loaded into the IP preload register. When HIGH it enables loading of the operand into the main register on the first CLK rising edge following the preload clock.

$\overline{ENB}$ — $\overline{ENB}$ is a registered enable for register B. This input is loaded into the IP preload register. When HIGH it enables loading of the operand into the main register on the first CLK rising edge following the preload clock.

$\overline{ENI}$ — $\overline{ENI}$ is a registered enable for the instruction, pipeline, and output registers. This input is loaded into the IP preload register. It determines operation on the next rising edge of CLK. When HIGH on the previous preload clock, internal operation will be disabled for the next rising edge of CLK. When LOW, operation is enabled.

$\overline{ENS}$ — $\overline{ENS}$ is a registered enable for the serial scan mode. It converts the parallel pipeline register into a 69-bit serial input, serial output shift register to allow testing of the internal logic. The instruction pipeline remains in parallel mode. It takes effect one ($\overline{PHASE}$ = HIGH) or two ($\overline{PHASE}$ = LOW) clock cycles after being set LOW.

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Controls (cont.)

$\overline{OEA}$, $\overline{OES}$ Asynchronous ($\overline{OEA}$) and synchronous ($\overline{OES}$) output enables. $\overline{OES}$ is a registered control which enables the result and status flag output drivers. $\overline{OES}$ is loaded into the IP preload register and internally registered. $\overline{OEA}$ is the unregistered, asynchronous control. These inputs are exclusive-ORed to enable the output. When they differ (XOR($\overline{OES}$, $\overline{OEA}$) = 1) the outputs are enabled; when they are equal (XOR($\overline{OES}$, $\overline{OEA}$) = 0) the output is in high-impedance. In normal operation, one signal is wired HIGH or LOW and the other is used as the output enable.

MLA, MLS Asynchronous (MLA) and synchronous (MLS) output mux selects. MLS is a registered control for the selection of MSW or LSW. MLS is loaded by the preload clock. MLA is an unregistered, asynchronous select. These inputs are exclusive-ORed to select the 16-bit output word. When they are equal (XOR(MLS, MLA) = 0) the LSW is output, when they differ (XOR(MLS, MLA) = 1) the MSW is output. In normal operation, one signal is wired HIGH or LOW and the other used as the output mux select.

$OP_{3\text{-}0}$ Instruction operation code. These bits determine the operation to be performed by the TMC3202 (see ***Table 3***). The instruction is first placed into the preload register, then loaded into the main instruction register if $\overline{ENI}$ was LOW on the previous preload clock.

FTI Feedthrough control for the A and B operand preload registers. FTI determines the loading sequence for the main operand register. When FTI is LOW, the MSW (AM, BM) is loaded into the preload register first. When FTI is HIGH, the LSW (AL, BL) is loaded first.

FTP Feedthrough control for the internal pipeline register. When FTP is HIGH, the pipeline register is transparent. This control should not be changed during operation.

FTO Feedthrough control for the output register. When FTO is HIGH, the output register is transparent. This control should not be changed during operation.

Status Outputs

FPO The floating-point overflow flag indicates that the exponent of the floating-point result has exceeded $7F_H$. This flag can be used to generate a "pending interrupt" to the 1750A processor.

FPU The floating-point underflow flag indicates that the floating-point result is too small to be normalized but is not precisely zero. When this flag is HIGH, the output has been forced to zero by the limiter. This flag can be used to generate a "pending interrupt" to the 1750A processor.

FXO Fixed-point overflow flag indicates that the 16-bit multiplication result exceeds $7FFF_H$ (maximum positive) or is less than 8000_H (maximum negative). This flag will also be set for DEN instructions when Exp B > Exp A, and for FIX instructions when Exp > 15.

ZERO This flag is set HIGH if the result of any operation results in zero (floating-point or fixed-point). Both the exponent and significand are set to zero. This flag is also set for underflow conditions, in which the limiter forces the output to zero.

POS This flag indicates that the result is greater than zero.

NEG This flag indicates that the result is less than zero.

Package Interconnections

Signal Type	Signal Name	Function	L3 Package Pins
Power	V_{DD}	Supply Voltage	12, 28, 33, 73, 84
	GND	Ground	1, 11, 27, 32, 52, 74
Data Input	AIN_{15-0}	A Input	69, 68, 67, 66, 65, 64, 63, 62, 61, 60, 59, 58, 57, 56, 55, 54
	BIN_{15-0}	B Input	50, 49, 48, 47, 46, 45, 44, 43, 42, 41, 40, 39, 38, 37, 36, 35
	SI	Serial Data Input	34
Data Output	R_{15-0}	Result Output	8, 9, 10, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25
	SO	Serial Data Output	26
Clock	CLK	Clock	75
Controls	$\overline{PHASE}$	Clock Phase Control	52
	$\overline{ENA}$	Register A Enable	71
	$\overline{ENB}$	Register B Enable	70
	$\overline{ENI}$	Instruction Register Enable	72
	$\overline{ENS}$	Serial Mode Enable	31
	$\overline{OEA}$, $\overline{OES}$	Output Enables	83, 81
	MLA, MLS	Output Mux Selects	82, 80
	OP_{3-0}	Instruction Op Code	79, 78, 77, 76
	FTI	Input Feedthrough Control	51
	FTP	Pipeline Feedthrough	30
	FTO	Output Feedthrough	29
Flags	FPO	Floating-Point Overflow	5
	FPU	Floating-Point Underflow	6
	FXO	Fixed-Point Overflow	7
	ZERO	Zero Flag	2
	POS	Positive Flag	3
	NEG	Negative Flag	4

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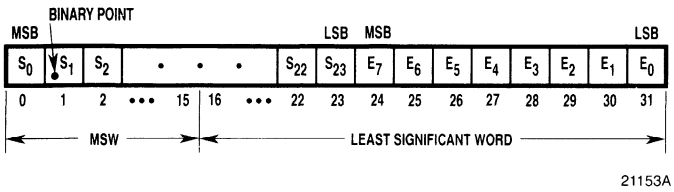
Data Formats

The TMC3202 conforms to MIL-STD-1750A (notice 1, May 1982) data format for single precision floating-point and 16-bit fixed-point arithmetic. The TMC3202 also performs multiplication on unsigned, 16-bit integer numbers.

Figure 2. MIL-STD-1750A 32-Bit Floating-Point Format



The numerical value of a 1750A floating-point number can be interpreted as:

$$\text{Number} = F \cdot 2^{E}$$

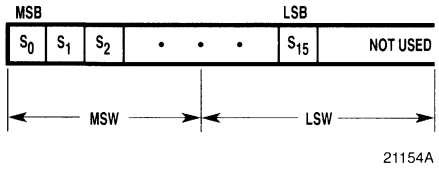
The two's complement, fractional part (F) is interpreted as:

$$F = (-2^{0}) \cdot S_0 + \sum_{n=1}^{23} S_n \cdot (2^{-n})$$

The exponent, represented as two's complement integer, is interpreted as:

$$E = (-2^{-7}) \cdot E_7 + \sum_{n=0}^{6} E_n \cdot (2^{n})$$

Figure 3. MIL-STD-1750A 16-Bit Fixed-Point Format



The TMC3202 supports the MIL-STD-1750A 16-bit fixed-point multiplication and conversion between fixed and floating-point formats. These operations ignore the data on the least-significant-half (LSW) of the 32-bit data. The 1750A single precision, fixed-point format is a 16-bit two's complement number, interpreted as:

$$\text{Number} = (-2^{15}) \cdot S_0 + \sum_{n=1}^{15} S_n \cdot 2^{(15-n)}$$

Timing

The following diagrams show timing for various modes of operation. Input timing is independent of the number of internal pipeline delays and dependent only on selection of single phase (rising edge loading) or two phase (rising and falling edge) input clocking.

$\overline{\text{PHASE}}$ = FTP = FTO = HIGH

This mode uses registered inputs while the pipeline and output registers are in feedthrough mode. On cycle-2 the enable controls are set LOW and MSW_0 and INS_0 are loaded into preload registers. The next cycle loads LSW_0 and MSW_0 into main operand registers. The user must wait for the output delay (t_D) before the result output becomes valid. When using the synchronous mux select (MLS), the device requires two cycles to output a full 32-bit result. The maximum operating speed is limited by the output delay time (t_D). In *Figure 4*, cycle-3 loads the operand register and the output becomes valid after t_D. The following cycle loads the MSW_1 into preload registers and outputs the second half of result 0.

Use of the asynchronous mux select (MLA) may allow the user to operate the device at higher speeds than the t_{CY} specified for FTP = FTO = HIGH. Two phase clocking may be preferred when using feedthrough mode (see *Figure 7*).

$\overline{\text{PHASE}}$ = FTP = HIGH, FTO = LOW

This mode registers the inputs and has one internal pipeline delay. For applications using one pipeline, enabling the output register (FTO = LOW) is recommended. The mode FTO = HIGH and FTP = LOW is not recommended since no increase in speed is obtained and the internal logic delays are greater. Two cycles are required to load the 32-bit operands (cycles 1 and 2) and the first result appears on the output two cycles (cycle 4) plus an output delay (t_D) later.

$\overline{\text{PHASE}}$ = HIGH, FTP = FTO = LOW

All internal registers are enabled in this mode. Inputs are loaded on cycles 1 and 2 and the first result is available on the output four cycles (cycle 6) plus an output delay (t_D) later.

$\overline{PHASE}$ = LOW, FTP = FTO = HIGH

This mode allows the user to load the full 32-bit input in one clock period. The first 16 bits (MSW_0) are loaded into preload registers on the falling edge of CLK. The next rising edge loads the preload register and the LSW data into the main register. The output is valid after the delay time (t_D) for FTP = FTO = HIGH. Synchronous output controls ($\overline{OES}$ and MLS) are sampled on the clock falling edge only. The user may prefer to use the asynchronous controls for this mode.

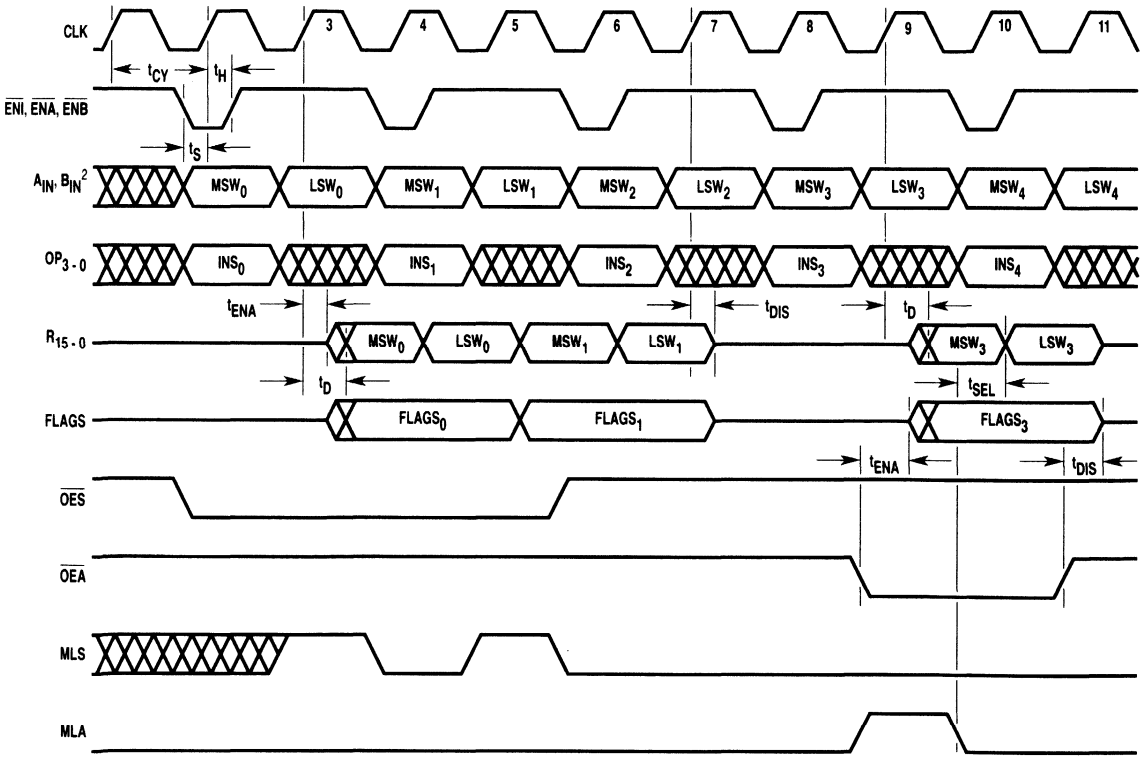
FTP = HIGH, $\overline{PHASE}$ = FTO = LOW

Controls and the first data words are loaded on the falling edge of CLK. The next rising edge loads the 32-bit operand registers and the result is available on the output one cycle (cycle 2) and an output delay (t_D) later. Use of FTP = LOW and FTO = HIGH is not recommended since there is no increase in speed and internal logic delays are greater.

$\overline{PHASE}$ = FTP = FTO = LOW

Controls are sampled and loaded on the CLK falling egde along with the first half of the data inputs. The next rising edge loads the 32-bit operand registers and the result is available on the output two cycles (cycle 2) and an output delay later.

Figure 4. Timing Diagram, Feedthrough Mode, Single Phase Clocking



Notes: 1. FTI = LOW, $\overline{ENS}$, $\overline{PHASE}$, FTP, FTO = HIGH.
2. For FTI = HIGH, MSW and LSW are reversed.

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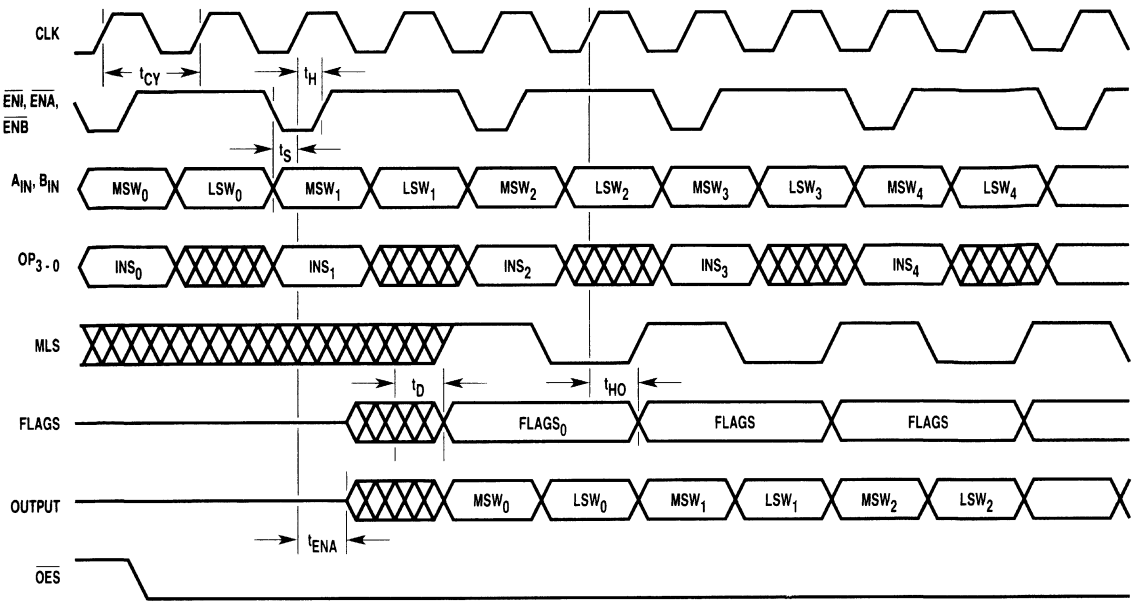
Figure 5. Timing Diagram, One Pipeline, Single Phase Clocking



Notes:
1. FTI = LOW.
2. $\overline{OEA}$, MLA, $\overline{ENS}$, $\overline{PHASE}$ = HIGH, FTO = LOW and FTP = HIGH.
3. FTO = HIGH, FTP = LOW not recommended.

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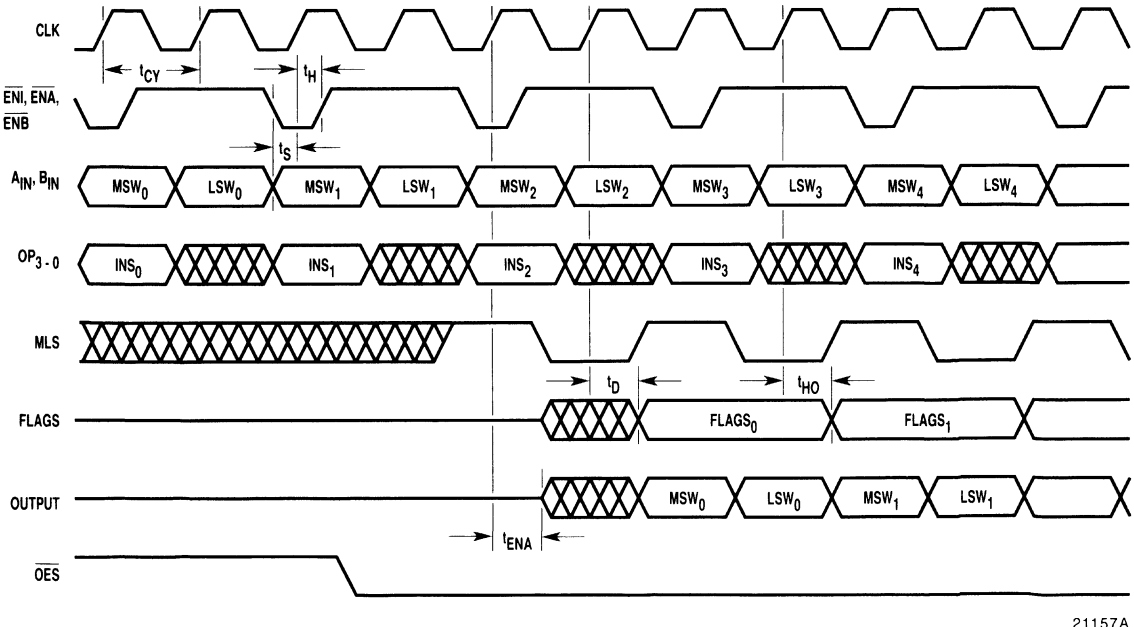
Figure 6. Timing Diagram, Two Pipeline, Single Phase Clocking



Notes:
1. FTI, FTO, FTP = LOW.
2. $\overline{OEA}$, MLA, $\overline{ENS}$, $\overline{PHASE}$ = HIGH.

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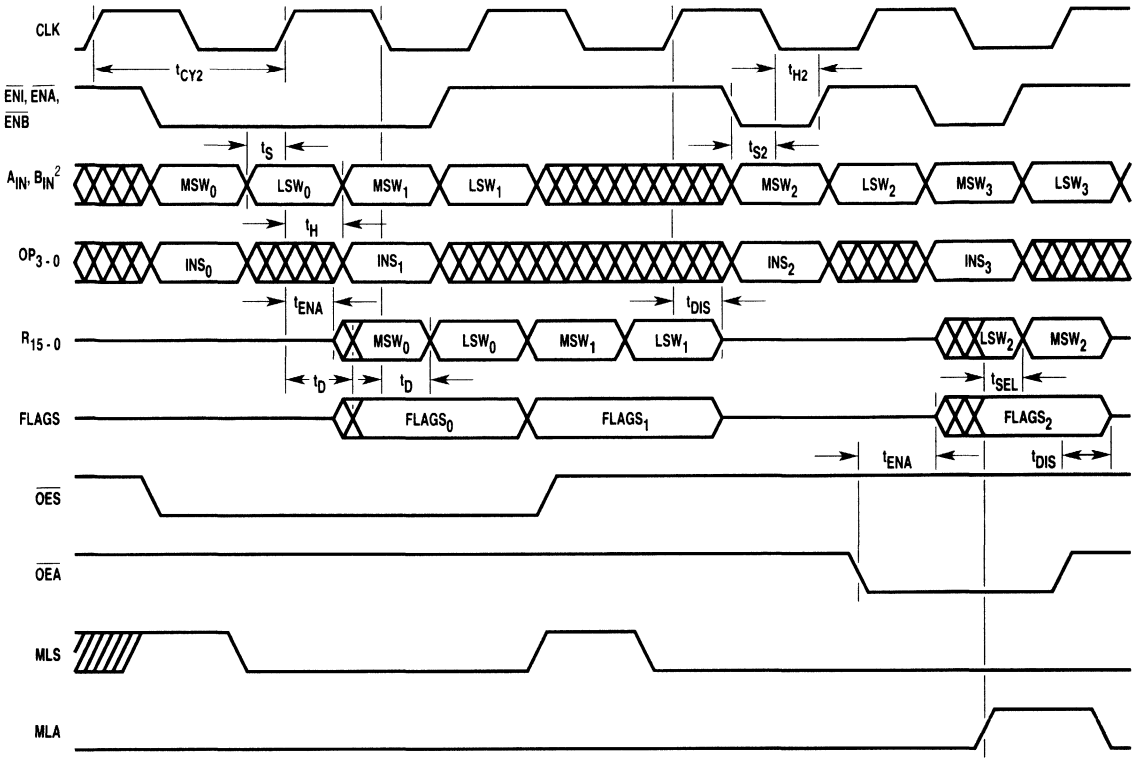
Figure 7. Timing Diagram, Feedthrough Mode, Two Phase Clocking



Notes: 1. FTI, $\overline{PHASE}$ = LOW, FTP, FTO = HIGH.
2. For FTI = LOW, MSW and LSW are reversed.

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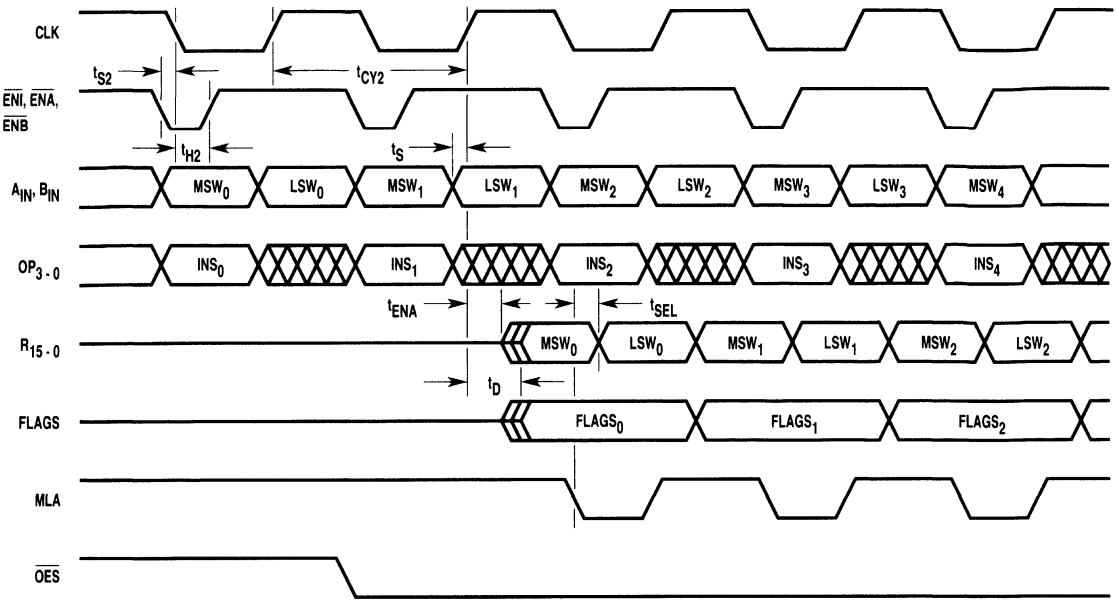
Figure 8. Timing Diagram, One Pipeline, Two Phase Clocking



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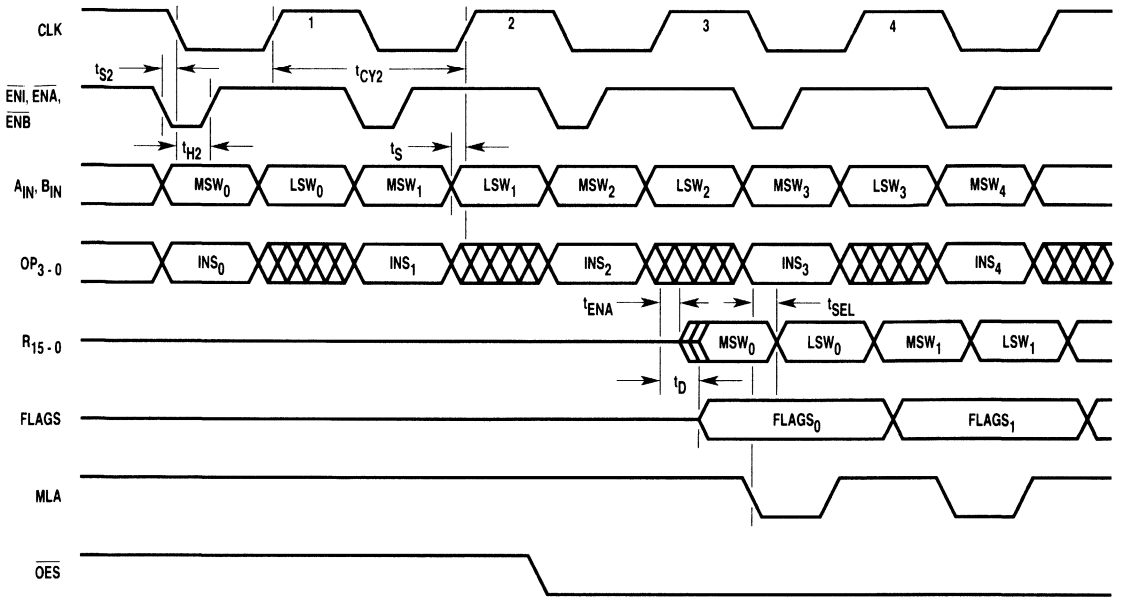
Notes:
1. FTI, $\overline{PHASE}$, MLS = LOW, $\overline{OEA}$, $\overline{ENS}$ = HIGH.
2. FTP = HIGH, FTO = LOW.
3. FTP = LOW, FTO = HIGH not recommended.

Figure 9. Timing Diagram, Two Pipeline, Two Phase Clocking



Note: 1. FTI, $\overline{PHASE}$, MLS, FTP, FTO = LOW, $\overline{OEA}$, $\overline{ENS}$ = HIGH.

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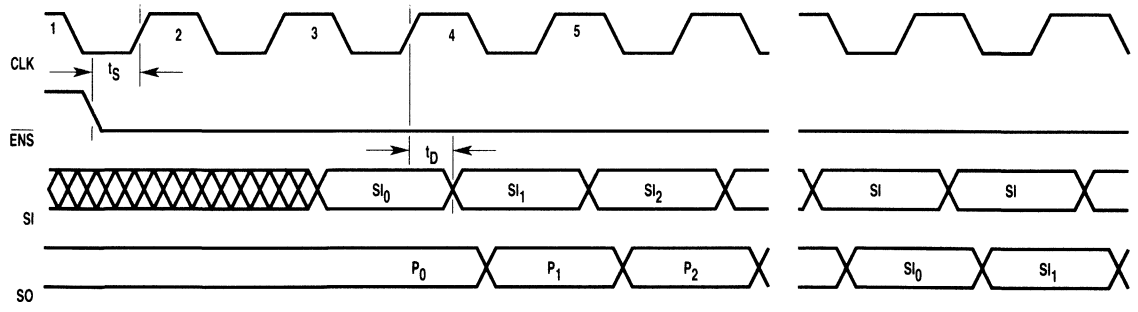
Figure 10. Scan Register Timing



Note: 1. $\overline{PHASE}$ = HIGH.

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Figure 11. Equivalent Input Circuit

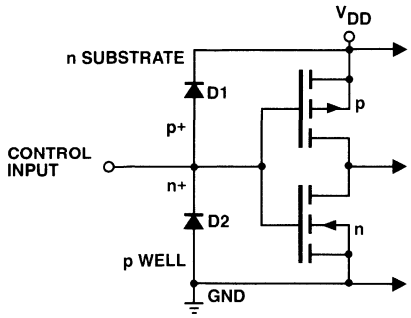


Figure 12. Equivalent Output Circuit

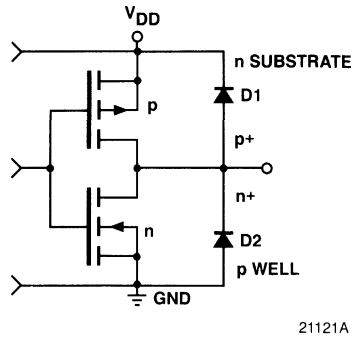
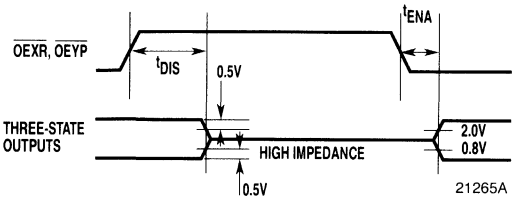


Figure 13. Threshold Levels for Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5V)
Output	
Applied voltage [2]	−0.5 to (V_{DD} + 0.5V)
Forced current [3,4]	−6.0 to 10.0mA
Short-circuit duration (single output in HIGH state to ground)	1 Second
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	15			15			ns
t_{PWH}	Clock Pulse Width, HIGH	15			15			ns
t_S	Input Setup Time to CLK HIGH	20			20			ns
$t_{S(L)}$	Input Setup Time to CLK LOW ($\overline{PHASE}$ = HIGH)	20			20			ns
t_H	Input Hold Time to CLK HIGH	3			3			ns
$t_{H(L)}$	Input Hold Time to CLK LOW ($\overline{PHASE}$ = HIGH)	5			5			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			8.0			8.0	mA
I_{OH}	Output Current, Logic HIGH			−4.0			−4.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range Standard/Extended		Units
			Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, $\overline{OEA}$ = 5V, f = 20MHz		100	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		−10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = 8mA		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = −4mA	2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		−40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		−100	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10	pF

Note: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard/Extended Min	Temperature Range Standard/Extended Max	Units
t_{CY}	Cycle Time, Single Phase Clock	V_{DD} = Min, FTP = L, FTO = L, $\overline{PHASE}$ = H		50	ns
		V_{DD} = Min, FTP = H, FTO = L, $\overline{PHASE}$ = H		100	ns
		V_{DD} = Min, FTP = H, FTO = H, $\overline{PHASE}$ = H		200	ns
t_{CY2}	Cycle Time, Two Phase Clock	V_{DD} = Min, FTP = L, FTO = L, $\overline{PHASE}$ = L		75	ns
		V_{DD} = Min, FTP = H, FTO = L, $\overline{PHASE}$ = L		100	ns
		V_{DD} = Min, FTP = H, FTO = H, $\overline{PHASE}$ = L		200	ns
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 25pF			
		FTO = LOW		35	ns
		FTO = HIGH		200	ns
t_{SEL}	MLA Select to Output	V_{DD} = Min, C_{LOAD} = 25pF		55	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 25pF		5	ns
t_{ENA}	Three-State Output Enable Delay [1]	V_{DD} = Min, C_{LOAD} = 25pF			
		$\overline{OES}$ (Synchronous Enable)		35	ns
		$\overline{OEA}$ (Asynchronous Enable)		35	ns
t_{DIS}	Three-State Output Disable Delay [1]	V_{DD} = Min, C_{LOAD} = 40pF			
		$\overline{OES}$ (Synchronous Enable)		35	ns
		$\overline{OEA}$ (Asynchronous Enable)		25	ns

Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC3202L3C	STD – T_A = 0°C to 70°C	Commercial	84 Leaded Ceramic Chip Carrier	3202L3C
TMC3202L3V	EXT – T_C = – 55°C to 125°C	MIL-STD-883	84 Leaded Ceramic Chip Carrier	3202L3V

TMC3210

CMOS Floating-Point Divider
32-Bit, 2.5MFLOPS

The TMC3210 is a CMOS monolithic device which is capable of performing a full 32-bit floating-point division in
400 nanoseconds. The floating-point device divides normalized numbers expressed in IEEE 32-bit single-precision format and can also accommodate denormalized operands if they are first "wrapped" by a companion TMC3033 arithmetic unit. The user can select either FAST mode (output zero) or IEEE mode (output a wrapped quotient) to handle underflows. With wrapping and unwrapping externally provided, the TMC3210 is fully compliant with the number format and single-precision division operation described in Version 10.0 of IEEE Standard 754. The TMC3210 is built using TRW's OMICRON-C™ one-micron CMOS process.

All data and instruction inputs are registered. The two input operands (divisor and dividend) are each loaded in two 16-bit words through the dedicated half-width bus and the output is produced in two 16-bit words through the dedicated output port. With a clock rate of 20MHz, the divider has a 2.5 Megaflop pipelined throughput rate with a latency on any given operation of 6 internal clock cycles (600ns). Renormalizing, rounding and limiting functions are all generated per IEEE specification. The output quotient and status flag ports are driven by three-state buffers.

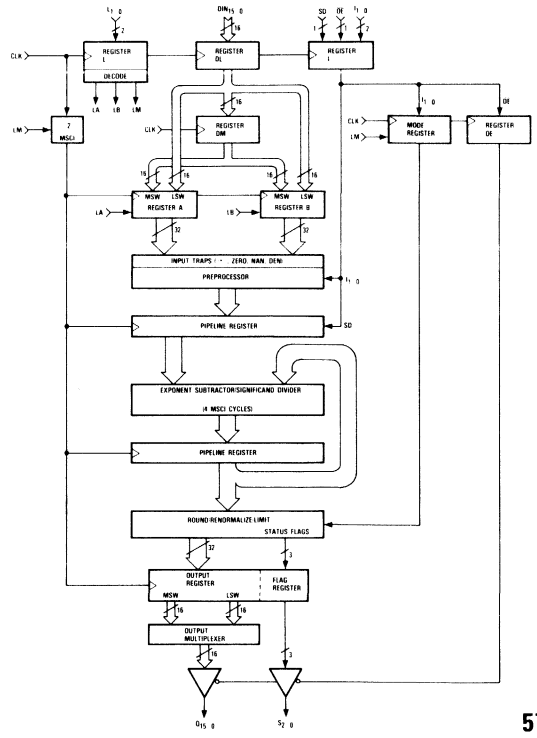
Features

- IEEE Standard 754 Version 10.0 32-Bit Floating-Point Data Format
- 20MHz Bus Clock Rate; 2.5 Megaflop Pipelined Throughput Rate
- IEEE Unbiased Round To Nearest, Round Toward Zero, Round Toward Positive Infinity And Round Toward Negative Infinity Modes
- Supports Denormalized Operands/Results Through "Wrapping/Unwrapping" By External TMC3033 Arithmetic Unit
- Two-Bus Architecture (Dedicated Input And Output) Works With Single Bus Or Data Flow Systems
- IEEE Exception Flags Including Inexact Result, Overflow, Underflow, Divide By Zero, Invalid Operation And Denormalized Operands
- Automatic Limiting For Overflow Or Underflow
- Input Traps For Infinity, Zero, Not-A-Number And Denormalized Operand
- All Inputs And Outputs Registered And TTL Compatible
- Low Power CMOS Construction
- Available In A 48 Pin Hermetic Ceramic DIP

Applications

- Graphics And Image Processors
- Solids Modeling
- Matrix Operations And Geometric Transforms
- Microcomputers/Minicomputers

Functional Block Diagram



J

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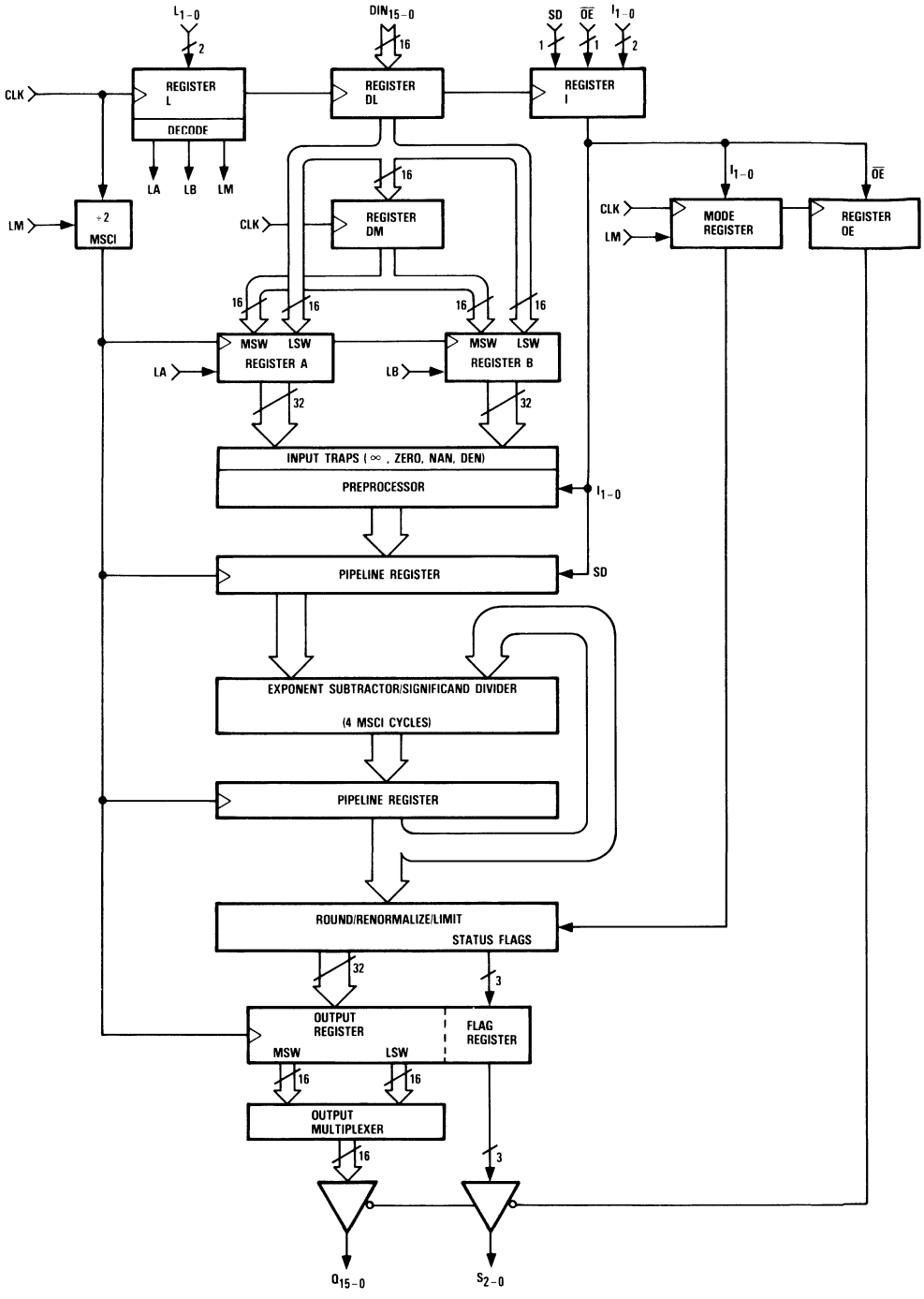
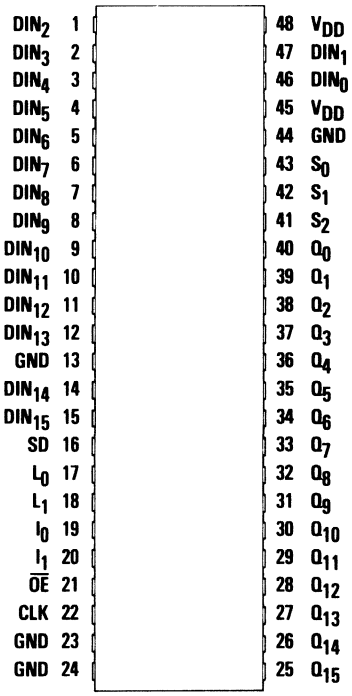
Printed in the U.S.A.

Functional Block Diagram



Pin Assignments



48 Lead DIP – J4 Package

Functional Description

General Information

The TMC3210 consists of five sections: the input registers, the input preprocessor, the exponent subtractor/significand divider, the round/renormalize/limit block, and the output multiplexer, registers and drivers.

Input Registers

The input section accepts the data input (DIN) operand for the divisor (B) or dividend (A) along with an instruction which sets the mode (rounding) or format (wrapped or normalized number) depending on the load instructions. The external clock (CLK) strobes the DL and DM input preload registers, as well as the Load (L), Instruction (I) and Mode registers. CLK is internally divided by two to support an internal pipeline rate which is half the external bus clock rate.

The Most Significant Word (MSW) and the Least Significant Word (LSW) of both operands enter through the single 16-bit half-width input bus. The input preload register DL latches in the contents on the bus on the rising edge of CLK. The load instruction L_{1-0} enables the A, B or Mode register and must be input at the same time as the A operand (dividend), B operand (divisor) or selected rounding mode instruction I_{1-0} respectively. L_{1-0} must be held for two clock cycles while the MSW and then the LSW of the dividend or divider is loaded. The two operands may be loaded in either order, but each always enters on two consecutive rising edges of CLK with the MSW first. If either operand is not updated, the next division will use the respective value from the previous operation, facilitating repeated divisions by or into a constant.

Table 1. Load Instructions

L_{1-0}	Mnemonic	Operation
00	NOP	No loading of A, B, or Mode registers
01	LA	Load register A from DL and DM preload registers
10	LB	Load register B from DL and DM preload registers
11	LM	Load Mode register from I register

One of the four IEEE rounding modes is selected by I_{1-0} when the Mode register is enabled through the LM load instruction. During a Load Mode, the Start Divide (SD) control selects either FAST or IEEE mode for the handling of underflowing results.

Table 2. Mode Instructions

I_{1-0}[1]	Mnemonic	Operation
00	RN	Round to nearest number, or nearest even number if distances are equal (IEEE Standard 754 default)
01	RZ	Round toward zero (truncate product significand)
10	RP	Round toward positive infinity
11	RM	Round toward negative infinity

Note:
1. I_{1-0} selects the rounding mode during a Load Mode (LM) instruction.

Table 3. Mode Control

SD[1]	Mnemonic	Operation
0	IEEE	Gradual Underflow (wrap exponent underflow values)
1	FAST	Flush-to-zero (replace exponent underflow numbers with zero)

Note:
1. SD selects IEEE or FAST mode during a Load Mode (LM) instruction.

The registered Start Divide control initiates a division. SD must remain HIGH for two CLK cycles and may be asserted during the loading of the second operand. After SD is exercised, the user may load the next set of operands without interfering with the operation in progress. Another SD may occur every four internal MSCI clock cycles (eight external CLK cycles).

The format instructions I_{1-0} select the dividend and divisor format and must be input with the loading of the second operand. If only one operand needs to be loaded for a division, I_{1-0} is registered at the same time as the operand. Wrapped operands are too small to be expressed as standard IEEE normalized values, therefore instead of being denormalized with an exponent and hidden bit of 0, they are represented with a nonpositive two's complement exponent and a hidden bit of 1. A wrapped number is normalized, but has a special exponent. This special format allows the divider to handle denormalized numbers without large on-board normalizing shifters.

Table 4. Format Instructions

I_{1-0}	Mnemonic	Operation
00	A/B	Divide normalized A by normalized B
01	WA/B	Divide wrapped A by normalized B
10	A/WB	Divide normalized A by wrapped B
11	WA/WB	Divide wrapped A by wrapped B

Input Preprocessor

This section includes the input traps which detect infinity, zero, not-a-number and denormalized operand to generate the appropriate status flag.

Main Section (Exponent Subtractor/Significand Divider)

The difference of the exponents and the quotient of the significands is computed including the IEEE guard, round and sticky bits. This operation requires eight CLK cycles from the initial rising edge of SD. To avoid disruption, the next SD must not begin for eight CLK cycles. After the unrounded, unnormalized intermediate result leaves this section, the user may exercise SD to bring in the next set of operands from the input block.

Round/Renormalize/Limit Section

The significand of the quotient is rounded and readjusted so that the Most Significant Bit (MSB) occupies the nominal hidden bit position. If necessary, the exponent is adjusted to compensate for the renormalization shift. The final exponent is compared to the IEEE limits of 0 and 255 to generate the appropriate output condition and exception flag S_{2-0}.

Table 5. Status Outputs

S_{2-0}	Mnemonic	Exceptions
00X	OK	No exceptions
01X	UNF	Exponent underflow
10X	OVF	Exponent overflow or divide by zero
110	INV	Invalid operands or invalid operation
111	DIN	Denormalized operand

Table 6. Divider Exception Flags and Outputs

A Operand (Dividend)	B Operand (Divisor)				
	ZERO	DNRM	NRM/WNRM	INF	NaN
ZERO	INV, NaN	OK, ZERO	OK, ZERO	OK, ZERO	INV, NaN
DNRM	OVF, INF	INV[1], NaN	OK[1], ZERO	OK, ZERO	INV, NaN
NRM/WNRM	OVF, INF	OVF[1], INF	See Note 2	OK, ZERO	INV, NaN
INF	OK, INF	OK, INF	OK, INF	INV, NaN	INV, NaN
NaN	INV, NaN	INV, NaN	INV, NaN	INV, NaN	INV, NaN

Notes:

1. In IEEE mode, DIN (S_{2-0} = 111) is the status flag output.
2. In the case of NRM/WNRM divided by NRM/WNRM.
   OVF: Output is OVF, +NRM.MAX if (RM,RZ) and TRESULT > NRM.MAX.
   OVF, −NRM.MAX if (RP,RZ) and TRESULT < −NRM.MAX.
   OVF, +INF if (RN,RP) and TRESULT > NRM.MAX.
   OVF, −INF if (RN,RM) and TRESULT < −NRM.MAX.
   UNF: Output is zero with UNF if | TRESULT | < NRM.MIN (FAST mode).
   Output is WNRM with UNF if | TRESULT | < NRM.MIN (IEEE mode).
   ELSE: Output is OK with normalized value.
   NRM.MIN ≤ | TRESULT | ≤ NRM.MAX.
3. Terms used in this table include:
   OK = No exceptions raised.
   NRM = Normalized number.
   DNRM = Denormalized number.
   WNRM = Wrapped number.
   INF = Infinity (±, Exponent = FF_H, Significand = 000000_H).
   NaN = Not-A-Number (±, Exponent = FF_H, Significand = 600000_H).
   TRESULT = Normalized, rounded, true result before limiting.
   NRM.MAX = Maximum allowable positive normalized number ($2^{+128} - 2^{+104}$ or Sign = 0, Exponent = FE_H, Significand = $7FFFFF_H$).
   NRM.MIN = Minimum allowable positive normalized number (2^{-126} or Sign = 0, Exponent = 01_H, Significand = 000000_H).

In FAST mode, all underflows are forced to zero and the underflow flag is generated. In IEEE mode, underflowing values are wrapped and the underflow flag is generated. Overflows are limited to the infinities for round toward nearest and to maximum magnitude normalized values for round toward zero. Round toward positive infinity limits the output to a positive infinity or a negative limit of maximum magnitude, negative normalized number. Round toward negative infinity limits the output to a negative infinity or a positive limit of maximum magnitude, positive normalized number.

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Output Multiplexer, Registers and Drivers

The 32-bit output register and 3-bit flag register are clocked by MSCI. The quotient is output through the 16-bit output port via the output multiplexer which selects either the MSW or LSW. The synchronization of MSW or LSW with CLK is set by the LM load instruction. After the SD control is HIGH for two CLK cycles to begin a division, the MSW of the quotient is output after the 12th rising edge of CLK. The output will toggle MSW and LSW with CLK until the quotient from the next division is available. The state of the status flags will remain set until new exception conditions occur. The output drivers are enabled and disabled by the Output Enable ($\overline{OE}$) control.

Signal Definitions

Power

V_{DD}, GND — The TMC3210 operates from a single +5 Volt supply. All power and ground lines must be connected.

Data Inputs

DIN_{15-0} — DIN is the 16-bit input to the preload register DL which is loaded on the rising edge of CLK. All data operands (dividends and divisors) are loaded through the DIN port, MSW followed by the LSW.

Data Outputs

Q_{15-0} — Q is the 16-bit output from the output register which is clocked by MSCI. The output multiplexer is internally synchronized to select MSW then LSW of the quotient which is output through three-state output drivers.

Clock

CLK — The CLK frequency is twice the internal clock rate to allow for input/output data multiplexing. All operations are with respect to the rising edge CLK. The A and B input registers, pipeline registers and output registers are clocked by internal MSCI which is generated by dividing CLK by two.

Controls

I_{1-0} — The Mode/Format Instructions determine the rounding mode during a Load Mode, and select the input data formats when the operands are loaded. The rounding mode controls must be held for both CLK cycles during the loading of the Mode register. The format controls must be held for two CLK cycles during the loading of the last operand for a division.

L_{1-0} — The Load Instructions generate LA, LB and LM which enable the A, B and Mode input registers respectively. The load controls are read on every rising edge of CLK. All data transfers into these input registers take place on the rising edge of CLK following the load controls commanding the data transfer. L_{1-0} must be valid for two CLK cycles since the MSW and LSW must be loaded in two consecutive cycles. The LM instruction establishes the internal synchronization of CLK with MSCI and should not be asserted during a division.

$\overline{OE}$ — Output Enable is a registered control which enables the quotient and status outputs when LOW. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state. $\overline{OE}$ is read on the rising edge of CLK. The state of the output drivers will change after the next rising edge of CLK. Therefore, two CLK cycles are required to enable or disable the three-state drivers.

SD — Start Divide is an active HIGH control which begins the four MSCI clock cycle division. SD must remain HIGH for two CLK cycles and be asserted during or after the loading of the last operand of the divide. Subsequent SD may begin eight CLK cycles after the SD of the previous division. During the loading of the Mode register, SD selects whether FAST or IEEE mode is used in handling underflows.

Status Outputs

S_{2-0} — The status flags indicate the presence of exception conditions with the input operands or output quotient. The flags are valid while both the MSW and the LSW are output as long as the output buffer is enabled.

Package Interconnections

Signal Type	Signal Name	Function	J4 Package
Power	V_{DD}	Supply Voltage	45, 48
	GND	Ground	13, 23, 24, 44
Data Input	DIN_{15-0}	Input Data Word	15, 14, 12-1, 47, 46
Data Output	Q_{15-0}	Output Quotient Word	25-40
Clock	CLK	Clock	22
Controls	I_{1-0}	Mode/Format Instructions	20, 19
	L_{1-0}	Load Instructions	18, 17
	$\overline{OE}$	Output Enable	21
	SD	Start Divide	16
Flags	S_{2-0}	Status Outputs	41-43

Data Format

The TMC3210 conforms to IEEE Standard 754, Version 10.0 data format for 32-bit arithmetic. The divider requires two clock cycles to transfer a data word since the input and output buses are 16-bit wide.

Standard IEEE 32-Bit Floating-Point Format

The IEEE Standard 754, Version 10.0 specifies a 32-bit data format for floating-point arithmetic. In this format the MSB (bit 31) is the sign bit, the next eight bits (bits 30-23) are the exponent field and the 23 LSBs are the fractional significand field (bits 22-0). The "hidden bit" completes the 24-bit significand.

Sign Bit

The MSB carries the sign information. A HIGH for a sign bit indicates a negative number and a LOW indicates a positive number.

Exponent Field

The 8-bit exponent field determines whether the floating-point number is a signed infinity, a NaN, a zero, a denormalized number or a normalized floating-point number.

The exponent values 0 and 255 are special. If the exponent field is all ones (1111 1111, 255_{10}) and the fraction (bits 22-0) is zero, the number is evaluated as infinity x $(-1)^S$ with S being the sign bit. Any exponent of 255 with a nonzero fraction is a NaN. A NaN is generally used to communicate error information such as invalid operation or uninitialized memory and has no numerical value.

When the exponent field is all zeros (0000 0000) and the fraction is also zero, the number is a true floating-point zero. Note that this data format allows both positive and negative zeros which are computationally treated identically. When the exponent is zero and the fraction is nonzero, the number is a denormalized floating-point number evaluated as:

$$\text{Number} = (-1)^S \times 2^{E-126} \times (0.F)$$

where S is the sign bit, E is the value of the exponent field (base 10) and F is the value of the fractional field.

If the exponent field is neither all zeros nor all ones, the floating-point number is normalized and evaluated as:

$$\text{Number} = (-1)^S \times 2^{E-127} \times (1.F)$$

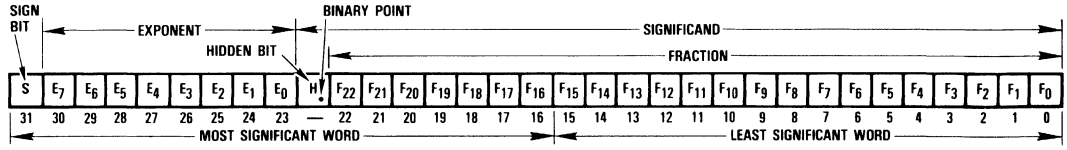
Note that the exponent bias has changed from 126 to 127 and that 1.0 has been added to the fractional field. The exponent can assume values which run from -126 to +127 (0 to 254 biased by 127). Note that both exponent fields of zero and one map onto the exponent value of -126. These provisions ensure a smooth transition from normalized numbers through gradual underflow into the denormalized numbers.

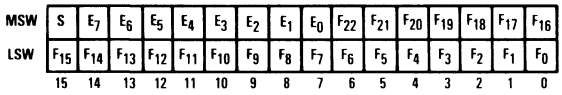
Fractional Field

Bits 22–0 comprise the fractional field (mantissa). There is a binary point assumed between bit 22 and the implied "hidden" bit 23. For a nonzero exponent, the hidden bit assumes a value of "1." For a zero exponent, the hidden bit has a value of "0." Bit 22 carries a binary weighting of 2^{-1}. The following bits carry decreasing binary weights down to the LSB (bit 0) which carries the weight of 2^{-23}. This is identical to treating the fractional part (bits 22–0) like an integer F multiplied by 2^{-23}. The fractional part of the floating-point number is either 0 + F (in the case of a zero exponent), or 1 + F (in the case of a nonzero exponent).

The difference between the smallest normalized number (exponent = 1, fractional part = 0) and the largest denormalized number (exponent = 0, fractional part = all ones) is one LSB. The smallest normalized number is: exponent = −126, significand = 1.00...00 written as exponent = 01_H, significand = 000000_H. The largest denormalized number is: exponent = −126, significand = 0.11...11 written as exponent = 00_H, significand = $7FFFFF_H$.

Figure 1. IEEE 32-Bit Floating-Point Format





Exponent	Fraction	Value	Name	Mnemonic
255	Not all zeros	--	Not-A-Number	NaN
255	All zeros	$(-1)^S \times \infty$	Signed Infinity	INF
1 through 254	Any	$(-1)^S \times (1.F) \times 2^{E-127}$	Normalized Number	NRM
0	Not all zeros	$(-1)^S \times (0.F) \times 2^{E-126}$	Denormalized Number	DNRM
0	All zeros	$(-1)^S \times 0.0$	Zero	ZERO

Note:

1. H, the hidden bit, is one except for zero and denormalized numbers when it is zero.

Figure 2. Timing Diagram

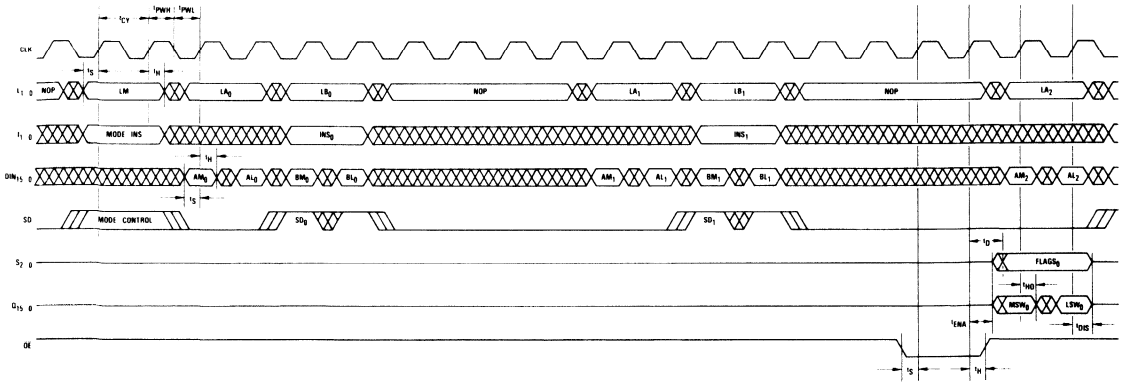


Figure 3. Equivalent Input Circuit

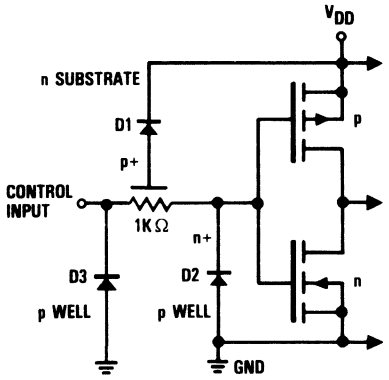


Figure 4. Equivalent Output Circuit

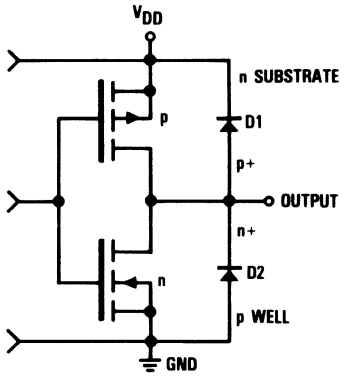
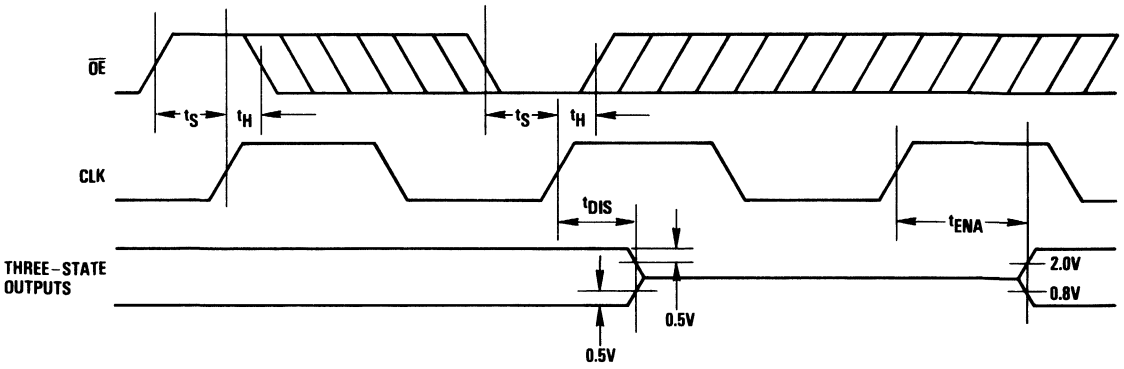


Figure 5. Threshold Levels For Three-State Measurement



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} +0.5)V
Output	
Applied voltage [2]	−0.5 to (V_{DD} +0.5)V
Forced current [3,4]	−1.0 to +6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

		Temperature Range						
		Standard			Extended			
Parameter		**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Units**
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

DC characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		10		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, $\overline{OE}$ = 5V					
		f = 20MHz		50		70	mA
		f = 10MHz		25		35	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		-10		-40	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		40	μA
V_{IL}	Input Voltage, Logic LOW			0.8		0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0		2.0		V
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = 4mA		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = -2mA	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		-40		-40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		-100		-120	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note:

1. Actual test conditions may vary from those shown, but guarantee operation as specified.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{CY}	Cycle Time	V_{DD} = Min		50		55	ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD} = Min	30		35		ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD} = Min	15		15		ns
t_S	Input Setup Time		15		15		ns
t_H	Input Hold Time		0		3		ns
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		20		25	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF	5		5		ns
t_{ENA}	Three-State Output Enable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF		20		25	ns
t_{DIS}	Three-State Output Disable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF		25		30	ns

Note:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}

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Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC3210J4C	STD – T_A = 0°C to 70°C	Commercial	48 Pin Hermetic Ceramic DIP	3210J4C
TMC3210J4V	EXT – T_C = –55°C to 125°C	MIL-STD-883	48 Pin Hermetic Ceramic DIP	3210J4V

Memory/Storage

Signal processing puts extraordinary demands on memory and storage elements. The high speeds involved call for multi-port memories. Asynchronous system interfaces need high-speed FIFO buffers. The highly pipelined architectures require a variety of short, wide, variable delays to compensate unequal data paths. At times, long delays are needed.

TRW provides solutions to all of those problems with special-purpose memories and storage elements. The TDC1005/TDC1006 shift registers are basic long, fast serial storage elements. The TDC1030 FIFO provides a flexible asynchronous interface. For equalization problems, the TMC2011/2111 are an easy solution, with a byte-wide architecture and fully-programmable lengths up to 18 words. The TMC3220 3-port Register file (one write with two simultaneous reads) will relieve dataflow bottlenecks.

Product	Description	Size	Clock Rate [1] (MHz)	Power [1] (Watts)	Package		Grades [2]	Notes	Page
TDC1005	Shift Register	64 x 2 Bit	25	0.6	B9	16 Pin DIP	C	Expandable/Cascadable.	K3
			24	0.6	B9	16 Pin DIP	A		
TDC1006	Shift Register	256 x 1 Bit	25	0.7	B9	16 Pin DIP	C	Expandable/Cascadable.	K9
			24	0.7	B9	16 Pin DIP	A		
TDC1011	Programmable Digital Delay	3-18 x 8 Bit	18	0.8	B2, B7	24 Pin DIP	C	Also 21-36 x 4 Split Mode.	K15
					C3	28 Contact CC	C		
			15	1.1	B2, B7	24 Pin DIP	A		
					C3	28 Contact CC	A		
TMC2011	Programmable Digital Delay	3-18 x 8 Bit	30	0.2	B2	24 Pin DIP	C	Also 21-36 x 4 Split Mode.	K37
			28	0.2	B2	24 Pin DIP	V, SMD		
					C3	28 Contact CC	V, SMD		
TMC2111	Programmable Digital Delay	1-16 x 8 Bit	30	0.2	B2	24 Pin DIP	C		K37
			28	0.2	B2	24 Pin DIP	V, SMD		
					C3	28 Contact CC	V, SMD		
TMC3220	Three Port Register File	32 x 8 Bit	20	0.15	J4	48 Pin DIP	C, V	1 Write, 2 Read Ports	K45

Notes: 1. Guaranteed. See product specifications for test conditions.

2. A = High Reliability, $T_C = -55°C$ to 125°C.
C = Commercial, $T_A = 0°C$ to 70°C.
V = MIL-STD-883 Compliant, $T_C = -55°C$ to 125°C
SMD = Available per Standardized Military Drawing, $T_C = -55°C$ to 125°C.

TDC1005

Serial Shift Register
Dual 64-Bit

The TRW TDC1005 is a dual 64-bit positive-edge-triggered serial shift register which operates at 25MHz. This device is cascadable in the number of words and the word size.

Complementary TTL outputs Q and $\overline{Q}$ are provided. The two data inputs in each shift register, D0 and D1, are controlled by a data select input, DS. This provides on-chip recirculate gating when the true output is hard-wired to one of the inputs.

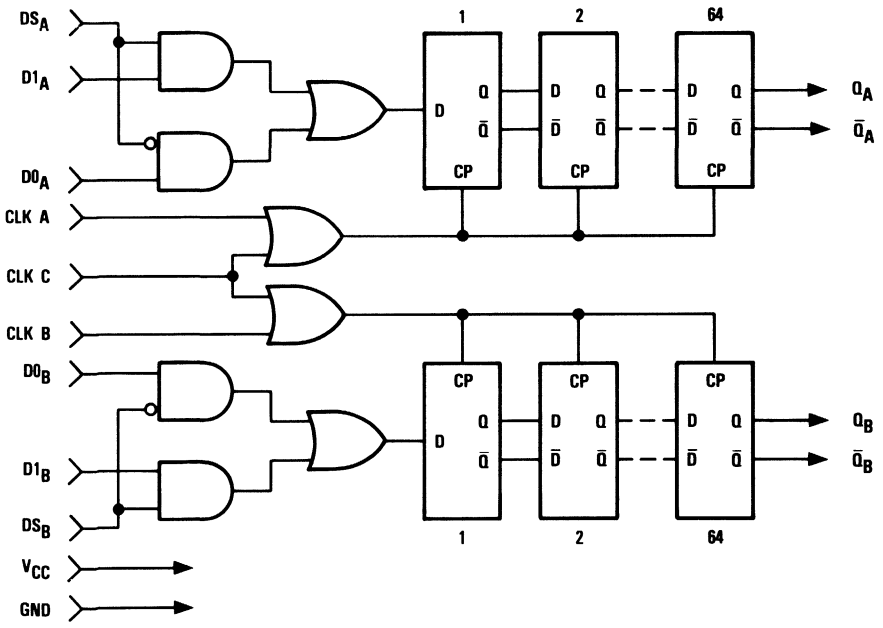
Features

- 25MHz Guaranteed Clock Frequency
- Fully TTL Compatible
- True and Complementary Outputs
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In A 16 Pin CERDIP
- Horizontal And Vertical Cascadability

Applications

- High-Speed Data Acquisition
- First-In First-Out Data Buffers
- Coefficient Storage For FIR Filters
- Digital Delay Lines
- Local Storage Registers

Functional Block Diagram



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40G00275 Rev. G – 11/90
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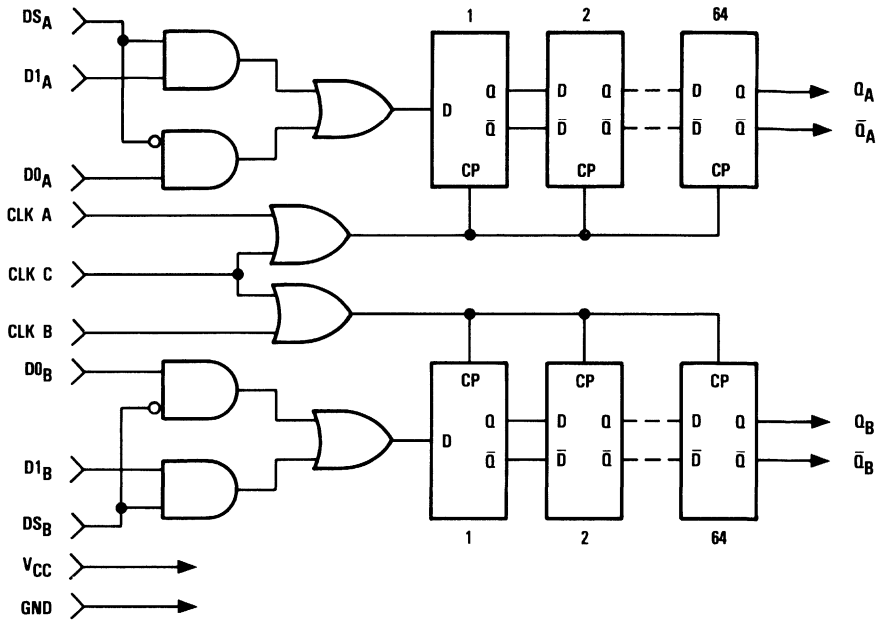
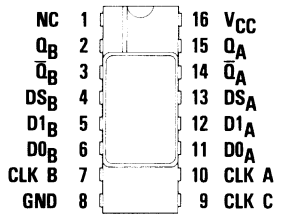
Functional Block Diagram



Pin Assignments



16 Pin CERDIP – B9 Package

Functional Description

General Information

The TDC1005 is a positive-edge-triggered dual 64-bit serial shift register. One of two data inputs (D0 and D1) is selected by the Data Select control (DS). Complementary outputs Q and $\overline{Q}$ are available.

Power

The TDC1005 operates from a single +5 Volt power supply.

Name	Function	Value	J9 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 16
GND	Ground	0.0V	Pin 8

Data Inputs

The TDC1005 has two data inputs per block, ($D0_A$ and $D0_B$, $D1_A$ and $D1_B$).

Name	Function	Value	J9 Package
$D0_A$	Data Input 0, Block A	TTL	Pin 11
$D1_A$	Data Input 1, Block A	TTL	Pin 12
$D0_B$	Data Input 0, Block B	TTL	Pin 6
$D1_B$	Data Input 1, Block B	TTL	Pin 5

Data Select

Two data select controls, one for Block A (DS_A) and one for Block B (DS_B), are provided to select between inputs 0 and 1. The 0 input is selected when DS is LOW; the 1 input is selected when DS is HIGH.

Name	Function	Value	J9 Package
DS_A	Block A Data Select	TTL	Pin 13
DS_B	Block B Data Select	TTL	Pin 4

Data Outputs

Complementary outputs Q and $\overline{Q}$ are provided for the TDC1005.

Name	Function	Value	J9 Package
QA	Data Output Block A	TTL	Pin 15
$\overline{QA}$	Data Output (Inv.) Block A	TTL	Pin 14
QB	Data Output Block B	TTL	Pin 2
$\overline{QB}$	Data Output (Inv.) Block B	TTL	Pin 3

Clocks

The TDC1005 has three clock inputs (CLK A, CLK B, CLK C) which are combined to provide the clock signals for the two blocks. Block A is clocked by the logical OR of CLK A and CLK C. Block B is clocked by the logical OR of CLK B and CLK C. This allows the two blocks to be clocked either independently or simultaneously.

Name	Function	Value	J9 Package
CLK A	Clock A	TTL	Pin 10
CLK B	Clock B	TTL	Pin 7
CLK C	Clock C	TTL	Pin 9

No Connects

Pin 1 on the TDC1005 is not connected internally. This pin may be left unconnected.

Name	Function	Value	J9 Package
NC	No connection	Open	Pin 1

Figure 1. Timing Diagram

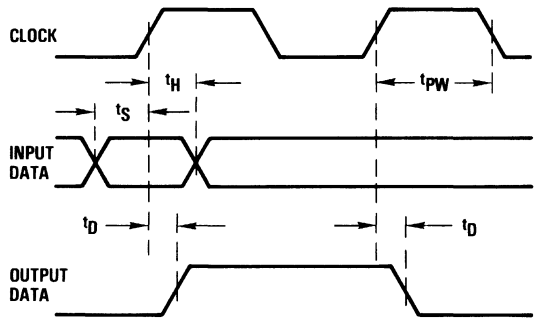


Figure 2. Input/Output Schematics

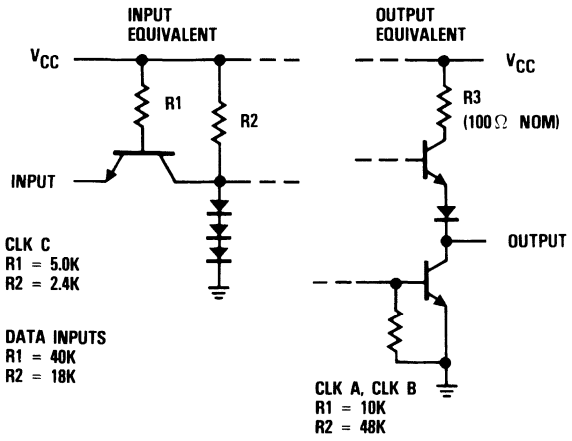
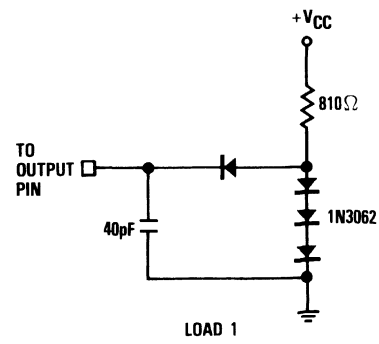


Figure 3. Test Load for Delay Measurement (Typical)



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	0 to +5.5V
Output	
Applied voltage (measured to GND)	0 to +5.5V [2]
Applied current, externally forced	−1.0 to 6.0ma [3,4]
Short circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, ambient	−55 to +150°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width	18			18			ns
t_S	Input Register Setup Time	7			7			ns
t_H	Input Register Hold Time	10			10			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = Max		105		120	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{IL}	Input Current, Logic LOW [1]	V_{CC} = Max, V_{IL} = 0.4V		−0.5		−0.8	mA/Load
I_{IH}	Input Current, Logic HIGH [1]	V_{CC} = Max, V_{IH} = 2.4V		20		50	μA/Load

Note: 1. CLK C: Eight equivalent loads
CLK A, CLK B: Four equivalent loads

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_C	Clock Frequency	See Figure 3	25		24		MHz
t_D	Output Delay	See Figure 3		35		35	ns

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1005B9C	STD − T_A = 0°C to 70°C	Commercial	16 Pin CERDIP	1005B9C
TDC1005B9A	EXT − T_C = −55°C to 125°C	High Reliability	16 Pin CERDIP	1005B9A

TDC1006

Serial Shift Register
256-Bit

The TRW TDC1006 is a positive-edge-triggered serial shift register which operates at 25MHz. This device is cascadable in the number of words and the word size.

Complementary TTL outputs Q and $\overline{Q}$ are provided. Two data inputs, D0 and D1, are controlled by a data select input, DS. This provides on-chip recirculate gating when the true output is hard-wired to one of the inputs.

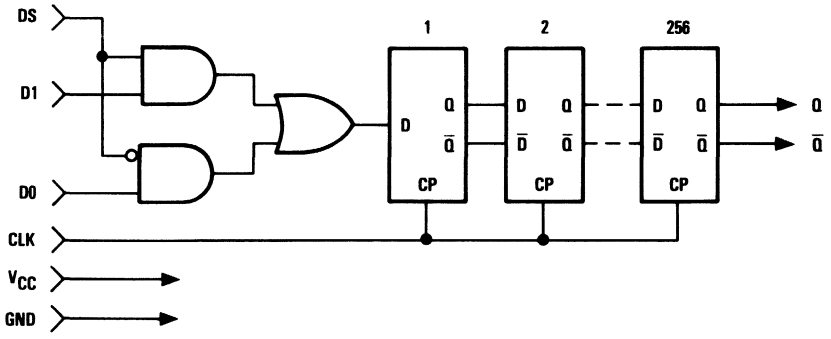
Features

- 25MHz Guaranteed Clock Frequency
- Fully TTL Compatible
- True and Complementary Outputs
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In A 16 Pin CERDIP
- Horizontal And Vertical Cascadability

Applications

- High-Speed Data Acquisition
- First-In First-Out Data Buffers
- Coefficient Storage For FIR Filters
- Digital Delay Lines
- Local Storage Registers

Functional Block Diagram



K

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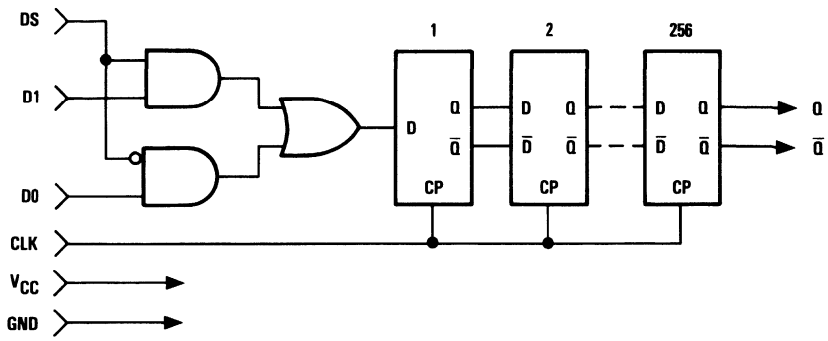
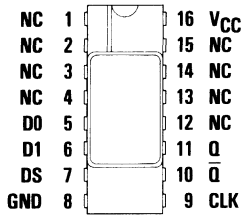
Functional Block Diagram



Pin Assignments



16 Pin CERDIP – B9 Package

Functional Description

General Information

The TDC1006 is a 256-bit positive-edge-triggered serial shift register. One of two data inputs (D0 and D1) is selected by the Data Select control DS. Complementary outputs Q and $\overline{Q}$ are available.

Power

The TDC1006 operates from a single +5 Volt power supply.

Name	Function	Value	J9 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 16
GND	Ground	0.0V	Pin 8

Data Inputs

The TDC1006 is a single 256-bit shift register with two data inputs D0 and D1.

Name	Function	Value	J9 Package
D0	Data Input 0	TTL	Pin 5
D1	Data Input 1	TTL	Pin 6

Data Select

The TDC1006 has one data select control (DS) to select between inputs D0 and D1. Input D1 is selected when DS is HIGH, D0 is selected when DS is LOW.

Name	Function	Value	J9 Package
DS	Data Select	TTL	Pin 7

Data Outputs

Complementary outputs Q and $\overline{Q}$ are provided for the TDC1006.

Name	Function	Value	J9 Package
Q	Data Output	TTL	Pin 11
$\overline{Q}$	Data Output Inverted	TTL	Pin 10

Clocks

The TDC1006 has one clock signal, CLK.

Name	Function	Value	J9 Package
CLK	Clock	TTL	Pin 9

K

No Connects

There are several pins on the TDC1006 which are not connected internally. These pins may be left unconnected.

Name	Function	Value	J9 Package
NC	No Connect	Open	Pins 1-4, 12-15

Figure 1. Timing Diagram

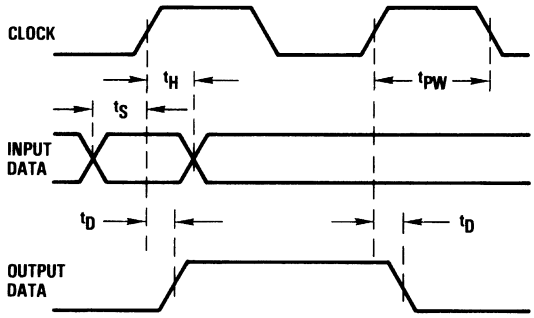
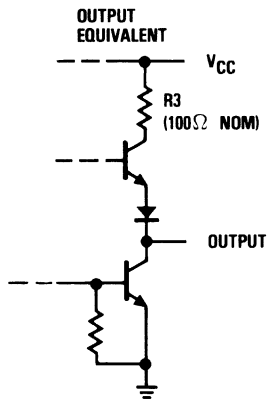


Figure 2. Equivalent Input/Output Schematics



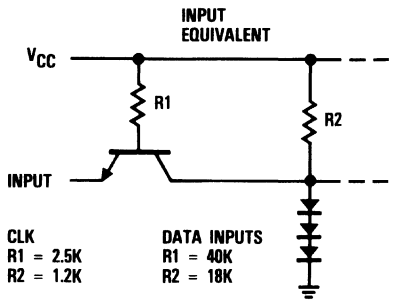
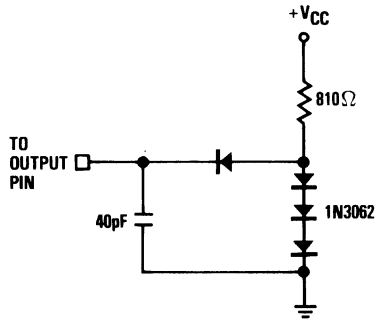


Figure 3. Test Load



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0 V
Input Voltage	0 to +5.5V
Output	
Applied voltage (measured to GND)	0 to +5.5V [2]
Applied current, externally forced	−1.0 to +6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, ambient	−55 to +150°C
junction	+175°C
Lead, soldering (10 sec.)	+300°C
Storage	−65 to +160°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width	15			15			ns
t_S	Input Register Setup Time	7			7			ns
t_H	Input Register Hold Time	10			10			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = Max		135		155	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{IL}	Input Current, Logic LOW [1]	V_{CC} = Max, V_{IL} = 0.4V		−0.5		−0.8	mA/Load
I_{IH}	Input Current, Logic HIGH [1]	V_{CC} = Max, V_{IH} = 2.4V		20		50	μA/Load

Note: 1. CLK: Sixteen equivalent loads.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_C	Clock Frequency	See Figure 1	25		24		MHz
t_D	Output Delay	See Figure 1		32		35	ns

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1006B9C	STD − T_A = 0°C to 70°C	Commercial	16 Pin CERDIP	1006B9C
TDC1006B9A	EXT − T_C = −55°C to 125°C	High Reliability	16 Pin CERDIP	1006B9A

TDC1011

Variable-Length Shift Register
8-Bit, 18MHz

The TRW TDC1011 is a high-speed, byte-wide shift register which can be programmed to any length between 3 and 18 stages. It operates at a 56ns cycle time (18MHz shift rate). A special split-word mode is provided for use with the TRW TDC1028.

The TDC1011 is fully synchronous, with all operations controlled by a single master clock. Input and output registers are positive-edge-triggered D-type flip-flops. The length control inputs are also registered.

Built with TRW's OMICRON-B™ 1-micron bipolar process, the TDC1011 provides the system designer with a unique variable-delay capability at video speeds.

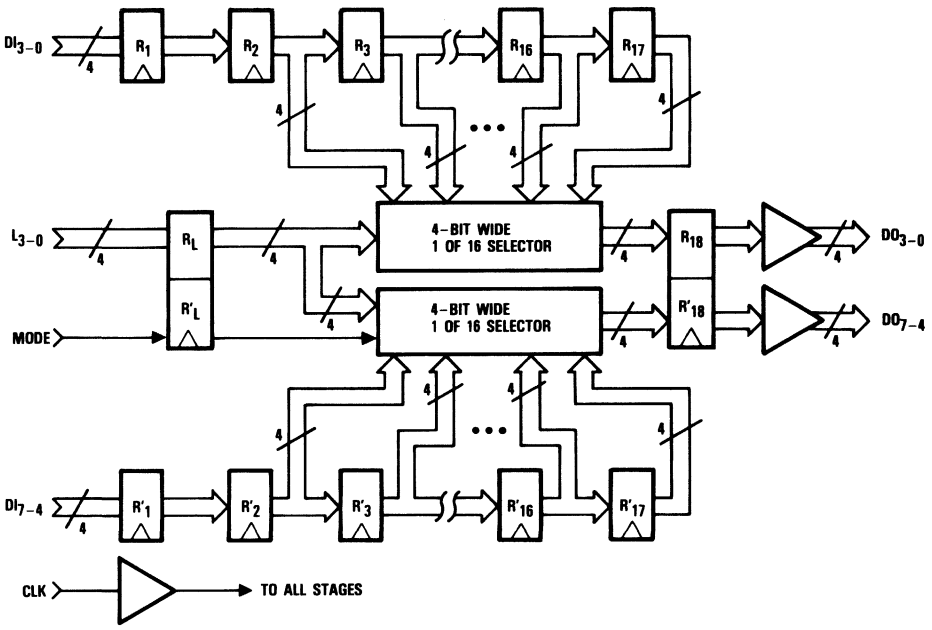
Features

- 56ns Cycle Time (Worst Case)
- Single +5V Power Supply
- TTL Compatible
- Selectable Length From 3 To 18 Stages
- Special 4-Bit Wide Mixed-Delay Mode
- Available In 24 Pin DIP, CERDIP And 28 Contact Chip Carrier

Applications

- Word Size Expansion Of TDC1028
- Video Filtering
- High-Speed Data Acquisition
- Local Storage Registers
- Digital Delay Lines
- Television Special Effects

Functional Block Diagram



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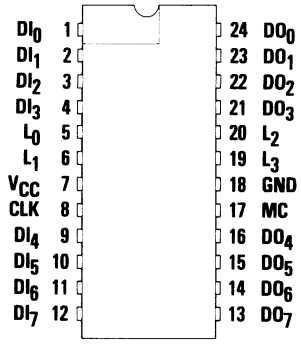
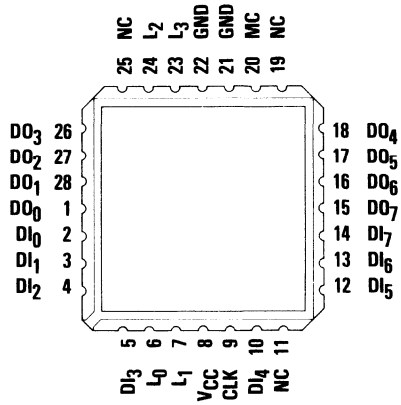
Pin Assignments



24 Pin DIP – J7 Package
24 Pin CERDIP – B2 Package
24 Pin CERDIP – B7 Package



28 Contact Chip Carrier – C3 Package

Functional Description

General Information

The TDC1011 consists of two 4-bit wide, adjustable length shift registers. These registers share control signals and a common clock.

Power

The TDC1011 operates from a single +5 Volt supply.

Inputs

The eight inputs to the TDC1011 are divided into two groups of four, and are intended to support the TDC1028, which has inputs in groups of four bits. The lengths of these two groups are different when the Mode Control (MC) is HIGH (refer to the ***Controls*** section). The incoming data is unchanged by the TDC1011. All inputs are fully TTL compatible and all internal circuitry is static.

Outputs

The outputs of the TDC1011 are delayed relative to the input signals. The amount of the delay is programmable (refer to the ***Controls*** section). The outputs remain valid for a minimum of t_{HO} nanoseconds after the leading edge of CLK. This allows the data to be latched into circuits with non-zero hold time requirements.

Clock

The TDC1011 operates synchronously from a single master clock line, which can be clocked up to 18MHz. All operations occur at the rising edge of the master clock. Since the internal circuitry is static, the clock can be gated if desired.

Controls

The TDC1011 has four length selection controls and one mode selection control. The operation of these controls is shown in *Table 1*.

No Connect

There are several pins labeled no connect (NC) on the TDC1011 C3 Package, which have no connections to the chip. These pins should be left open.

Package Interconnections

Signal Type	Signal Name	Function	Value	J7, B2, B7 Package Pins	C3 Package Pins
Power	V_{CC}	Positive Supply Voltage	5.0V	7	8
	GND	Ground	0.0V	18	21, 22
Inputs	DI_{0-7}	Data Input	TTL	1, 2, 3, 4, 9, 10, 11, 12	2, 3, 4, 5, 10, 12, 13, 14
Outputs	DO_{0-7}	Data Output	TTL	24, 23, 22, 21, 16, 15, 14, 13	1, 28, 27, 26, 18, 17, 16, 15
Clock	CLK	Clock	TTL	8	9
Controls	L_0	Length Select LSB	TTL	5	6
	L_1	Length Select	TTL	6	7
	L_2	Length Select	TTL	20	24
	L_3	Length Select MSB	TTL	19	23
	MC (Mode)	Mode Control	TTL	17	20
No Connect	NC	No Connect	Open	None	11, 19, 25

Table 1. Length Programming

Input Code				Mode (MC) = 0		Mode (MC) = 1	
L_3	L_2	L_1	L_0	DO_{3-0} Length	DO_{7-4} Length	DO_{3-0} Length	DO_{7-4} Length
0	0	0	0	3	3	3	18
0	0	0	1	4	4	4	18
0	0	1	0	5	5	5	18
0	0	1	1	6	6	6	18
0	1	0	0	7	7	7	18
0	1	0	1	8	8	8	18
0	1	1	0	9	9	9	18
0	1	1	1	10	10	10	18
1	0	0	0	11	11	11	18
1	0	0	1	12	12	12	18
1	0	1	0	13	13	13	18
1	0	1	1	14	14	14	18
1	1	0	0	15	15	15	18
1	1	0	1	16	16	16	18
1	1	1	0	17	17	17	18
1	1	1	1	18	18	18	18

Figure 1. Timing Diagram (Preset Length Controls)

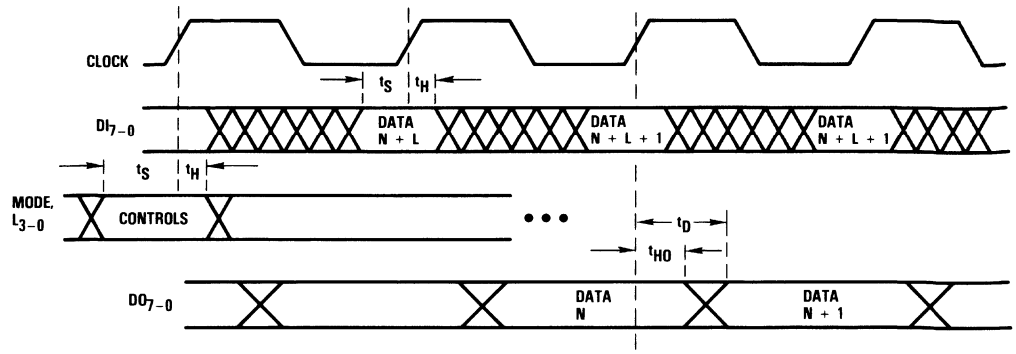


Figure 2. Length Control Operation

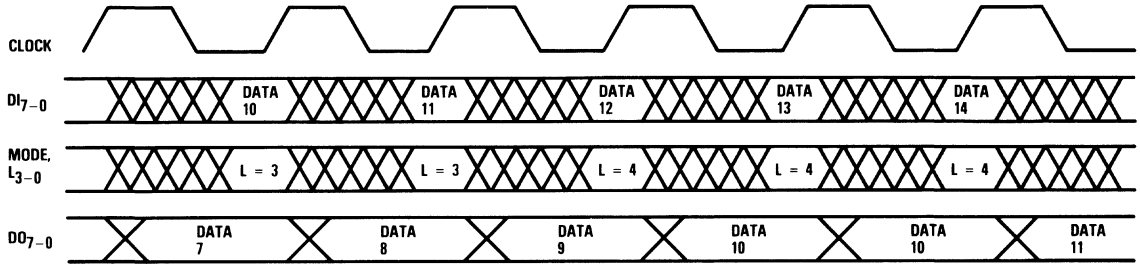
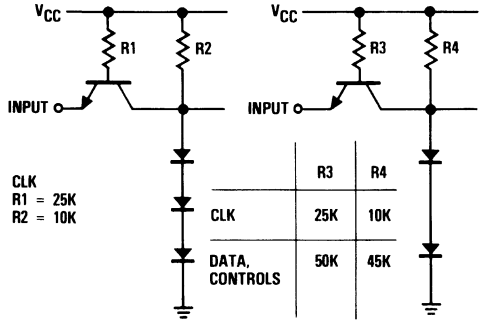


Figure 3. Equivalent Input Circuit



	R3	R4
CLK	25K	10K
DATA, CONTROLS	50K	45K

Figure 4. Equivalent Output Circuit

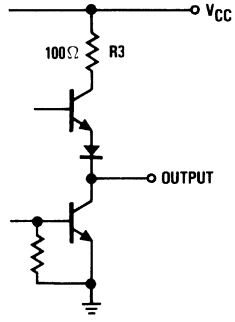
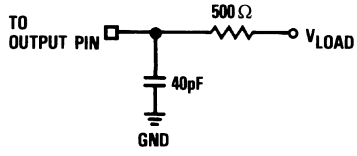


Figure 5. Test Load



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input

Applied voltage ..... −0.5 to +5.5V [2]
Forced current ..... −6.0 to +6.0mA [3,4]

Output

Applied voltage ..... −0.5 to +5.5V [2]
Forced current ..... −1.0 to 6.0mA [3,4]
Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −55 to +125°C
junction ..... 175°C
Lead, soldering (10 seconds) ..... 300°C
Storage ..... −65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Extended Min	Extended Nom	Extended Max	Units
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	15			15			ns
t_{PWH}	Clock Pulse Width, HIGH	15			15			ns
t_S	Input Setup Time	20			25			ns
t_H	Input Hold Time	0			2			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
V_{IHC}	Input Voltage, Logic HIGH, Clock	2.4			2.4			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = Max, Static		150		200	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.4V					
		Data Inputs		−0.4		−0.4	mA
		Clock		−1.0		−1.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V		75		75	μA
I_I	Input Current, Max Input Voltage	V_{CC} = Max, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{OS}	Short-Circuit Output Current	V_{CC} = Max, Output HIGH, one pin to ground, one second duration max.		−40		−40	mA
C_I	Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{CLK}	Clock Rate	V_{CC} = Min					
		Static Length Controls	18		15		MHz
		Dynamic Length Controls	15		10		MHz
t_D	Output Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		25		30	ns
t_{HO}	Output Hold Time [2]	V_{CC} = Max, Test Load: V_{LOAD} = 2.2V	5		5		ns

Notes: 1. All transitions are measured at a 1.5V level.
2. Guaranteed, not tested.

Application Notes

The TDC1011 has two types of applications: as a support device for the TDC1028, and as a general variable-length shift register.

To support the TDC1028, the lengths will be set to one of the following:

1. Both sections 9 stages long.
2. One section 9 stages long, the other section 18 stages long.
3. Both sections 18 stages long.

The sections are interchangeable only if the lengths are identical.

Further description of the use of the TDC1011 to support the TDC1028 is given in TRW LSI Products Inc. *Application Note TP-22.*

For general use, it is important to note that the length control inputs are registered. There are no constraints on the use of the control leads other than the operational requirements shown in the *Operating Conditions Table.* Specifically, the length can be increased from one clock period to another and proper operation will occur; no data is lost, except the eighteenth stage.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1011B2C	STD – T_A = 0°C to 70°C	Commercial	24 Pin CERDIP [1]	1011B2C
TDC1011B2A	EXT – T_C = –55°C to 125°C	High Reliability	24 Pin CERDIP [1]	1011B2A
TDC1011B7C	STD – T_A = 0°C to 70°C	Commercial	24 Pin CERDIP [2]	1011B7C
TDC1011B7A	EXT – T_C = –55°C to 125°C	High Reliability	24 Pin CERDIP [2]	1011B7A
TDC1011C3C	STD – T_A = 0°C to 70°C	Commercial	28 Contact Hermetic Ceramic Chip Carrier	1011C3C
TDC1011C3A	EXT – T_C = –55°C to 125°C	High Reliability	28 Contact Hermetic Ceramic Chip Carrier	1011C3A
TDC1011J7C	STD – T_A = 0°C to 70°C	Commercial	24 Pin Hermetic Ceramic DIP	1011J7C
TDC1011J7A	EXT – T_C = –55°C to 125°C	High Reliability	24 Pin Hermetic Ceramic DIP	1011J7A

Notes: 1. 0.3 inches wide.
2. 0.6 inches wide.

TDC1030

First-In First-Out Memory
64 Words by 9 Bits Cascadable

The TRW TDC1030 is an expandable, First-In First-Out (FIFO) memory organized as 64 words by 9 bits. A 15MHz data rate makes it ideal in high-speed applications. Burst data rates of 18MHz can be obtained in applications where the device status flags are not used.

With separate Shift-In (SI) and Shift-Out (SO) controls, reading and writing operations are completely independent, allowing synchronous and asynchronous data transfers. Additional controls include a Master Reset ($\overline{MR}$), and Output Enable ($\overline{OE}$). Input Ready (IR) and Output Ready (OR) flags are provided to indicate device status.

Devices can be easily interconnected to expand word and bit dimensions. The device has all output pins directly opposite the corresponding input pins, facilitating board layouts in expanded format. All inputs and outputs are TTL compatible.

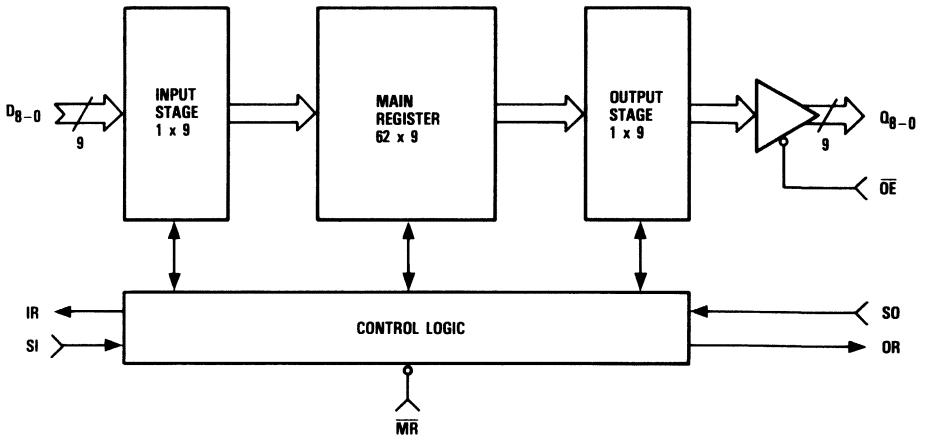
Features

- 64 Words By 9 Bits Organization
- 15MHz Shift-In, Shift-Out Rates With Flags
- 18MHz Burst-In, Burst-Out Rates Without Flags
- Cascadable To 13MHz
- Readily Expandable In Word And Bit Dimension
- TTL Compatible
- Asynchronous Or Synchronous Operation
- Three-State Outputs
- Master Reset Input To Clear Control
- Output Pins Directly Opposite Corresponding Input Pins For Easy Board Layout
- Available In 28 Pin Ceramic DIP, CERDIP, Or Contact Chip Carrier

Applications

- High-Speed Disk Or Tape Controller
- Video Time Base Correction
- A/D Output Buffers
- Voice Synthesis
- Input/Output Formatter For Digital Filters And FFTs

Functional Block Diagram



TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

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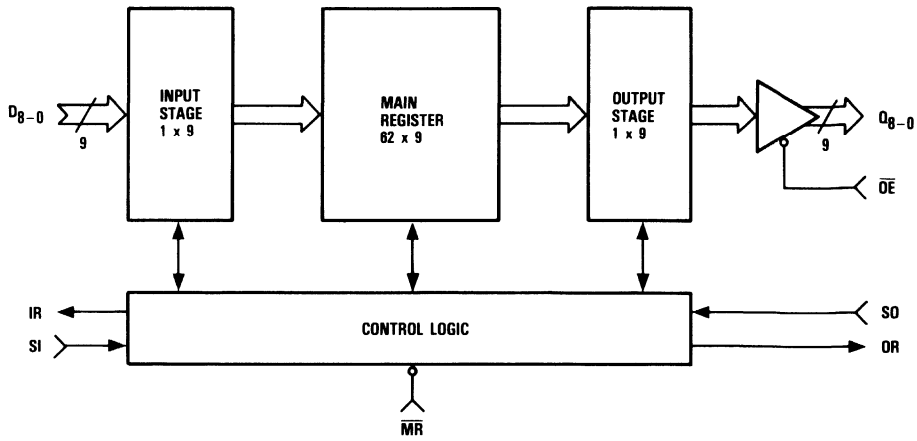
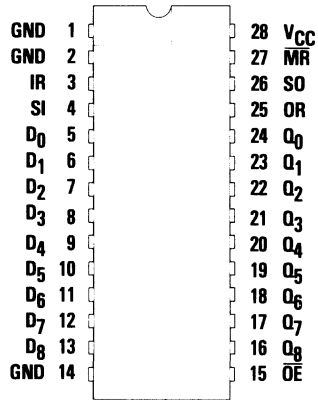
FAX: (619) 455-6314

40G00400 Rev. J – 11/90
Printed in the U.S.A.

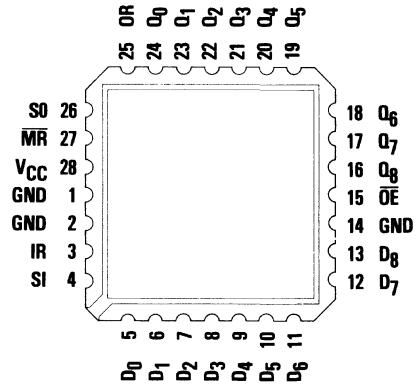
Functional Block Diagram



Pin Assignments



28 Lead DIP - J6 Package
28 Lead CERDIP - B6 Package



28 Contact Chip Carrier - C3 Package

Functional Description

Data Input (Figure 1)

Following power up, the Master Reset ($\overline{MR}$) is pulsed LOW to clear the FIFO (Figure 2). The Input Ready (IR) flag HIGH indicates that the FIFO input stage is empty and available to receive data. When IR is valid (HIGH), Shift-In (SI) may be asserted, thus loading the data present at D_0 through D_8 into the FIFO. Bringing the SI signal HIGH causes IR to drop LOW. The data remains at the first location until SI is set LOW. With SI LOW, the data then propagates to the second location and continues to "fall through" to the output stage or last empty location. If the FIFO is not full after the SI pulse, IR will again be valid (HIGH), indicating that there is space available in the FIFO. If the memory is full, the IR flag remains invalid (LOW).

With the FIFO full, the SI can be held HIGH until a Shift-Out (SO) occurs (Figure 3). Following the SO pulse, the empty location "bubbles up" to the input stage. This results in an Input Ready (IR) pulse HIGH and awaiting data is shifted in. The SI must be brought LOW before additional data can be shifted in.

Data Transfer

After data has been transferred into the second location by bringing SI LOW, the data continues to "fall through" the FIFO in an asynchronous manner. The data stacks up at the end of the device, leaving the empty locations up front.

Data Output (Figure 4)

The Output Ready (OR) flag HIGH indicates that there is valid data at the output stage (pins Q_0-Q_8). An initial Master Reset ($\overline{MR}$) pulse LOW at power up sets the Output Ready LOW (Figure 2). Although the internal control circuitry is cleared, random data remains on the output pins. Data shifted into the FIFO (after $\overline{MR}$) "falls through" to the output stage, causing OR to go HIGH, and replaces the random data with valid data.

When the OR flag is valid (HIGH), data can be transferred out via the Shift-Out (SO) control. An SO HIGH results in a "busy" (LOW) signal at the OR flag. When SO is brought LOW, data is shifted to the output stage, and the empty location "bubbles up" to the input stage. At the completion of the SO pulse, OR goes HIGH. If the last valid piece of data has been shifted out, leaving the memory empty, the OR flag remains invalid (LOW). With the FIFO empty, the last word shifted out remains on the output pins Q_0-Q_8.

With the FIFO empty, the SO can be held HIGH until a SI occurs (Figure 5). Following the SI pulse, the data "falls through" to the output stage. This results in an OR pulse HIGH and data is shifted out. The SO must be brought LOW before additional data can be shifted out.

Data Inputs

The nine data inputs of the TDC1030 are TTL compatible. There is no weighting to the inputs, and any one of them can be assigned as the MSB. The memory size of the FIFO can be reduced from the 9 x 64 configuration by leaving open unused data input pins (i.e., 8 x 64, 7 x 64 . . . 1 x 64). In the reduced format, the unused data output pins must also be left open.

Name	Function	Value	J6, C3, B6 Package
D_0	Data Input	TTL	Pin 5
D_1		TTL	Pin 6
D_2		TTL	Pin 7
D_3		TTL	Pin 8
D_4		TTL	Pin 9
D_5		TTL	Pin 10
D_6		TTL	Pin 11
D_7		TTL	Pin 12
D_8	Data Input	TTL	Pin 13

Data Outputs

The nine data outputs of the TDC1030 are TTL compatible, capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. There is no weighting to the outputs, and any one of them can be assigned as the MSB.

The memory size of the FIFO can be reduced from the 9 x 64 configuration by leaving open unused data output pins (i.e., 8 x 64, 7 x 64 . . . 1 x 64). In the reduced format, the unused data input pins must also be left open.

Name	Function	Value	J6, C3, B6 Package
Q_0	Data Output	TTL	Pin 24
Q_1		TTL	Pin 23
Q_2		TTL	Pin 22
Q_3		TTL	Pin 21
Q_4		TTL	Pin 20
Q_5		TTL	Pin 19
Q_6		TTL	Pin 18
Q_7		TTL	Pin 17
Q_8	Data Output	TTL	Pin 16

Controls

SI — The rising edge loads data into the input stage. The falling edge triggers the automatic data transfer process.

SO — The rising edge causes OR to go LOW. The falling edge moves upstream data into the output stage and triggers the "bubble up" process of empty locations.

$\overline{MR}$ — $\overline{MR}$ LOW clears all data and control within the FIFO: Input Ready flag is set HIGH, Output Ready flag is set LOW, and the FIFO is cleared. The output stage remains in the state of the last word shifted out, or in the random state of power up.

$\overline{OE}$ — With the $\overline{OE}$ LOW, the outputs of the FIFO are TTL compatible. When disabled ($\overline{OE}$ HIGH), the outputs go into their high-impedance state.

Name	Function	Value	J6, C3, B6 Package
SI	Shift-In	TTL	Pin 4
SO	Shift-Out	TTL	Pin 26
$\overline{MR}$	Master Reset	TTL	Pin 27
$\overline{OE}$	Output Enable	TTL	Pin 15

Power

The TDC1030 operates from a single +5.0V supply. All power and ground pins must be connected.

Name	Function	Value	J6, C3, B6 Package
V_{CC}	Supply Voltage	+5.0	Pin 28
GND	Digital Ground	0.0	Pins 1, 2, 14

Status Flags

Input Ready (IR) and Output Ready (OR) flags are provided to indicate the status of the FIFO. Operation with use of the flags is explained in the Functional Description. In this mode of operation, the Shift-In and Shift-Out rates are determined by the status flags. It is assumed that a Shift-In or Shift-Out pulse is not applied until the respective flag (IR, OR) is valid (Figures 1 and 4).

The IR and OR flags are not required to operate the device. A high-speed burst mode is achievable when operating without the flags. Refer to the High-Speed Burst Mode section for a complete description.

IR — An IR flag HIGH indicates that the input stage is empty and ready to accept valid data. An IR LOW indicates that the FIFO is full or that a previous SI operation is not complete.

OR — An OR flag HIGH assures valid data at the output stage (pins Q_0-Q_8). However, the OR flag does not indicate whether or not there is any new data awaiting transfer into the output stage. An OR LOW indicates that the output stage is "busy", or that there is no valid data.

Name	Function	Value	J6, C3, B6 Package
IR	Input Ready Flag	TTL	Pin 3
OR	Output Ready Flag	TTL	Pin 25

Application Notes

Expanded Format

The TDC1030 is easily cascaded to increase word capacity without any external circuitry. Word capacity can be expanded beyond the 128 words X 9 bits configuration shown in Figure 6. In the cascaded format, all necessary communications and timing are handled by the FIFOs themselves. The intercommunication speed is controlled by the minimum flag pulse widths and the flag delays. (See Figures 7 and 8.)The maximum data rate when cascading devices is 13MHz.

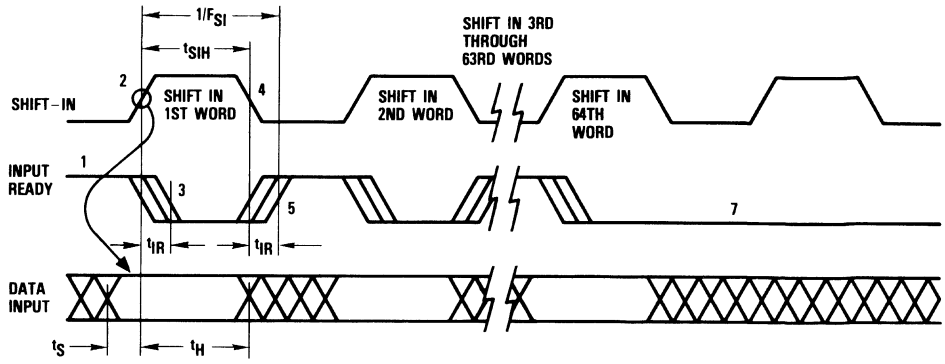
With the addition of a logic gate, the FIFO is easily expanded to increase word length (Figure 9). The basic operation and timing are identical to a single FIFO, with the exception of an additional gate delay on the flags. Word length can be expanded beyond the 18 bits X 64 words configuration shown in Figure 9.

High-Speed Burst Mode

Burst rates of 18MHz can be obtained for applications in which the device status flags are not used. In this mode of operation, the Burst-In and Burst-Out rates are determined by the minimum Shift-In Pulse Widths, and Shift-Out Pulse Widths (See Figures 10 and 11). With the Input Ready and Output Ready flags not monitored, a shift pulse can be applied without regard to the status flag. However, a Shift-In pulse which would overflow the storage capacity of the FIFO is not permitted.

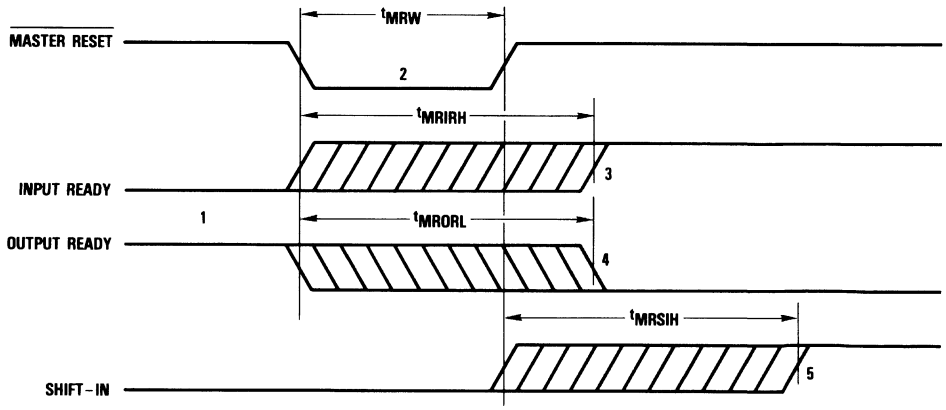
TDC1030 Timing Diagrams

Figure 1. Shifting In Sequence, FIFO Empty To FIFO Full



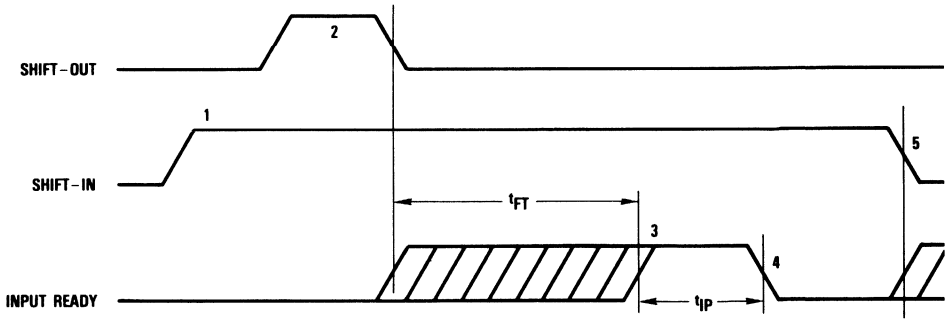
1. Input Ready initially HIGH – FIFO is prepared for valid data.
2. Shift-In set HIGH – data loaded into input stage.
3. Input Ready drops LOW (t_{IR} delay after SI HIGH) – input stage "busy."
4. Shift-In set LOW – data from first location "falls through."
5. Input Ready goes HIGH (t_{IR} delay after SI LOW) – status flag indicates FIFO prepared for additional data.
6. Repeat process to load 2nd through 64th word into FIFO.
7. Input Ready remains LOW – with attempt to shift into full FIFO, no data transfer occurs.

Figure 2. Master Reset Applied With FIFO Full



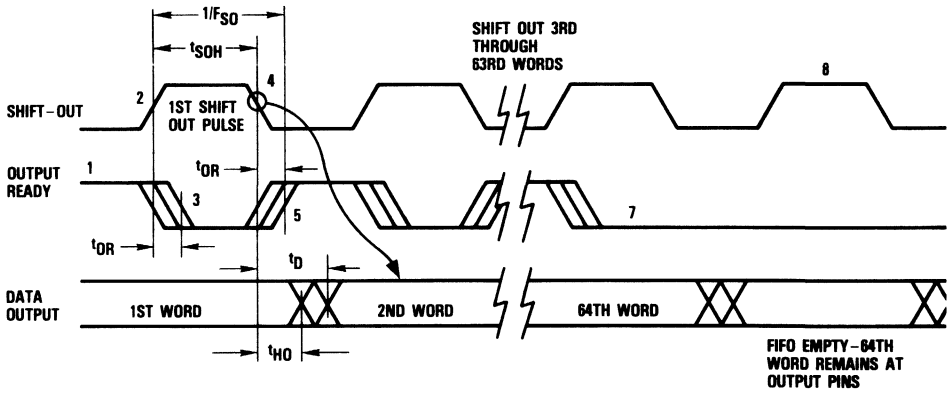
1. Input Ready LOW, Output Ready HIGH – assume FIFO is full.
2. Master Reset pulse LOW – clears FIFO.
3. Input Ready goes HIGH (t_{MRIRH} delay after $\overline{MR}$) – flag indicates input prepared for valid data.
4. Output Ready drops LOW (t_{MRORL} delay after $\overline{MR}$) – flag indicates FIFO empty.
5. Shift-In HIGH (t_{MRSI} delay after $\overline{MR}$) – clearing process complete, move new data into FIFO.

Figure 3. With FIFO Full, Shift-In Held High In Anticipation Of Empty Location



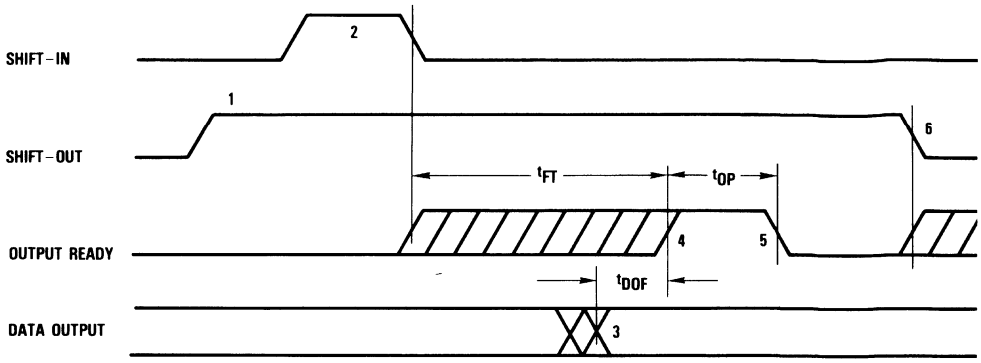
1. FIFO is initially full, Shift-In is held HIGH.
2. Shift-Out pulse - data in the output stage is unloaded, "bubble up" process of empty location begins.
3. Input Ready HIGH (t_{FT} fallthrough delay after SO pulse) - when empty location reaches input stage, flag indicates FIFO is prepared for data input.
4. Input Ready returns LOW - data Shift-In to empty location is complete, FIFO is again full.
5. SI brought LOW - necessary to complete Shift-In process, allows data "fall through" if additional empty location "bubbles up."

Figure 4. Shifting Out Sequence, FIFO Full to FIFO Empty



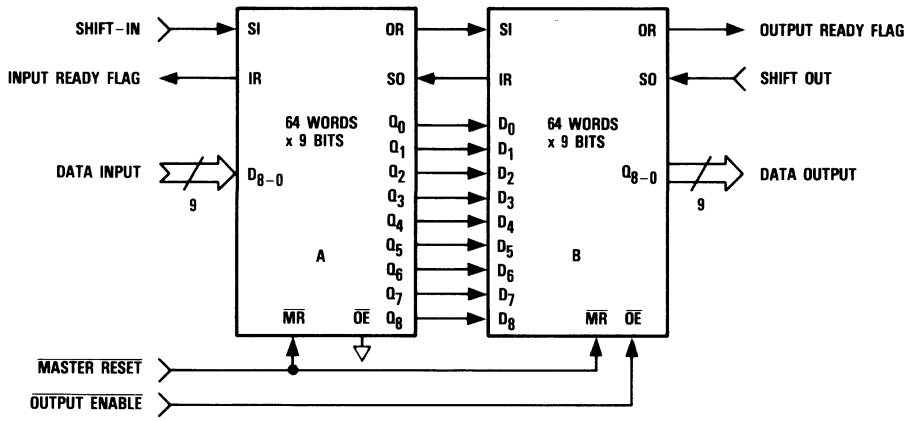
1. Output Ready HIGH - no data transferring in progress, valid data is present at output stage.
2. Shift-Out set HIGH - results in OR LOW.
3. Output Ready drops LOW (t_{OR} delay after SO HIGH) - output stage "busy."
4. Shift-Out set LOW - data in the input stage is unloaded, and new data replaces it as empty location "bubbles up" to input stage.
5. Output Ready goes HIGH - transfer process completed, valid data present at output.
6. Repeat process to unload the 3rd through 64th word from FIFO.
7. Output Ready remains LOW - FIFO is empty.
8. Shift-Out pulse asserted - with attempt to unload from empty FIFO, no data transfer occurs.

Figure 5. With FIFO Empty Shift Out Is Held High In Anticipation Of Data



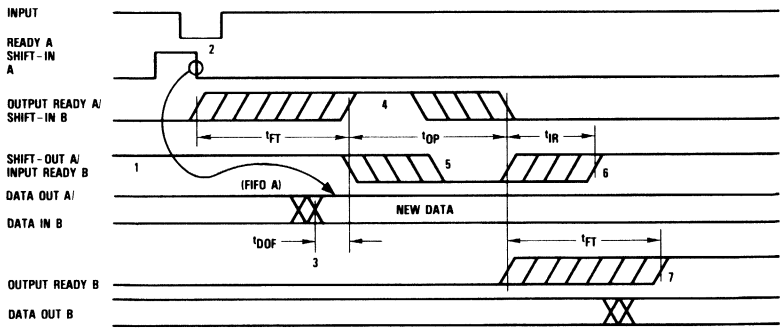
1. FIFO is initially empty, Shift-Out is held HIGH.
2. Shift-In pulse – loads data into FIFO and initiates "fall through" process.
3. Data Output transition – (t_{DOF} delay before OR HIGH), valid data arrives at output stage.
4. Output Ready HIGH – (t_{FT} fallthrough delay after SI pulse), OR flag signals the arrival of valid data at the output stage.
5. Output Ready goes LOW – data Shift-Out is complete, FIFO is again empty.
6. Shift-Out set LOW – necessary to complete Shift-Out process, allows "bubble up" of empty location as data "falls through."

Figure 6. Cascading For Increased Word Capacity – 128 Words X 9 Bits



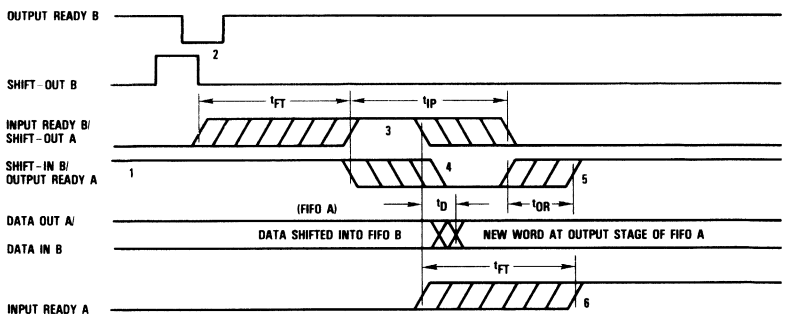
The TDC1030 is easily cascaded to increase word capacity without any external circuitry. In the cascaded format, all necessary communications are handled by the FIFOs themselves. Figures 7 and 8 demonstrate the intercommunication timing between FIFO A and FIFO B.

Figure 7. FIFO – FIFO Communication: Input Timing Under Empty Condition



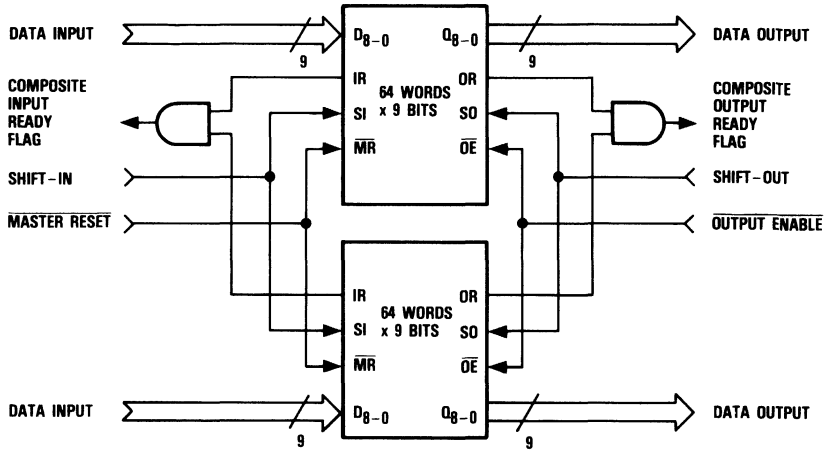
1. FIFO A and B initially empty, SO (A) held HIGH in anticipation of data.
2. Load one word into FIFO A – SI pulse applied, IR pulse results.
3. Data Out A/Data In B transition – (t_{DOF} delay before OR (A) HIGH), valid data arrives at FIFO A output stage prior to OR flag, meeting data input setup requirements of FIFO B.
4. OR (A) and SI (B) pulse HIGH – (t_{FT} delay after SI (A) LOW), data is unloaded from FIFO A as a result of the Output Ready Pulse (T_{OP}), data is shifted into FIFO B.
5. IR (B) and SO (A) go LOW – (t_{IR} delay after SI (B) HIGH), flag indicates input stage of FIFO B is "busy," Shift-Out of FIFO A is complete.
6. IR (B) and SO (A) go HIGH – (t_{IR} delay after SI (B) LOW), input stage of FIFO B is again available to receive data, SO is held HIGH in anticipation of additional data.
7. OR (B) goes HIGH – (t_{FT} delay after SI (B) LOW), valid data is present at the FIFO B output stage.

Figure 8. FIFO – FIFO Communication: Output Timing Under Full Condition



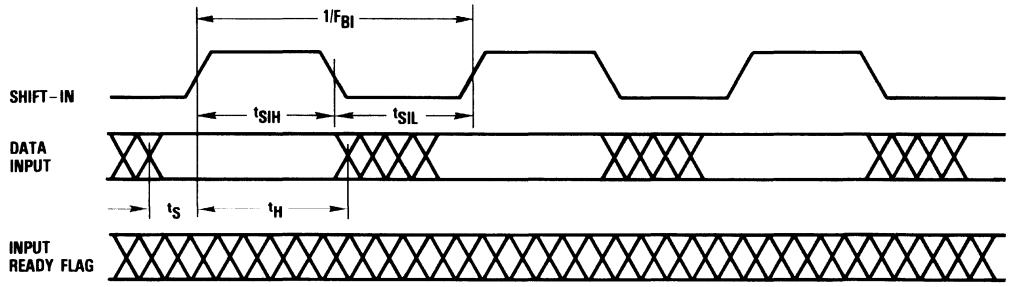
1. FIFO A and B initially full, SI (B) held HIGH in anticipation of shifting in new data as empty location "bubbles up."
2. Unload one word from FIFO B – SO pulse applied, OR pulse results.
3. IR (B) and SO (A) pulse HIGH – (t_{FT} delay after SO (B) LOW), data is loaded into FIFO B as a result of the Input Ready Pulse (tIP), data is shifted out of FIFO A.
4. OR (A) and SI (B) go LOW – (t_{OR} delay after SO (A) HIGH), flag indicates the output stage of FIFO A is "busy," Shift-In to FIFO B is complete.
5. OR (A) and SI (B) go HIGH – (t_{OR} delay after SO (A) LOW), flag indicates valid data is again available at the FIFO A output stage, SI (B) is held HIGH, awaiting "bubble up" of empty location.
6. IR (A) goes HIGH – (t_{FT} delay after SO (A) LOW), an empty location is present at input stage of FIFO A.

Figure 9. Expanded FIFO for Increased Word Length – 64 Words X 18 Bits



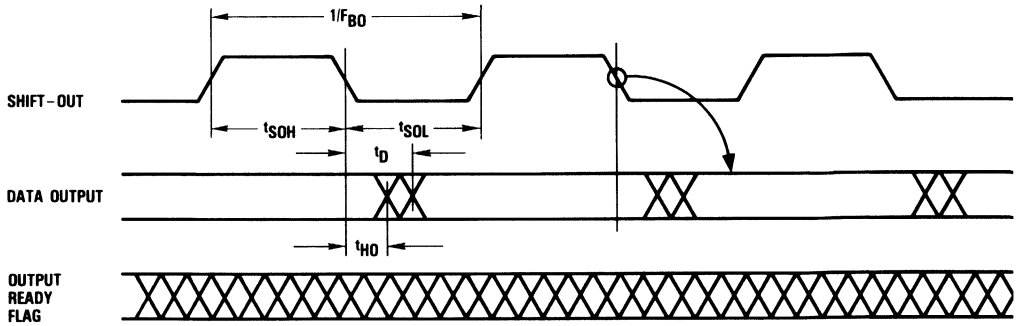
The TDC1030 is easily expanded to increase word length. Composite Input Ready and Output Ready flags are formed with the addition of an AND logic gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.

Figure 10. Shift-In Operation In High-Speed Burst Mode



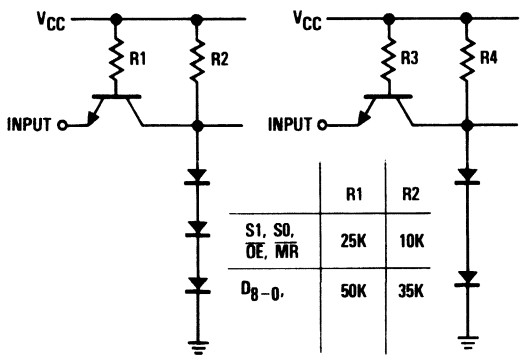
In the high-speed mode, the Burst-In rate is determined by the minimum Shift-In HIGH and Shift-In LOW specifications. The IR status flag is a "don't care" condition, and a Shift-In pulse can be applied without regard to the flag. A Shift-In pulse which would overflow the storage capacity of the FIFO is not permitted.

Figure 11. Shift-Out Operation In High-Speed Burst Mode



In the high-speed mode, the Burst-Out rate is determined by the minimum Shift-Out HIGH and Shift-Out LOW specifications. The OR flag is a "don't care" condition, and a Shift-Out pulse can be applied without regard to the flag.

Figure 12. Equivalent Input Circuit



	R1	R2
S1, S0, $\overline{OE}$, $\overline{MR}$	25K	10K
D_{8-0},	50K	35K

Figure 13. Equivalent Output Circuit

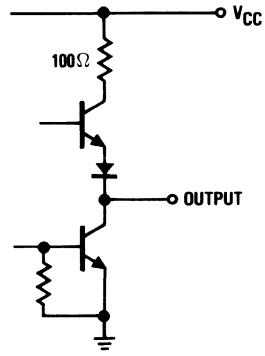


Figure 14. Test Load

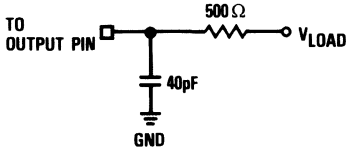
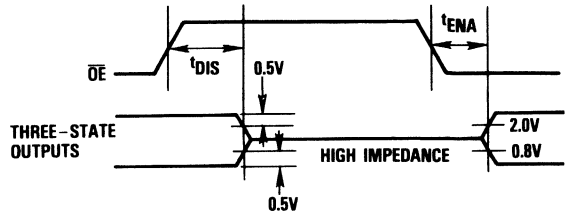


Figure 15. Transition Levels For Three-State Measurements



Absolute maximum ratings (beyond which the device will be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−6.0 to +6.0mA
Output	
Applied voltage	−0.5 to +5.5V [2]
Forced current	−1.0 to +6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, case	−60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{SIL}	Shift-In Pulse Width, LOW	20			20			ns
t_{SIH}	Shift-In Pulse Width, HIGH	15			18			ns
t_S	Input Setup Time	0			0			ns
t_H	Input Hold Time	25			30			ns
t_{SOL}	Shift-Out Pulse Width, LOW	20			20			ns
t_{SOH}	Shift-Out Pulse Width, HIGH	15			18			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = Max, static					
		T_A = 0°C to 70°C		350			mA
		T_A = 70°C		280			mA
		T_C = −55°C to 125°C				400	mA
		T_C = 125°C				260	mA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.4V					
		D_{8-0}		−0.4		−0.4	mA
		SI, SO, $\overline{OE}$, $\overline{MR}$		−1.0		−1.0	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V		75		75	μA
I_I	Input Current, Max Input Voltage	V_{CC} = Max, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	HIGH-Z Output, Leakage Current, Logic LOW	V_{CC} = Max, V_I = 0.4V		−40		−40	μA
I_{OZH}	HIGH-Z Output, Leakage Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V		40		40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, One pin to ground, one second duration, output HIGH.		−40		−40	mA
C_I	Input Capacitance	T_A = 25°C, F = 1.0MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, F = 1.0MHz		15		15	pF

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_{SI}	Shift-In Clock Rate	V_{CC} = Min	18		16		MHz
F_{BI}	Burst-In Clock Rate	V_{CC} = Min	20		18		MHz
t_{IR}	Input Ready Delay	V_{CC} = Min		40		50	ns
t_{FT}	Fallthrough Time	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		1.6		1.8	μs
F_{SO}	Shift-Out Clock Rate	V_{CC} = Min	15		13		MHz
F_{BO}	Burst-Out Clock Rate	V_{CC} = Min	18		16		MHz
t_{OR}	Output Ready Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		51		65	ns
t_D	Data Output Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		50		65	ns
t_{HO}	Data Output Hold Time	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V	15		15		ns
t_{MRW}	Master Reset Pulse Width	V_{CC} = Min	20		25		ns
t_{MRORL}	Master Reset to OR LOW	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		60		80	ns
t_{MRIRH}	Master Reset to IR HIGH	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V		45		65	ns
t_{MRSI}	Master Reset to SI	V_{CC} = Min	55		65		ns
t_{IP}	Input Ready Pulse	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V	40		45		ns
t_{OP}	Output Ready Pulse	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V	45		50		ns
t_{DOF}	Data To Output Flag Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.2V	1		1		ns
t_{ENA}	Three-State Output Enable Delay	V_{CC} = Min, Test Load: V_{LOAD} = 1.8V		35		45	ns
t_{DIS}	Three-State Output Disable Delay	V_{CC} = Min, Test Load: V_{LOAD} = 2.6V for t_{DIS0}, 0.0V for t_{DIS1} [2]		30		40	ns

Notes:
1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}, which are shown in Figure 15.
2. t_{DIS1} denotes the transition from logical 1 to three-state.
   t_{DIS0} denotes the transition from logical 0 to three-state.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1030B6C	STD – T_A = 0°C to 70°C	Commercial	28 Pin CERDIP	1030B6C
TDC1030B6A	EXT – T_C = –55°C to 125°C	High Reliability	28 Pin CERDIP	1030B6A
TDC1030C3C	STD – T_A = 0°C to 70°C	Commercial	28 Contact Hermetic Ceramic Chip Carrier	1030C3C
TDC1030C3A	EXT – T_C = –55°C to 125°C	High Reliability	28 Contact Hermetic Ceramic Chip Carrier	1030C3A
TDC1030J6C	STD – T_A = 0°C to 70°C	Commercial	28 Pin Hermetic Ceramic DIP	1030J6C
TDC1030J6A	EXT – T_C = –55°C to 125°C	High Reliability	28 Pin Hermetic Ceramic DIP	1030J6A

TMC2011/TMC2111

CMOS Variable-Length Shift Register

8-Bit, 30MHz

The TMC2011 and TMC2111 are high-speed, byte-wide shift registers with programmable delay lengths.

The TMC2011 can be programmed to any length between 3 and 18 stages. It offers a special split-word mode which allows for mixed delay lengths. The TMC2011, constructed in low-power CMOS, is pin and function compatible with the bipolar TDC1011.

The TMC2111 is a byte-wide shift register that can be programmed to lengths of 1 to 16 stages.

The TMC2011 and TMC2111 are fully synchronous, with all operations controlled by a single master clock. Input and output registers are positive-edge triggered D-type flip-flops. The length and mode controls are also registered. Both devices operate with a maximum clock rate of 30MHz.

Built with TRW's OMICRON-C™ one micron CMOS process, the TMC2011 and TMC2111 are TTL compatible, low-power replacements for the popular TDC1011, used in applications ranging from video to bit-slice processors.

Features

- Low Power CMOS
- Pin Compatible Replacement For The TDC1011 (TMC2011)
- Inputs And Outputs Fully TTL Compatible
- 30MHz Clock Rate (Worst Case Commercial)
- Selectable Delay Lengths (TMC2011: 3 To 18 Stages, TMC2111: 1 To 16 Stages)
- Special 4-Bit Wide Mixed-Delay Mode (TMC2011)
- Available In A 24 Pin, 0.3" Wide CERDIP

Applications

- Video Filtering
- High-Speed Data Acquisition
- Local Storage Registers
- Digital Delay Lines
- Television Special Effects
- Pipeline Register

K

TRW LSI Products Inc.
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La Jolla, CA 92038

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FAX: (619) 455-6314

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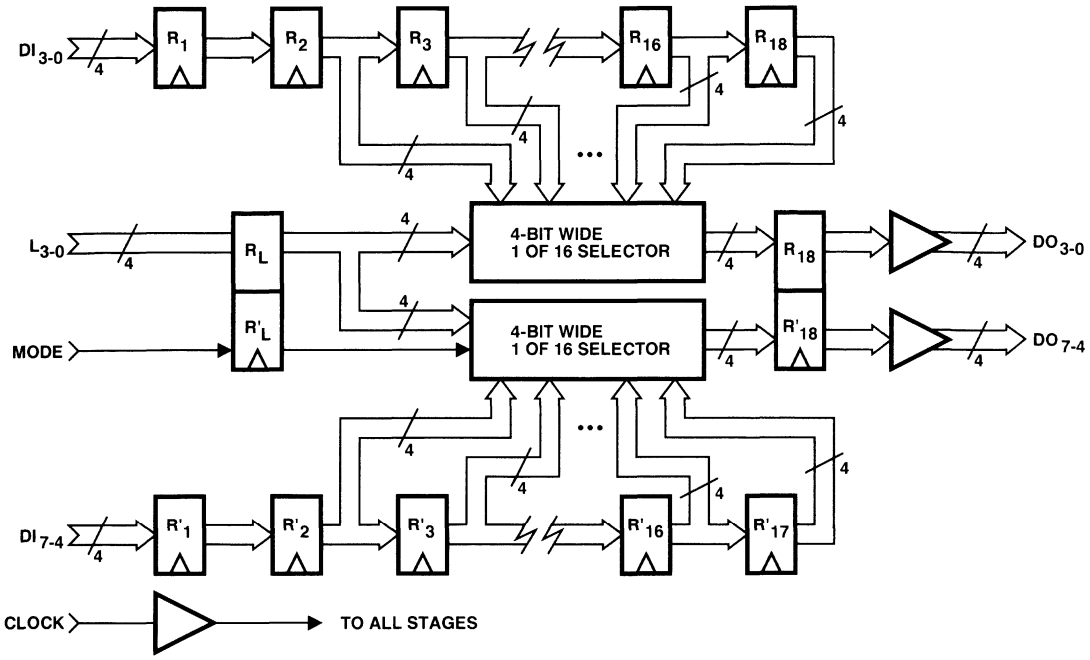
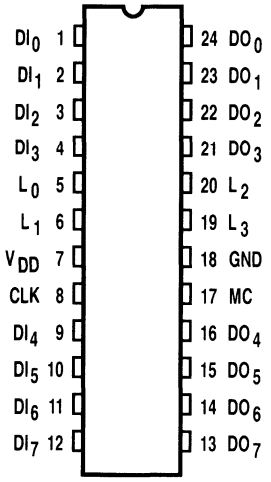
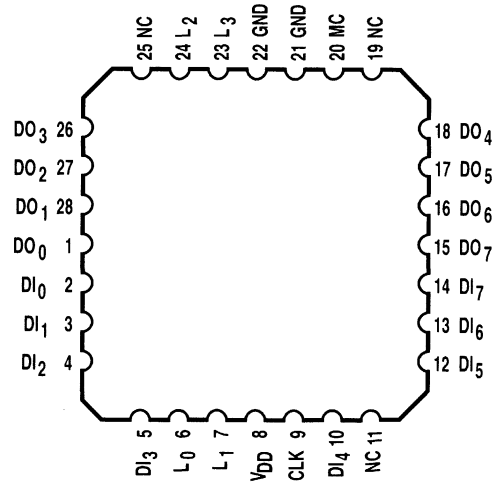
TMC2011 Functional Block Diagram



TMC2011 Pin Assignments

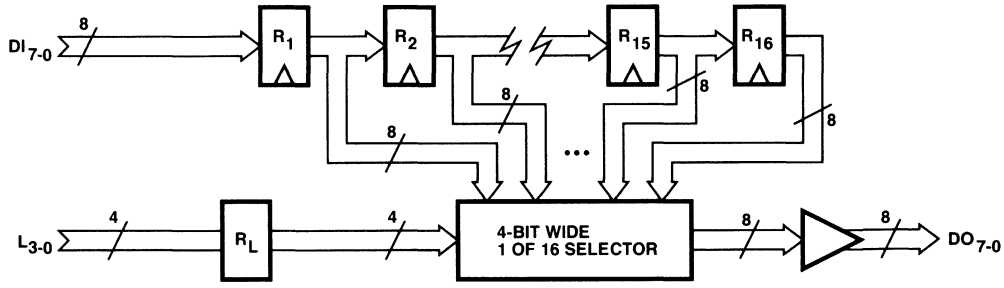


24 Lead CERDIP – B2 Package

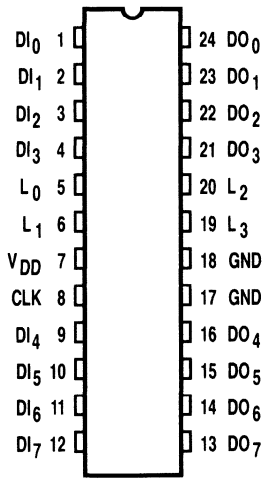


28 Contact Chip Carrier – C3 Package

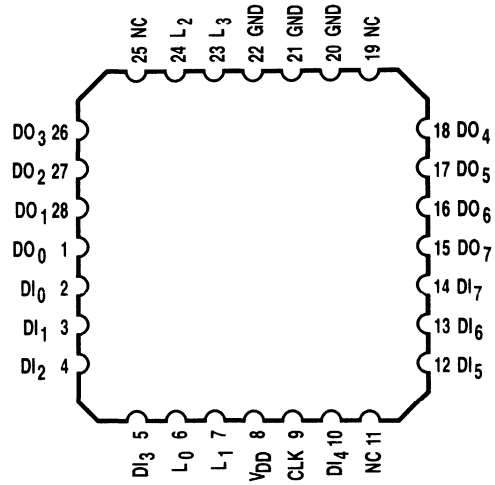
TMC2111 Functional Block Diagram



TMC2111 Pin Assignments



24 Pin CERDIP – B2 Package



28 Contact Chip Carrier – C3 Package

K

Functional Description

General Information

The TMC2011 consists of two 4-bit wide, programmable length shift registers. The TMC2111 consists of a single 8-bit wide, programmable length shift register. The internal registers of each device share control signals and a common clock.

Signal Definitions

Power

V_{DD}, GND — The TMC2011 and TMC2111 operate from a single +5V supply. All power and ground lines must be connected.

Data Inputs

DI_{0-7} — Eight inputs are provided for the data, which pass through the shift register unchanged. The eight inputs on the TMC2011 are divided into two groups of four bits to allow mixed delay operation. The lengths of these two groups are different when the Mode Control (MC) is HIGH (see *Table 1*). When MC is LOW both groups have equal delays. The TMC2111 consists of a single group of eight bits with all data bits having equal delays.

Data Outputs

DO_{0-7} — The outputs of the shift register are delayed relative to the input signals. The amount of the delay is programmable (see *Table 1*). The outputs remain valid for a minimum of t_{HO} nanoseconds after the leading edge of CLK. This allows the data to be latched into circuits with non-zero hold time requirements.

Controls

CLK — All inputs and outputs are synchronous and operate from a single master clock. All operations occur on the rising edge of the master clock.

L_{0-3} — The length select input is used to determine the register delay of the TMC2011 and TMC2111. This input is registered and affects the output on the cycle following input into the device (see *Timing*). Delay lengths are as specified in *Table 1*.

MC — The Mode Control (TMC2011 Only) is used to select the special 4-bit wide split mode on the TMC2011. When HIGH the delay on DO_{7-4} is fixed at 18 stages, while DO_{3-0} have the delay specified by the length select. When MC is LOW, all eight bits have equal delays as specified by the length select.

Table 1. Programming Length Controls

Input Code				TMC2011				TMC2111
				Mode (MC) = 0		Mode (MC) = 1		
L_3	L_2	L_1	L_0	DO_{3-0} Length	DO_{7-4} Length	DO_{3-0} Length	DO_{7-4} Length	DO_{7-0} Length
0	0	0	0	3	3	3	18	1
0	0	0	1	4	4	4	18	2
0	0	1	0	5	5	5	18	3
0	0	1	1	6	6	6	18	4
0	1	0	0	7	7	7	18	5
0	1	0	1	8	8	8	18	6
0	1	1	0	9	9	9	18	7
0	1	1	1	10	10	10	18	8
1	0	0	0	11	11	11	18	9
1	0	0	1	12	12	12	18	10
1	0	1	0	13	13	13	18	11
1	0	1	1	14	14	14	18	12
1	1	0	0	15	15	15	18	13
1	1	0	1	16	16	16	18	14
1	1	1	0	17	17	17	18	15
1	1	1	1	18	18	18	18	16

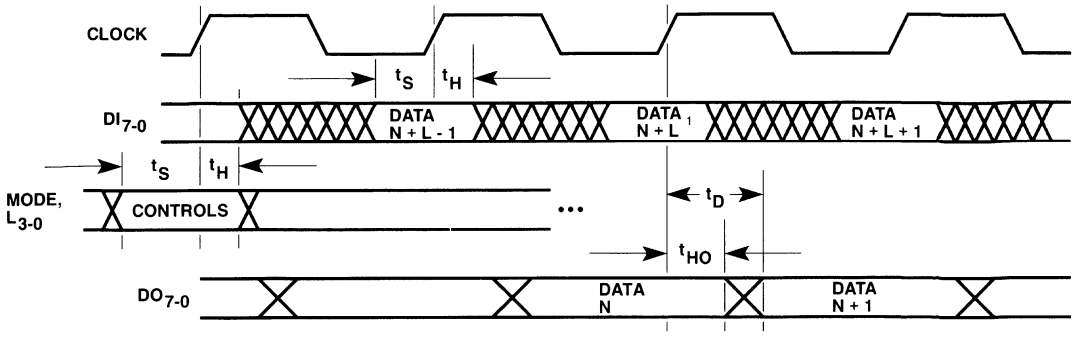
TMC2011 Package Interconnections

Signal Type	Signal Name	Function	B2 Package Pins	C3 Package Pins
Power	V_{DD}	Supply Voltage	7	8
	GND	Ground	18	21, 22
Inputs	DI_{7-0}	Data Input	12, 11, 10, 9, 4, 3, 2, 1	14, 13, 12, 10, 5, 4, 3, 2
Outputs	DO_{7-0}	Data Output	13, 14, 15, 16, 21, 22, 23, 24	15, 16, 17, 18, 26, 27, 28, 1
Clock	CLK	Master Clock	8	9
Controls	L_{3-0}	Length Select	19, 20, 6, 5	23, 24, 7, 6
	MC	Mode Control	17	20

TMC2111 Package Interconnections

Signal Type	Signal Name	Function	B2 Package Pins	C3 Package Pins
Power	V_{DD}	Supply Voltage	7	8
	GND	Ground	18, 17	21, 22, 20
Inputs	DI_{7-0}	Data Input	12, 11, 10, 9, 4, 3, 2, 1	14, 13, 12, 10, 5, 4, 3, 2
Outputs	DO_{7-0}	Data Output	13, 14, 15, 16, 21, 22, 23, 24	15, 16, 17, 18, 26, 27, 28, 1
Clock	CLK	Master Clock	8	9
Controls	L_{3-0}	Length Select	19, 20, 6, 5	23, 24, 7, 6

Figure 1. Timing Diagram (Preset Length Controls)



Note: 1. L is "DO_{7-4} Length" from Table 1.

Figure 2. Length Control Operation

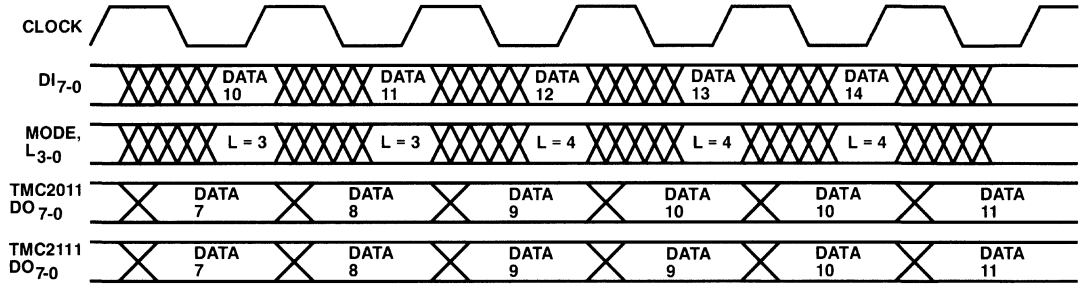


Figure 3. Equivalent Input Circuit

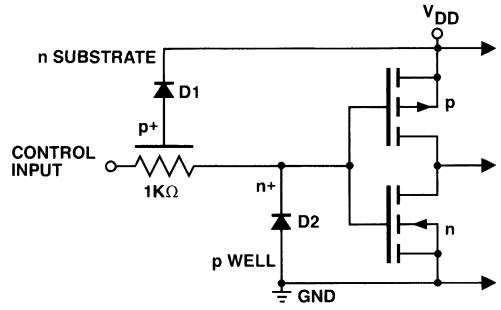
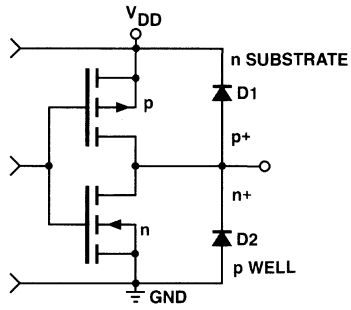


Figure 4. Equivalent Output Circuit



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD} + 0.5)V

Output

Applied voltage [2] ..... −0.5 to (V_{DD} + 0.5)V

Forced current [3,4] ..... −3.0 to +6.0mA

Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −60 to +130°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PWL}	Clock Pulse Width, LOW	12			12			ns
t_{PWH}	Clock Pulse Width, HIGH	12			12			ns
t_S	Input Setup Time	12			14			ns
t_H	Input Hold Time	0			0			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

K

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		5		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 30MHz		30		35	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	−10		−10		μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		+10		+10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		−100		−100	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.

Switching characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{CLK}	Maximum Clock Rate	V_{DD} = Min	30		28		MHz
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		20		24	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF	3		3		ns

Note: 1. All transitions are measured at a 1.5V level.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2011B2C	STD−T_A=0°C to 70°C	Commercial	24 Pin 0.3" CERDIP	2011B2C
TMC2011B2V	EXT−T_C=−55°C to 125°C	MIL-STD-883	24 Pin 0.3" CERDIP	2011B2V
TMC2111B2C	STD−T_A=0°C to 70°C	Commercial	24 Pin 0.3" CERDIP	2111B2C
TMC2111B2V	EXT−T_C=−55°C to 125°C	MIL-STD-883	24 Pin 0.3" CERDIP	2111B2V
TMC2011C3V	EXT−T_C=−55°C to 125°C	MIL-STD-883	28 Contact Hermetic Ceramic Chip Carrier	2011C3V
TMC2111C3V	EXT−T_C=−55°C to 125°C	MIL-STD-883	28 Contact Hermetic Ceramic Chip Carrier	2111C3V

TMC3220

Three Port Register File

32 Words x 8 Bits, 20MHz

The TMC3220 is a 32 word x 8-bit three port register file with one write port and two read ports. Separate enable controls on the data input and two independent outputs allow considerable flexibility in applications requiring synchronous or asynchronous data buffering or bus multiplexing. Manufactured in TRW's OMICRON-C™ CMOS process, the TMC3220 operates at a guaranteed clock rate of 20MHz over the commercial (0 to 70°C) and 15MHz over the extended (−55 to +125°C) temperature and supply voltage ranges. All input and outputs are TTL compatible.

Utilizing two separate 32 word x 8-bit dual-port RAMs, the TMC3220 allows the user to store input data in one or both Register Files, as determined by the write address and enables. Individual read addresses and three-state output enables allow data to be read from either register file independently.

The three-port register file is designed to operate with the TMC3200/3201 family of floating-point products, and has numerous applications as a scratch memory and flexible data buffer. Wider data paths and deeper memories are easily built by cascading multiple TMC3220s.

Features

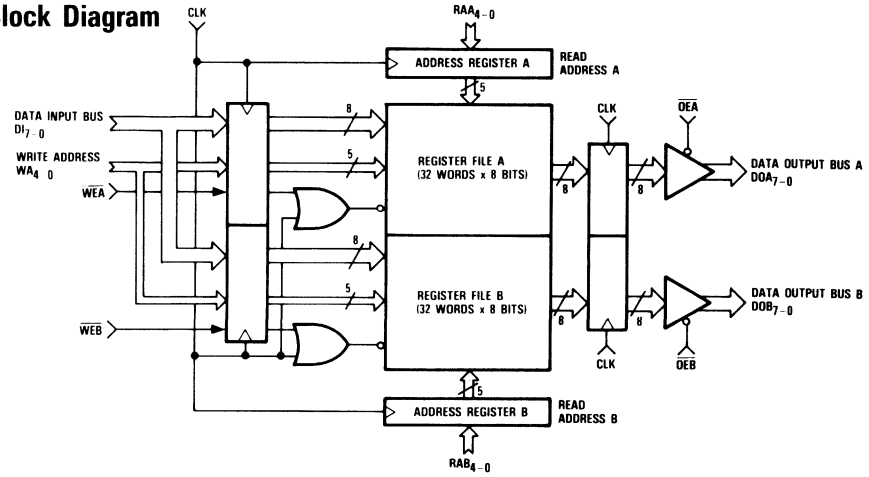
- 20MHz Clock Rate
- Configured For Use With TRW 32-Bit Floating-Point Product Family
- Two Fully Independent Read Ports
- Separate Write Enables
- Easily Cascadable In Word Size And Depth
- Low Power Consumption CMOS Process
- Three-State Outputs
- Available In A 48 Pin Hermetic Ceramic DIP Package

Applications

- Cache Memory For High-Speed Processors
- Interface For Multiple-Bus Systems
- Coefficient Storage For Image Processors
- High-Speed Program Memory

K

Functional Block Diagram



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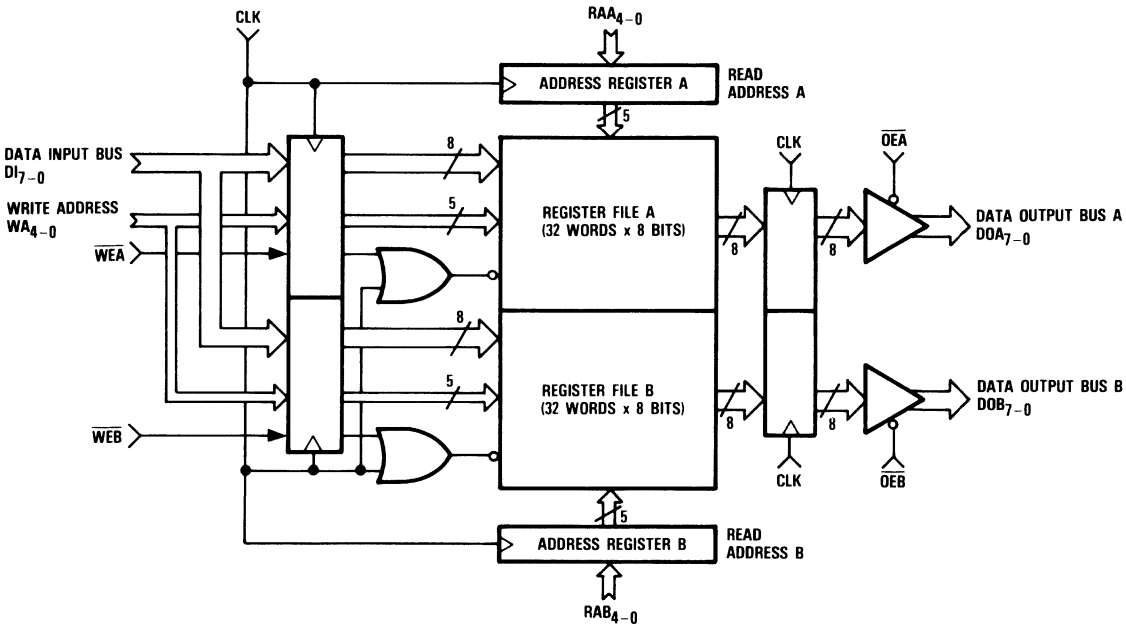
Functional Block Diagram



Pin Assignments

RAA_3	1	48	RAA_2
RAA_4	2	47	RAA_1
$\overline{OEA}$	3	46	RAA_0
DOA_0	4	45	$\overline{WEA}$
DOA_1	5	44	V_{DD}
DOA_2	6	43	DI_0
GND	7	42	DI_1
DOA_3	8	41	DI_2
DOA_4	9	40	DI_3
DOA_5	10	39	DI_4
DOA_6	11	38	DI_5
DOA_7	12	37	CLK
DOB_7	13	36	DI_6
DOB_6	14	35	DI_7
DOB_5	15	34	WA_0
DOB_4	16	33	WA_1
DOB_3	17	32	WA_2
V_{DD}	18	31	WA_3
DOB_2	19	30	WA_4
DOB_1	20	29	GND
DOB_0	21	28	$\overline{WEB}$
$\overline{OEB}$	22	27	RAB_0
RAB_4	23	26	RAB_1
RAB_3	24	25	RAB_2

48 Lead Ceramic DIP – J4 Package

Functional Description

General Information

The TMC3220 consists of two identical 32 word, 2-port RAMs. Data can be written to either or both register files as determined by the address and write enables. Data is independently read from either register file via seperate read address and output enable controls. All interface timing, except the output enables, is specified relative to the rising edge of Clock (CLK). All address and data inputs and outputs are registered, and both 8-bit read ports have independent three-state output enable controls.

The TMC3220 is a flexible member of the TRW 32-bit floating-point product family. See the example on page 7, which demonstrates the usefulness of the register file in a typical 32-bit floating-point application.

Read Sequence

Data can be read from either register file, independent of any other read or write operation, by presenting a 5-bit read address. With the appropriate output enables selected, 8-bit data will be available at the outputs within the specified delay. Otherwise, the output enables force the output ports to a high-impedance state.

Write Sequence

Data is written into either register file by presenting the 8-bit input data word, 5-bit write address, and the desired write enables to the input registers. Data is then written into memory after the clock goes LOW. All inputs must meet the indicated timing requirements.

The read cycle is initiated by the rising edge of Clock, and the data output latches are transparent while Clock is HIGH. The falling edge of Clock latches the read data and starts a write cycle, avoiding Read/Write contention.

Signal Definitions

Power

V_{DD}, GND — The TMC3220 operates from a single +5V supply. All pins must be connected.

Clock

CLK — The TMC3220 has a single clock input. All input registers are strobed on the rising edge of Clock, which is the reference for all timing specifications except the three-state output enables.

Inputs

DI_{7-0} — DI_7 through DI_0 is the 8-bit registered Data Input port for register files A and B.

Outputs

DOA_{7-0}, DOB_{7-0} — DOA and DOB are the latched 8-bit Data Output ports for register files A and B.

Controls

$\overline{WEA}$, $\overline{WEB}$ — The registered Write Enables for register files A and B are ORed with Clock to allow the registered input data to be written to memory when LOW.

WA_{4-0} — The 5-bit Write Address determines which memory location in register files A or B are to receive data during a write operation.

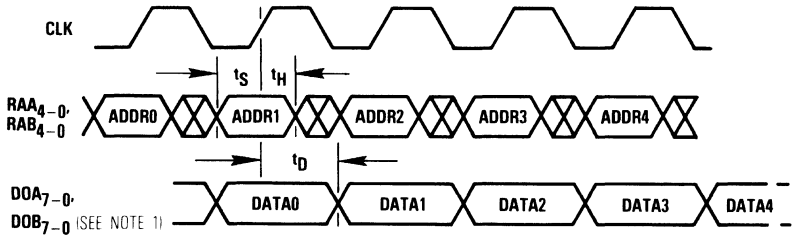
RAA_{4-0}, RAB_{4-0} — The 5-bit Read Address determines which memory location in register files A or B, respectively, will present data to the outputs after the specified delay.

$\overline{OEA}$, $\overline{OEB}$ — The Output Ports for register files A or B are in the high-impedance state when the respective Output Enable control is HIGH.

Package Interconnections

Signal Type	Signal Name	Function	J4 Package
Power	V_{DD}	Supply Voltage	18, 44
	GND	Ground	7, 29
Clock	CLK	Clock	37
Inputs	DI_{7-0}	Data Input	35, 36, 38, 39, 40, 41, 42, 43
Outputs	DOA_{7-0}	Data Output A	12, 11, 10, 9, 8, 6, 5, 4
	DOB_{7-0}	Data Output B	13, 14, 15, 16, 17, 19, 20, 21
Controls	$\overline{WEA}$	Write Enable A	45
	$\overline{WEB}$	Write Enable B	28
	WA_{4-0}	Write Address	30, 31, 32, 33, 34
	RAA_{4-0}	Read Address A	2, 1, 48, 47, 46
	RAB_{4-0}	Read Address B	23, 24, 25, 26, 27
	$\overline{OEA}$	Output Enable A	3
	$\overline{OEB}$	Output Enable B	22

Figure 1. Data Read Timing Diagram



Note 1. Assumes $\overline{OEA}$ and $\overline{OEB}$ = LOW.

Figure 2. Data Write Timing Diagram

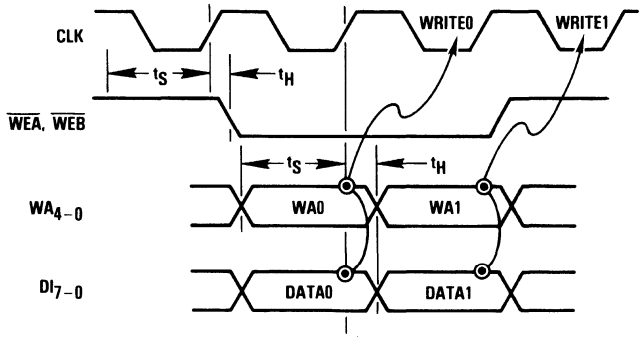


Figure 3. Equivalent Input Circuit

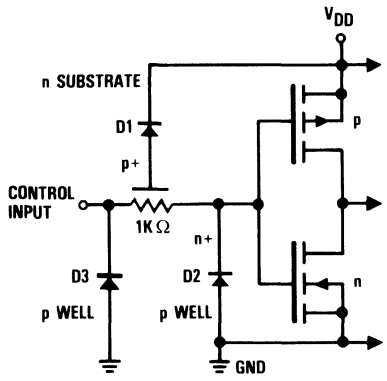


Figure 4. Equivalent Output Circuit

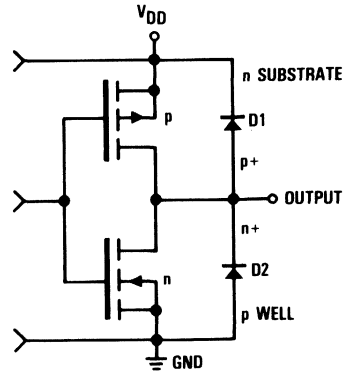
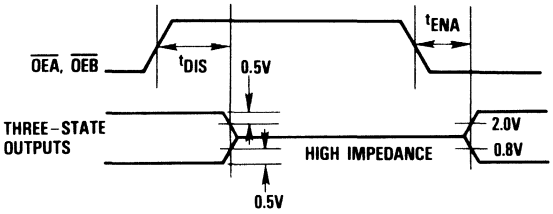


Figure 5. Threshold Levels for Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	-0.5 to +7.0V
Input Voltage	-0.5 to (V_{DD} +0.5V)
Output	
Applied voltage [2]	-0.5 to (V_{DD} +0.5V)
Forced current [3,4]	-1.0 to +6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	-60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	-65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current Logic LOW			4.0			4.0	mA
I_{OH}	Output Current Logic HIGH			-2.0			-2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				-55		125	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V, $\overline{OEA}$, $\overline{OEB}$ = HIGH		3		3	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz, $\overline{OEA}$, $\overline{OEB}$ = HIGH		30		30	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		-40		-40	µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	µA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		-40		-40	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	µA
I_{OS} [2]	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		-100		-100	mA
C_I [2]	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O [2]	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Notes: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Guaranteed but not tested.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_{CY}	Cycle Time	V_{DD} = Min		48		64	ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD} = Min	20		25		ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD} = Min	20		25		ns
t_S	Input Setup Time		12		15		ns
t_H	Input Hold Time		0		2		ns
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		36		45	ns
t_{ENA}	Three-State Output Enable Delay [1]	V_{DD} = Min, C_{LOAD} = 40pF		20		20	ns
t_{DIS}	Three-State Output Disable Delay [1]	V_{DD} = Min, C_{LOAD} = 40pF		18		20	ns

Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Application Notes

Using the TMC3220 with the TRW 32-Bit Floating-Point Arithmetic Products

The TMC3220 is a useful member of the TMC3200 family of 32-bit floating-point products. Figure 6 demonstrates how it can be used with in conjunction with the TMC3200 Floating-Point Arithmetic Unit and TMC3201 Floating-Point Multiplier to configure a flexible floating-point Multiplier-Accumulator module. The MSW flag of the TMC3200 is used to generate the least significant address bit for both TMC3220s, creating a multiplexed, "bit sliced" data path. The 16-bit output of the two register files is input alternately to the LSW and MSW ports of the TMC3200, the upper TMC3220 always storing the most significant and the lower TMC3220 always storing the least significant 8 bits of the 16-bit data path.

Since both the input and output ports are registered, the TMC3220 can handle "write-in-place" algorithms with a two clock-cycle latency. Figure 7 shows the block diagram and data timing for an application using the TMC3200 Floating-Point Arithmetic Unit in a user-configurable floating-point accumulator path. Note that the read and write addresses are identical. Also, the two TMC3220s are stacked to handle the 16-bit data path. The user writes into a particular address of the TMC3220 on one clock cycle, then reads from the same address on the next. When write enable is active, the input data is latched on the rising clock edge, but the new data does not appear on the outputs until after it is clocked through to the output register on the next clock cycle.

Figure 6. Multiplexed Addressing of the TMC3220 with TRW 32-Bit Floating-Point Arithmetic Products

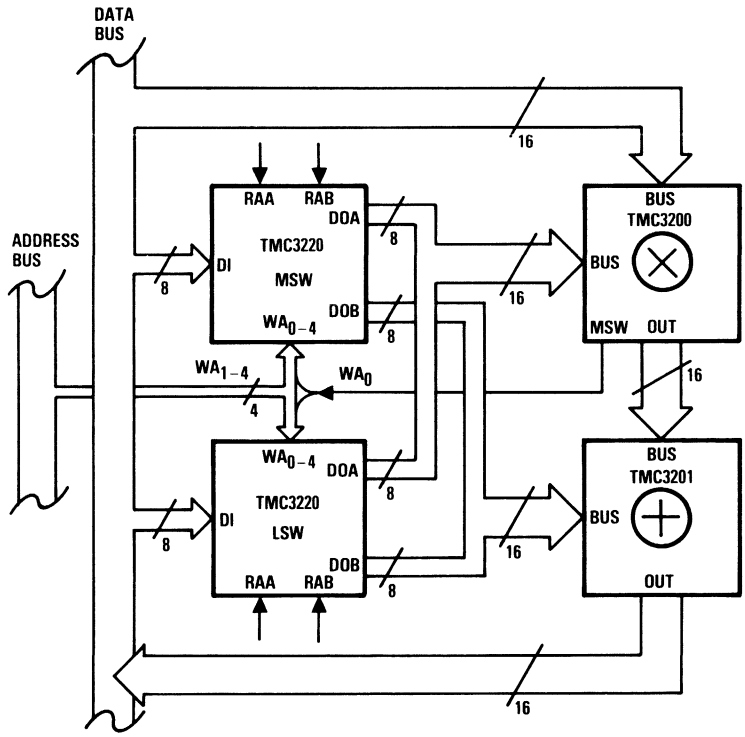
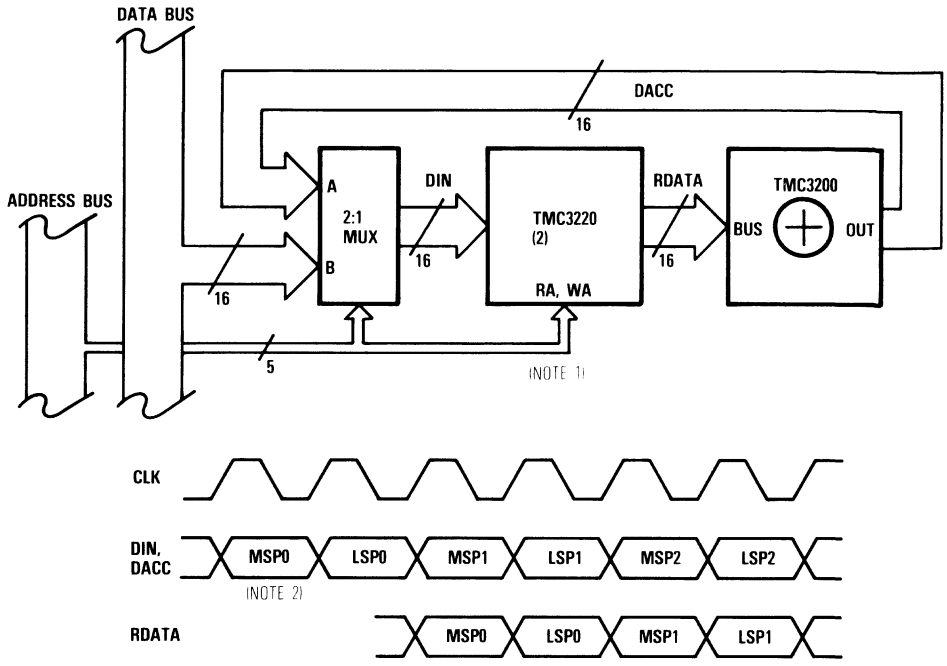


Figure 7. Accumulator Path Utilizing TMC3220



Notes:

1. $RAA_{4-0} = RAB_{4-0} = WA_{4-0}$
2. Timing Parameters are not shown on this diagram.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC3220J4C	STD – T_A = 0°C to 70°C	Commercial	48 Pin Hermetic Ceramic DIP	3220J4C
TMC3220J4V	EXT – T_C = – 55°C to 125°C	MIL-STD-883	48 Pin Hermetic Ceramic DIP	3220J4V

Quality: Meeting the Customers' Expectations
Reliability: Quality Over Time

Quality and Reliability begin long before mask is set to wafer. Our customers expect our products to easily solve difficult problems. Our products are expected to meet every published specification. Every part ordered is expected to arrive on time. Every product delivered is expected to work to specification when it is installed, and continue to perform to specification until the system itself reaches end of life.

These goals are accomplished through a rigorous program of product definition, development, characterization, process and product qualification, reliability testing, quality monitoring, reliability monitoring, and manufacturing controls. TRW's Total Quality Management (TQM) operating philosophy drives us to constantly improve every activity in the company, resulting in higher quality, more reliable, and more cost-effective products. A primary implementation tool is a company-wide Statistical Process Control (SPC) system that provides real-time feedback on the performance of all critical nodes throughout the manufacturing process. Work In Process (WIP) is kept as small as possible to minimize cycle times and speed the correction of process variations.

All employees have been trained in the process and procedures of Continuous Performance Improvement (CPI)™ as a means to resolve all manner of issues within our operations, and to implement changes to established systems. Numerous process-improvement teams are at work throughout the company analyzing, measuring, experimenting, testing, and implementing new methods and procedures. With company-wide participation, the TQM Operating Philosophy constantly reinforces the basic principle that the quality of the finished product (or service) is everyone's responsibility.

Manufacturing Flows

TRW LSI Products Inc. offers a number of manufacturing and screening flows to enable you to select the optimal product grade for your application. The flow used on a specific product is indicated by the grade:

Table 1. Product Manufacturing Flow Options.

Grade	Designation	Manufacturing Flow	Figure	Operating Temperature Range
A	High-Rel	High-Rel	1	–55°C to +125°C
B	Industrial	Commercial	2	–40°C to +85°C
C	Commercial	Commercial	2	0°C to +70°C
F	Extended Temp Range	Commercial	2	–55°C to +125°C
G	Burned-in	Com'l w/Burn-in	2	0°C to +70°C
V	MIL-STD-883	MIL-STD-883	1	–55°C to +125°C
SMD	Std Military Dwg	MIL-STD-883	1	–55°C to +125°C

Figure 1. Commercial and Industrial Product Flows (Grades B,C,F,G)

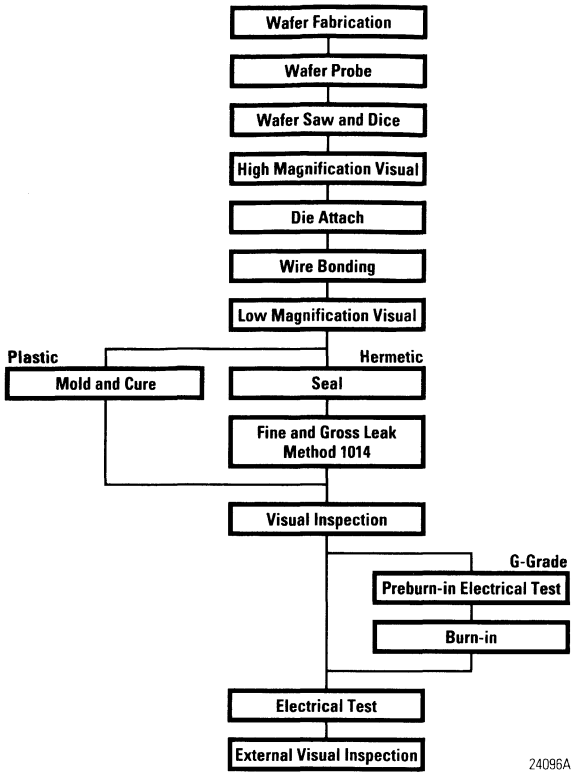
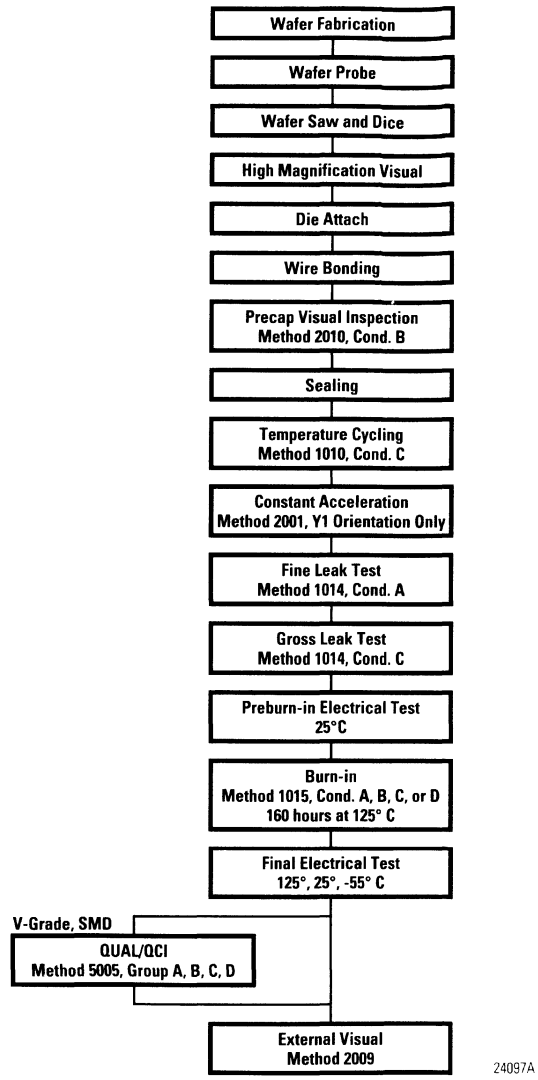


Figure 2. Military and High-Rel Product Flows (Grades A,V, and SMD)



TRW's quality systems comprise MIL-M-38510, Appendix A for High-Rel (A-Grade), MIL-STD-883 compliant (V-Grade), and Standardized Military Drawing (SMD) products; MIL-Q-9858, and MIL-I-45208 for Industrial (B-Grade), Extended Temperature Range (F-Grade), and Commercial (C,G-Grade) products. All quality systems adhere to MIL-STD-45662 for calibration of measurement and test equipment.

Military Products

Processing

TRW LSI Products Inc offers three levels of products for military applications:

V-Grade products are fully compliant with MIL-STD-883, Class B, and are processed in accordance with paragraph 1.2.1 of that specification.

Selected products are available under the **SMD** (Standardized Military Drawing) program supervised by DESC (Defense Electronics Supply Center). These products are processed identically to the V-Grade product, but their specifications are controlled by the US government. They are screened to the electrical requirements of the applicable military drawing. The SMD program is intended to reduce the number of Source Control Drawings (SCDs) in the military system, and has been highly successful in that effort. TRW is pleased to add products to the SMD program when appropriate: contact the factory for information on products not yet included in the SMD inventory.

A-Grade products receive the same screening as V-Grade products, but are not fully compliant with the current release of MIL-STD-883. These are typically older products that were introduced prior to revision C of MIL-STD-883.

Quality Assurance Provisions

TRW's military products are processed in accordance with the class B quality assurance level requirements of MIL-STD-883 and are 100% screened to the requirements Method 5004, outlined in *Figure 2*. After screening, Groups A, B, C, and D of MIL-STD-883, method 5005 are performed in support of V-Grade and SMD products. Inspection lots failing to meet these quality conformance inspections are rejected from further military processing.

Group A inspection (*Figure 3*) consists of electrical testing, and is performed on each inspection lot or sublot. The test criteria are the electrical parameters specified for that individual device in the applicable device detail specification. Group A inspection(s) may also be performed in-line in accordance with Method 5005 of MIL-STD-883.

Figure 3. Group A Inspection (Electrical Tests)

Test	Quantity (accept no.)
Subgroup 1 Static tests at 25°C	116 (0)
Subgroup 2 Static tests at maximum rated operating temperature	116 (0)
Subgroup 3 Static tests at minimum rated operating temperature	116 (0)
Subgroup 4 Dynamic tests at 25°C	116 (0)
Subgroup 5 Dynamic tests at maximum rated operating temperature	116 (0)
Subgroup 6 Dynamic tests at minimum rated operating temperatuer	116 (0)
Subgroup 7 Functional tests at 25°C.	116 (0)
Subgroup 9 Switching tests at 25°C.	116 (0)
Subgroup 10 Switching tests at maximum rated operating temperature	116 (0)
Subgroup 11 Switching tests at minimum rated operating temperature	116 (0)

Group B inspection (*Figure 4*) consists of construction testing, and is performed on each inspection lot, or date code, for each package type and lead finish. Group B tests comprise Resistance to Solvents, Solderability, and Bond Strength. Alternate Group B inspection(s) may be performed on devices from each week of seal in lieu of being performed on each inspection lot, as allowed per Method 5005.

Figure 4. Group B Inspection (Construction Related Tests)

Test	Method	Condition	Quantity (accept no.) or LTPD
Subgroup 2 Resistance to solvents	2015		4 (0)
Subgroup 3 (Note 1) solderability	2003 or 2022	Soldering temperature of 245°C ±5°C.	10
Subgroup 5 (Note 2) Bond Strength	2011	Condition C or D	15

Note: 1. The LTPD for solderability test applies to the number of leads inspected, except no less than 3 devices shall be used to provide the number of leads required.

2. The LTPD for bond strength test is the number of bond pulls selected from a minimum of 4 devices.

Group C inspection (*Figure 5*) consists of die related tests which stress the silicon and circuitry. These tests include operating life and associated end point electrical tests for each microcircuit group for wafers fabricated during each calendar quarter. Group C qualifies the fabrication lot from which the sample was selected and all die from the same microcircuit group by the same fabrication line for a period of one year.

Figure 5. Group C Inspection (Die Related Tests)

Test	Method	Condition	Quantity (accept no.) or LTPD
Subgroup 1 Operating life test	1005	Test conditions to be specified (1,000 hours at 125°C or equivalent)	5
End point electrical parameters		As specified per the applicable detail specification	

Group D inspection (*Figure 6*) consists of package related tests and additional tests to stress the silicon die. They comprise Physical Dimensions, Lead Integrity, Hermeticity, Thermal Shock, Temperature Cycling, Moisture Resistance, Mechanical Shock, Vibration Variable Frequency, Constant Acceleration, Salt Atmosphere, Visual Inspections and End Point Electricals; and are performed on each package type and lead finish. Group D qualifies the inspection lot from which the sample was selected and all lots of the same package type and lead finish for a period of one year.

Figure 6. Group D Inspection (Package Related Tests)

Test	Method	Condition	Quantity (accept no.) or LTPD
Subgroup 1 Physical diminsions	2016		15
Subgroup 2 Lead integrity	2004	Test Conditions B2 (lead fatigue)	15
Pin Grid Array Seal (fine and gross)	2028 1014	Condtion D Test Condition A & C	
Subgroup 3 Thermal shock Temperature cycling Moisture resistance Seal (fine and gross) Visual examination End point electrical parameters	1011 1010 1004 1014	Test Condition B - 15 cycles Test condition C – 100 cycles Test condition A & C Criteria per 1004 and 1010 As specified per the applicable detail specification	15
Subgroup 4 Mechanical shock Vibration, varible frequency Constant acceleration Seal (fine and gross) Visual examination End point electrical parameters	2002 2007 2001 1014	Test condition B Test condition A Test condition D or E, Y1 axis Test condition A & C Criteria per 1010 As specified per the applicable detail specification	15
Subgroup 5 Salt atmosphere Seal (fine and gross) Visual examination	1009 1014	Test condition A Test condition A & C Criteria per 1009	15 (0)
Subgroup 6 Internal water vapor content	1018	5,000 ppm maximum water content at 100°C.	3 (0) or 5 (1)
Subgroup 7 Adhesion of lead finish	2025		15 (0)
Subgroup 8 Lid Torque	2024		5 (0)

Reliability

TRW's integrated circuit operations were launched in the early 1960s to supply TRW's Spacecraft Manufacturing Sector with leading-edge semiconductors for advanced military satellite programs. In this application, reliability is of prime importance.

TRW conducts primary research into factors affecting semiconductor life in benign and hostile environments, in worst-case design methodologies, in semiconductor degradation in severe thermal and radiation environments, in the impact of component reliability on system performance, and in design techniques to maximize system availability and performance. A recent product of this work is the CPUAX, a 0.5μ CMOS SuperChip comprising 4.1 million active devices on a die 1.5 inches on a side, developed under VHSIC (Very High Speed Integrated Circuit) Program Phase II. This Processor performs 200 MFLOPS (Million Floating Point Operations per Second) and is self-testing, self-configuring, and self- healing.

The semiconductor processes and design techniques that have been applied to the merchant semiconductor business by TRW LSI Products Inc. reflect this heritage. Worst-case design is standard practice. Worst-case specifications are provided on all devices. The processes employed (including our original one-micron triple-diffused bipolar process - Omicron-B™ and advanced one-micron retrograde-well CMOS - Omicron-C™) are fundamentally reliable. From the starting wafer material through final passivation, every step is conservatively designed, carefully simulated, and closely monitored to ensure that your confidence is well placed, and that your system will perform to specification throughout its life.

All of these basic reliability-driving considerations are applied equally to product manufactured for satellites and to devices intended for PCs. They are designed to the same rules, built in in the same facility, monitored with the same process controls, and backed by the same reputation for reliability.

And the proof is in the practice. Time and again, TRW satellites, employing TRW semiconductors, have substantially exceeded their design lives.

Reliability Qualification

Even with a rigorous design and manufacturing methodology, it is important to monitor the reliability of the resulting product, both as verification of the completed product and as input to improving the systems for the the future. TRW LSI Products Inc. has a formalized reliability qualification program with a focus on design, development and manufacturing aspects to ensure superior performance, reliability, and compliance with all specification requirements. *Tables 2*, *3*, and *4* outline the qualification guidelines.

Table 2. Reliability Qualification Requirements For Hermetic Products

TEST	Duration	Full Qualification LTPD	Full Qualification ACC/SS	Test/ Method Condition
GROUP B TESTS				
B2				
Resistance to Solvents		15	0/15	2015
B3				
Solderability		15	0/15	2003, 3 Devices, 5 Leads/Device LPTD Applies to No. of Leads
B4				
Internal Visual			0/3	2014
B5				
Wire Bond Pull		15	0/15	2011, Cond.D, 4 Devices; 4 Wires/Devices LTPD Applies to No. of Wires
B7				
Seal				
Fine Leak		5	0/45	1014, Cond. A1
Gross Leak		5	0/45	1014, Cond. C1
B9				
Die Shear Strength		15	0/15	2019
GROUP C TESTS				
C1				
Steady State Life Test	125°C			
Bipolar	1000 Hrs	5	2/105	1005, Cond. B
	or			
Dynamic Life Test	125°C			
CMOS	1000 Hrs			1005, Cond. D
C2				
Temperature Cycle	10 Cyc	15	2/34	1010, Cond. C
Constant Acceleration		15	2/34	2001, Cond. E (30,000g) Y Orient. Only
Fine Leak		15	2/34	1014, Cond. A1
Gross Leak		15	2/34	1014, Cond. C1
Visual Examination		15	2/34	
End Point Electricals		15	2/34	Per Applicable Device Spec @ 25°C
GROUP D TESTS				
D1				
Physical Dimensions		15	0/15	2016
D2				
Lead Integrity		15	0/15	2004, Cond. B2
Fine Leak		15	0/15	1014, Cond. A1
Gross Leak		15	0/15	1014, Cond. C1
D3				
Thermal Shock	15 Cyc	15	2/34	1011, Cond. B
Temperature Cycle	100 Cyc	15	2/34	1010, Cond. C
Moisture Resistance	10 Cyc	15	2/34	1004
Fine Leak		15	2/34	1014, Cond. A1
Gross Leak		15	2/34	1014, Cond. C1
End Point Electricals		15	2/34	Per Applicable Device Spec @ 25°C
D4				
Mechanical Shock		15	2/34	2002, Cond. B
Vibration, Variable Freq.		15	2/34	2007, Cond. A
Constant Acceleration		15	2/34	2001, Cond E, Y Orient Only
Fine Leak		15	2/34	1014, Cond. A1
Gross Leak		15	2/34	1014, Cond. C1
End Point Electricals		15	2/34	Per Applicable Device Spec @ 25°C

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Table 3. Reliability Qualification Requirements For Plastic Products

TEST	Full Qualification Duration	LTPD	ACC/SS	Test/ Method Condition
C1[1] Steady State Life Test (Bipolar) Dynamic Life Test (CMOS)	1000 Hrs[2]	5	2/105	1005, Cond. B, 125°C 1005, Cond. D, 125°C
85/85 (Temp/Humidity/Bias-THB)	1000 Hrs[2]	5	1/77	JEDEC 22, A101, 85°C/85% R.H.
Pressure Cooker Test (PCT)	96 Hrs[3]	7	1/55	JEDEC 22, A102, 2 Atm. 121°C
Temperature Cycle	200 Cycles	7	2/75	1010, Cond. C, –65°C to 150°C
Thermal Shock	50 Cycles	7	2/75	1011, Cond, C. –65°C to 150°C
X-Ray		15	0/15	Top View
Die Shear Strength		15	0/15	2019
Wire Bond Pull		15	0/15	2011, Cond.D, 4 Devices, 4 Wires/Devices LTPD Applies to No. of Wires
B1 - Gp. D, Sub 2 Test per 883 Lead Integrity		15	0/15	2004, 4 Leads Per Unit
B2 Adhesion of Lead Finish		15	0/15	2025, 4 Leads Per Unit LTPD Applies to No. of Leads
B3 Solderability		15	0/15	2003, 3 Devices, 5 Leads/Device LTPD Applies to No. of Leads
B4 Resistance to Solvents		15	0/15	2015
B5 Physical Dimensions		15	0/15	2016

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Notes:
1. Burn-in and life test temperature may be adjusted to a lower temperature so the junction temperature will not exceed plastic glass transition temperature for a specified molding compound. Junction temperature shall be 10°C lower than molding compound glass transition temperature.
2. Interim readouts at 168, 500 and 1000 hrs.
3. Interim readouts at 48 and 96 hrs.

Table 4. Guidelines For Qualification Test Requirements

QUALIFICATION OBJECTIVE / TEST	OPR LIFE	HIGH TEMP STORAGE	T/C	T/S	*STEAM	*85/85	ESD	BOND PULL	DIE SHEAR	SOLDER ABILITY	LEAD INTEG	SALT ATMOS	RESIS SOLV.	+MECH SEQ.	+CAVITY MOIS.
New Product	X	0	0	0	0	0	X								
Die Metal	X	0	X	X	X	X		X							
Glassivation	X		0	0	X	X									
Die Layout	X	0	0	0	0	0	0								
Major Fab Process	X	0	0	0	0	0									
New Fab Location	X	0	X	X	X	X									
New Assy. Location	X		X	X	X	X		X	X	X	X	X	X		X
Wire Bond		0	X	X				X						X	
Die Attach	0	0	X	X	0	0		X	X					X	
Molding Compound	X	0	X	X	X	X		0				X			
Molding Process	X		X	X	X	X		0							
Lead Frame			0	0	X	X		X		X	X				
Hermetic Package			X	X				0	0					X	X
Seal +	0	0	0	0				X	X				X	X	X
Lead Finish					X					X		X			
Trim/Form											X	X			
Marking					X							X	X		

Notes: + Hermetic Package Only
X Mandatory
* Plastic Only
0 Optional - May be required if data/engineering judgement indicates need for assessment.
Mech Seq. - Mechanical Sequence - Gp D, Subgroup 4 Testing

24104A

Failure Rate Calculations and Predictions

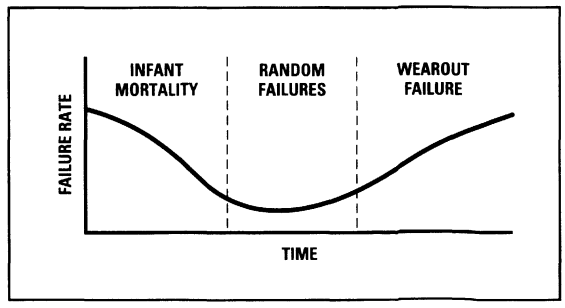
Accelerated stress testing is a very good means of performing reliability evaluations on semiconductor devices. Testing of this type induces certain reactions within the device and eventually causes it to degrade beyond specified operating limits (*Figure 7*). The reaction rate associated with these changes is given in terms of thermal activation energy, E_a. Additionally, the reaction rate increases exponentially with temperature and relates to increases in device failure rates. The physiochemical process which relates reaction rate to temperature can be expressed in the form of the Arrhenius equation:

$$R = R_O \exp(-E_a / kT) \qquad (1)$$

Where: R = Reaction rate as a function of time and temperature
R_O = Constant related to temperature
E_a = Thermal activation energy in electron-volts, eV
k = Boltzman's constant, 8.6 x 10^{-5} eV/°K
T = Absolute temperature, °K (°C + 273)

Obviously, the choice of an appropriate activation energy is of significance and should be carefully determined. *Table 5* defines common activation energies used for semiconductor devices. *Figure 8* represents the Arrhenius plot from which the data in *Table 5* was derived.

Figure 7. Failures vs Time (Bathtub Curve)

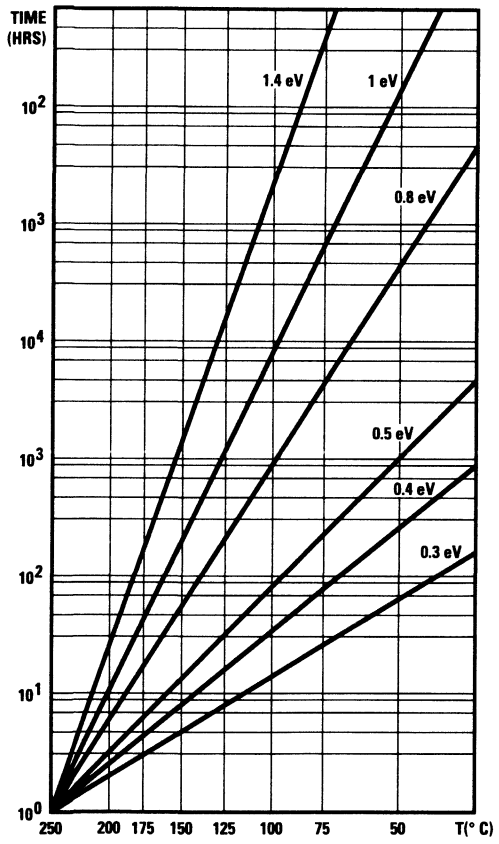


24105A

Table 5. Activation Energies for Primary Failure Mechanisms

Failure Mechanism	Ea
Contamination	1 ~ 1.4 eV
Polarization	1 eV
Aluminum Migration	0.5 eV
Trapping	1 eV
Oxide Breakdown	0.3 eV
Silicon Defects	0.5 eV

Figure 8. Arrhenius Plot



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Determination Of Failure Rates

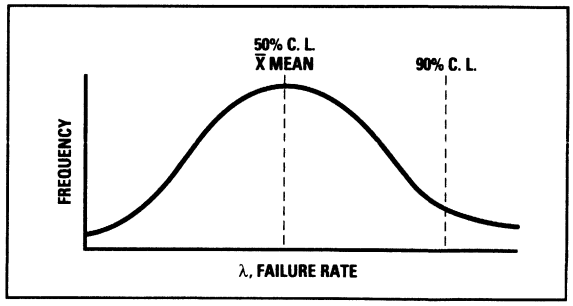
In the simplest form, the failure rate prediction at a given temperature can be predicted as follows.

$$\text{Failure Rate} = \lambda = \frac{N}{DH} \qquad (2)$$

Where: N = number of failure
D = number of devices
H = number of hours tested

Assuming that semiconductors exhibit a log normal distribution, the simple calculation above would coincide with a 50% confidence Level (C.L.), which is also known as the mean of the distribution. This indicates that 50% of the device population will have a failure rate equal to or less than the stated value. Other confidence levels may also be used (see *Figure 5*).

Figure 9. Failure Distribution



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Acceleration Factors

The effects of temperature, time, voltage and other related functions is key when predicting life times of semiconductor devices. Understanding these effects (i.e., failure analysis) with the use of a more accurate mathematical model, provides a better means of evaluating the change in reaction rate to changes in temperature. Hence, expressing the Arrhenius equation in a different form will allow the extrapolation of a given failure rate at one temperature to a corresponding failure rate at another. This form of the Arrhenius is given as:

$$F(T1,T2) = \exp\left(\frac{-E_a}{k}\left(\frac{1}{T1} - \frac{1}{T2}\right)\right) \quad (3)$$

Where: F = Acceleration factor
T1 = Test temperature
T2 = Desired temperature

From the above, the equivalent device hours can be determined at temperature T2 for a specific E_a.

$$EDH(T2) = F(T1,T2) \times DH(T1) \quad (4)$$

The failure rate, λ, at T2 can be expressed as:

$$\lambda(T2) = \frac{N}{EDH\ (T2)} \quad (5)$$

Where: N = Number of failures
EDH = Equivalent device hours

Chi Square Function

The most common method of failure rate calculations, which may be performed at any confidence level, is the use of the Chi Square, χ^2, function.

$$\lambda \leq \frac{\chi^2(\alpha, 2r + 2)}{2DH} \quad (6)$$

Where: α = 1 - C.L. (Confidence Level)
r = Number of rejects
D = Number of devices tested
H = Number of hours tested

From the failure rate, the MTTF (Mean Time To Fail) can be expressed as:

$$MTTF = \frac{1}{\lambda} \quad (7)$$

The FIT (Failures In Time) rate is the most common expression for failure rates. FITs are defined as 1 failure in 1 x 10^9 hours. FITs are expressed in the form:

$$FIT = \frac{\chi^2 \times 10^9}{2DH \times F(T1,T2)} \quad (8)$$

Reliability Monitor Program

TRW LSI Products Inc. has an ongoing reliability monitor program to ensure early detection of any potential reliability concern. This program requires that periodic reliability testing be performed on various products in order to provide a basic library of reliability information. Gathering this information provide the data to direct appropriate steps for further evaluations or corrective actions. Table presents some of the reliability monitors performed.

Table 6. Reliability Monitors

Test	Description	Test Method
Operating Life	2,000 hrs, 125°C	883, 1005
Autoclave (PCT)	96 hrs	JEDEC 22,A102
85/85 (THB)	1,000 hrs	JEDEC 22,A101
Thermal Shock	50 cycles	883, 1011/C
Temp Cycle	100 cycles	883, 1010/C

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Reliability and Quality Assurance Department

Policy

It is the Policy of the Reliability and Quality Assurance Department of TRW LSI Products Inc. to ensure that defect-free products and services are provided that conform to corporate and customer requirements through Prevention Methodologies, Statistical Process Control, and Total Quality Management operational philosophies.

Organization

At TRW LSI Products Inc, the Reliability and Quality Assurance Department reports directly to the Vice President and General Manager and comprises four functional areas:

- Quality Assurance/Quality Control
- Reliability/Qualification
- Failure Analysis/Analytical Services
- Engineering Services (Document Control)

Quality Assurance/Quality Control manages and implements quality programs to ensure the institution and verification of corrective actions. Specifically, Quality Control performs quality inspections and reports various quality statistics and indicies.

Reliability/Qualification is responsible for reliability and qualification testing and performance of those tests required during screening and quality conformance testing. Additionally, this section provides reliability predictions and statistics to our customers on released products and processes.

Failure Analysis/Analytical Services provides the continued monitoring of manufacturing processes as established by Quality Assurance. Failure Analyses provide data to implement changes ensuring that repetitive type failures are prevented.

Engineering Services (Document Control) maintains the Configuration Management and Document Control systems. These systems are used to manage and control the formal release of all documents to appropriate control files throughout manufacturing and engineering operations. These systems also ensure that the rules and processes employed in design and manufacturing are properly documented and controlled, and that changes are not implemented without proper review.

Notes

Package Information

Package Information

Packaging is constantly evolving to meet the needs of the customer. We are active participants in the JEDEC JC-11 committee on mechanical outlines, and the JEDEC JC-13 committee on military specifications. Package outlines are designed to be in compliance with JEDEC Publication 95 and MIL-M-38510 Appendix C outlines (where applicable).

Products are offered in both hermetic and plastic versions. Hermetic packages offered include:

1) Sidebraze multilayer ceramic DIPs in leadcounts 16 thru 64 (.100 pitch),
2) Top/bottom brazed multilayered ceramic formed lead DIPs in leadcount 64 (.100 pitch),
3) CERDIP frit sealed in leadcounts 8 thru 40 (.100 pitch),
4) Ceramic quad flatpacks in leadcounts 64 (.040 and .050 pitch), 68 (.050 pitch), 84, 100 and 132 (.025 pitch),
5) Ceramic JEDEC Type C leadless chip carrier (.050 pitch) in pad counts 28, 44, 68;
6) Ceramic JEDEC Type A leadless chip carrier (.050 pitch) in pad count 68;
7) Ceramic brazed pin PGA (large outline, .100 grid centers) in pin counts 68, 88, and 120;
8) Metal DIPs in leadcounts 24 thru 46 (.100 pitch),
9) Metal cans.

Plastic packages offered include:

1) Plastic DIPs in leadcounts 8 thru 64 (.100) pitch,
2) Plastic leaded chip carrier in leadcounts 28 thru 84 (.050 pitch),
3) Plastic small outline IC in leadcounts 8 thru 20 (.050 pitch),
4) Plastic pin grid array in leadcounts 68 thru 120 (.100 pitch).

See the device detail information to identify which packages are offered on a given device.

Lead finish of the various packages are:

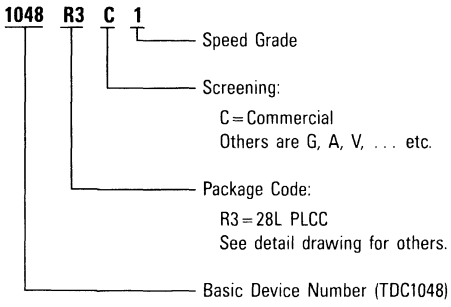
Package	Code	Gold	Tin	Solder	Note
Plastic DIP	N		X	X	1
Sidebraze DIP	J	X		X	2
Top/Bottom Brazed DIP	J	X		X	2
CERDIP	B			X	
Ceramic Quad Flatpack	L, F	X	X	X	
Type C Chip Carrier	C			X	
Type A Chip Carrier	A	X			
Ceramic PGA	G	X			
PLCC	R		X		
SOIC	M		X		
PPGA	H			X	
Metal DIPs	S	X			

Notes: 1. Solder offered on most products.
2. Solder offered on all MIL products.

For hermetic packages, we use the same package materials for both military and commercial grade devices. You are ensured that commercial grade hermetic packages have been procured and qualified to the same standards used for our military grade products.

Product Marking

Generic product's part number:

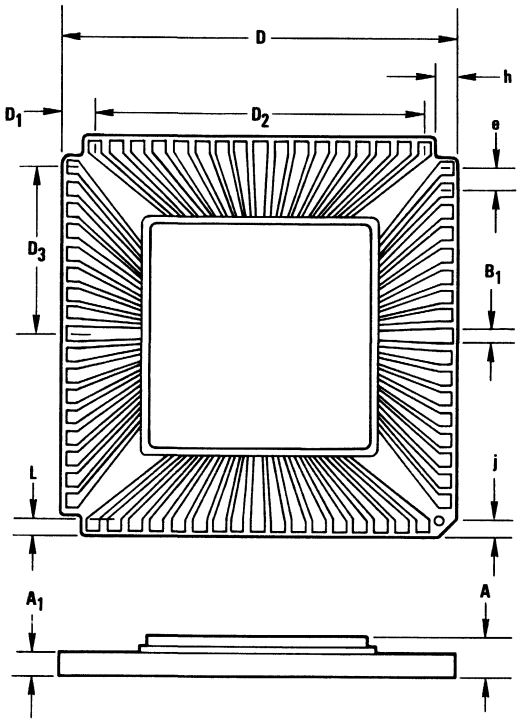


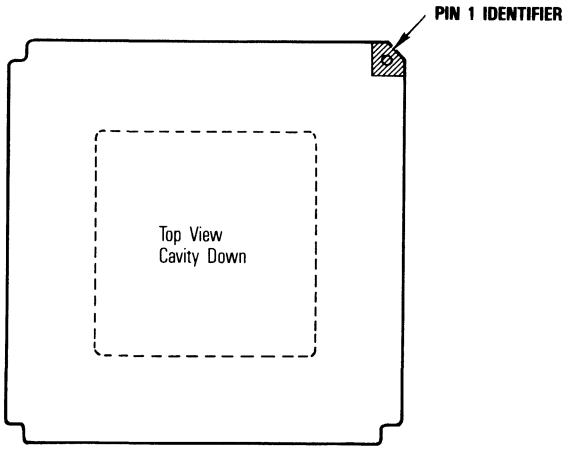
The following codes, one of which is stamped on the back of each TRW LSI Products Inc. device, identify the "country of origin" in which the device was manufactured.

Code	Country of Origin
Korea	Korea
Hong Kong	Hong Kong, BCC
Philippines	Philippines
Taiwan	Taiwan
CP	San Diego, CA, U.S.A.
SJ	San Jose, CA, U.S.A.
MA	Massachusetts, U.S.A.

A1 Package

68 Contact Hermetic Ceramic Chip Carrier
JEDEC Type A





Dimensions

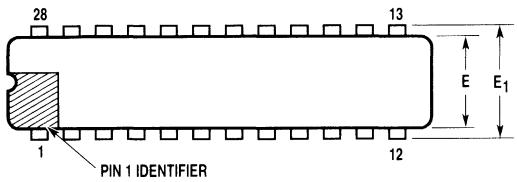
	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.075 (1.90)	.110 (2.79)	
A_1	.050 (1.27)	.070 (1.78)	
B_1	.033 (0.84)	.039 (0.99)	
D	.940 (23.88)	.960 (24.38)	Note 3
D_1			.075 (1.90) Ref.
D_2			.800 (20.32) Basic
D_3			.400 (10.16) Ref.
e			.050 (1.27) Basic
h			.050 (1.27) Ref.
j			.040 (1.02) Ref.
L	.040 (1.02)	.055 (1.40)	
N			68, Note 4
ND			17, Note 5

Ref. 90X00181

Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .007 inch (0.18mm) of its true longitudinal position.
3. Dimension D: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
4. Dimension N: number of terminals.
5. Dimension ND: number of terminals per package edge.
6. Controlling dimension: inch.

B2 Package
24 Pin CERDIP

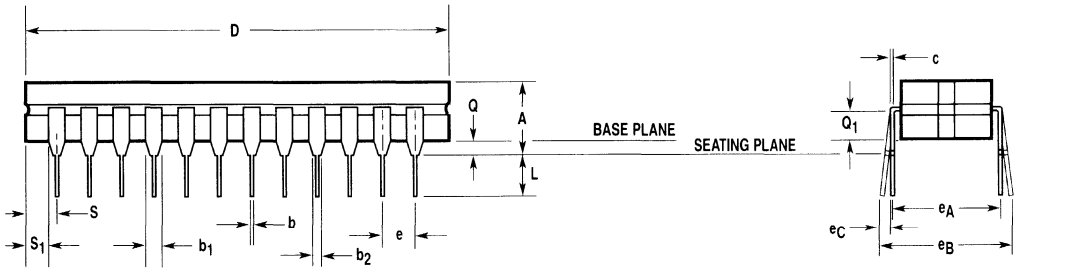
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.150 (3.81)	.200 (5.08)	
b	.014 (0.36)	.023 (0.58)	
b_1	.050 (1.27)	.070 (1.78)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.015 (0.38)	
D	1.235 (31.37)	1.280 (32.51)	
E	.280 (7.11)	.305 (7.75)	
E_1	.300 (7.62)	.320 (8.13)	
e			.100 (2.54) Basic
e_A			.300 (7.62) Basic
e_B		.400 (10.16)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			24, Note 8
Q	.015 (0.38)	.060 (1.52)	
Q_1	.070 (1.78)		
S		.098 (2.49)	
S_1	.005 (0.13)		

Ref. 90X00181



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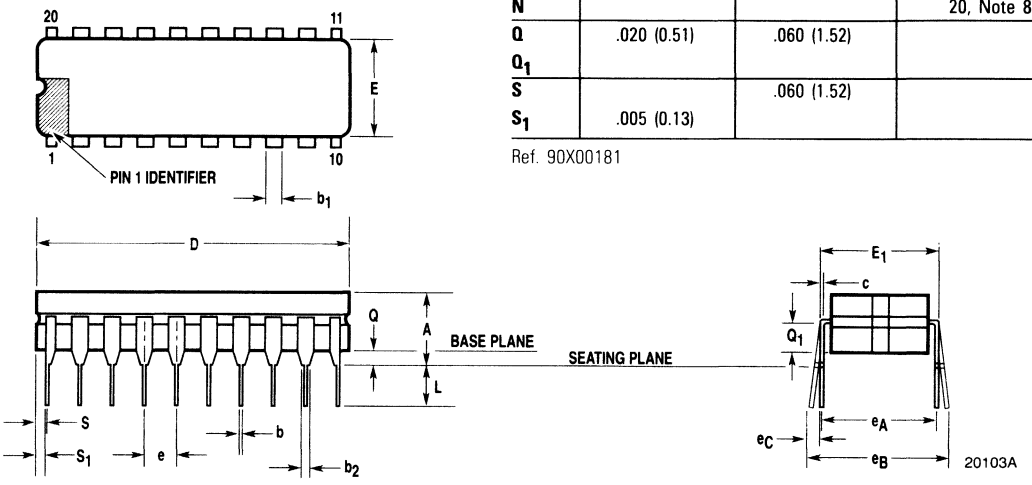
B3 Package
20 Pin CERDIP

Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.



Dimensions

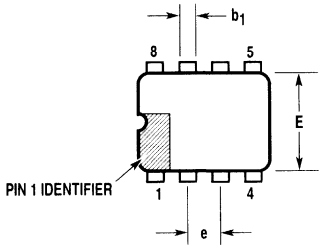
	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.150 (3.81)	.200 (5.08)	
b	.015 (0.38)	.021 (0.53)	
b_1	.050 (1.27)	.060 (1.52)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.012 (0.31)	
D		.985 (25.02)	
E	.220 (5.59)	.310 (7.87)	
E_1	.290 (7.37)	.320 (8.13)	
e	.090 (2.29)	.110 (2.79)	
e_A			.300 (7.62) Basic
e_B	.310 (7.78)	.410 (10.41)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			20, Note 8
Q	.020 (0.51)	.060 (1.52)	
Q_1			
S		.060 (1.52)	
S_1	.005 (0.13)		

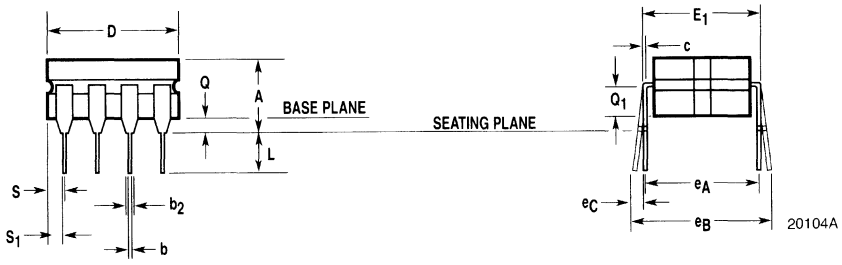
Ref. 90X00181

M

B4 Package
8 Pin CERDIP

Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.





Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.150 (3.81)	.200 (5.08)	
b	.015 (0.38)	.021 (0.53)	
b_1	.030 (0.76)	.070 (1.78)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.012 (0.31)	
D		.400 (10.16)	
E	.220 (5.56)	.291 (7.39)	
E_1	.290 (7.37)	.320 (8.13)	
e	.090 (2.29)	.110 (2.79)	
e_A			.300 (7.62) Basic
e_B		.310 (7.78)	.410 (10.41)
e_C			
L	.125 (3.17)	.200 (5.08)	
N			8, Note 8
Q	.020 (0.51)	.060 (1.52)	
Q_1			
S		.055 (1.40)	
S_1	.015 (0.38)		

Ref. 90X00181

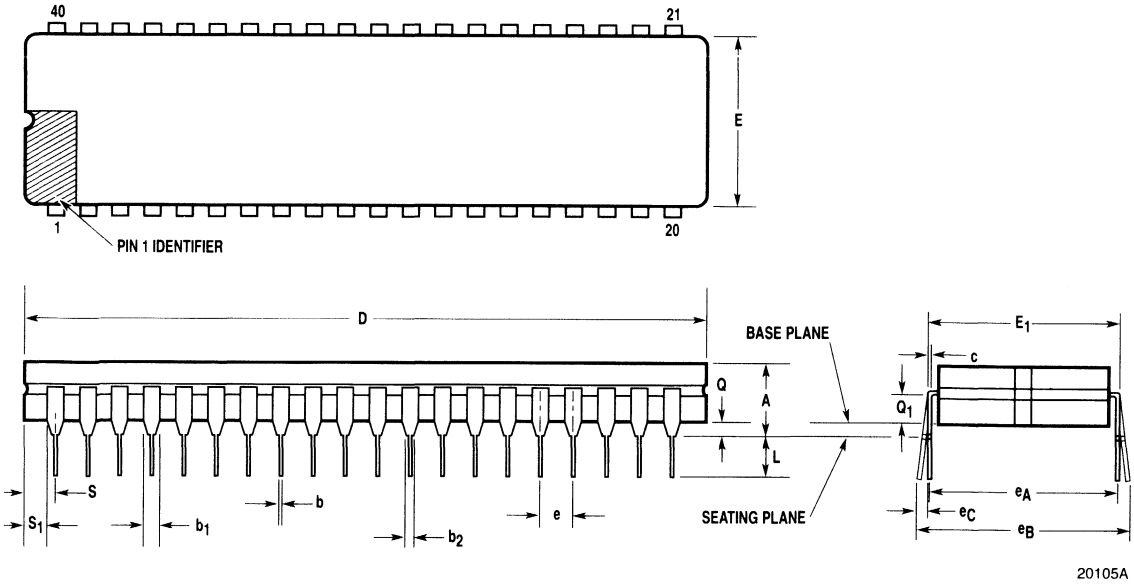
B5 Package
40 Pin CERDIP

Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.150 (3.81)	.225 (5.72)	
b	.014 (0.36)	.023 (0.58)	
b_1	.050 (1.27)	.065 (1.65)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.015 (0.38)	
D	2.030 (51.56)	2.096 (53.24)	
E	.510 (12.95)	.600 (15.24)	
E_1	.590 (14.99)	.620 (15.75)	
e			.100 (2.54) Basic
e_A			.600 (15.24) Basic
e_B		.700 (17.78)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			40, Note 8
Q	.015 (0.38)	.060 (1.52)	
Q_1	.070 (1.78)		
S		.098 (2.49)	
S_1	.005 (0.13)		

Ref. 90X00181

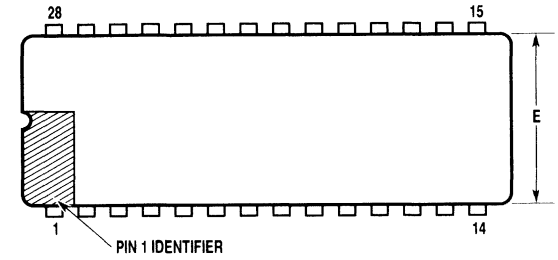


20105A

M

B6 Package
28 Pin CERDIP

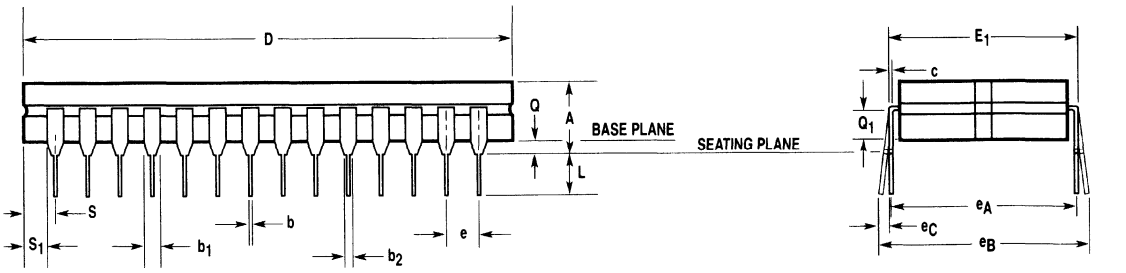
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.150 (3.81)	.200 (5.08)	
b	.014 (0.36)	.023 (0.58)	
b_1	.050 (1.27)	.070 (1.78)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.015 (0.38)	
D	1.435 (36.45)	1.480 (37.59)	
E	.500 (12.70)	.600 (15.24)	
E_1	.590 (14.99)	.620 (15.75)	
e			.100 (2.54) Basic
e_A			.600 (15.24) Basic
e_B		.700 (17.78)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			28, Note 8
Q	.015 (0.38)	.060 (1.52)	
Q_1	.070 (1.78)		
S		.098 (2.49)	
S_1	.005 (0.13)		

Ref. 90X00181



20106A

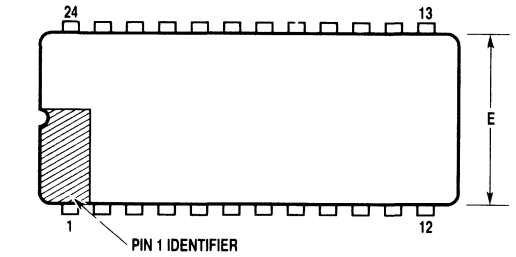
B7 Package
24 Pin CERDIP

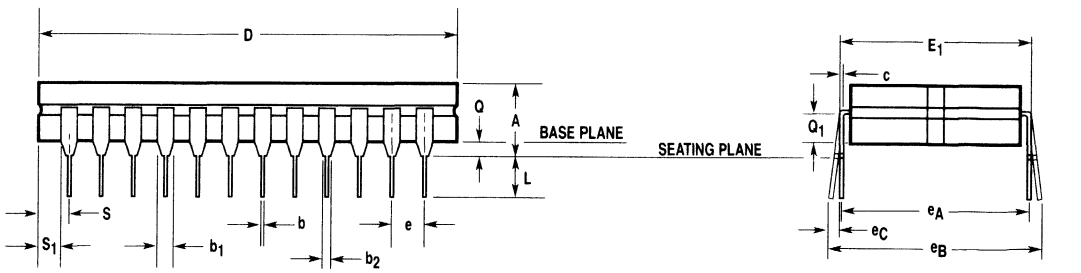
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.

Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.150 (3.81)	.200 (5.08)	
b	.014 (0.36)	.023 (0.58)	
b_1	.050 (1.27)	.070 (1.78)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.015 (0.38)	
D	1.235 (31.40)	1.280 (32.51)	
E	.510 (12.95)	.610 (15.49)	
E_1	.590 (14.99)	.620 (15.75)	
e			.100 (2.54) Basic
e_A			.600 (15.24) Basic
e_B		.700 (17.78)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			24, Note 8
Q	.015 (0.38)	.060 (1.52)	
Q_1	.070 (1.78)		
S		.098 (2.49)	
S_1	.005 (0.13)		

Ref. 90X00181

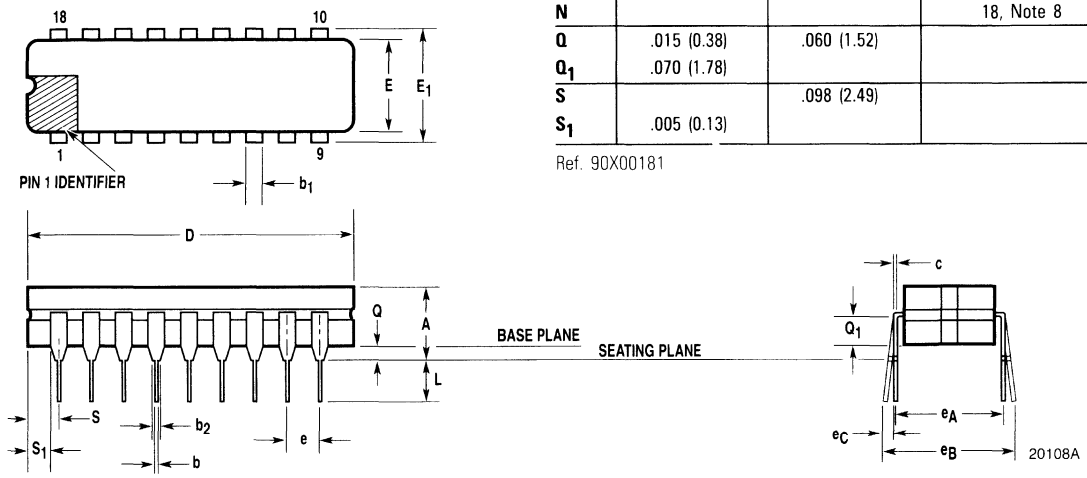




20107A

B8 Package
18 Pin CERDIP

Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.



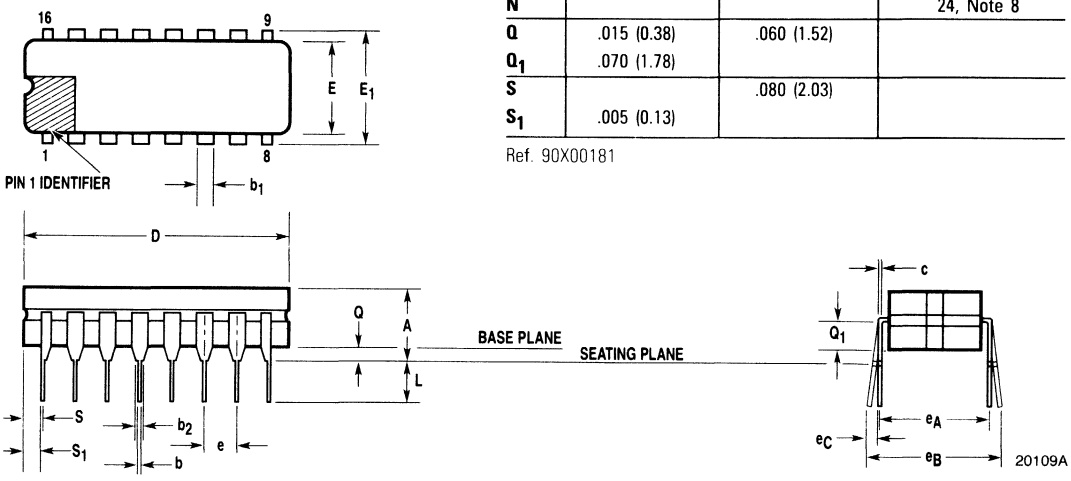
Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.150 (3.81)	.200 (5.08)	
b	.014 (0.36)	.023 (0.58)	
b_1	.050 (1.27)	.065 (1.65)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.015 (0.38)	
D	.875 (22.22)	.920 (23.37)	
E	.280 (7.11)	.305 (7.75)	
E_1	.290 (7.37)	.320 (8.13)	
e			.100 (2.54) Basic
e_A			.300 (7.62) Basic
e_B		.400 (10.16)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			18, Note 8
Q	.015 (0.38)	.060 (1.52)	
Q_1	.070 (1.78)		
S		.098 (2.49)	
S_1	.005 (0.13)		

Ref. 90X00181

B9 Package
16 Pin CERDIP

Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = lead count).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimensions b, b_1 and c: increase maximum limits by .003 inch (0.08mm) when solder finish applied.
8. Dimension N: number of leads.
9. Standard lead finish is tin plate for all grades.
10. Controlling dimension: inch.



Dimensions

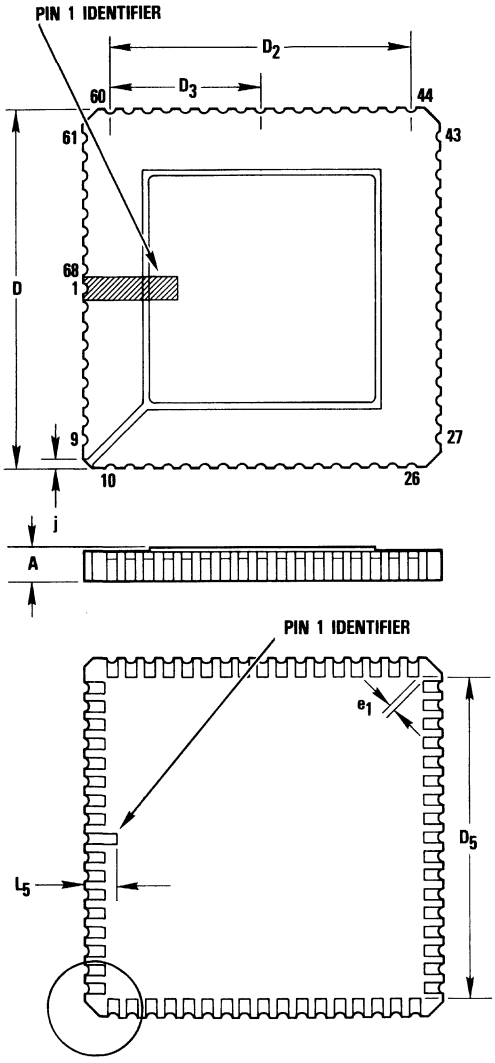
	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.150 (3.81)	.200 (5.08)	
b	.014 (0.36)	.023 (0.58)	
b_1	.050 (1.27)	.065 (1.65)	
b_2			.040 (1.02) Nominal
c	.008 (0.20)	.015 (0.38)	
D	.750 (19.05)	.820 (20.83)	
E	.240 (7.11)	.305 (7.75)	
E_1	.290 (7.37)	.320 (5.13)	
e			.100 (2.54) Basic
e_A			.300 (7.62) Basic
e_B		.400 (10.16)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			24, Note 8
Q	.015 (0.38)	.060 (1.52)	
Q_1	.070 (1.78)		
S		.080 (2.03)	
S_1	.005 (0.13)		

Ref. 90X00181

M

C1 Package

68 Contact Hermetic Ceramic Chip Carrier

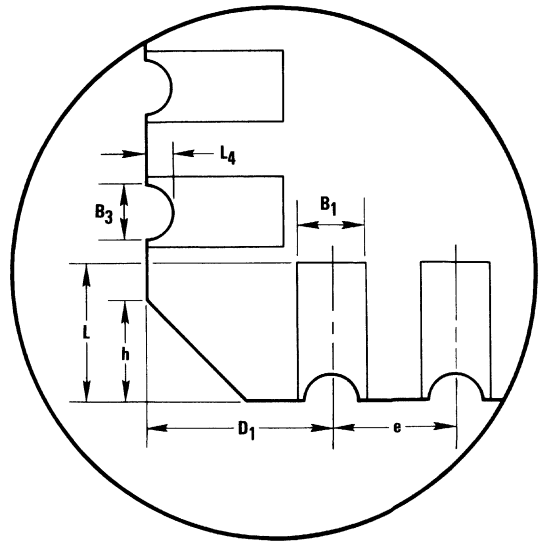


Dimensions

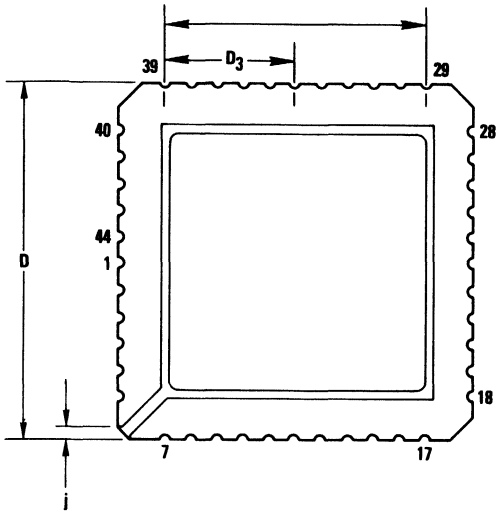
	Inches (Millimeters)		
Sym	Min	Max	Notes
A	.082 (2.08)	.110 (2.79)	
B_1	.022 (0.56)	.028 (0.71)	
B_3	.006 (0.15)	.022 (0.56)	
D	.938 (23.82)	.962 (24.43)	
D_1			.075 (1.90) Ref.
D_2			.800 (20.32) Basic
D_3			.400 (10.16) Basic
D_5			.850 (21.59) Ref.
e			.050 (1.27) Basic
e_1	.015 (0.38)		
h			.040 (1.02) Ref.
j			.020 (0.51) Ref.
L	.045 (1.14)	.055 (1.40)	
L_4	.003 (0.08)	.015 (0.38)	
L_5	.075 (1.91)	.095 (2.41)	
N			68, Note 4
ND			17, Note 5

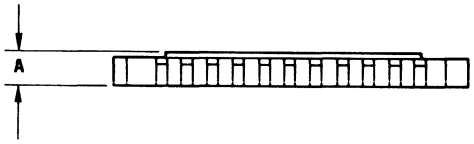
Ref. 90X00181

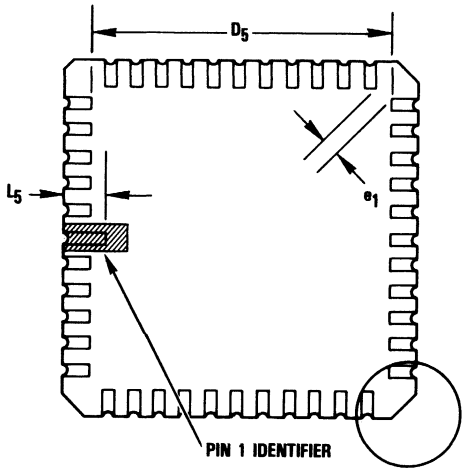
Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .007 inch (0.18mm) of its true longitudinal position.
3. Dimension D: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
4. Dimension N: number of terminals.
5. Dimension ND: number of terminals per package edge.
6. Controlling dimension: inch.



C2 Package
44 Contact Hermetic Ceramic Chip Carrier





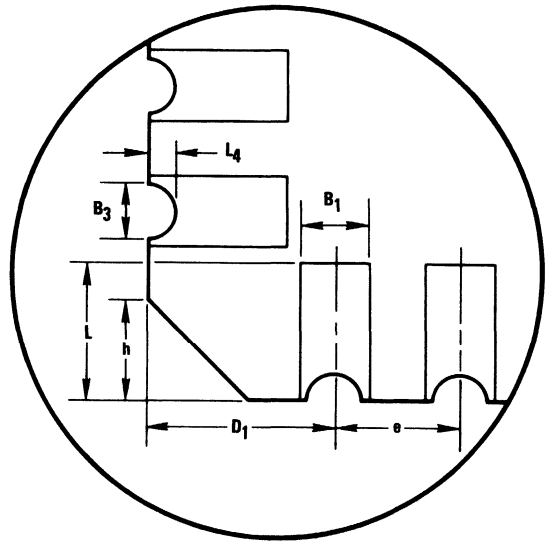


Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.064 (1.62)	.110 (2.79)	
B_1	.022 (0.56)	.028 (0.71)	
B_3	.006 (0.15)	.022 (0.56)	
D	.640 (16.26)	.660 (16.76)	
D_1			.075 (1.90) Ref.
D_2			.500 (6.35) Basic
D_3			.250 (6.35) Basic
D_5			.550 (13.97) Ref.
e			.050 (1.27) Basic
e_1	.015 (0.38)		
h			.040 (1.02) Ref.
j			.020 (0.51) Ref.
L	.045 (1.14)	.055 (1.40)	
L_4	.003 (0.08)	.015 (0.38)	
L_5	.075 (1.91)	.095 (2.41)	
N			44, Note 4
ND			11, Note 5

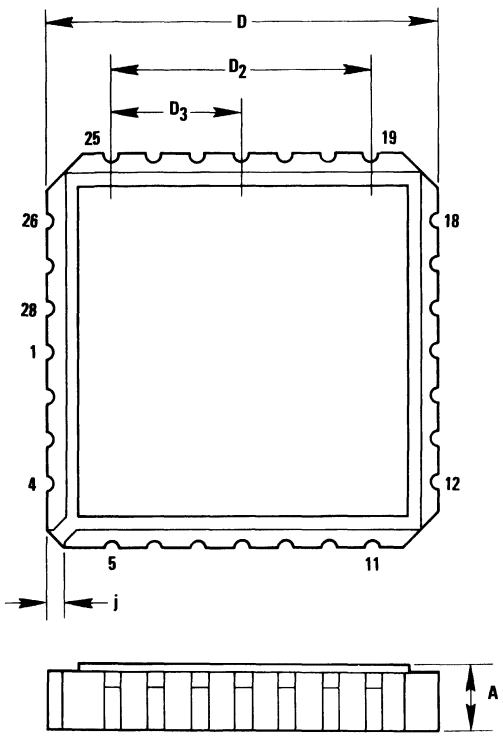
Ref. 90X00181

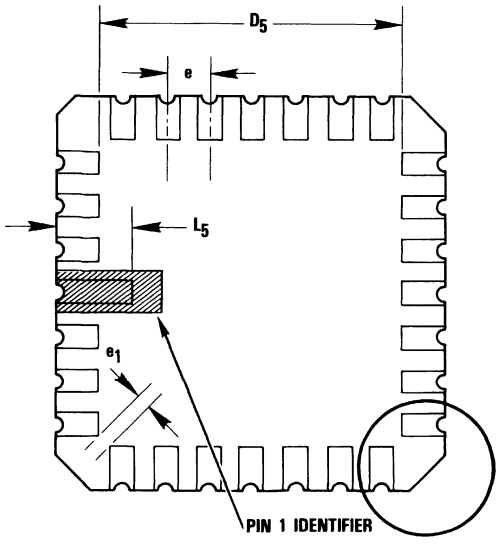
Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .007 inch (0.18mm) of its true longitudinal position.
3. Dimension D: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
4. Dimension N: number of terminals.
5. Dimension ND: number of terminals per package edge.
6. Controlling dimension: inch.



M

C3 Package
28 Contact Hermetic Ceramic Chip Carrier



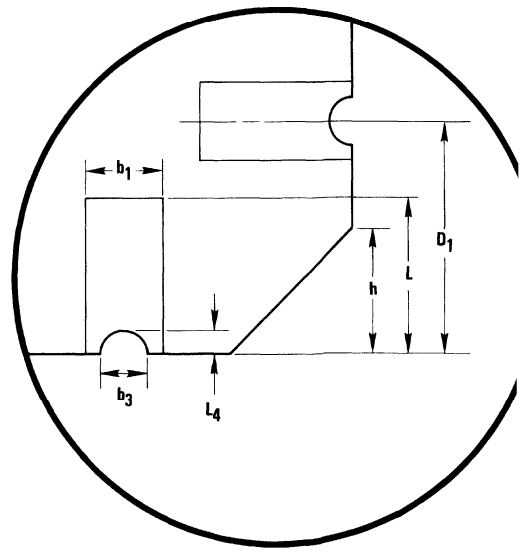


Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.064 (1.62)	.100 (2.54)	
B_1	.022 (0.56)	.028 (0.71)	
B_3	.006 (0.15)	.022 (0.56)	
D	.442 (11.23)	.460 (11.68)	
D_1			.075 (1.90) Ref.
D_2			.300 (7.62) Basic
D_3			.150 (3.81) Basic
D_5			.350 (8.89) Ref.
e			.050 (1.27) Basic
e_1	.015 (0.38)		
h			.040 (1.02) Ref.
j			.020 (0.51) Ref.
L	.045 (1.14)	.055 (1.40)	
L_4	.003 (0.08)	.015 (0.38)	
L_5	.075 (1.91)	.095 (2.41)	
N			28, Note 4
ND			7, Note 5

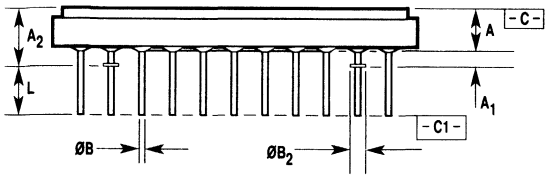
Ref. 90X00181

Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .007 inch (0.18mm) of its true longitudinal position.
3. Dimension D: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
4. Dimension N: number of terminals.
5. Dimension ND: number of terminals per package edge.
6. Controlling dimension: inch.



G0 Package
68 Pin Grid Array, Cavity Down
with Flat Heat Sink

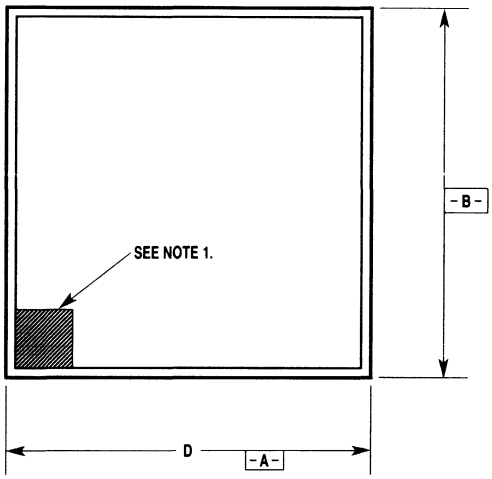
Notes:
1. Pin one identifier shall be within shaded area shown.
2. Dimension M: defines matrix size.
3. Dimension N: defines pin count.
4. Controlling dimension: inch.
5. Optional (TRW option) index pin.

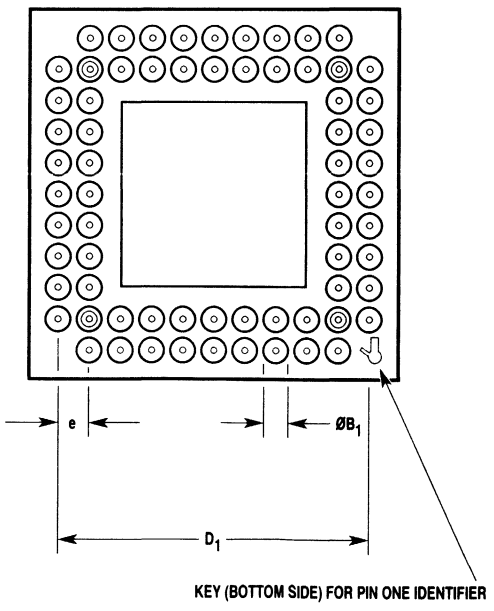


Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.120 (3.05)	.185 (4.70)	
A_1	.025 (0.63)	.060 (1.52)	
A_2	.150 (3.81)	.240 (6.10)	
ϕB	.017 (0.43)	.020 (0.51)	
ϕB_1		.080 (2.03)	
ϕB_2			.050 (1.27) Nominal
D	1.140 (28.96)	1.180 (29.97)	
D_1			1.000 (25.40) Basic
e			.100 (2.54) Basic
L	.120 (3.05)	.140 (3.56)	
M			11, Note 2
N			68, Note 3

Ref. 90X00181



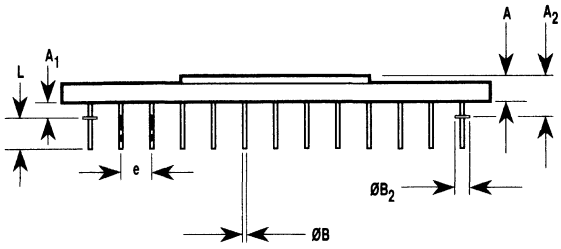


20125A

M

G5 Package
89 Pin Grid Array

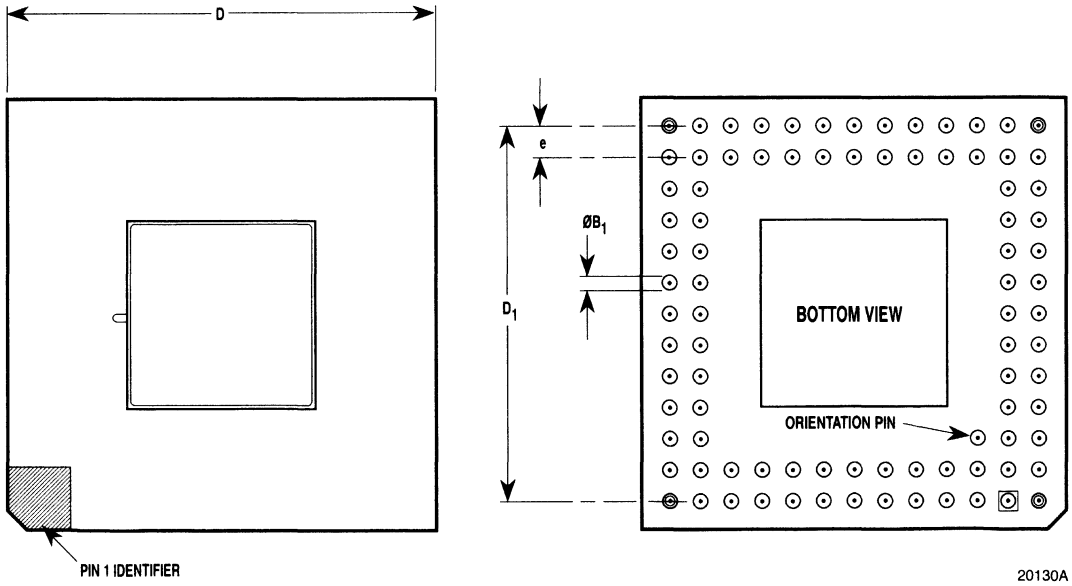
Notes:
1. Pin one identifier shall be within shaded area shown.
2. Dimension M: defines matrix size.
3. Dimension N: defines pin count.
4. Controlling dimension: inch.
5. Optional (TRW option) index pin.



Dimensions

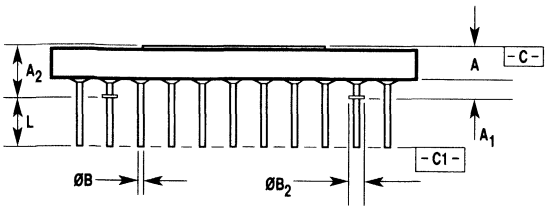
	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.080 (2.03)	.125 (3.18)	
A_1	.040 (1.02)	.060 (1.52)	
A_2	.115 (2.92)	.190 (4.83)	
ϕB	.017 (0.43)	.020 (0.51)	
ϕB_1		.080 (2.03)	
ϕB_2			.050 (1.27) Nominal
D	1.340 (34.04)	1.380 (35.05)	
D_1			1.200 (30.48) Basic
e			.100 (2.54) Basic
L	.120 (3.05)	.150 (3.81)	
M			13, Note 2
N			88, Note 3

Ref. 90X00181



G8 Package
68 Pin Grid Array

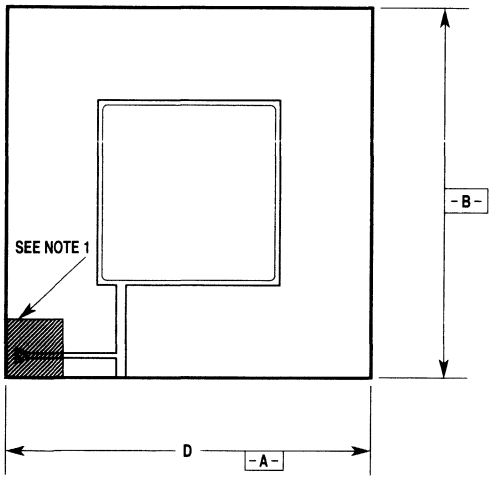
Notes:
1. Pin one identifier shall be within shaded area shown.
2. Dimension M: defines matrix size.
3. Dimension N: defines pin count.
4. Controlling dimension: inch.
5. Optional (TRW option) index pin.

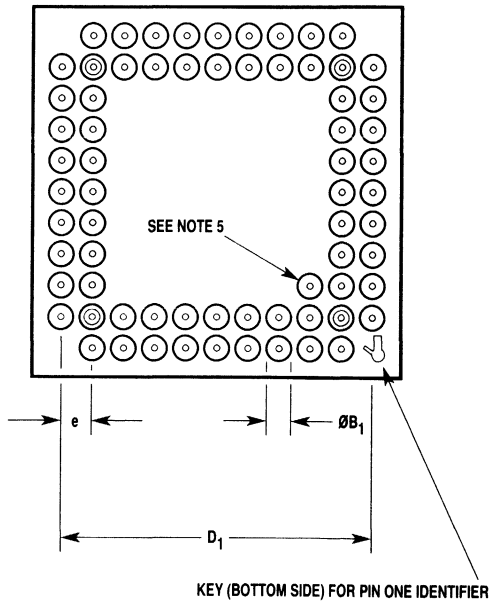


Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.080 (2.03)	.125 (3.18)	
A_1	.040 (1.02)	.060 (1.52)	
A_2	.115 (2.92)	.190 (4.83)	
ϕB	.017 (0.43)	.020 (0.51)	
ϕB_1		.080 (2.03)	
ϕB_2			.050 (1.27) Nominal
D	1.140 (28.96)	1.180 (29.97)	
D_1			1.00 (25.4) Basic
e			.100 (2.54) Basic
L	.120 (3.05)	.150 (3.81)	
M			11, Note 2
N			68, Note 3

Ref. 90X00181



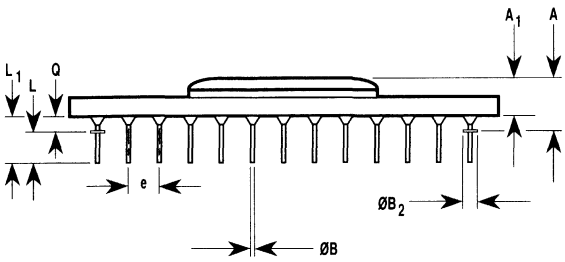


20133A

M

H5 Package
121 Printed Circuit Board
Pin Grid Array, Cavity Up

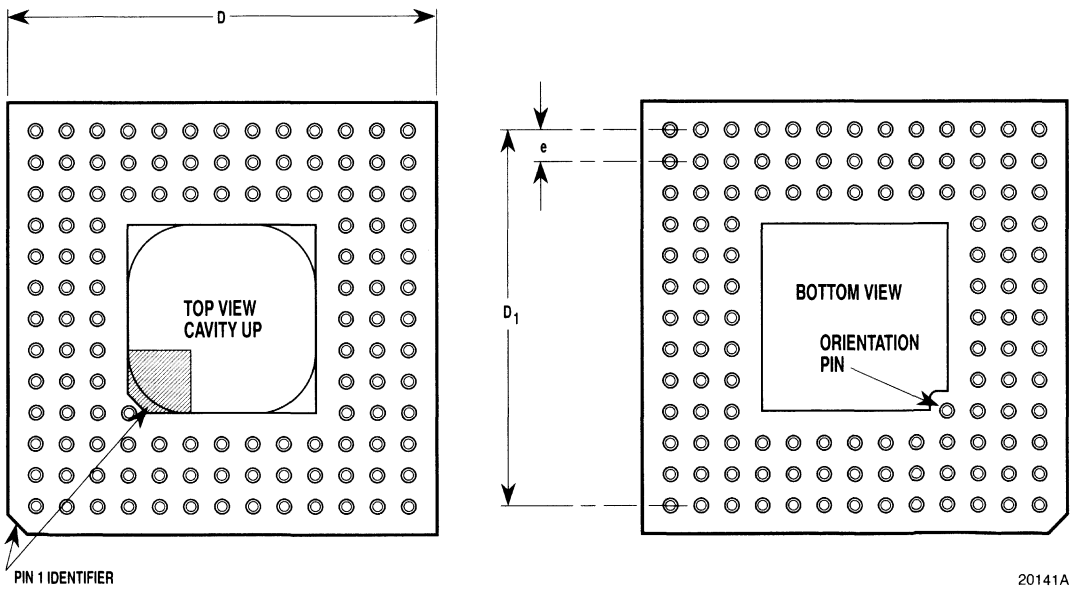
Notes:
1. Pin one identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension M: defines matrix size.
4. Dimension N: defines the maximum possible number of pins. Orientation pin is at supplier's option.
5. Controlling dimension: inch.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.125 (3.17)	.215 (5.46)	
A_1	.080 (2.03)	.160 (4.06)	
ϕB	.016 (0.41)	.020 (0.51)	Note 2
ϕB_2			.050 (1.27) Nominal, Note 2
D	1.340 (34.04)	1.380 (35.05)	Square
D_1			1.200 (30.48) Basic
e			.100 (2.54) Basic
L	.110 (2.79)	.145 (3.68)	
L_1	.170 (4.32)	.190 (4.83)	
M			13, Note 3
N			120, Note 4
Q	.040 (1.02)	.060 (1.52)	

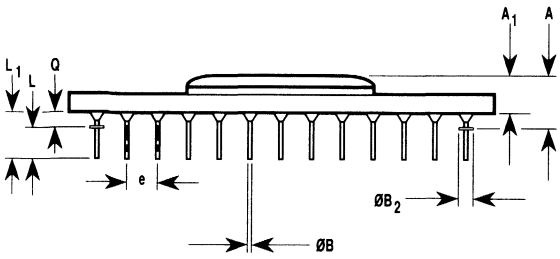
Ref. 90X00181



20141A

H7 Package
89 Printed Circuit Board
Pin Grid Array, Cavity Up

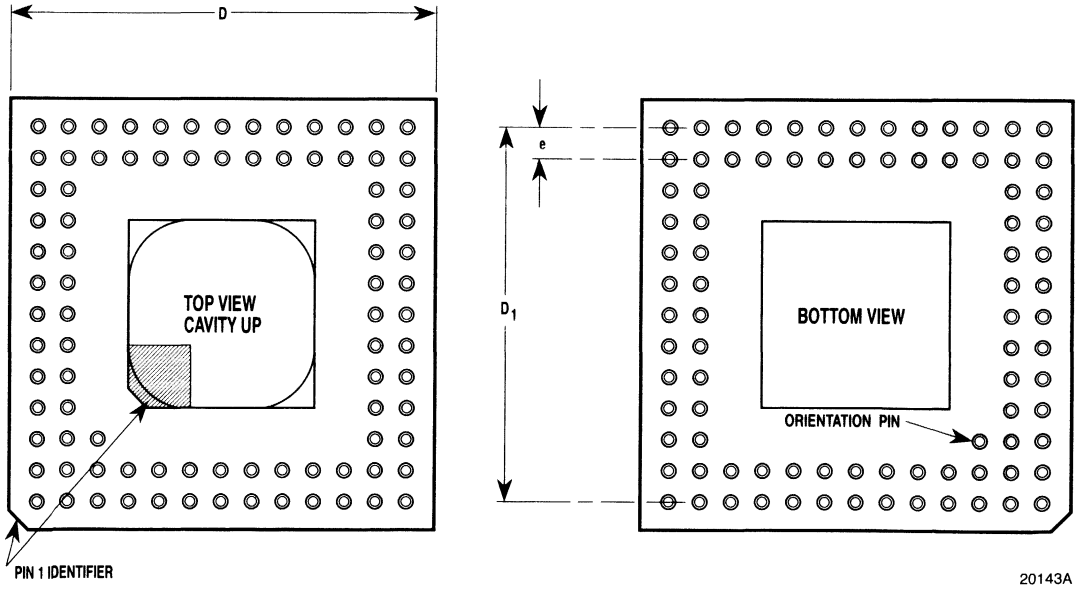
Notes:
1. Pin one identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension M: defines matrix size.
4. Dimension N: defines the maximum possible number of pins. Orientation pin is at supplier's option.
5. Controlling dimension: inch.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.125 (3.17)	.215 (5.46)	
A_1	.080 (2.03)	.160 (4.06)	
ϕB	.016 (0.41)	.020 (0.51)	Note 2
ϕB_2			.050 (1.27) Nominal, Note 2
D	1.340 (34.04)	1.380 (35.05)	Square
D_1			1.200 (30.48) Basic
e			.100 (2.54) Basic
L	.110 (2.79)	.145 (3.68)	
L_1	.170 (4.32)	.190 (4.83)	
M			13, Note 3
N			88, Note 4
Q	.040 (1.02)	.060 (1.52)	

Ref. 90X00181

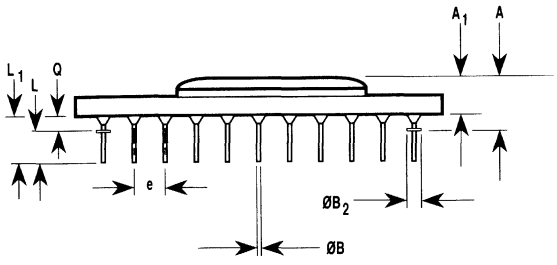


20143A

M

H8 Package
69 Printed Circuit Board
Pin Grid Array, Cavity Up

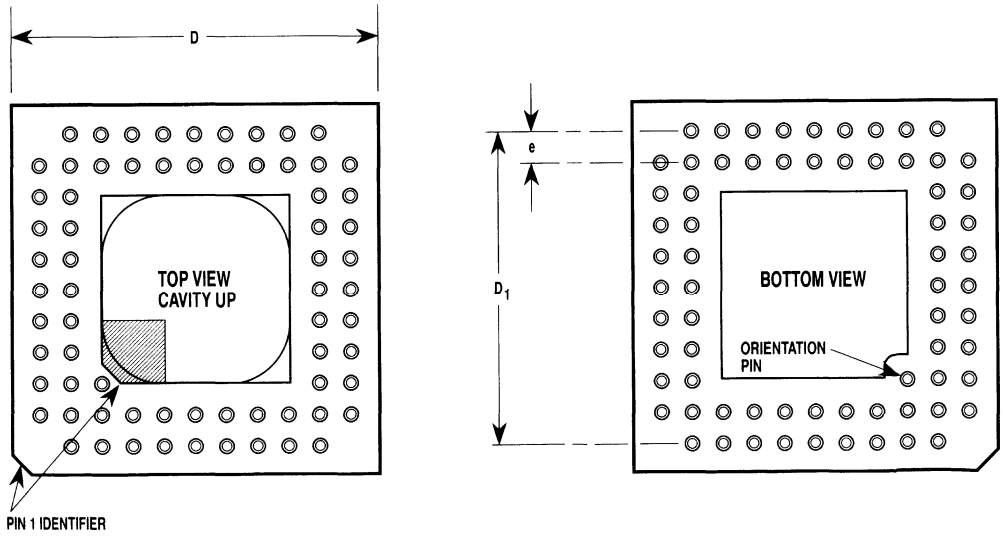
Notes:
1. Pin one identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension M: defines matrix size.
4. Dimension N: defines the maximum possible number of pins. Orientation pin is at supplier's option.
5. Controlling dimension: inch.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.125 (3.17)	.215 (5.46)	
A_1	.080 (2.03)	.160 (4.06)	
ϕB	.016 (0.41)	.020 (0.51)	Note 2
ϕB_2			.050 (1.27) Nominal, Note 2
D	1.140 (28.96)	1.180 (29.97)	Square
D_1			1.000 (25.40) Basic
e			.100 (2.54) Basic
L	.110 (2.79)	.145 (3.68)	
L_1	.170 (4.32)	.190 (4.83)	
M			11, Note 3
N			68, Note 4
Q	.040 (1.02)	.060 (1.52)	

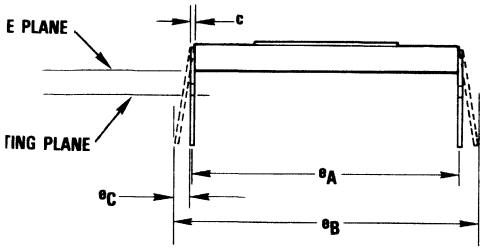
Ref. 90X00181



20144A

J0 Package
64 Pin Hermetic Ceramic DIP

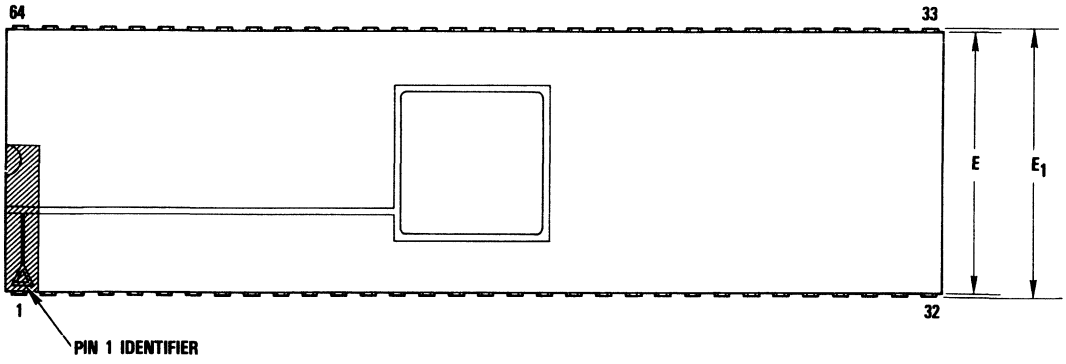
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1, E_3 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimensions E_3 and e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimension N: defines pin count.
8. Controlling dimension: inch.

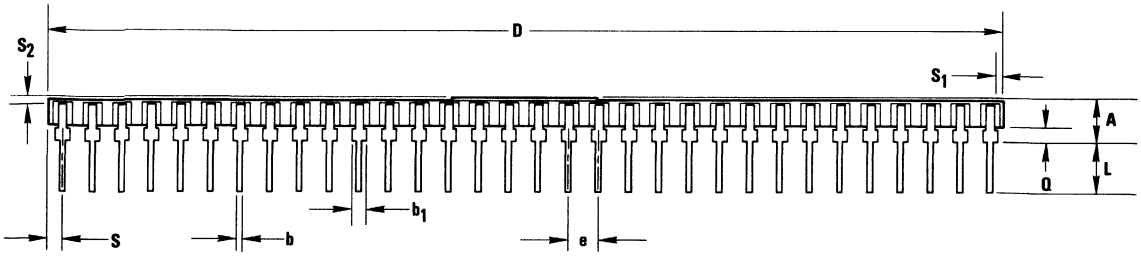


Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.120 (3.05)	.175 (4.44)	
b	.015 (0.38)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	3.170 (80.52)	3.240 (82.30)	
E	.880 (22.35)	.910 (23.11)	
E_1	.890 (22.61)	.930 (23.62)	
e			.100 (2.54) Basic
e_A			.900 (22.86) Basic
e_B		1.000 (25.40)	
e_C			
L	.125 (3.17)	.175 (4.44)	
N			64, Note 7
Q	.025 (0.63)	.065 (1.65)	
S		.100 (2.54)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

Ref. 90X00181

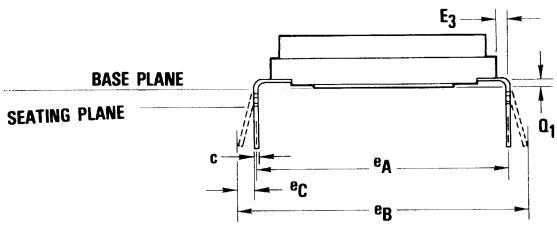




J1 Package

64 Pin Hermetic Ceramic DIP
Bottombraze with Heat Sink

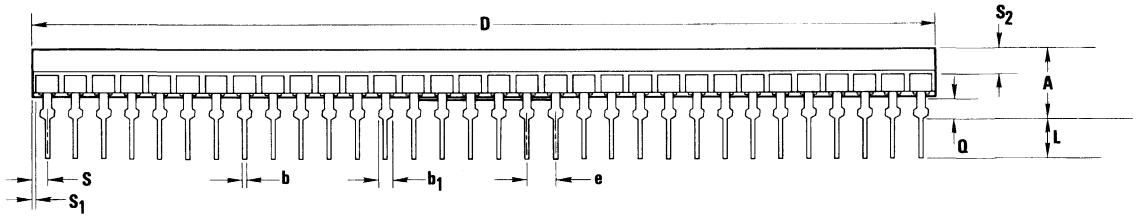
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1, E_3 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimensions E_3 and e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Controlling dimension: inch.
8. Dimension Q_1: measured from lead braze/ceramic interface.
9. Dimension N: defines pin count.

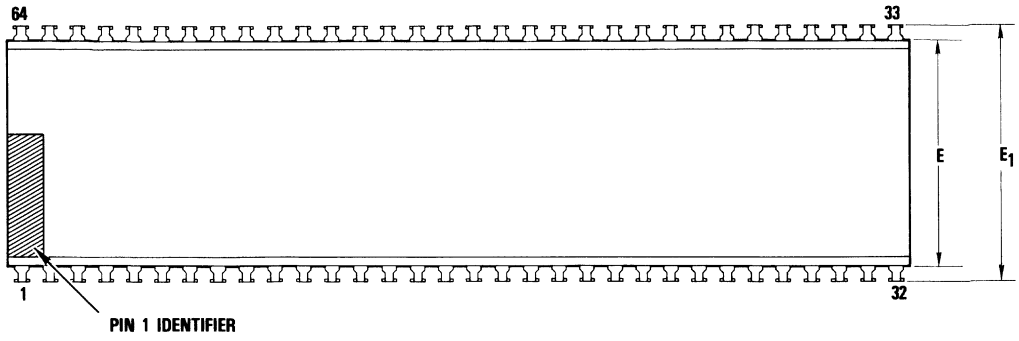


Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.190 (4.83)	.275 (6.99)	
b	.015 (0.38)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	3.170 (80.52)	3.240 (82.30)	
E	.790 (20.07)	.810 (20.57)	
E_1	.880 (22.35)	.930 (23.62)	
E_3	.025 (0.63)		
e			.100 (2.54) Basic
e_A			.900 (22.86) Basic
e_B		1.050 (26.67)	
e_C	.000 (0.00)		
L	.125 (3.17)	.175 (4.44)	
N			64, Note 9
Q	.050 (1.27)	.100 (2.54)	
Q_1	.026 (0.66)		
S		.100 (2.54)	
S_1	.005 (0.13)		
S_2	.060 (1.52)		

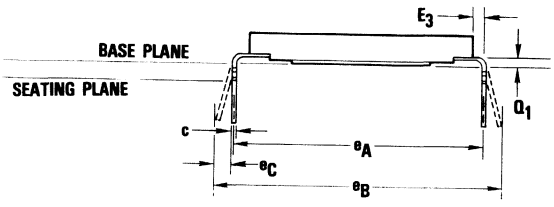
Ref. 90X00181





J3 Package
64 Pin Hermetic Ceramic DIP
Bottombraze

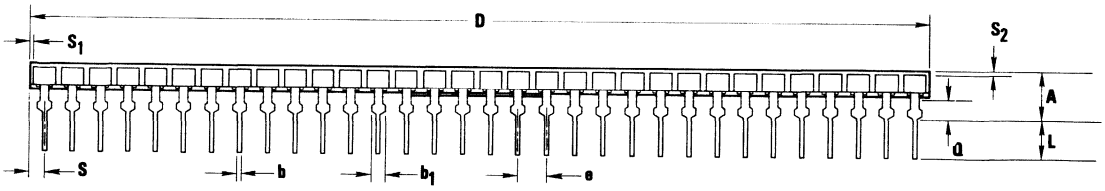
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1, E_3 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimensions E_3 and e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Controlling dimension: inch.
8. Dimension Q_1: measured from lead braze/ceramic interface.
9. Dimension N: defines pin count.

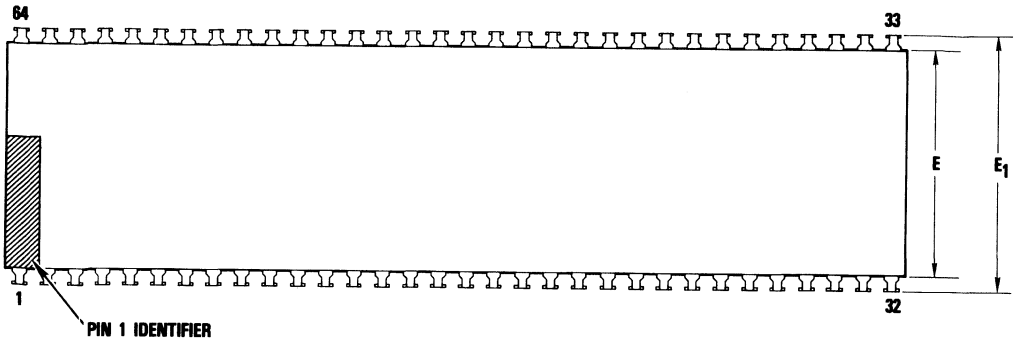


Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.125 (3.17)	.200 (5.08)	
b	.015 (0.38)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	3.170 (80.52)	3.240 (82.30)	
E	.790 (20.07)	.810 (20.57)	
E_1	.880 (22.35)	.930 (23.62)	
E_3	.025 (0.63)		
e			.100 (2.54) Basic
e_A			.900 (22.86) Basic
e_B		1.050 (26.67)	
e_C			
L	.125 (3.17)	.175 (4.44)	
N			64, Note 9
Q	.050 (1.27)	.100 (2.54)	
Q_1	.026 (0.66)		
S		.100 (2.54)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

Ref. 90X00181

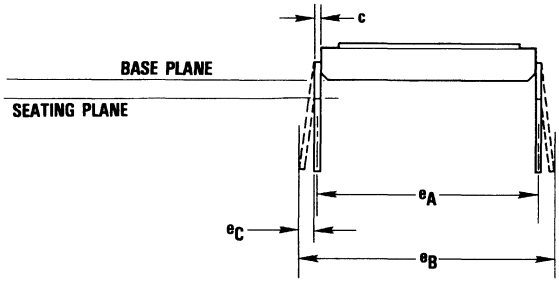




M

J4 Package
48 Pin Hermetic Ceramic DIP

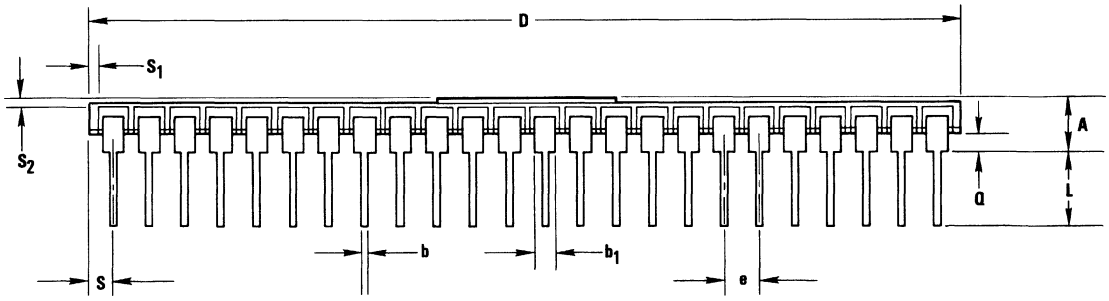
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimension N: defines pin count.
8. Controlling dimension: inch.

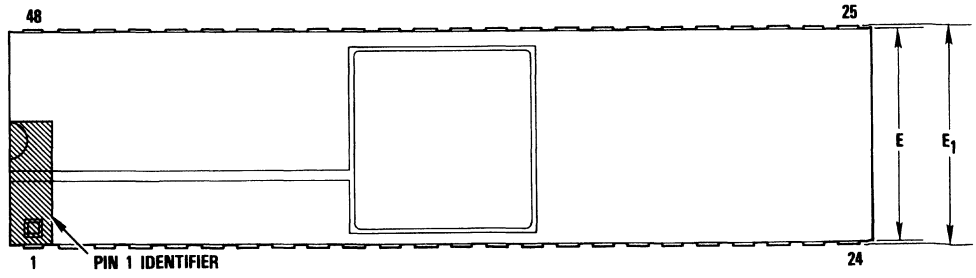


Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.120 (3.05)	.175 (4.44)	
b	.014 (0.35)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	2.370 (60.20)	2.435 (61.85)	
E	.575 (14.60)	.610 (15.49)	
E_1	.590 (14.99)	.620 (15.75)	
e			.100 (2.54) Basic
e_A			.600 (15.24) Basic
e_B		.700 (17.78)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			48, Note 7
Q	.025 (0.63)	.060 (1.52)	
S		.100 (2.54)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

Ref. 90X00181





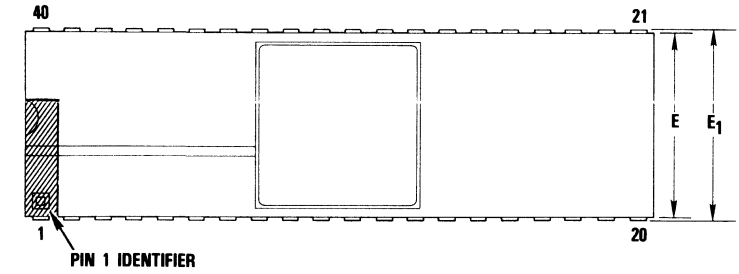
J5 Package
40 Pin Hermetic Ceramic DIP

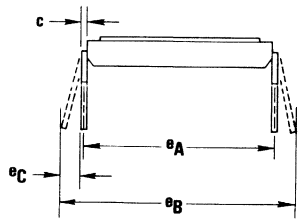
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimension N: defines pin count.
8. Controlling dimension: inch.

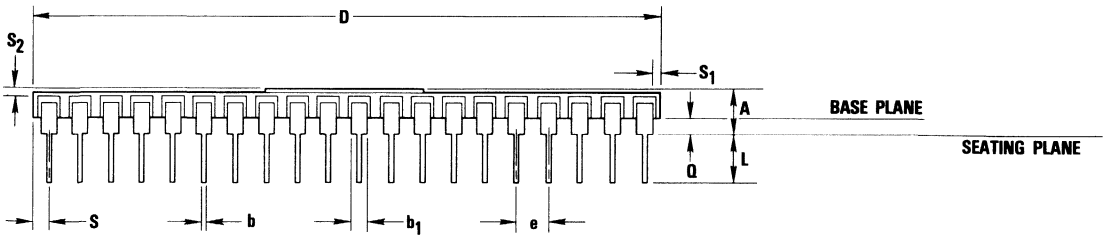
Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.120 (3.05)	.175 (4.44)	
b	.014 (0.35)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	1.970 (50.04)	2.030 (51.56)	
E	.575 (14.60)	.610 (15.49)	
E_1	.590 (14.99)	.620 (15.75)	
e			.100 (2.54) Basic
e_A			.600 (15.24) Basic
e_B		.700 (17.78)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			40, Note 7
Q	.025 (0.63)	.060 (1.52)	
S		.098 (2.49)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

Ref. 90X00181







M

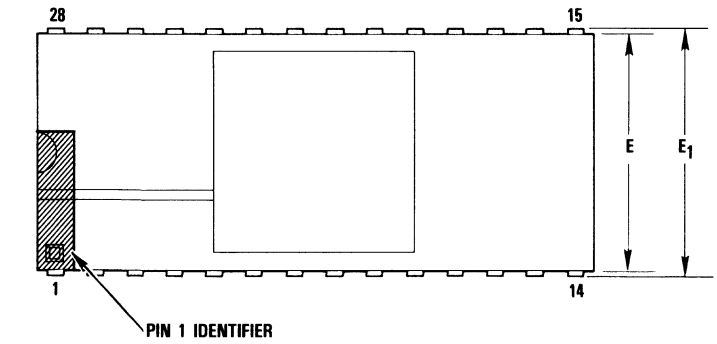
J6 Package
28 Pin Hermetic Ceramic DIP

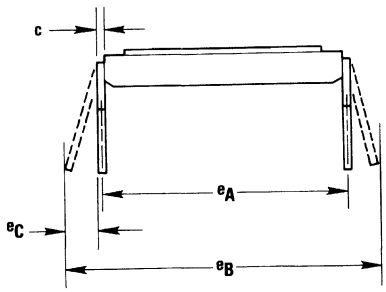
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimension N: defines pin count.
8. Controlling dimension: inch.

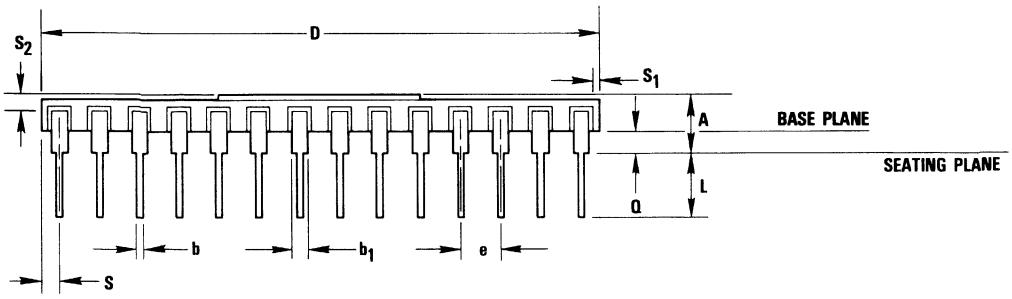
Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.120 (3.05)	.175 (4.44)	
b	.014 (0.35)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	1.380 (35.05)	1.420 (36.07)	
E	.575 (14.60)	.610 (15.49)	
E_1	.590 (14.99)	.620 (15.75)	
e			.100 (2.54) Basic
e_A			.600 (15.24) Basic
e_B		.700 (17.78)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			28, Note 7
Q	.025 (0.63)	.060 (1.52)	
S		.098 (2.49)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

Ref. 90X00181

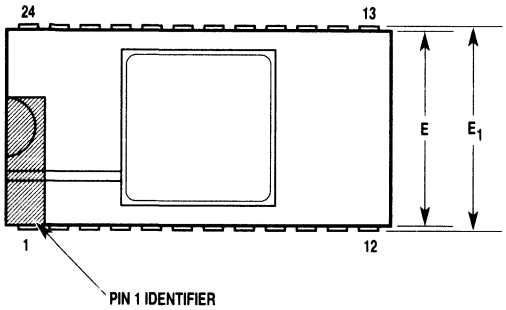






J7 Package
24 Pin Hermetic Ceramic DIP

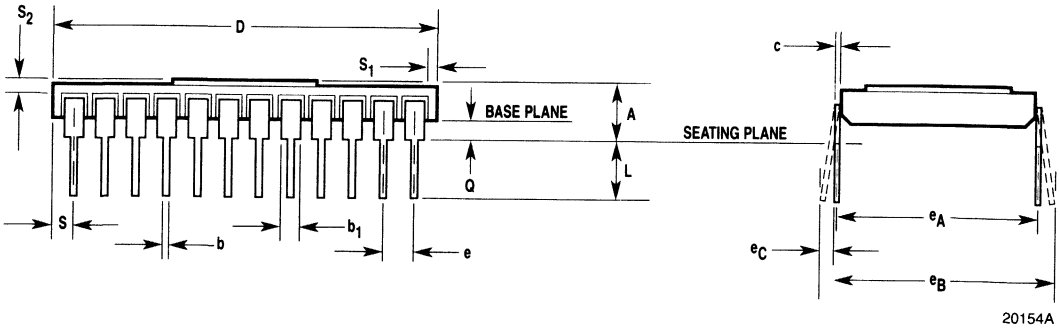
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimension N: defines pin count.
8. Controlling dimension: inch.



Dimensions

Sym	Min	Max	Notes
	Inches (Millimeters)		
A	.120 (3.05)	.175 (4.44)	
b	.014 (0.35)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	1.180 (29.97)	1.220 (30.99)	
E	.575 (14.60)	.610 (15.49)	
E_1	.590 (14.99)	.620 (15.75)	
e			.100 (2.54) Basic
e_A			.600 (15.24) Basic
e_B		.700 (17.78)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			24, Note 7
Q	.025 (0.63)	.060 (1.52)	
S		.098 (2.49)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

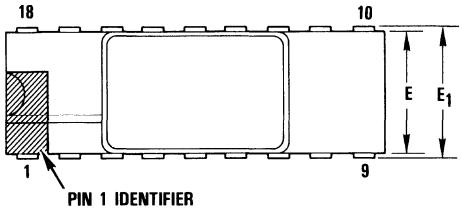
Ref. 90X00181

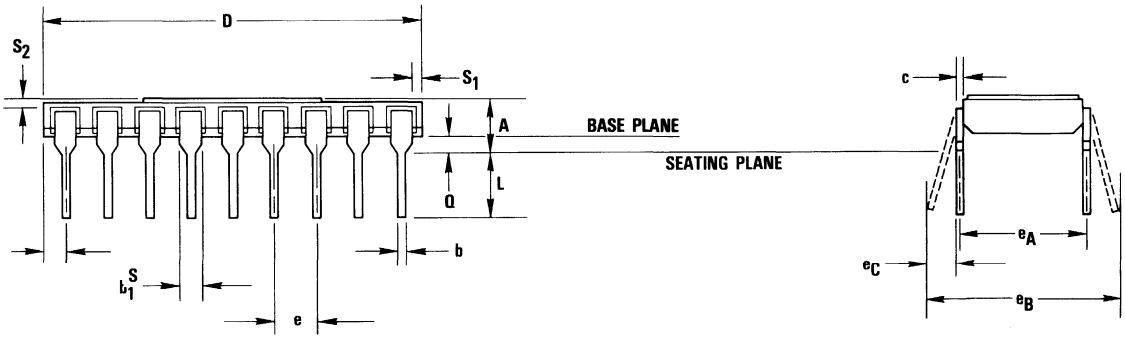


M

J8 Package
18 Pin Hermetic Ceramic DIP

Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimension N: defines pin count.
8. Controlling dimension: inch.





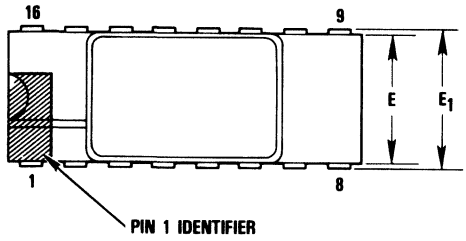
Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.100 (2.54)	.175 (4.44)	
b	.014 (0.35)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	.885 (22.48)	.915 (23.24)	
E	.285 (7.24)	.305 (7.75)	
E_1	.290 (7.37)	.320 (8.13)	
e			.100 (2.54) Basic
e_A			.300 (7.62) Basic
e_B		.400 (10.16)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			18, Note 7
Q	.015 (0.38)	.060 (1.52)	
S		.098 (2.49)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

Ref. 90X00181

J9 Package
16 Pin Hermetic Ceramic DIP

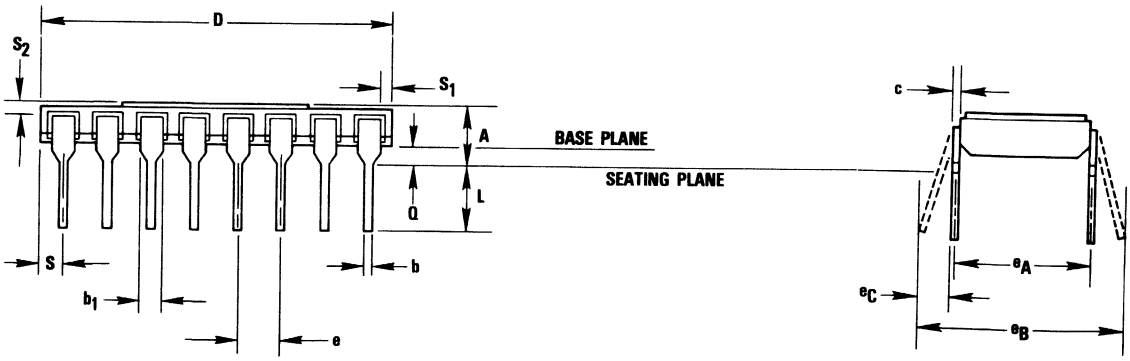
Notes:
1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position relative to pins 1 and N (N = leadcount).
3. Dimensions E_1 and e_A: measured with leads perpendicular to the base plane.
4. Dimensions E_1, e_B and e_C: measured to outside edge of lead.
5. Dimension e_A: measured to lead center.
6. Dimensions D and E: inclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
7. Dimension N: defines pin count.
8. Controlling dimension: inch.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.100 (2.54)	.175 (4.44)	
b	.014 (0.35)	.023 (0.58)	
b_1	.040 (1.02)	.065 (1.65)	
c	.008 (0.20)	.015 (0.38)	
D	.790 (20.07)	.810 (20.57)	
E	.285 (7.24)	.305 (7.75)	
E_1	.290 (7.37)	.320 (8.13)	
e			.100 (2.54) Basic
e_A			.300 (7.62) Basic
e_B		.400 (10.16)	
e_C			
L	.125 (3.17)	.200 (5.08)	
N			16, Note 7
Q	.015 (0.38)	.060 (1.52)	
S		.080 (2.03)	
S_1	.005 (0.13)		
S_2	.005 (0.13)		

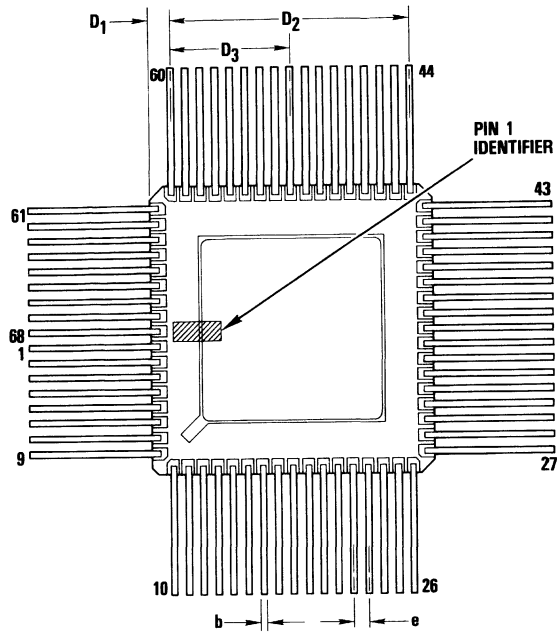
Ref. 90X00181

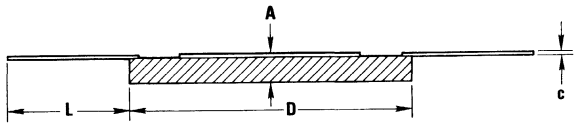


M

L1 Package

68 Leaded Hermetic Ceramic Chip Carrier



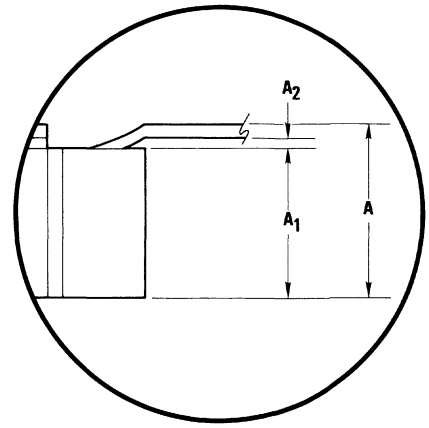


Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.080 (2.03)	.115 (2.92)	
A_1	.070 (1.78)	.100 (2.54)	
A_2	.005 (0.13)	.015 (0.38)	
b	.016 (0.41)	.022 (0.56)	
c	.009 (0.23)	.012 (0.30)	
D	.935 (23.75)	.970 (24.64)	
D_1			.075 (1.91) Ref.
D_2			.800 (20.32) Basic
D_3			.400 (10.16) Basic
e			.050 (1.27) Basic
L	.350 (8.98)	.400 (10.16)	
N			68, Note 4
ND			17, Note 5

Ref. 90X00181

Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension e: each pin centerline shall be located within .007 inch (0.18mm) of its true longitudinal position.
3. Dimension D_1: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
4. Dimension N: number of terminals.
5. Dimension ND: number of terminals per package edge.
6. Controlling dimension: inch.



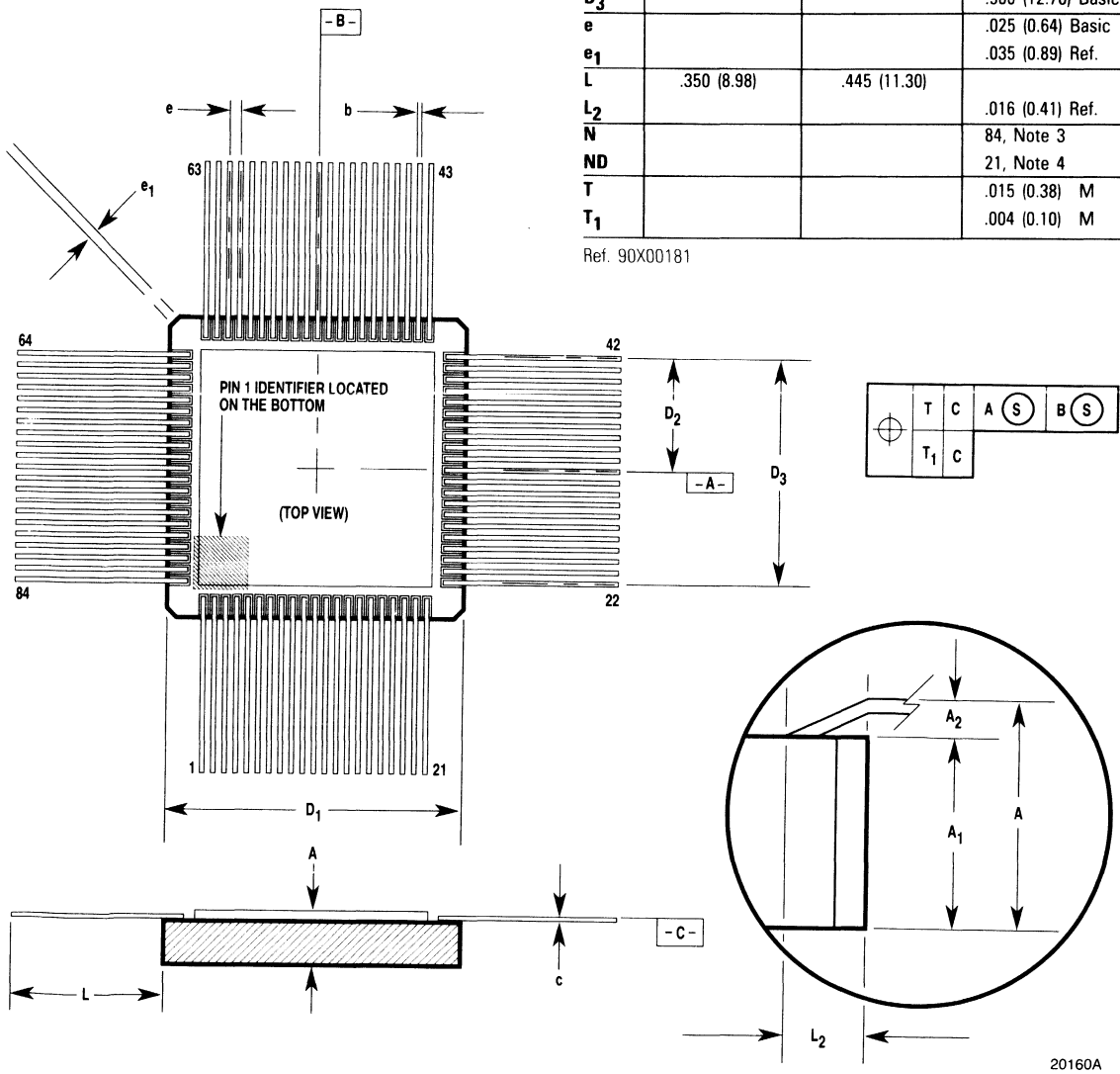
L3 Package
84 Leaded Hermetic Ceramic Chip Carrier

Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension D_1: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
3. Dimension N: number of terminals.
4. Dimension ND: number of terminals per package edge.
5. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.060 (1.52)	.100 (2.54)	
A_1	.055 (1.40)	.075 (1.91)	
A_2	.005 (0.13)	.025 (0.64)	
b	.008 (0.20)	.012 (0.30)	
c	.005 (0.13)	.009 (0.23)	
D_1	.640 (16.25)	.660 (16.76)	
D_2			.250 (6.35) Basic
D_3			.500 (12.70) Basic
e			.025 (0.64) Basic
e_1			.035 (0.89) Ref.
L	.350 (8.98)	.445 (11.30)	
L_2			.016 (0.41) Ref.
N			84, Note 3
ND			21, Note 4
T			.015 (0.38) M
T_1			.004 (0.10) M

Ref. 90X00181



20160A

M

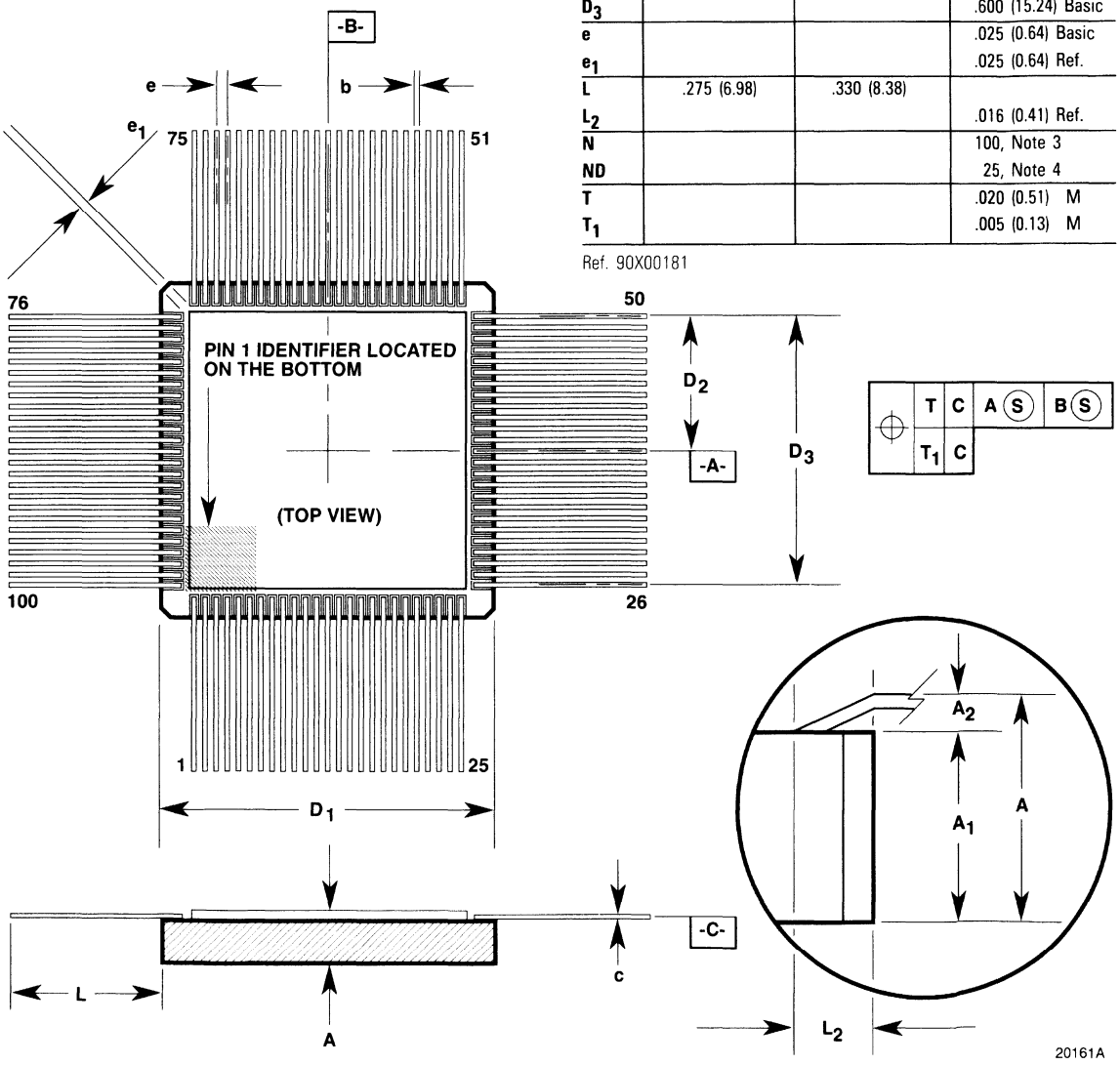
L4 Package
100 Leaded Hermetic Ceramic Chip Carrier

Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimension D_1: exclusive of package anomalies (lid misalignment, ceramic particles, etc.) Such anomalies shall not exceed .010 inch (0.25mm).
3. Dimension N: number of terminals.
4. Dimension ND: number of terminals per package edge.
5. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.080 (2.03)	.120 (3.05)	
A_1	.075 (1.91)	.095 (2.41)	
A_2	.005 (0.13)	.025 (0.64)	
b	.008 (0.20)	.012 (0.30)	
c	.005 (0.13)	.009 (0.23)	
D_1	.740 (18.80)	.760 (19.30)	
D_2			.300 (7.62) Basic
D_3			.600 (15.24) Basic
e			.025 (0.64) Basic
e_1			.025 (0.64) Ref.
L	.275 (6.98)	.330 (8.38)	
L_2			.016 (0.41) Ref.
N			100, Note 3
ND			25, Note 4
T			.020 (0.51) M
T_1			.005 (0.13) M

Ref. 90X00181



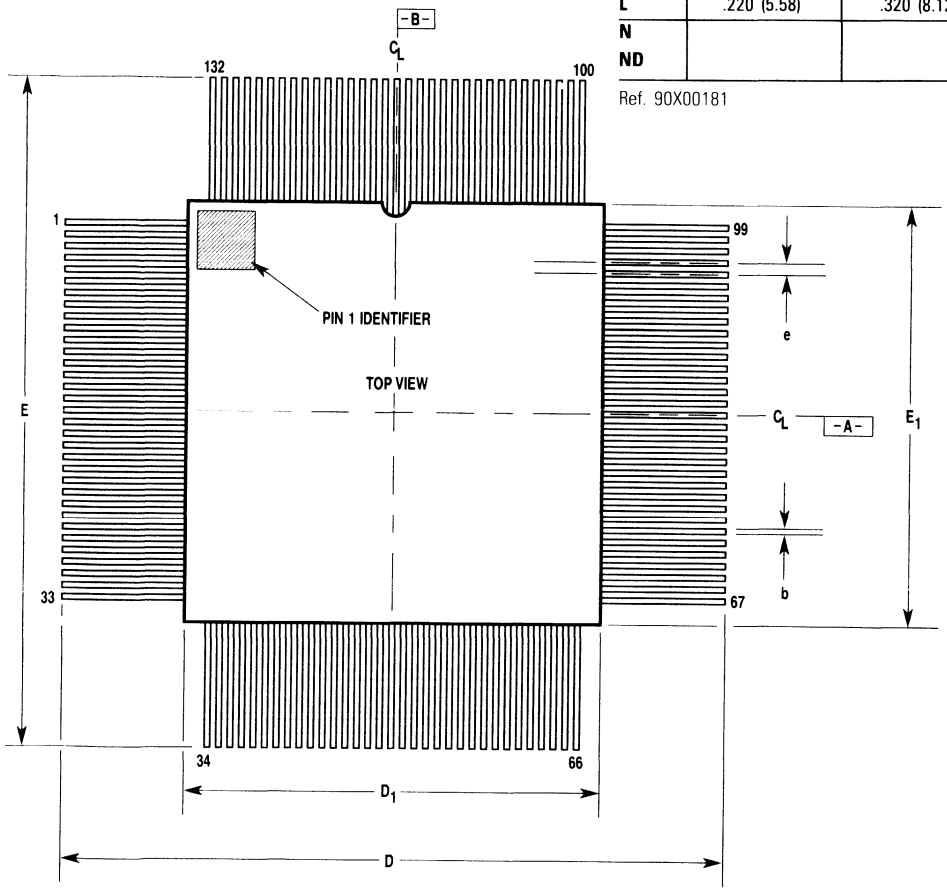
L5 Package
132 Leaded CERQUAD

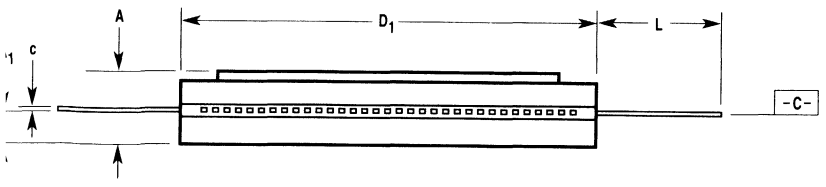
Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimensions D_1 and E_1: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
3. Dimension N: number of terminals.
4. Dimension ND: number of terminals per package edge.
5. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.114 (2.89)	.154 (3.91)	
A_1	.055 (1.40)	.075 (1.90)	
b	.008 (0.20)	.012 (0.30)	
c	.005 (0.13)	.009 (0.23)	
D, E			1.415 (35.94) Ref.
D_1, E_1	.860 (21.83)	.900 (22.84)	
e			.025 (0.64) Basic
L	.220 (5.58)	.320 (8.12)	
N			132, Note 3
ND			33, Note 4

Ref. 90X00181





20162A

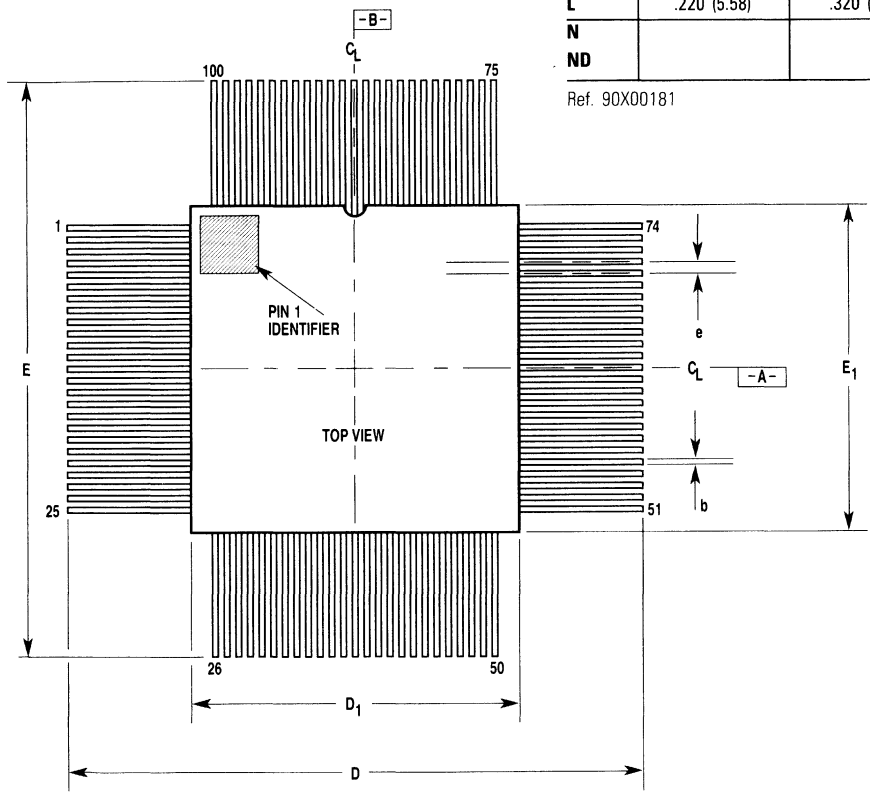
L6 Package
100 Leaded CERQUAD

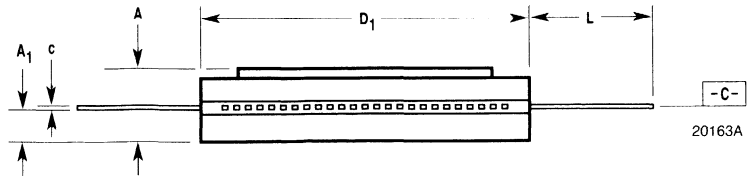
Notes:
1. A pin one identifier shall be located adjacent to pin one and within the shaded area shown.
2. Dimensions D_1 and E_1: exclusive of package anomalies (lid misalignment, ceramic particles, etc.). Such anomalies shall not exceed .010 inch (0.25mm).
3. Dimension N: number of terminals.
4. Dimension ND: number of terminals per package edge.
5. Controlling dimension: inch.

Dimensions

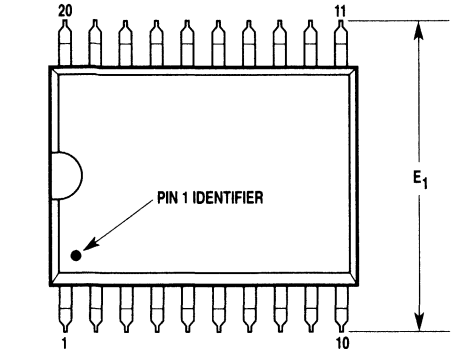
	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.114 (2.89)	.154 (3.91)	
A_1	.055 (1.40)	.075 (1.90)	
b	.008 (0.20)	.012 (0.30)	
c	.005 (0.13)	.009 (0.23)	
D, E			1.300 (32.95) Ref.
D_1, E_1	.670 (17.02)	.760 (19.30)	
e			.025 (0.64) Basic
L	.220 (5.58)	.320 (8.12)	
N			100, Note 3
ND			25, Note 4

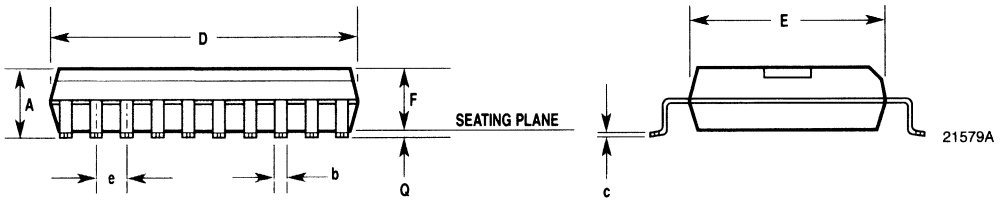
Ref. 90X00181





M3 Package
20 Pin Plastic SOIC .300"





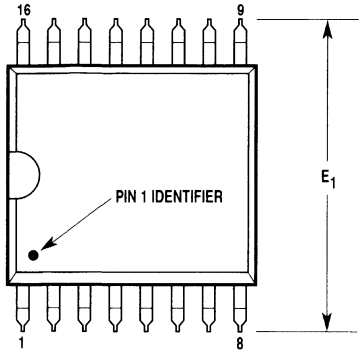
Dimensions

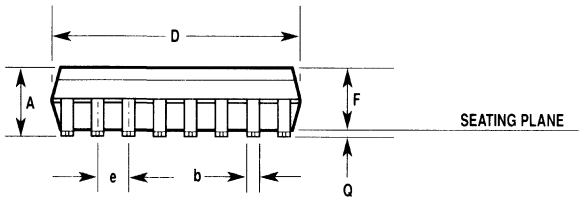
	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.093 (2.36)	.104 (2.64)	
b	.014 (0.36)	.019 (0.48)	
b_1			
c	.009 (0.23)	.013 (0.33)	
D	.496 (12.60)	.512 (13.01)	
E	.291 (7.39)	.299 (7.60)	
E_1	.394 (10.01)	.419 (10.64)	
e			.050 (1.27) Typ.
L			
N			20
Q	.004 (0.10)	.012 (0.30)	

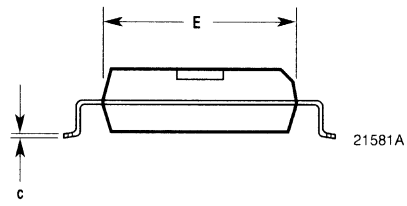
Ref. 90X00181

M

M9 Package
16 Pin Plastic SOIC .300"





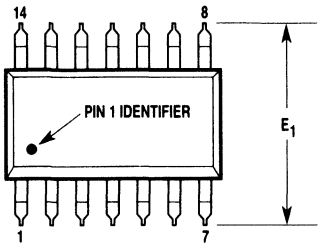


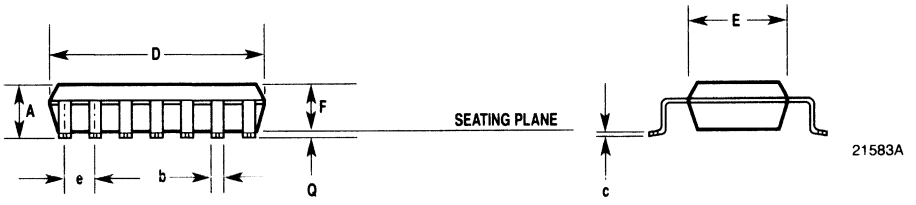
Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.093 (2.36)	.104 (2.64)	
b	.014 (0.36)	.020 (0.51)	
b_1			
c	.009 (0.23)	.013 (0.33)	
D	.398 (10.11)	.413 (10.50)	
E	.291 (7.39)	.299 (7.60)	
E_1	.394 (10.01)	.419 (10.64)	
e			.050 (1.27) Typ.
F	.089 (2.26)	.092 (2.34)	
L			
N			16
Q	.004 (0.10)	.012 (0.30)	
α			

Ref. 90X00181

ME Package
14 Pin Plastic SOIC .150"





Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.053 (1.35)	.069 (1.75)	
b	.014 (0.36)	.020 (0.51)	
b_1			
c	.008 (0.20)	.010 (0.25)	
D	.335 (8.51)	.344 (8.74)	
E	.150 (3.81)	.157 (3.99)	
E_1	.228 (5.79)	.244 (6.20)	
e			.050 (1.27) Typ.
F	.049 (1.25)	.059 (1.50)	
L			
N			14
Q	.004 (0.10)	.010 (0.25)	
α			

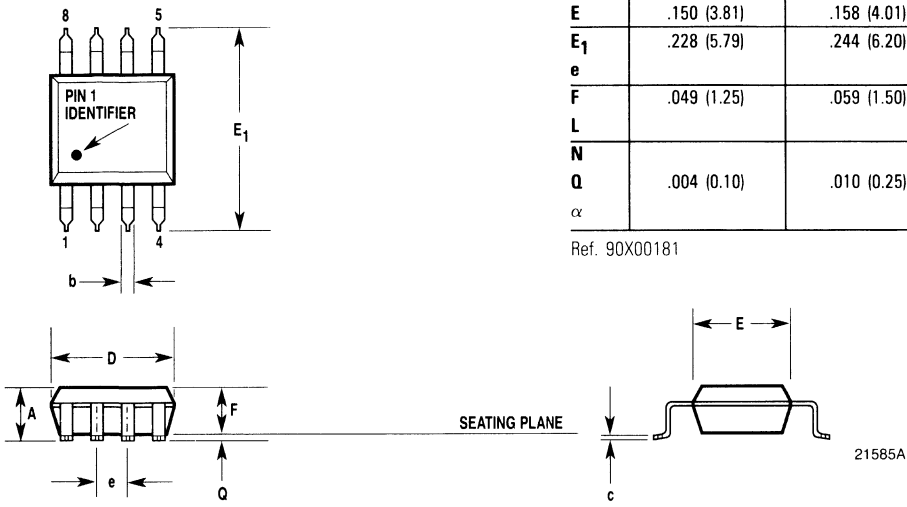
Ref. 90X00181

MH Package
8 Pin Plastic SOIC .150"

Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.053 (1.35)	.069 (1.75)	
b	.014 (0.36)	.019 (0.48)	
b_1			
c	.007 (0.18)	.010 (0.25)	
D	.188 (4.78)	.196 (4.98)	
E	.150 (3.81)	.158 (4.01)	
E_1	.228 (5.79)	.244 (6.20)	
e			.050 (1.27) Typ.
F	.049 (1.25)	.059 (1.50)	
L			
N			8
Q	.004 (0.10)	.010 (0.25)	
α			

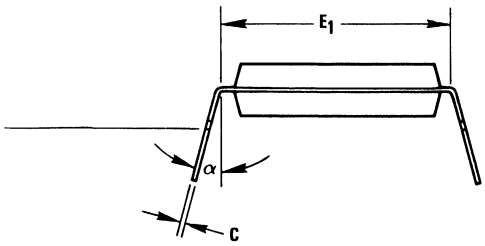
Ref. 90X00181



NO Package
64 Pin Plastic DIP

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

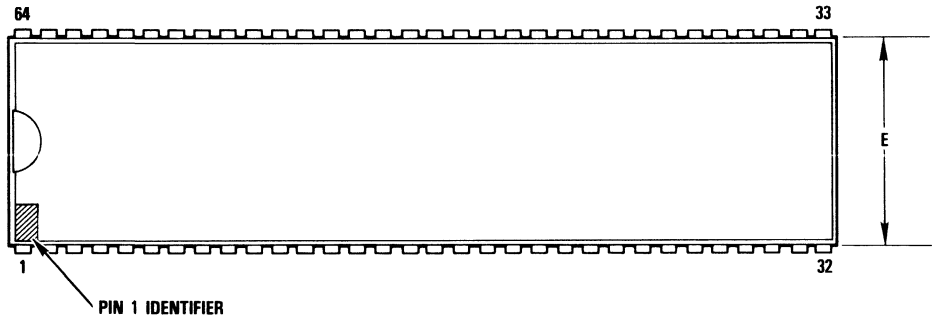
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.

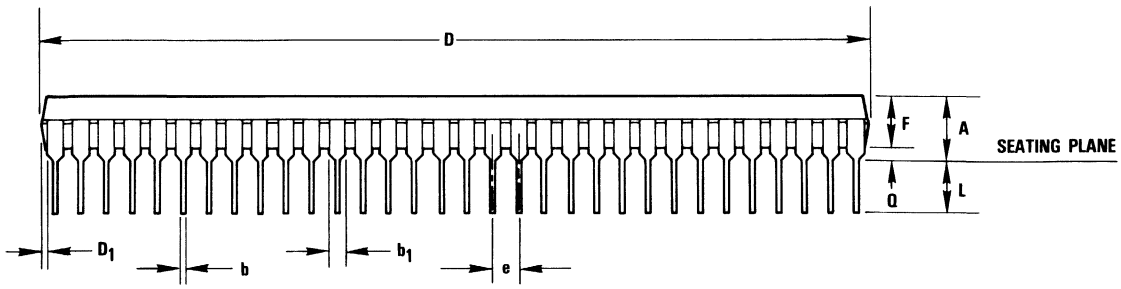


Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A		.250 (6.35)	
b	.014 (0.35)	.022 (0.56)	
b_1	.030 (0.76)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	3.05 (77.47)	3.245 (82.42)	
D_1	.005 (0.13)		
E	.745 (18.92)	.840 (21.34)	
E_1	.900 (22.86)	.925 (23.50)	
e			.100 (2.54) Basic
F	.125 (3.18)	.195 (4.95)	
L	.115 (2.92)	.200 (5.08)	
Q	.015 (0.38)		
α	0°	15°	

Ref. 90X00181



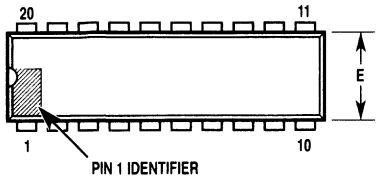


M

N1 Package
20 Pin Plastic DIP

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

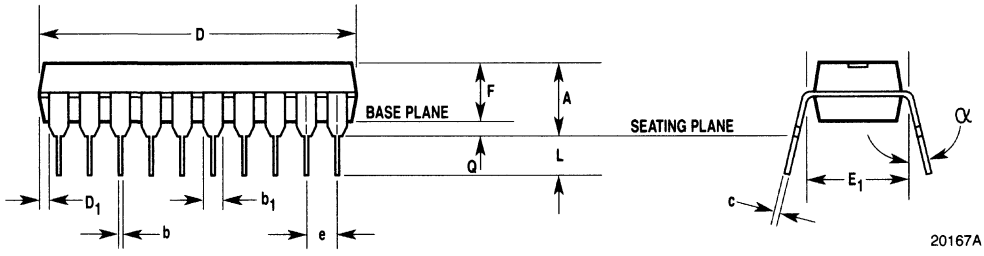
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.145 (3.68)	.200 (5.08)	
b	.015 (0.38)	.021 (0.53)	
b_1			.060 (1.52) Typ.
C	.009 (0.23)	.015 (0.38)	
D	1.013 (25.73)	1.040 (26.42)	
D_1	.005 (0.13)		
E	.255 (6.48)	.265 (6.73)	
E_1	.310 (7.87)	.363 (9.27)	
e	.090 (2.29)	.110 (2.79)	
F	.125 (3.18)	.135 (3.43)	
L	.125 (3.18)	.140 (3.56)	
Q	.020 (0.51)		
α	0°	15°	

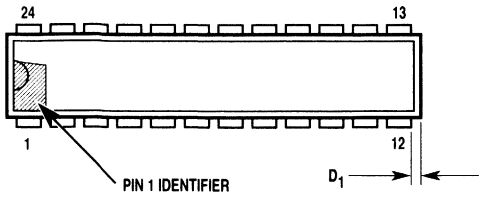
Ref. 90X00181



N2 Package
24 Pin Plastic DIP .300"

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

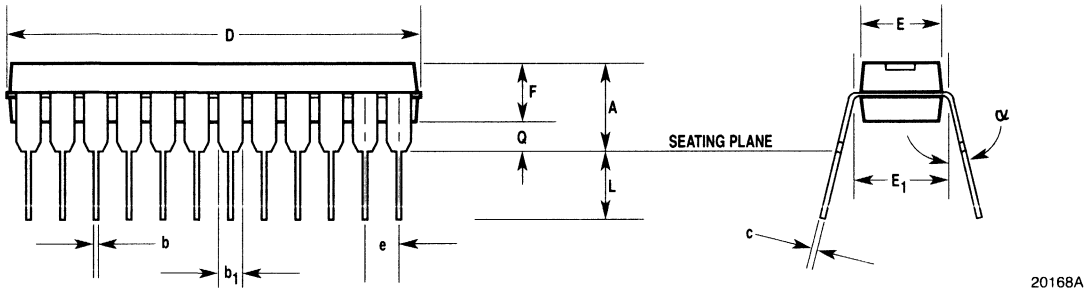
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.130 (3.30)	.230 (5.84)	
b	.01+ (0.35)	.023 (0.58)	
b_1	.045 (1.14)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	1.180 (29.97)	1.285 (32.64)	
D_1	.005 (0.13)		
E	.240 (6.10)	.310 (7.87)	
E_1			.300 (7.62) Basic
e			.100 (2.54) Basic
F	.115 (2.92)	.195 (4.95)	
L	.115 (2.92)	.200 (5.08)	
Q	.015 (0.38)		
α	0°	15°	

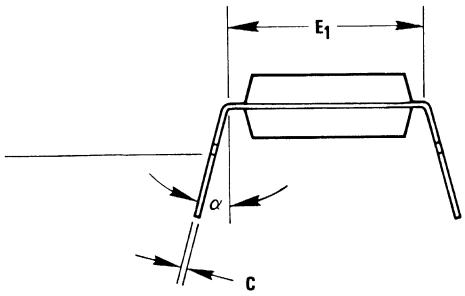
Ref. 90X00181



N4 Package
48 Pin Plastic DIP

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

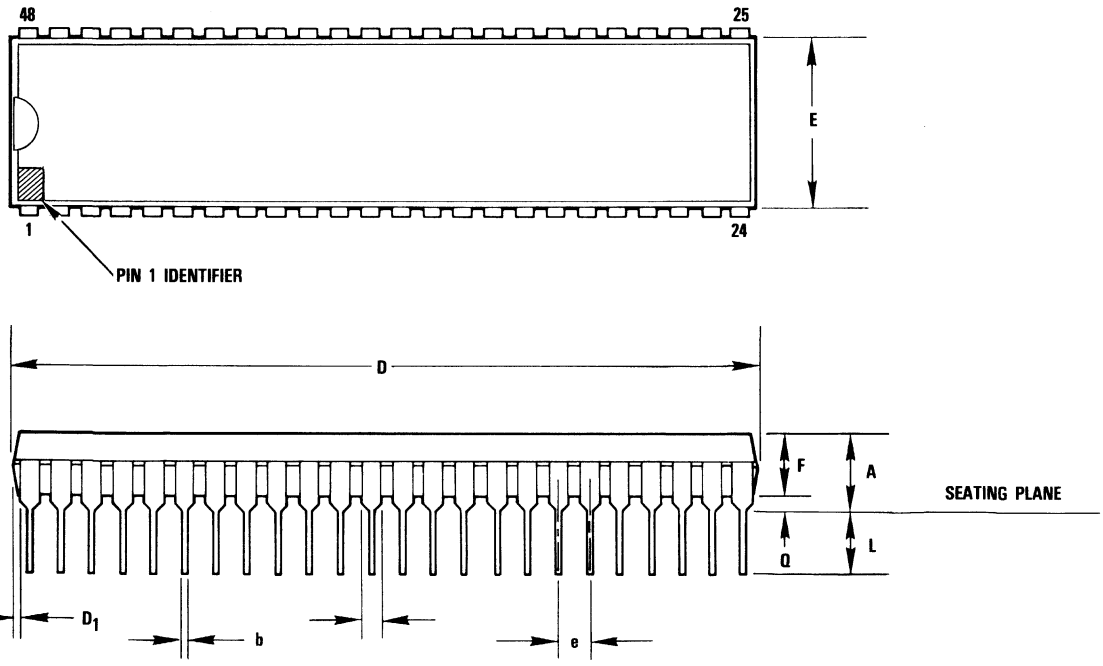
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A		.250 (6.35)	
b	.014 (0.35)	.022 (0.56)	
b_1	.030 (0.76)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	2.375 (60.32)	2.490 (63.25)	
D_1	.005 (0.13)		
E	.485 (12.32)	.580 (14.73)	
E_1	.600 (15.24)	.625 (15.87)	
e			.100 (2.54) Basic
F	.125 (3.18)	.195 (4.95)	
L	.115 (2.92)	.200 (5.08)	
Q	.015 (0.38)		
α	0°	15°	

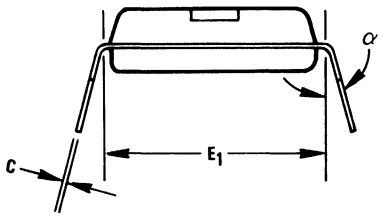
Ref. 90X00181



N5 Package
40 Pin Plastic DIP

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

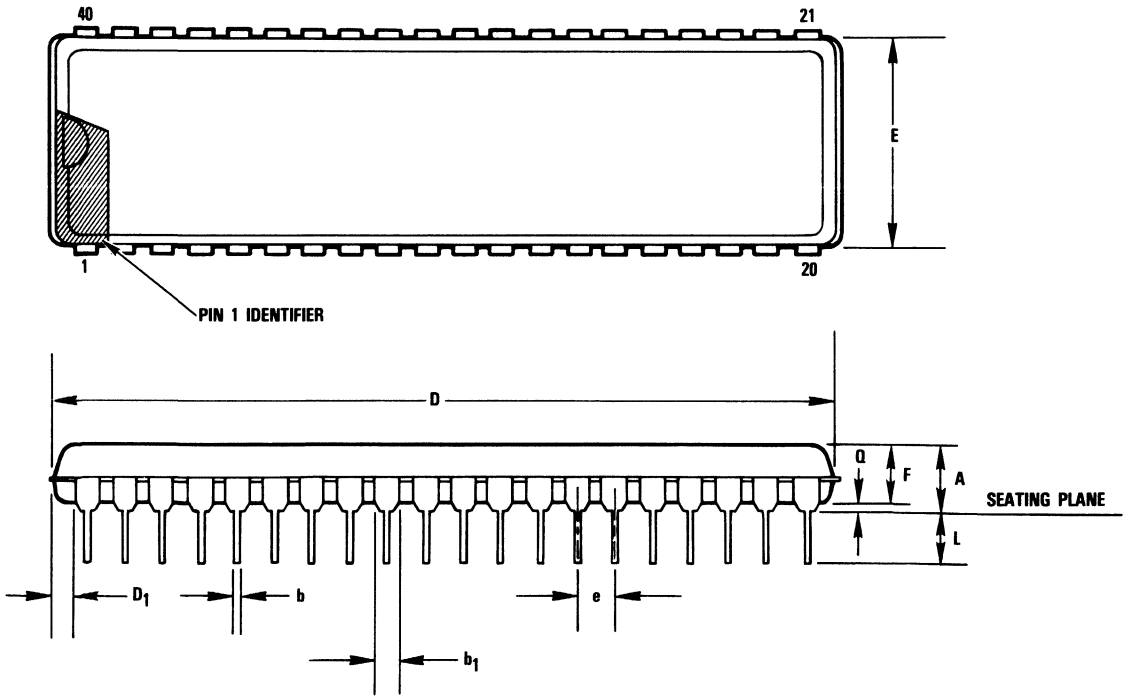
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A		.250 (6.35)	
b	.014 (0.35)	.022 (0.56)	
b_1	.030 (0.76)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	1.980 (50.29)	2.095 (53.21)	
D_1	.005 (0.13)		
E	.485 (12.32)	.580 (14.73)	
E_1	.600 (15.24)	.625 (15.87)	
e			.100 (2.54) Basic
F	.125 (3.18)	.195 (4.95)	
L	.115 (2.92)	.200 (5.08)	
Q	.015 (0.38)		
α	0°	15°	

Ref. 90X00181

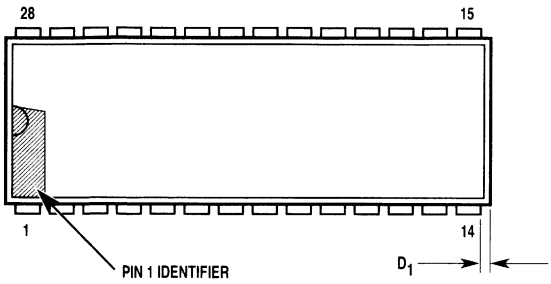


M

N6 Package
28 Pin Plastic DIP

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

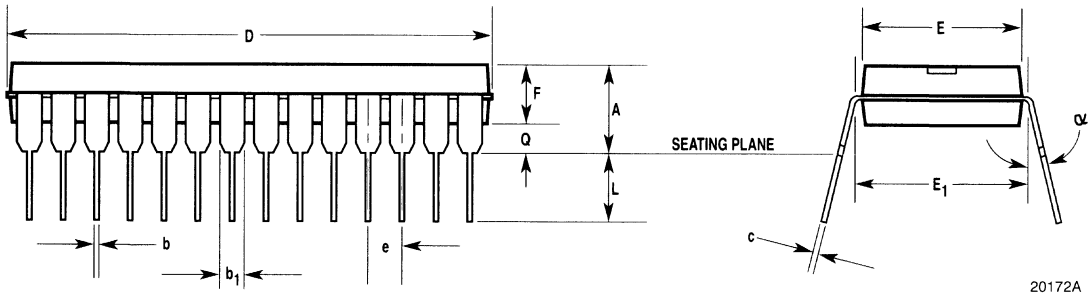
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A		.250 (6.35)	
b	.014 (0.36)	.022 (0.56)	
b_1	.030 (0.76)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	1.380 (35.05)	1.565 (39.75)	
D_1	.005 (0.13)		
E	.485 (12.32)	.580 (14.73)	
E_1	.600 (15.24)	.625 (15.88)	
e			.100 (2.54) Basic
F			
L	.115 (2.92)	.200 (5.08)	
Q	.015 (0.38)		
α	0°	15°	

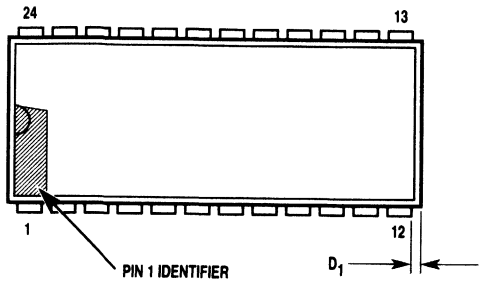
Ref. 90X00181



N7 Package
24 Pin Plastic DIP

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

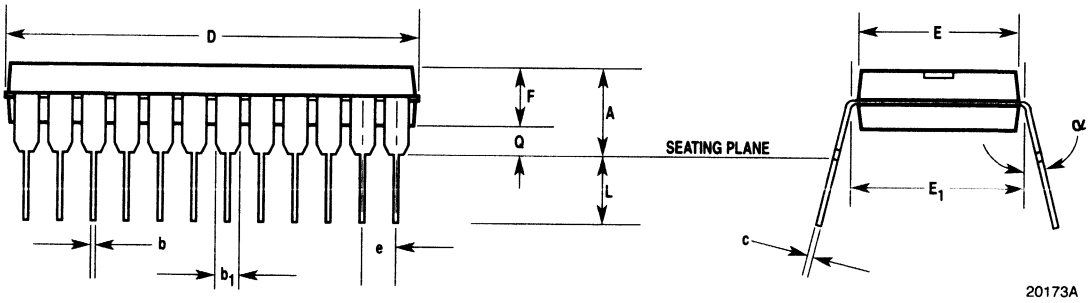
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A		.250 (6.35)	
b	.014 (0.35)	.022 (0.56)	
b_1	.030 (0.76)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	1.150 (29.21)	1.290 (32.77)	
D_1	.005 (0.13)		
E	.485 (12.32)	.580 (14.73)	
E_1	.600 (15.24)	.625 (15.88)	
e			.100 (2.54) Basic
F	.125 (3.18)	.195 (4.95)	
L	.115 (2.92)	.200 (5.08)	
Q	.015 (0.38)		
α	0°	15°	

Ref. 90X00181

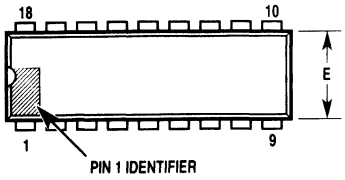


M

N8 Package
18 Pin Plastic DIP

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

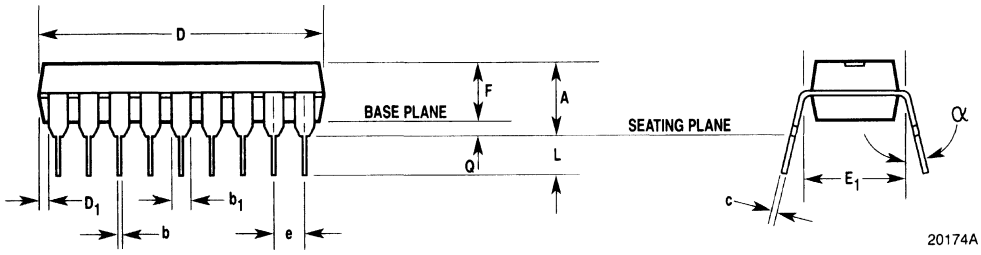
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A		.210 (5.33)	
b	.014 (0.36)	.022 (0.56)	
b_1	.045 (1.14)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	.845 (21.46)	.925 (23.50)	
D_1	.005 (0.13)		
E	.240 (6.10)	.280 (7.11)	
E_1	.300 (7.62)	.325 (8.25)	
e			.100 (2.54) Basic
F	.115 (2.92)	.195 (4.95)	
L	.115 (2.92)	.160 (4.06)	
Q	.015 (0.38)		
α	0°	15°	

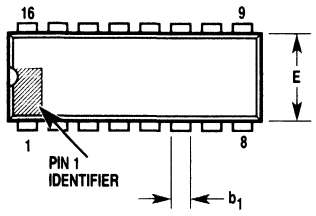
Ref. 90X00181



N9 Package
16 Pin Plastic DIP

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

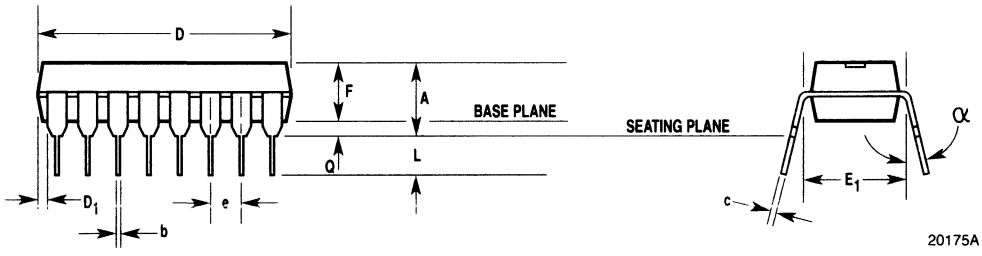
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A		.210 (5.33)	
b	.014 (0.35)	.022 (0.56)	
b_1	.045 (1.14)	.070 (1.78)	
C	.008 (0.20)	.015 (0.38)	
D	.745 (18.92)	.840 (21.34)	
D_1	.005 (0.13)		
E	.240 (6.10)	.280 (7.11)	
E_1	.300 (7.62)	.325 (8.25)	
e			.100 (2.54) Basic
F	.115 (2.92)	.195 (4.95)	
L	.115 (2.92)	.160 (4.06)	
Q	.015 (0.38)		
α	0°	15°	

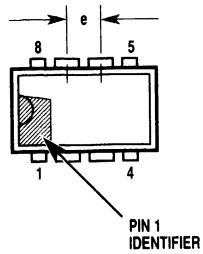
Ref. 90X00181



NH Package
8 Pin Plastic DIP

Notes: 1. A notch or pin one identifier shall be located adjacent to pin one and within the shaded area shown.

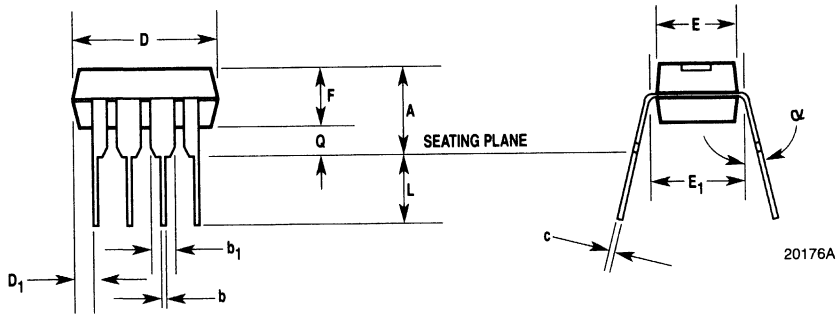
2. Each pin centerline shall be located within .010 inch (0.25mm) of its true longitudinal position.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.145 (3.68)	.200 (5.08)	
b	.015 (0.38)	.021 (0.53)	
b_1			.060 (1.52) Typ.
C	.009 (0.23)	.015 (0.38)	
D	.373 (9.47)	.400 (10.16)	
D_1	.005 (0.13)		
E	.245 (6.22)	.255 (6.48)	
E_1	.310 (7.87)	.365 (9.27)	
e	.090 (2.29)	.110 (2.79)	
F	.125 (3.18)	.135 (3.43)	
L	.125 (3.18)	.140 (3.56)	
Q	.020 (0.51)		
α	0°	15°	

Ref. 90X00181



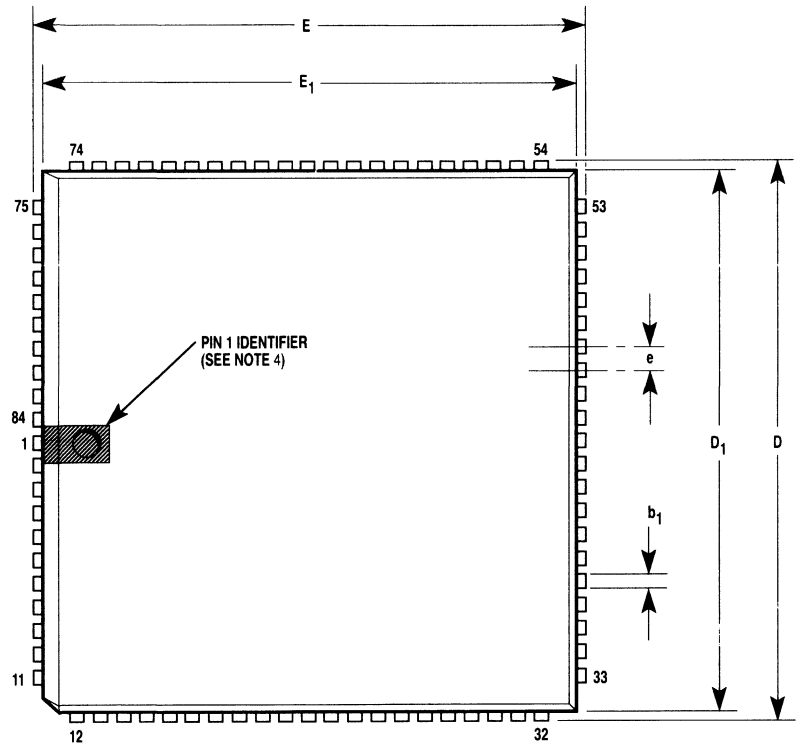
RO Package
84 Lead Plastic J-Leaded Chip Carrier

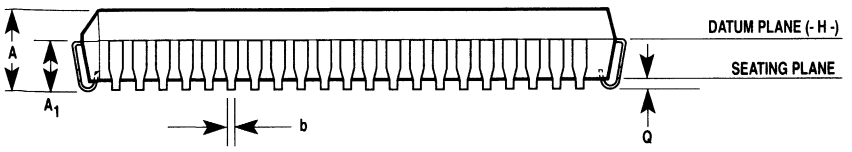
Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane **(-H-)** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Dimension D_1 and E_1 do not include mold protrusion. Allowable protrusion is .010 inch (0.25mm).
4. Details of pin 1 identifier are optional but must be located within the zone indicated.
5. Dimension N: number of terminals.
6. Dimension ND: number of terminals per package edge.
7. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.165 (4.20)	.200 (5.08)	
A_1	.090 (2.29)	.130 (3.30)	
b	.013 (0.33)	.021 (0.53)	
b_1	.026 (0.66)	.032 (0.81)	
D	1.185 (30.10)	1.195 (30.35)	
D_1	1.150 (29.21)	1.158 (29.41)	Note 3
E	1.185 (30.10)	1.195 (30.35)	
E_1	1.150 (29.21)	1.158 (29.41)	Note 3
N			84, Note 5
ND			21, Note 6
Q	.020 (0.51)		

Ref. 90X00181





20180A

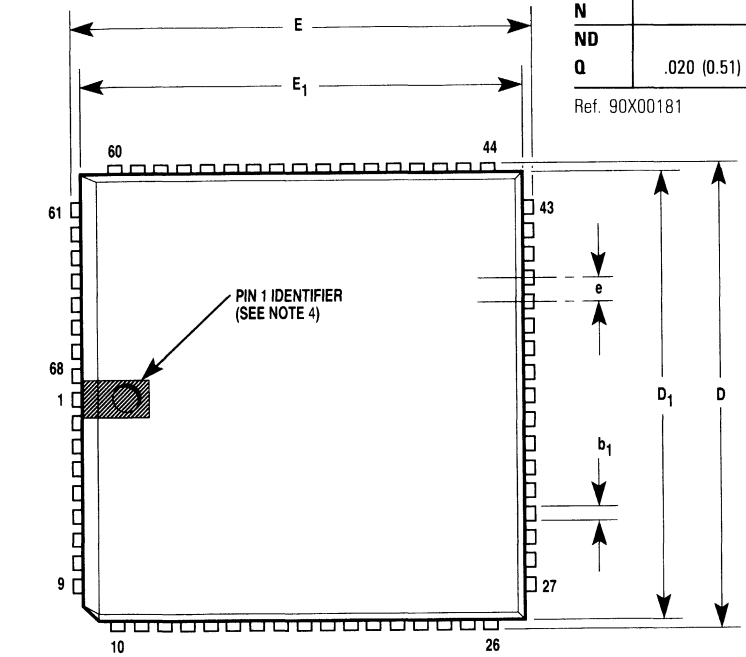
R1 Package
68 Lead Plastic J-Leaded Chip Carrier

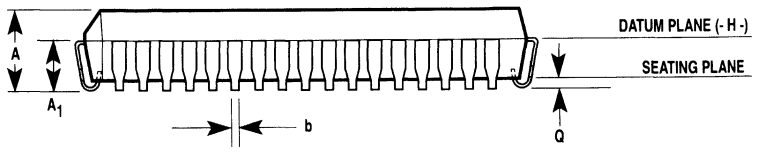
Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane **(–H–)** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Dimension D_1 and E_1 do not include mold protrusion. Allowable protrusion is .010 inch (0.25mm).
4. Details of pin 1 identifier are optional but must be located within the zone indicated.
5. Dimension N: number of terminals.
6. Dimension ND: number of terminals per package edge.
7. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.165 (4.20)	.200 (5.08)	
A_1	.090 (2.29)	.130 (3.30)	
b	.013 (0.33)	.021 (0.53)	
b_1	.026 (0.66)	.032 (0.81)	
D	.985 (25.02)	.995 (25.27)	
D_1	.950 (24.13)	.958 (24.33)	Note 3
E	.985 (25.02)	.995 (25.27)	
E_1	.950 (24.13)	.958 (24.33)	Note 3
e			.050 (1.27) Basic
N			68, Note 5
ND			17, Note 6
Q	.020 (0.51)		

Ref. 90X00181

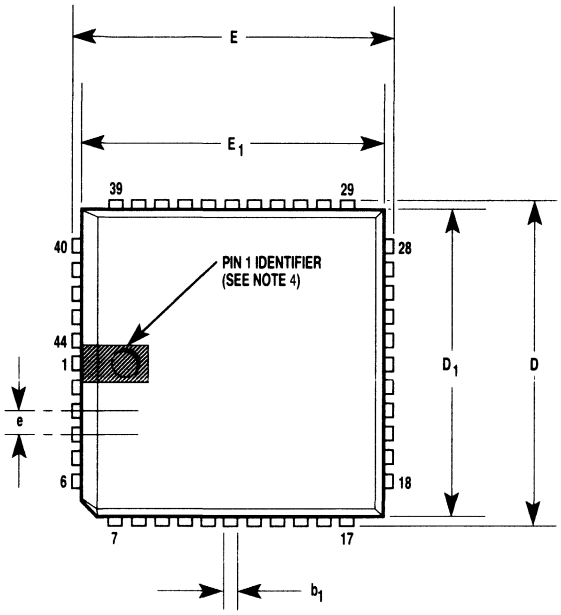




20181A

R2 Package
44 Lead Plastic J-Leaded Chip Carrier

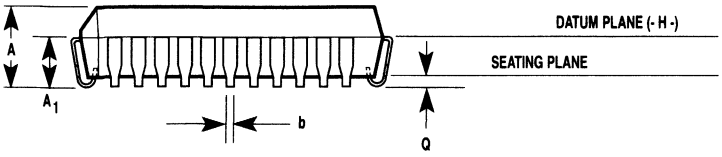
Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M 1982.
2. Datum plane **(–H–)** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Dimension D_1 and E_1 do not include mold protrusion. Allowable protrusion is .010 inch (0.25mm).
4. Details of pin 1 identifier are optional but must be located within the zone indicated.
5. Dimension N: number of terminals.
6. Dimension ND: number of terminals per package edge.
7. Controlling dimension: inch.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.165 (4.20)	.180 (4.57)	
A_1	.090 (2.29)	.120 (3.04)	
b	.013 (0.33)	.021 (0.53)	
b_1	.026 (0.66)	.032 (0.81)	
D	.685 (17.40)	.695 (17.65)	
D_1	.650 (16.51)	.656 (16.66)	Note 3
E	.685 (17.40)	.695 (17.65)	
E_1	.650 (16.51)	.656 (16.66)	Note 3
e			.050 (1.27) Basic
N			44, Note 5
ND			11, Note 6
Q	.020 (0.51)		

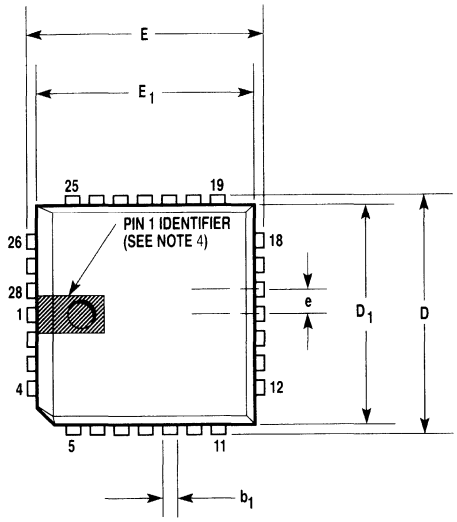
Ref. 90X00181

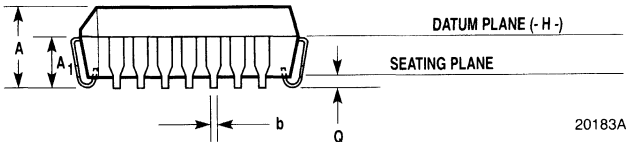


20182A

R3 Package
28 Lead Plastic J-Leaded Chip Carrier

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane **(-H-)** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Dimension D_1 and E_1 do not include mold protrusion. Allowable protrusion is .010 inch (.245mm).
4. Details of pin 1 identifier are optional but must be located within the zone indicated.
5. Dimension N: number of terminals.
6. Dimension ND: number of terminals per package edge.
7. Controlling dimension: inch.





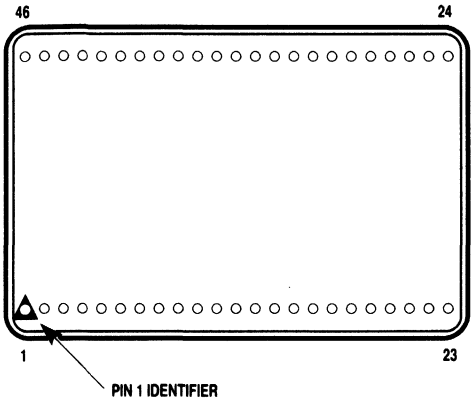
Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A	.165 (4.20)	.180 (4.57)	
A_1	.900 (2.29)	.120 (3.04)	
b	.013 (0.33)	.021 (0.53)	
b_1	.026 (0.66)	.032 (0.81)	
D	.485 (12.32)	.495 (12.57)	
D_1	.450 (11.43)	.456 (11.58)	Note 3
E	.485 (12.32)	.495 (12.57)	
E_1	.450 (11.43)	.456 (11.58)	Note 3
e			.050 (1.27) Basic
N			28, Note 5
ND			7, Note 6
Q	.020 (0.51)		

Ref. 90X00181

S3 Package
46 Pin Hermetic Metal DIP, Top Sealed

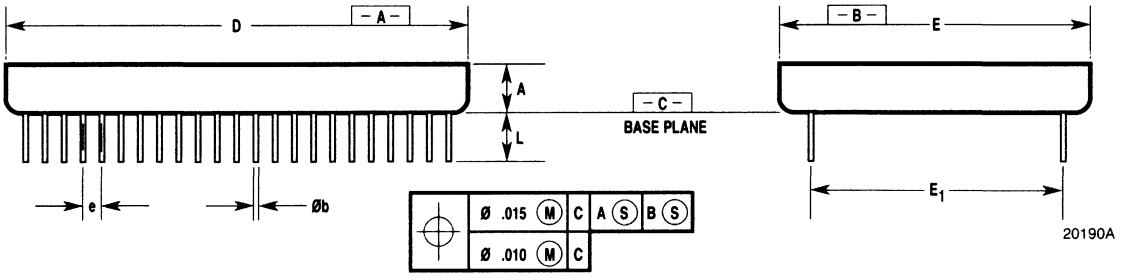
Notes: 1. Dimension N: number of terminals.
2. Dimension ND: number of terminals per package edge.
3. Controlling dimension: inch.



Dimensions

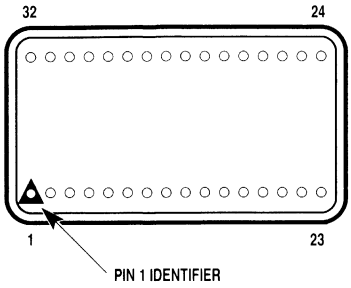
	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A		.250 (6.35)	
ϕb	.016 (0.41)	.020 (0.51)	
D		2.390 (60.71)	
E		1.590 (40.39)	
E_1			1.300 (33.02) Basic
e			.100 (2.54) Basic
L	.175 (4.44)	.220 (5.59)	
N			46, Note 1
ND			23, Note 2

Ref. 90X00181



S5 Package
32 Pin Hermetic Metal DIP

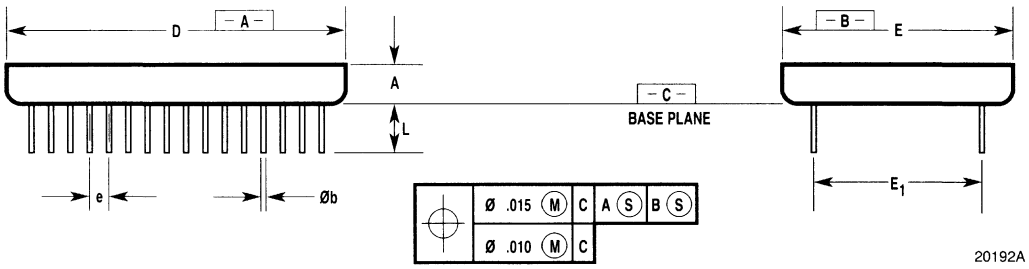
Notes: 1. Dimension N: number of terminals.
2. Dimension ND: number of terminals per package edge.
3. Controlling dimension: inch.



Dimensions

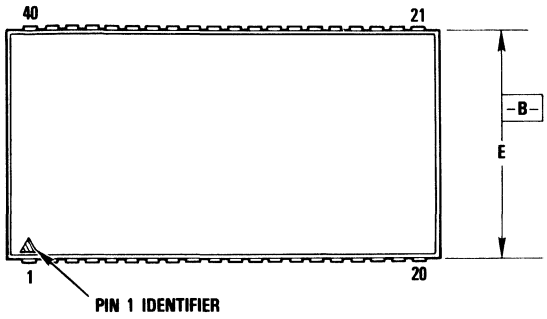
Inches (Millimeters)			
Sym	**Min**	**Max**	**Notes**
A		.240 (6.10)	
ϕb	.016 (0.41)	.020 (0.51)	
D		1.750 (44.45)	
E		1.150 (29.21)	
E_1			.900 (22.86) Basic
e			.100 (2.54) Basic
L	.175 (4.44)	.220 (5.59)	
N			32, Note 1
ND			16, Note 2

Ref. 90X00181



S6 Package
40 Pin Hermetic Ceramic DIP

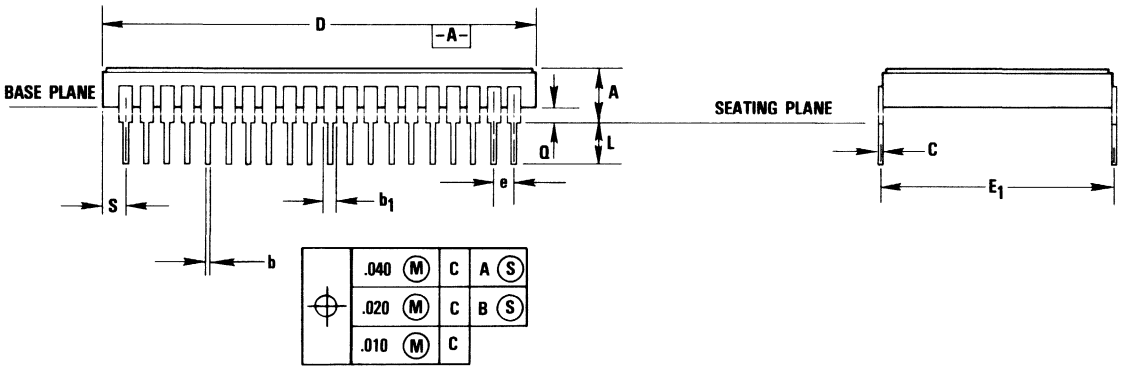
Notes: 1. Dimension N: the total leadcount.
2. Dimension ND: the leadcount per package side.
3. Controlling dimension: inch.



Dimensions

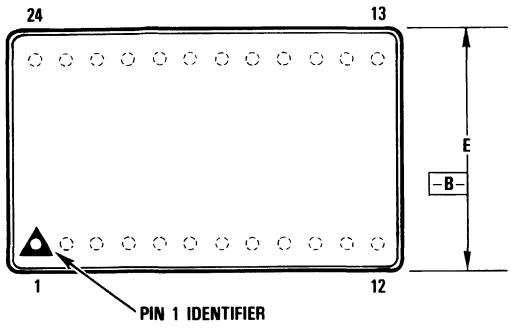
Sym	Inches (Millimeters) Min	Max	Notes
A		.240 (6.10)	
b	.016 (0.41)	.020 (0.51)	
b_1	.040 (1.02)	.060 (1.52)	
C	.008 (0.20)	.015 (0.38)	
D		2.130 (54.10)	
E		1.110 (28.19)	
E_1			1.096 (27.84) Basic
e			.100 (2.54) Basic
L	.125 (3.17)	.200 (5.08)	
N			40, Note 1
ND			20, Note 2
Q	.035 (0.89)	.065 (1.65)	
S			.100 (2.54) Ref.

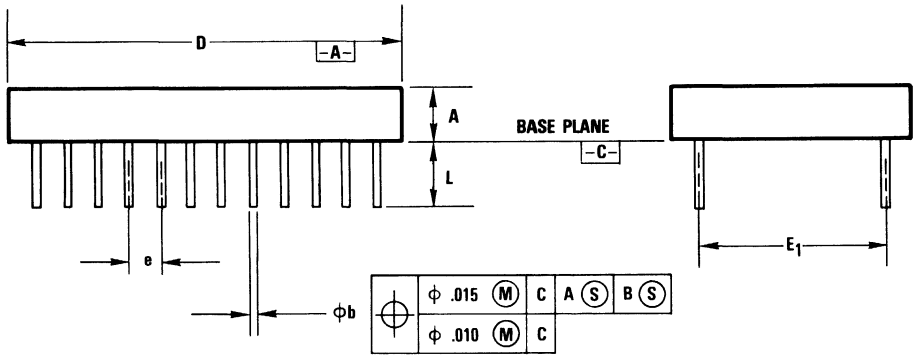
Ref. 90X00181



S7 Package (Commercial)
24 Pin Hermetic Metal DIP

Notes: 1. Dimension N: the total leadcount.
2. Dimension ND: the leadcount per package side.
3. Controlling dimension: inch.





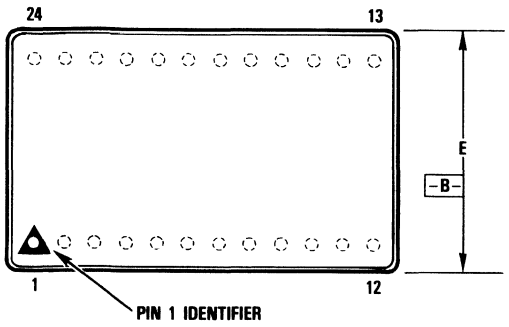
Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A		.225 (5.72)	
ϕb	.016 (0.41)	.020 (0.51)	
D		1.400 (35.56)	
E		.840 (21.34)	
E_1			.600 (15.24) Basic
e			.100 (2.54) Basic
L	.175 (4.44)	.220 (5.59)	
N			24, Note 1
ND			12, Note 2

Ref. 90X00181

S7 Package (Military)
24 Pin Hermetic Metal DIP, Top Sealed

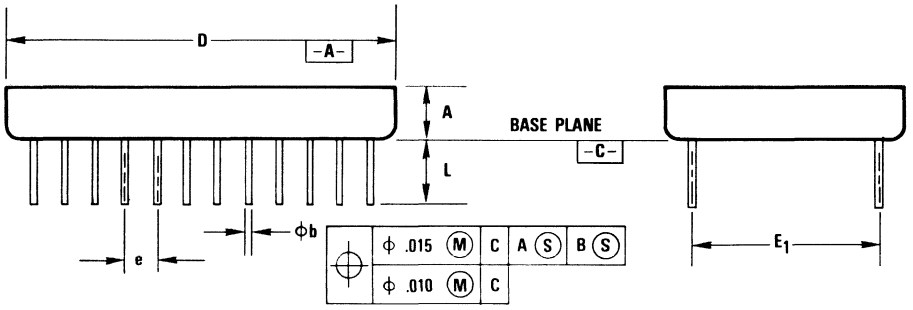
Notes: 1. Dimension N: the total leadcount.
2. Dimension ND: the leadcount per package side.
3. Controlling dimension: inch.



Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A		.220 (5.59)	
ϕb	.016 (0.41)	.020 (0.51)	
D		1.285 (32.64)	
E		.785 (19.94)	
E_1			.600 (15.24) Basic
e			.100 (2.54) Basic
L	.175 (4.44)	.220 (5.59)	
N			24, Note 1
ND			12, Note 2

Ref. 90X00181



S7 Package (Platform Style)

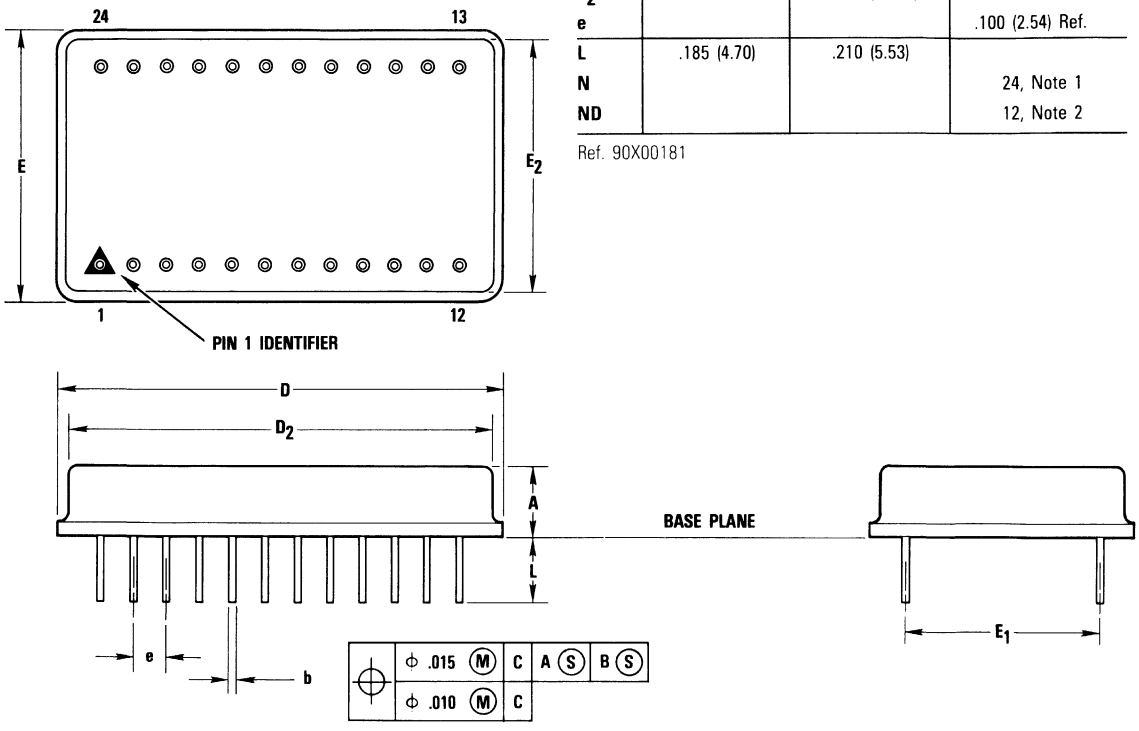
24 Pin Hermetic Metal DIP, Bottom Sealed

Notes:
1. Dimension N: the total leadcount.
2. Dimension ND: the leadcount per package side.
3. Controlling dimension: inch.

Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A		.225 (5.72)	
b	.016 (0.41)	.020 (0.51)	
D		1.400 (35.56)	
D_2		1.300 (33.02)	
E		.840 (21.34)	
E_1			.600 (15.24) Ref.
E_2		.760 (19.30)	
e			.100 (2.54) Ref.
L	.185 (4.70)	.210 (5.53)	
N			24, Note 1
ND			12, Note 2

Ref. 90X00181



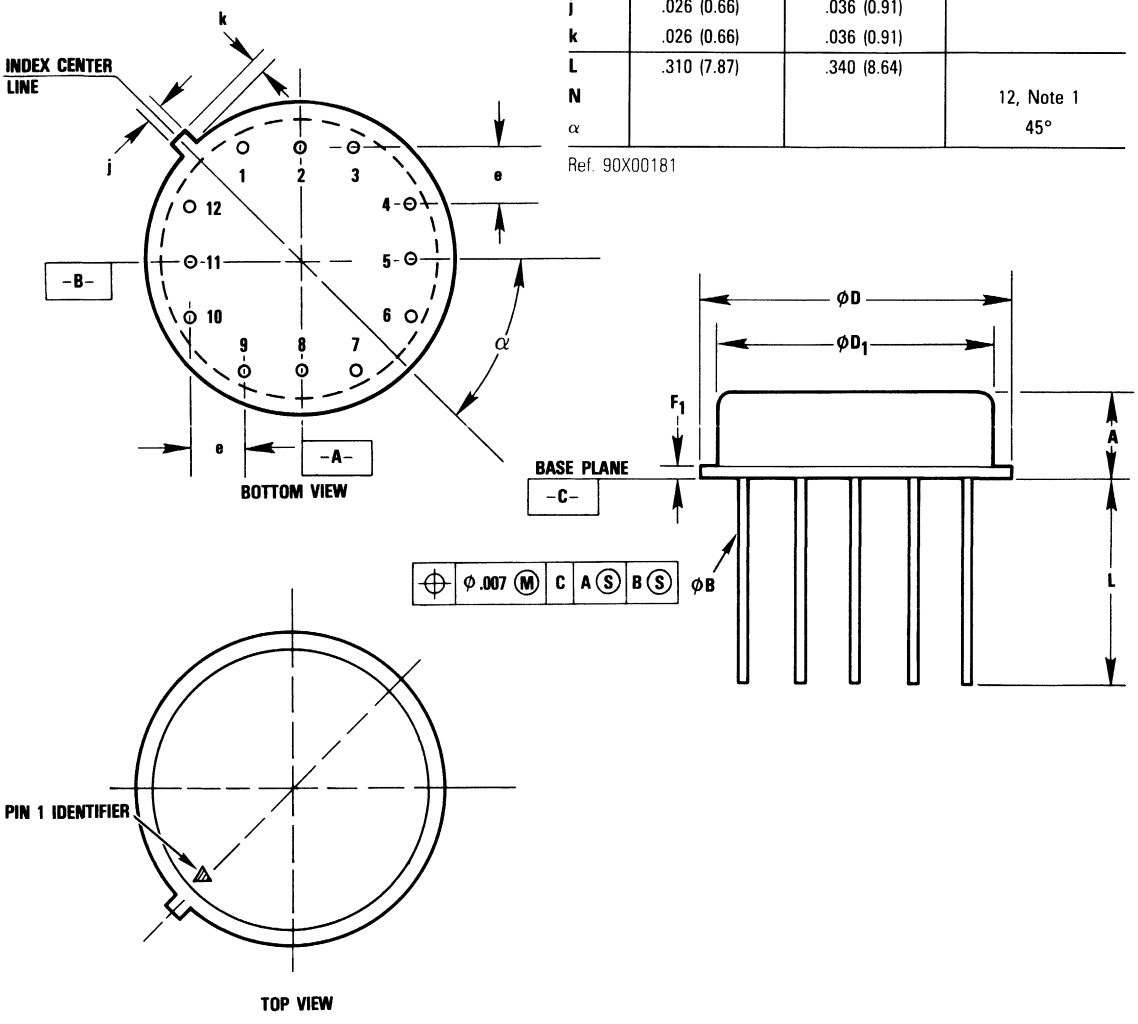
X1 Package
12 Lead Metal Can (TO-8/MO-12 Style)

Notes: 1. Dimension N: maximum quantity of lead positions.
2. Controlling dimension: inch.

Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.145 (6.68)	.170 (4.32)	
ϕB	.016 (0.41)	.019 (0.48)	
ϕD	.598 (15.19)	.602 (15.29)	
ϕD_1	.545 (13.84)	.550 (13.97)	
e			.100 (2.54) Basic
F_1	.010 (0.25)	.040 (1.02)	
j	.026 (0.66)	.036 (0.91)	
k	.026 (0.66)	.036 (0.91)	
L	.310 (7.87)	.340 (8.64)	
N			12, Note 1
α			45°

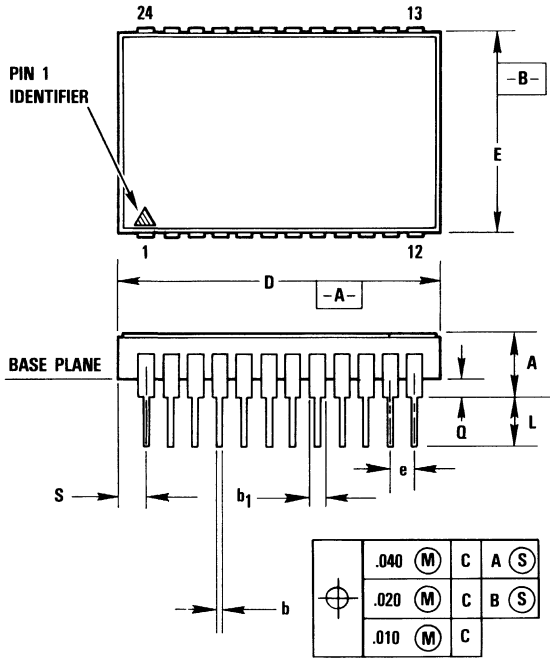
Ref. 90X00181

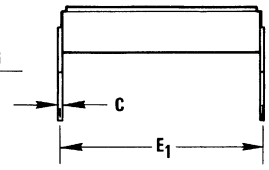


M

X2 Package
24 Pin Ceramic DIP

Notes: 1. Dimension N: number of terminals.
2. Dimension ND: number of terminals per package edge.
3. Controlling dimension: inch.





Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
A		.265 (6.73)	
b	.016 (0.41)	.020 (0.51)	
b_1	.040 (1.02)	.060 (1.52)	
C	.008 (0.20)	.015 (0.38)	
D		1.320 (33.53)	
E		.815 (20.70)	
E_1			.800 (20.32) Basic
e			.100 (2.54) Basic
L	.125 (3.17)	.200 (5.08)	
N			24, Note 1
ND			12, Note 2
Q	.035 (0.89)	.065 (1.65)	
S			.100 (2.54) Ref.

Ref. 90X00181

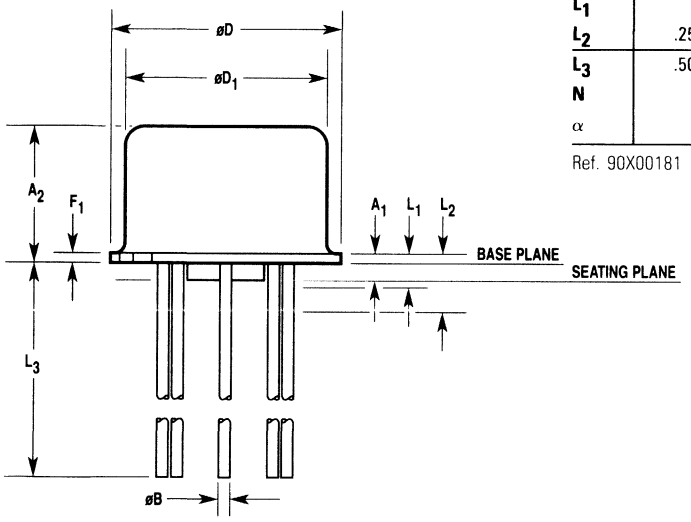
Y8 Package
8 Lead Metal Can

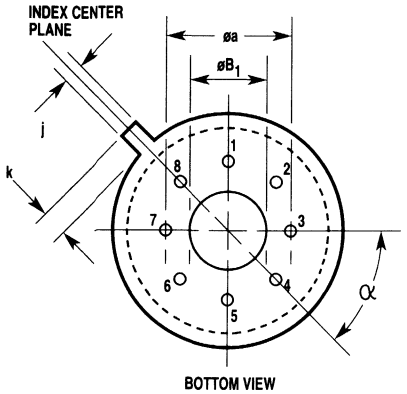
Notes: 1. Dimension N: maximum quantity of lead positions.
2. Controlling dimension: inch.

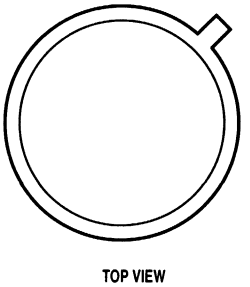
Dimensions

	Inches (Millimeters)		
Sym	**Min**	**Max**	**Notes**
ϕa	.195 (4.95)	.205 (5.21)	
A_1	.015 (0.38)	.040 (1.02)	
A_2	.165 (4.91)	.185 (4.70)	
ϕB	.016 (0.41)	.019 (0.48)	
ϕB_1	.120 (3.05)	.140 (3.56)	
ϕD	.350 (8.89)	.370 (9.40)	
ϕD_1	.315 (8.00)	.335 (8.51)	
F_1		.025 (0.89)	
j	.028 (0.71)	.034 (0.86)	
k	.029 (0.74)	.045 (1.14)	
L_1			
L_2	.250 (6.35)	.500 (12.70)	
L_3	.500 (12.70)		
N			8, Note 1
α			45° Typ.

Ref. 90X00181







21587A

M

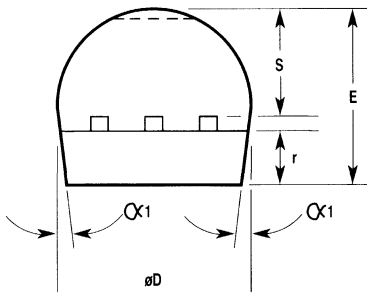
Z3 Package
3 Lead TO-92

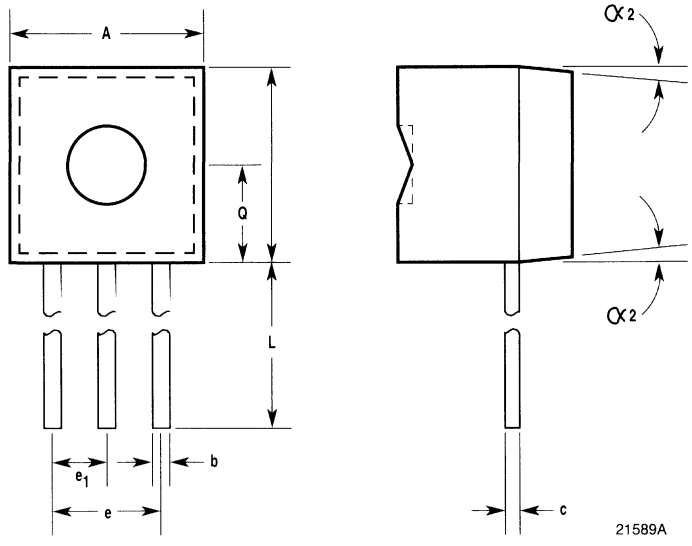
Dimensions

Sym	Inches (Millimeters) Min	Max	Notes
A	.175 (4.44)	.185 (4.70)	
A_1			
b	.014 (0.36)	.016 (0.41)	
c	.0145 (0.37)	.0155 (0.39)	
ϕb			
ϕD			.190 (4.57) Nominal
ϕD_1			
E	.135 (3.43)	.145 (3.68)	
e	.090 (2.29)	.110 (2.79)	
e_1	.045 (1.14)	.055 (1.40)	
j			
L	.500 (12.70)		
L_1			
L_2			
Q			.090 (2.29) Nominal
r			.090 (2.29) Nominal
S	.083 (2.11)		
α_1			10° Nominal
α_2			5° Nominal

Ref. 90X00181

Note: 1. Controlling dimension: inch.





Glossary

ACC Accumulate (Control)

An active-HIGH control signal which causes the contents of the product register to be added to (or subtracted from) the output of the multiplier in a multiplier-accumulator.

A_{GND} Analog Ground

Ground reference point for analog power supply and analog circuitry.

BW Full Power Bandwidth

Bandwidth specified for a flash Analog-to-Digital (A/D) converter is different from the bandwidth specification given for a purely analog device. Before attenuation becomes a significant factor in the performance of the converter, other problems may arise, leading to degraded performance. Spurious and missing codes might be encountered when the analog input frequency exceeds the bandwidth specification. Bandwidth for an A/D converter is the maximum frequency full-scale input sinewave that can be accurately quantized by the A/D converter without spurious or missing codes. A spurious code is a code which is grossly inaccurate, such as when the input signal is near mid-scale and an output code which is a full-scale output is generated. When the signal is reconstructed with a D/A converter, this spurious code looks like a glitch, and is therefore sometimes referred to as a glitch. Bandwidth is measured with worst case power supply conditions and sampling at the maximum sampling rate. (F_S).

The test used to determine the bandwidth of an A/D converter is the "Beat Frequency Test." The principle behind this test is to use "aliasing" to convert a high-frequency input signal to a low-frequency output signal which is easier to analyze. This is done by providing the A/D converter with a high-frequency sine wave input, and then sampling the input at a rate offset by a small delta in frequency from an integral (N) multiple of the input frequency. A D/A converter is given every Nth A/D output; this produces an output signal of the A/D which is an aliased version of the input. This is shown in figure 1, where the upper high frequency input is sampled at a rate slightly faster than three times its frequency (A/D samples are taken at the locations of the upper bars), every third A/D sample (lower bars) is presented to a D/A converter, and the resultant output signal is the bottom low frequency signal. In a typical set-up, the analog reconstruction (D/A output) is examined on an oscilloscope for spurious and missing codes. Figure 2 shows a typical test set-up. A spurious code is defined as a non-continuous change in the output of the A/D which is not reflected in the input signal. Figure 3 shows an example of a spurious code in the reconstructed output of an A/D converter. A missing code is defined as a code which has a code size less than the minimum specified (see definition for Q, code size). Figure 4 shows an example of the output of an A/D which has missing codes. The photographs for figures 3 and 4 were both obtained with a beat frequency test.

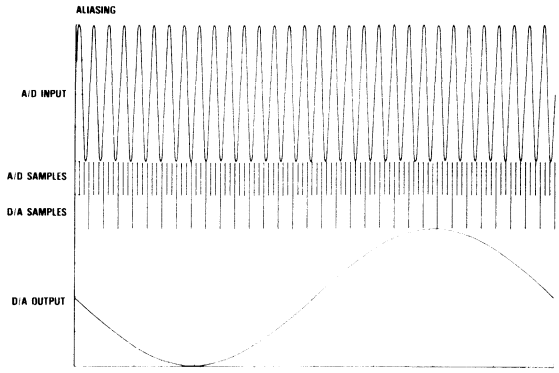


Figure 1. Beat Frequency Test

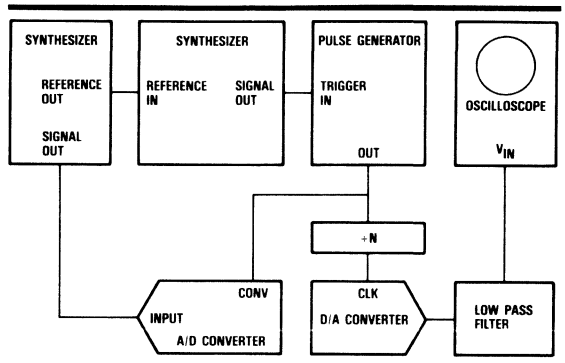


Figure 2. Beat Frequency Test Set-Up

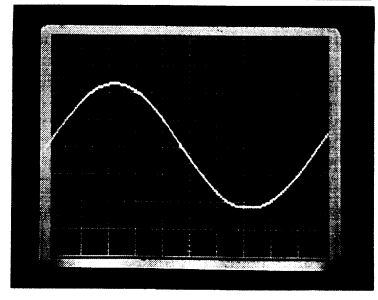


Figure 3. Spurious Code

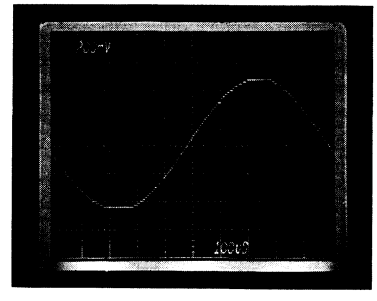


Figure 4. A/D Converter With Missing Codes

N

BWR Bandwidth, Reference

BWR specifies the maximum frequency at which the reference (V_{REF}) may be exercised. It is a small signal parameter since in many cases the reference may only be varied by a small portion of its full-scale value. Exceeding the BWR specification may result in the same types of coding errors encountered when the BW specification is violated.

C_I Digital Input Capacitance

The amount of capacitive loading present at a digital input. Digital input capacitance is measured with a capacitance bridge, applying a 1MHz signal to the input.

C_{IN} Input Equivalent Capacitance

C_{IN} is an approximation of the largely capacitive input impedance of a flash A/D converter. The input capacitance is slightly dependent upon the DC level of the analog input voltage and the input frequency. The input equivalent capacitance must be taken into account when designing a buffer to drive a flash A/D.

The method used to test input capacitance involves sending a high-frequency signal through a transmission line to the analog input, and determining the input impedance by analysis of the reflected wave. This type of test is performed by an R.F. impedance analyzer.

C_O Output Capacitance

Parasitic capacitance between the output terminal of a device and ground.

CONV Convert (Input)

An input signal whose rising edge initiates sampling in a flash analog-to-digital converter. The input signal is quantized after a delay of t_{STO}.

C_{REF} Input Capacitance, Reference

Parasitic capacitance between the reference input terminal and analog ground.

DG Differential Gain

Differential Gain is defined as "The difference between (1) the ratio of the output amplitudes of a small high-frequency sine wave signal at two stated levels of a low frequency signal on which it is superimposed and (2) unity" [1]. Distortion-free processing of a color television signal demands that the amplitude of the chrominance signal not be affected by the luminance function. This is a relevant specification for the video industry since the saturation of the color being shown is represented by the amplitude of a small signal superimposed upon another signal which determines the brightness of the color. The standard method for measuring the differential gain of a device is by using a standardized test signal, known as a modulated ramp (refer to figure 5). The output of the A/D is then reconstructed by a reference D/A and low pass filter; the resultant signal is displayed on a vectorscope which is defined in reference [2]. During DG measurements the vectorscope display will be fuzzy due to quantizing errors in the A/D and D/A. The measurement requires interpretation of the peak-to-peak curvature of the center of the waveform. Figure 6 shows a vectorscope photo with DG testing in progress. The center line is indicated with a dashed line. There are theoretical bounds on differential gain performance described in [3]. The number specified on an A/D converter data sheet is the difference between the actual differential gain of the device and the theoretical performance. Figure 7 shows the typical test set-up that might be used in Differential Gain testing, which is described in more detail in reference [2].

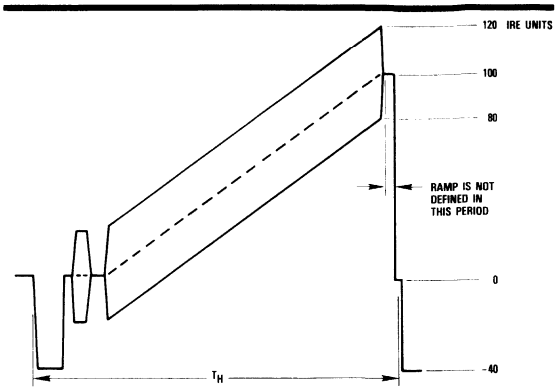


Figure 5. Modulated Ramp Test Signal

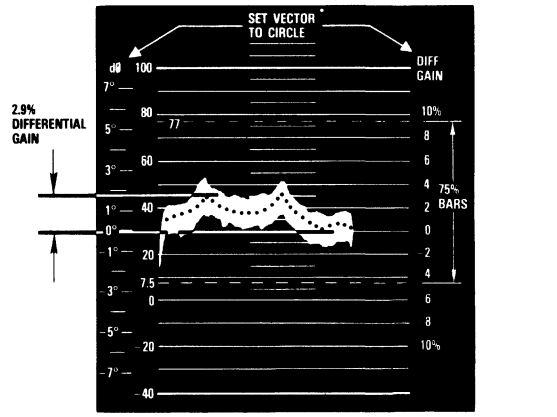


Figure 6. Differential Gain, Example Results

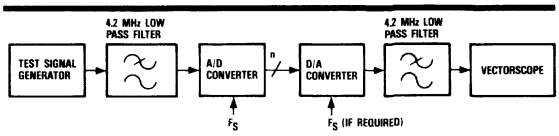


Figure 7. Differential Gain And Phase, Test Set-Up

D_{GND} Digital Ground

Ground reference point for digital power supply and digital circuitry.

DP Differential Phase

Differential Phase is defined as "the difference in output phase of a small, high-frequency, sine wave signal at the two stated levels of a low frequency signal on which it is

superimposed" [1]. Distortion-free processing of a color television signal demands that the phase of the chrominance signal not be affected by the luminance function.

Differential phase errors appear on the T.V. screen as changes in the hue of the colors (tint) as the brightness changes. Differential phase testing is very similar to differential gain testing. The equipment shown in figure 7 is identical, and the display shown in figure 8 is similar to that of figure 6. The results are analyzed in the same manner as Differential Gain, taking the center line of the fuzzy line and finding its maximum peak-to-peak deviation. Reference [2] also describes differential phase testing of A/D converters.

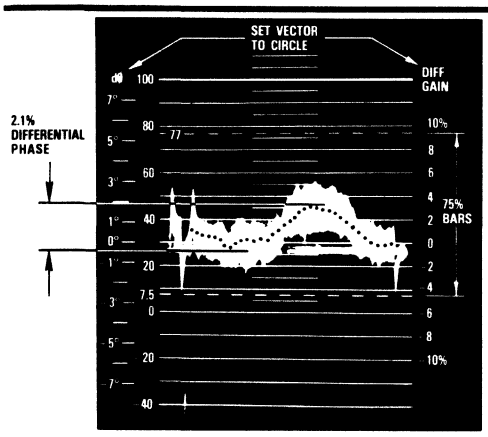


Figure 8. Differential Phase, Example Results

E_{AP} Aperture Error

Since there is an aperture of non-zero duration during which the A/D looks at a signal before conversion, there are errors introduced in the conversion. These errors are the effect of: aperture time (the amount of time during which the input signal is considered before conversion), aperture time uncertainty (the variation in aperture time) and aperture jitter which is the uncertainty in the starting instant of the aperture time. All of these effects are combined in a single parameter, Aperture Error (E_{AP}). Aperture errors cause a degradation of the SNR of the A/D converter with higher analog input frequencies and are estimated based upon this SNR degradation.

E_G Absolute Gain Error

The variation in the slope (gain) of the transfer function of a converter with respect to an established ideal transfer function. This error may be eliminated by adjusting the reference voltage or current applied to the device.

E_{LD} Linearity Error, Differential

Differential non-linearity is a measure of the uniformity of the code midpoint spacing. Differential linearity is defined as the maximum of the difference between adjacent code midpoints and the width of one Least Significant Bit (LSB), divided by the width of an ideal LSB (all units are in LSBs). If there is a missing code, the center of that code is considered to be the transition which skips that code. A differential non-linearity calculation is shown in figure 9. Another method that can be used to determine differential non-linearity is by a subtractive ramp test which examines the difference between adjacent quantization levels (see E_{LI}). This method is shown in figure 10. Differential non-linearity is sometimes measured with a statistical (histogram) test. In the histogram test the A/D converter is provided a full-scale sinusoidal analog input, and a large number of output samples are collected. The probability of obtaining each code is then calculated and the actual ratio of number of samples at that code to total number of samples is compared to this ideal probability. The differential linearity is then estimated, with the assumption that an increase in code width would result in a corresponding increase in the number of occurrences of that particular code.

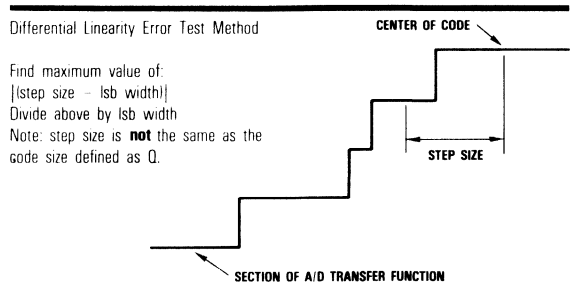


Figure 9. Differential Linearity Error

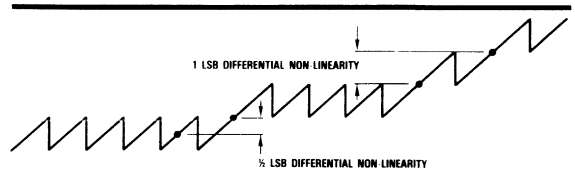


Figure 10. Differential Non-Linearity Measurement

E_{LI} Integral Linearity Error

Integral linearity is a measure of how the ideal and actual transfer functions of the A/D compare. The integral linearity error is the maximum difference between the actual and ideal quantization levels (the midpoint between adjacent threshold levels). A typical A/D transfer function showing different types of linearity errors is shown in figure 11. There are several methods for measuring integral linearity. Zero-based linearity is used mainly in bipolar systems with adjustments that allow the user to null any errors at the origin (the center of the transfer function). To measure zero-based integral linearity, a "straight line of best fit" is drawn through the origin. Then the maximum deviation of the actual transfer function from this line is determined. Terminal-based linearity measurements are similar to the zero-based; however the line is drawn between the two end points of the transfer function. The same difference signal is generated, and the same method is used for interpreting the results. The last common method for measuring independent-based integral linearity involves drawing the "straight line of best fit" through the transfer function, independent of the mid or end points, then calculating the error. When measuring integral linearity, a common test is the subtractive

ramp test. A low-frequency ramp is digitized by the A/D converter, then the signal is reconstructed with a D/A converter. The reconstructed signal is now subtracted from the original ramp with a differential amplifier and the difference (error signal) is displayed on an oscilloscope. The sawtooth wave displayed on the oscilloscope can now be examined for integral non-linearities. Figure 12 shows the test set-up for the subtractive ramp test, and figure 13 is a photo of the oscilloscope screen during such a test. Figures 14, 15 and 16 show the measurement of zero-based, terminal-based and independent-based linearity error using the subtractive ramp test.

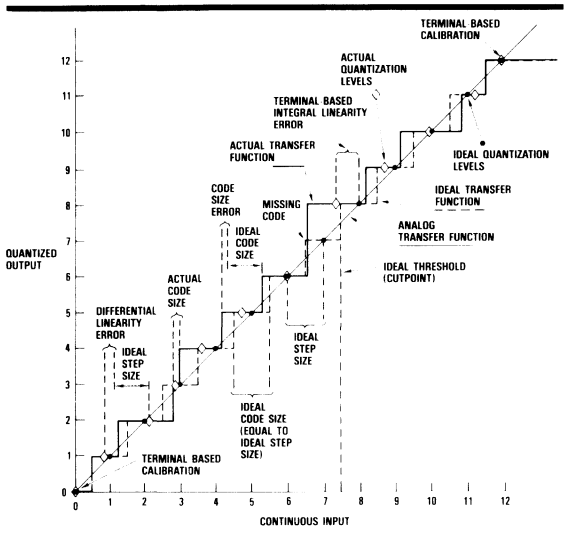


Figure 11. A/D Converter Transfer Function

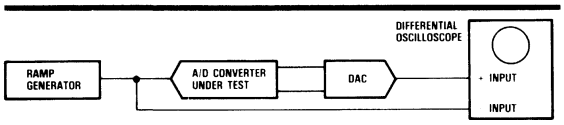


Figure 12. Subtractive Ramp Test Set-Up

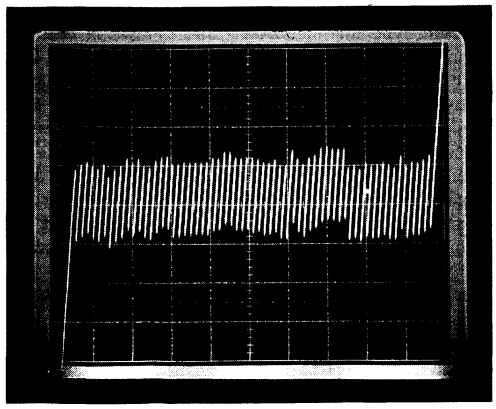


Figure 13. Subtractive Ramp, Example Results

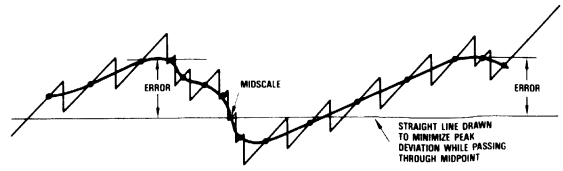


Figure 14. Zero-Based Linearity Measurement

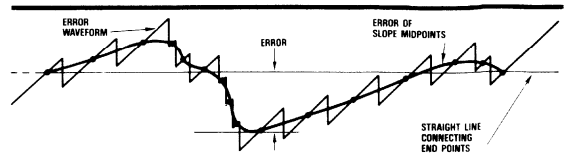


Figure 15. Terminal-Based Linearity Measurement

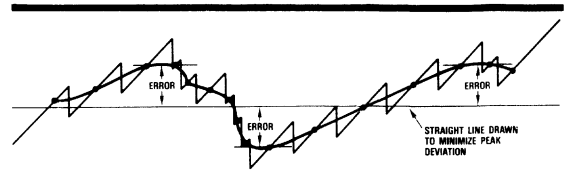


Figure 16. Independent-Based Linearity Measurement

E_{LI} Integral Linearity Error (Terminal-Based)

The maximum difference between the actual transfer characteristics of a converter and the straight line that passes through the end-points (terminals) of that data.

E_{OB}, E_{OT} Offset Voltage Bottom, Offset Voltage Top

Figure 17 shows the block diagram for a typical 6-bit flash A/D converter. There is a parasitic (R_P) resistance between the R_T lead and the first resistor. The voltage drop across this resistor is an offset voltage between the first code quantization level and the voltage applied to R_T. This offset is referred to as E_{OT}. The similar offset voltage at the bottom of the resistor chain is E_{OB}. E_{OT} and E_{OB} are measured by applying a known voltage to R_T and R_B and measuring the difference between these voltages and the voltages of the first and last code transitions of the A/D converter. In an ideal A/D, the first transition occurs at a point 1/2 LSB more negative than the top of the range. Therefore, if the input voltage to the device is set 1/2 LSB closer to R_B than zero, and V_{RT} is adjusted to get toggling between codes 0 and 1, then the voltage on R_T will be E_{OT}.

E_{OBS}, E_{OTS} Offset Errors, Sense Connected

To minimize the effect of offset errors, some A/D converters have sense outputs. These allow the use of a sense pin, which carries minimal current to close a feedback path around the reference input, resulting in lower offset errors. Figure 18 shows a block diagram for an A/D converter which has sense connections. Figure 19 shows how a feedback path is closed around an operational amplifier to make use of the offset sense point. E_{OBS} and E_{OTS} are the residual offset errors when the sense leads are used.

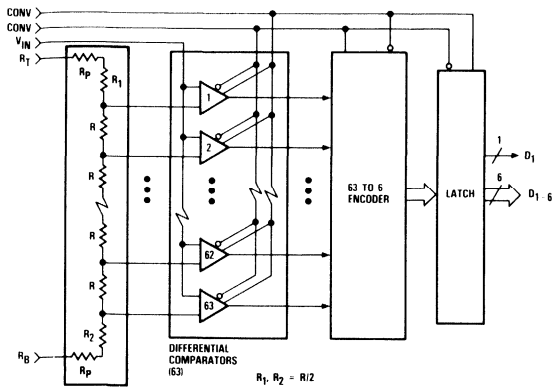


Figure 17. 6-Bit Flash A/D Block Diagram

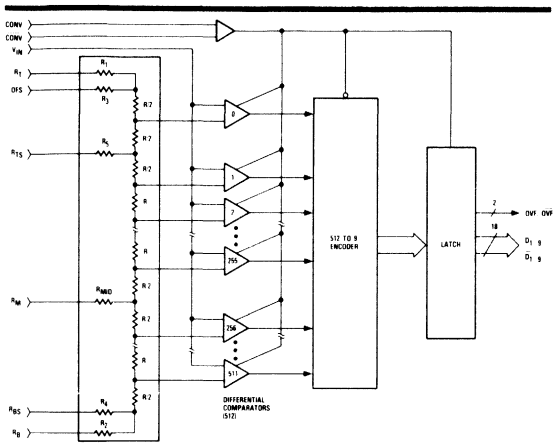


Figure 18. 9-Bit Flash A/D Block Diagram

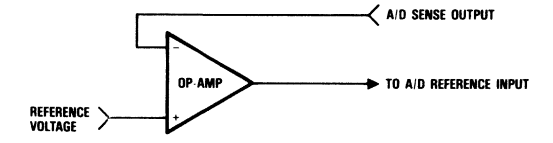


Figure 19. Driving A Reference With The Sense Connection

F_S Maximum Sampling Rate

F_S is a sampling rate (samples per second) at which the converter is guaranteed to operate. Most flash A/D converters will operate reliably at any rate up to the maximum sampling rate, which is measured with worst case supply, worst case duty cycle conditions, and maximum full-power input frequency.

FT_C, FT_D, FT_R Feedthrough -clock, -data, -reference

A measure of unwanted leakage from an input port of a device to another port (e.g., the analog output of a D/A converter), which is expressed in decibels relative to the full-scale value of the output. Clock and data feedthrough refer to spurious output noise arising from logic transitions at the clock and data inputs. Reference feedthrough relates to output variation as a function of reference variation in a D/A converter when data inputs correspond to a zero output.

G_C Peak Glitch Charge

The maximum product of the glitch current and the duration of the glitch; usually given in units of picoCoulombs (pC). Since glitches tend to be symmetric, the average glitch charge is usually much less than the peak glitch charge.

G_E Peak Glitch "Energy" (Area)

The maximum product of the glitch voltage and the duration of the glitch; usually given in units of picoVolt-seconds (pV-sec). Since glitches tend to be symmetric, the average glitch area is usually much less than the peak glitch area.

G_I Peak Glitch Current

The transient current deviation from the ideal output current during an input code transition.

G_V Peak Glitch Voltage

The transient voltage deviation from the ideal output voltage during an input code transition.

I_{CB} Input Current, Constant Bias[1]

The current drawn by the input of the A/D converter is dependent upon frequency and voltage level of the analog input. The current is sometimes also dependent upon the phase of the convert signal. This dependence is explained under I_{SB}, synchronous bias current; however, neglecting all of these second order effects, the current drawn by the input of the A/D is I_{CB}. This can be thought of as the sum of the comparator input bias currents which is dependent upon the input voltage level.

I_{CC} Supply Current[1]

I_{CC} is the current drawn by the device from the V_{CC} supply. I_{CC} is a positive valued parameter. I_{CC} decreases with increasing temperatures in bipolar devices and is measured with V_{CC} at the maximum rated value.

I_{DDL} Loaded Supply Current

Current flowing into the positive power supply terminals with all inputs and outputs toggling at the maximum clock rate, and an output test load of 500 Ohms and 40pF for CMOS devices. I_{DDL} is the current measurement under worst case conditions. In addition to the internal or unloaded supply current, the output buffer now requires current to charge and discharge the load capacitance. This parameter is frequency-dependent. (See I_{DDQ} and I_{DDU} for CMOS supply current under different measurement conditions.)

Note: 1. All currents are defined as positive when flowing into the device.

I_{DDQ} Quiescent Supply Current

Current flowing into the positive power supply terminals under quiescent conditons for CMOS devices. If the inputs are tied LOW, and the outputs are in a high-impedance state, no gates are switching. As a result, the p-channel and n-channel transistors that compose the basic CMOS gate are neither charging nor discharging stray capacitance, and only leakage current flows into the positive supply. (See I_{DDU} and I_{DDL} for CMOS supply current under different measurement conditions.)

I_{DDU} Unloaded Supply Current

Current flowing into the positive power supply terminals of a CMOS device with all inputs toggling at the maximum clock rate, and the outputs in a high-impedance state. With the device unloaded, I_{DDU} includes only the components that contribute to the internal current: the leakage current when the gate is in a "0" or "1" state, and the current drawn during a gate transition. An increase in average gate switching frequency will lead to an increase in current. (See I_{DDQ} and I_{DDL} for CMOS supply current under different measurement conditions.)

I_{EE} Supply Current[1]

I_{EE} is the current drawn by the device from the V_{EE} supply. Since I_{EE} is referenced to a negative supply, it is a negative valued parameter (current flows out of the device). In TRW bipolar devices, I_{EE} decreases with increasing temperatures and is measured with the maximum (most negative) rated V_{EE}.

I_I Input Current, Maximum Input Voltage[1]

Current flowing into a digital input under worst-case power supply and input voltage conditions.

I_{IH} Input current, Logic HIGH[1]

I_{IH} is the current drawn by a digital input to the device when the potential of the terminal is in the logic HIGH state.

I_{IL} Input Current, Logic LOW[1]

I_{IL} is the current drawn by a digital input to the device when the potential of the terminal is in the logic LOW state.

I_{OF} Output Offset Current[1]

The residual output current of a D/A converter that flows when all internal current sinks are switched off.

I_{OH} Output Current, Logic HIGH[1]

I_{OH} is the maximum current that can be forced into (this is a negative value, therefore current flow is out of the device) an output terminal in the HIGH state, while potential at the terminal remains within the V_{OH} specification.

I_{OL} Output Current, Logic LOW[1]

I_{OL} is the maximum current that can be forced into an output terminal on the LOW state, while the potential at the terminal remains within the V_{OL} specification.

I_{ON} Maximum Current, - Output[1]

The maximum current that flows into the "OUT-" output of a D/A converter.

I_{OP} Maximum Current, + Output[1]

The maximum current that flows into the "OUT+" output of a D/A converter.

I_{OS} Output Short Circuit Current[1]

The current flowing from an output when the output is short circuited to ground while in the logic high state. This specification is usally indicated only on TTL compatible devices.

I_{REF} Reference Current

Current Flowing into or out of the reference input terminals of an A/D or D/A converter.

I_{SB} Input Current, Synchronous Bias

In some flash converters, the current flowing into the analog input varies slightly depending upon the state of the CONV signal. If the comparators are in the track mode (CONV LOW), then the input current is greater, and the amount of this current change is ISB, synchronous bias current.

MSPS Megasamples Per Second

The abbreviation for the conversion rate (clock or convert frequency) at which an A/D or D/A converter is operating.

NPR Noise Power Ratio

"NPR is the decibel ratio of the noise level in a measuring channel with the baseband fully noise loaded to the level in that channel with all of the baseband noise loaded except the measuring channel: [4]. To test NPR, the input of the A/D converter is presented with white noise having a frequency spectrum from low frequencies up to 1/2 the sampling rate. The power of the input noise is adjusted so that the converter is fully loaded, but not clipping excessively. The output of the A/D converter is then converted back into an analog signal with a D/A. The D/A output is passed through a very narrow band pass filter, and the output power of the signal is measured. The process is now repeated, but with a notch filter at the input of the A/D converter. The ratio of the two measured powers is the Noise Power Ratio, and is often expressed in dB:

$$NPR = 10 \log_{10}(ratio)$$

NPR is often used to determine how much noise will "bleed" into one channel from other channels in a broadband, frequency domain multiplexed system.

PREL Preload (Control)

A control signal which determines (in conjunction with the three-state control pins) which of three signals is to be loaded into the output register at the rising edge of the product clock: the result of the calculations which were just performed, the present contents of the output register, or a value applied to the output port by external circuitry.

Note: 1. All currents are defined as positive when flowing into the device.

PSS Power Supply Sensitivity

A measure of DC variation of an output under consideration (e.g., the analog output of a D/A converter) as the power supply voltage is varied around the nominal value. PSS is specified in milliAmps or milliVolts of output change per Volt of supply change.

PSRR Power Supply Rejection Ratio

A measure of high-frequency noise rejection from the power supply inputs of a device to the output under consideration (e.g., the analog output of a D/A converter). Expressed in decibels relative to full-scale output. Generally, PSRR decreases with increasing frequency and for this reason is often specified at more than one frequency.

Q, CS Code Size

Code size is the size of the individual codes, from code transition to code transition. It is often expressed as a percentage of the ideal code size. The ideal code size is given by:

$$\frac{\text{Input Voltage Range}}{2^N}$$

Where N is the number of bits of resolution of the A/D converter.

Q is also defined as the total number of quantizing levels or codes output by a converter (2_N) with N being the number of bits of resolution provided by the A/D.

RES Resolution

The smallest level separation (input level of A/Ds and output level for D/As) that is unambiguously distinguishable over the full-scale range of a converter. It is expressed as a percentage of full-scale or as an equivalent number of bits, usually the number of data inputs of a D/A or data outputs of an A/D converter.

R_{IN} Analog Input Impedance

Although the input impedance of a flash A/D converter is largely capacitive, it does have a resistive component which is approximated with R_{IN} the input resistance. R_{IN} varies with the input voltage.

R_O Equivalent Output Resistance

The effective equivalent resistance between an analog output terminal of a D/A converter and analog ground.

R_{REF} Reference Resistance

R_{REF} is the total resistance of the entire reference resistor chain, including parasitics. It can be measured directly between R_T and R_B. Another method of testing R_{REF} is to calculate it from I_{REF} and (V_{RT} - V_{RB}).

R_S Register Shift (Control)

A control signal which changes the output format to permit a valid result for the product of two most negative numbers.

SNR Signal-To-Noise Ratio

The signal-to-noise ratio is the ratio of the value of the signal to that of the noise. The values of the signal and of the noise are usually RMS, but for some signals such as video, it is defined as peak-to-peak signal vs RMS noise, because it is difficult to determine the RMS value of a video signal, and the meaning of peak-to-peak noise is not a useful parameter. The signal-to-noise ratio of an A/D converter provides a good figure of merit for the dynamic accuracy of the device. To test SNR, the A/D converter is given a high purity sine wave input. This is sampled at a non-harmonic sampling rate and the output of the A/D converter is stored in memory. The data from the A/D are then transformed into the frequency domain with a Fast Fourier Transform (FFT) and analyzed to determine the SNR. When analyzing the data most of the "noise" will be located at the harmonic frequencies; therefore the SNR is a good estimate of total harmonic distortion. The analysis method takes the RMS or peak-to-peak voltage of the signal, and divides it by the RMS value of the noise. SNR is usually expressed in dB with the formula below:

$$SNR = 20 \log_{10} \frac{\text{Signal}}{\text{Noise}}$$

SUB Subtract (Control)

A control signal which determines whether the present contents of the output register is added to (SUB = LOW) or subtracted from (SUB = HIGH) the product at the output.

T_A Ambient Temperature

For standard temperature range devices, the temperature range is specified in terms of the ambient temperature (still air) surrounding the converter.

T_C Case Temperature

For extended temperature range devices, the temperature range is specified in terms of the case temperature.

TC Two's Complement (General Definition)

Two's complement is a binary numbering system in which the Most Significant Bit (MSB) carries the sign information by virtue of a negative place value. In two's complement, an MSB of ZERO signifies a positive number, a ONE denotes a negative number, and the negative number order is reversed from straight binary. That is, the number which consists of all ONEs is the least negative number, and the number which consists of a ONE and all ZEROs is the most negative number.

TC Two's Complement (Control)

An active HIGH signal which designates one or both inputs as two's complement numbers. If TC is LOW, unsigned magnitude processing will be used. Note that some parts allow independent designation of each input as two's complement or unsigned magnitude, and other parts do not.

TC_G Gain Error Tempco

The factor which linearly approximates the variation with temperature of Absolute Gain Error, E_G.

T_{CO} Temperature Coefficient

T_{CO} is the factor which linearly approximates the variation with temperature of Offset Errors (E_{OT}, E_{OB}). This is a first order approximation and the actual temperature coefficient is a function of temperature which may exceed the maximum of T_{CO} in some temperature ranges.

t_D Output Delay

t_D is the time between the rising edge of the CONV signal and the time at which the output data from the A/D is guaranteed to be stable. On many TTL flash A/D converters, this delay can be reduced by the addition of pull-up resistors from the data outputs of the device to the V_{CC} supply. This output delay is measured with the test load specified in the corresponding data sheet.

t_H Hold Time

The time period after the operative edge of CLK signal during which input data must be constant in order to be correctly registered.

t_{HO} Output Hold Time

The time from the rising edge of the convert signal to the time when the output data lines begin to change.

t_{PW} Pulse Width

The time period between consecutive edges of a logic pulse.

t_{PWH} Pulse Width High

t_{PWH} is the minimum width high CONV pulse with which the A/D will accurately operate if all other specifications are met. t_{PWH} is measured from the 1.3 Volt level of the rising edge of the CONV signal to the 1.3 Volt level of the falling edge of the CONV signal on TTL compatible devices. If the CONV signal has a low portion of t_{PWL}, and a high portion of t_{PWH}, the device may be exceeding F_S in which case it may not operate properly. The performance of many A/D converters performance can be improved by making t_{PWH} as long as possible.

t_{PWL} Pulse Width Low

t_{PWL} is the minimum width low CONV pulse with which the A/D will accurately operate if all other specs are met. t_{PWL} is measured from the 1.3 Volt level of the falling edge of the CONV signal to the 1.3 Volt level of the rising edge of the CONV signal on TTL compatible devices.

TRIL Three-State Least Significant Product (Control)

A control which enables the output state for the least significant product when in the LOW state, and places the output stage for the least significant product in the high-impedance state when HIGH.

TRIM Three-State Most Significant Product (Control)

A control which enables the output stage for the most significant product when in the LOW state, and places the output stage for the most significant product in the high-impedance state when HIGH.

t_S Setup Time

The time period prior to the operative edge of the clock signal during which input data must be stable in order to be correctly registered.

TSL Three-State Least Significant Product (Control)

A control which enables the output stage for the least significant product when in the LOW state, and places the output stage for the least significant product in the high-impedance state when HIGH. A HIGH on this control also forces the most significant product section of the output register to be preloaded at the rising edge of the product clock when PREL is active.

TSM Three-State Most Significant Product (Control)

A control which enables the output stage for the most significant product when in the LOW state, and places the output stage for the most significant product in the high-impedance state when HIGH. A HIGH on this control also forces the most significant product section of the output register to be preloaded at the rising edge of the product clock when PREL is active.

t_{STO} Sampling Time Offset

Sampling time offset is the time interval between the rising edge of the CONV signal and the actual instant at which the A/D samples the input signal.

TSX Three-State Extended Product (Control)

A control which enables the output stage for the extended product when in the LOW state, and places the output stage for the extended product in the high-impedance state when HIGH. A HIGH on this control also forces the extended product section of the output register to be preloaded at the rising edge of the product clock when PREL is active.

t_{TR} Transient Response

t_{TR} is the amount of time required for the converter to recover from a fullscale input transition, before valid data can be produced. The comparators in a flash A/D converter have a finite slew rate and a finite settling time. If a device is presented with a full-scale input change (which exceeds that slew rate), it takes t_{TR} for the input circuit to recover and provide accurate data.

V_{AGND} Analog Ground Voltage

Potential of the analog ground terminal with respect to the digital ground terminal.

V_{CC} Positive Supply Voltage

The positive power supply voltage required for operation of a device.

V_{EEA}, V_{EED}, V_{EE} Supply Voltage

V_{EE} is the negative supply voltage. On converters with both digital and analog negative supplies, the analog supply is denoted $V_{EE}A$, and the digital supply is $V_{EE}D$.

V_{ICM} Input Voltage, Common Mode Range

The operational limit over which a differential logic input voltage may be varied.

V_{IDF} Input Voltage, Differential

The voltage difference between a logic input and its complementary input.

V_{IH} Input Voltage, Logic HIGH

The voltage required on a digital input in order for that input to be forced to a valid logic HIGH state.

V_{IL} Input Voltage, Logic LOW

The voltage required on a digital input in order for that input to be forced to a valid logic LOW state.

V_{OCN} Voltage Compliance, - Output

A measure of the range over which the output voltage of a current generator may be varied. V_{OCN} is the voltage compliance of the - output of a D/A converter.

V_{OCP} Voltage Compliance, + Output

V_{OCP} is the voltage compliance of the + output of a D/A converter. See V_{OCN}.

V_{OH} Output High Voltage

The potential at an output terminal in the high state with respect to digital ground, when loaded with the test load defined in the data sheet. V_{OH} is measured with V_{CC} at a minimum.

V_{OL} Output Low Voltage

The potential at an output terminal in the low state with respect to digital ground, when loaded with the test load defined in the data sheet. V_{OL} is measured with V_{CC} set to the maximum value.

V_{OZS} Output Voltage, Zero Scale

The residual output voltage of a D/A converter that appears at its output when all internal current sinks are switched off.

V_{RB} Reference Bottom Voltage

The potential of the R_B terminal with respect to analog ground.

V_{RM} Reference Middle Voltage

The potential of the R_M terminal with respect to analog ground.

V_{RT} Reference Top Voltage

The potential of the R_T terminal with respect to analog ground.

References

[1] IEEE Standard Dictionary of Electrical and Electronic terms, IEEE Std 100-1977, p. 177.

[2] IEEE Standard Definitions of Terms Relating to Television, IEEE Std 201-1979.

[3] F.A. Williams and R.K. Olsen, "Quantization Effects on Differential Phase and Gain Measurements," SMPTE Journal, November, 1982.

[4] The White Noise Book, M.J. Kant.

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IEEE Broadcast Technology Society. "Proposed Standard for Performance Measurements of A/D and D/A Converters for PCM Television Video Circuits, Project No. 746."

Application Notes

TP-1A "Multiplier-Accumulator Application Notes" by Louis Schirm IV.

An introduction to the use of MACs as the basic building blocks of all Digital Signal Processing (DSP). The construction of various kinds of filters, complex multiplication and Fast Fourier Transforms (FFTs) using discrete MACs is covered. Many of TRW LSI's most recent DSP products integrate several MACs on a single chip utilizing these techniques.

TP-2A "Monolithic Bipolar Circuits for Video Speed Data Conversion" by Willard K. Bucklen.

This application note describes TRW LSI's development of the world's first monolithic video ADC, the TDC1007, as well as other A/Ds and D/As. It is an excellent introduction to the operation of high-speed flash, successive-approximation and sub-ranging A/Ds, digital error correction and low-glitch, high-speed DACs.

TP-6A "Introduction to the Z Transform and Its Derivation" by R. J. Karwoski.

An introduction to the mathematics involved in most DSP systems. It is written to provide newcomers to the digital field familiar with analog signal processing a clear explanation of the use of the Z transform. The Z transform is a means of analysis and synthesis of digital and mixed signal (analog-digital) systems. This paper is designed to clarify many of the crucial issues that are omitted from most introductory texts.

TP-9A "A Four-Cycle Butterfly Arithmetic Architecture" by R. J. Karwoski.

Covers in detail the use of discrete multiplier-accumulators to implement Fast Fourier Transforms (FFTs). The "Butterfly" is a computational architecture with which this function is realized. Many of these techniques have been employed in the design of TRW LSI's dedicated FFT processor, the TMC2310, which integrates several MACs on a single monolithic chip. (The TMC2310 is currently recommended over the older, more complex application of many discrete MACs for the FFT function.)

TP-17B "Correlation - A Powerful Technique for Digital Signal Processing" by Dr. J. Eldon.

Correlation techniques find use in communications, instrumentation, computers, telemetry, sonar, radar, medical, and other signal processing systems. Electronic systems that perform correlation have been around for years, but they have been bulky and inefficient. The development of a family of correlators by TRW makes this powerful technique practical for a wider range of applications.

TP-18 "LSI Multipliers Applications Notes"

This application note covers four topics. It shows 1.) how to connect multipliers to increase the precision (number of bits) in a multiplication operation, 2.) how to receive the correct results when using multipliers in two's complement systems when lower precision (fewer bits) is required, 3.) how to multiplex multipliers to achieve higher speeds, and 4.) division using multipliers. (Of course, TRW also makes the world's only monolithic digital divider chips, the TMC3210 floating-point divider and the TMC3211 integer divider.)

TP-19 "Non-Linear A/D Conversion" by B. Friend.

Describes a method of dynamically modulating the reference of a flash A/D converter to achieve a desired non-linear transfer function. Developed for a high energy physics experiment, this technique has applications in numerous other fields.

TP-22 "A guide to the Use of the TDC1028; a Digital Filter Building Block" by F. Williams.

Discusses word and tap sizing of Finite Impulse Response (FIR) digital filters, and the implementation of filters with a variety of lengths and word sizes. Includes a circuit to autoload coefficients.

TP-30 "Understanding Flash A/D Converter Terminology" by M. Sauerwald.

Definitions of terms that TRW uses in A/D converter datasheets.

TP-31 "An Introduction to Two Different Finite Impulse Response Structures" by F. Williams.

Digital filtering is a rapidly expanding field, and the design process is not dramatically different from design techniques for high-performance analog filters. However, due to the flexibility of the digital approach, additional design decisions are necessary. This note presents the Tapped-Delay and the Frequency-Sampling forms of Finite Impulse Response (FIR) filters, with theoretical discussions.

TP-33 "Using the TDC1018 and TDC1034 in a TTL Environment" by D. Watson.

It is becoming an increasingly common practice to use components designed for ECL systems in a +5V only environment, interfacing them to TTL logic signals. Using the TDC1018 and TDC1034 D/As as examples, this note describes how that interface is accomplished, including data level shifting, D/A output level shifting, and noise considerations.

TP-39 "Interfacing the TMC2301 Image Resampling Sequencer" by Dr. John Eldon and Robert Cordova

The TMC2301 is a powerful device for image warping, rotation, panning, zooming, filtering, and other operations. It operates by calculating the addresses of input image pixels that correspond to each output pixel as the output image is scanned. User-selectable coefficients determine the locations of the pixels that are chosen and therefore the transform that is performed. This application note specifically addresses the application of the TMC2301 towards nearest neighbor resampling, bilinear interpolation (4 pixel kernels), and interpolation using kernels larger than 4 pixels.

TP-40 "Non-Linear Operations with the TMC2301 Image Resampling Sequencer" by Dr. John Eldon and John Watson.

The TMC2301 may be used to provide both linear (all straight lines in the image remain straight) and non-linear (straight lines may become curved) image transformations. Ordinary pan, zoom, and rotate operations are linear transformations. This application note guides the user through the use of the TMC2301's higher-order transformation coefficients to provide warped, twisted and curved (or unwarped, untwisted and uncurved) images.

TP-44A "Maximum and Minimum Value Detection with the TDC1035 Peak Digitizer" by Mark Sauerwald.

The TDC1035 is the world's only monolithic device that simultaneously detects and digitizes the peak value of a signal to 8 bit precision at high rates. This application note covers the practical application of two TDC1035s to the simultaneous capture of both positive and negative peak values. It includes schematics and circuit board patterns for a digital "glitch catcher"

TP-45A "Designing with the THC1200 A/D Converter Family" by Gerry Quilligan.

The THC1200, THC1201 and THC1202 A/D converters are the most versatile collection of 12-bit high-speed A/D converters available. This application note helps the user obtain the highest performance from these devices through proper grounding and ground plane technique, controlling common mode noise and impedance, power supply selection and decoupling, printed circuit board layout, and digital data and clock signal termination. Low-jitter clock generation, thermal considerations, and A/D converter testing are also discussed.

Application Note Cross - Reference

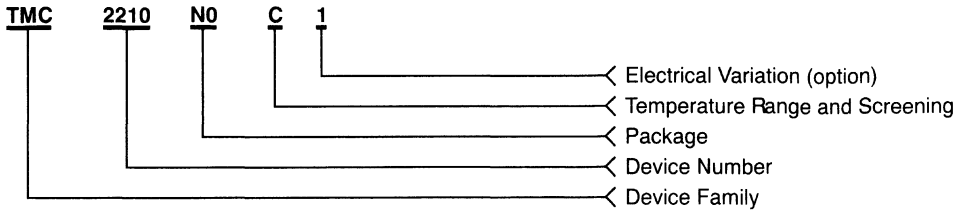
Part Number	Related App Notes
MPY208K	TP18
MPY28KU	TP18
MPY216H	TP18
TAC1020	TP30
TAC1025	TP30
TDC1001	TP2A, TP30
TDC1007	TP2A, TP30
TDC1014	TP2A, TP30
TDC1016	TP2A
TDC1018	TP33
TDC1020	TP30
TDC1025	TP30
TDC1028	TP22, TP31
TDC1029	TP30
TDC1034	TP33
TDC1035	TP30, TP44A
TDC1038	TP30
TDC1044	TP30
TDC1046	TP19, TPTP30
TDC1047	TP30
TDC1048	TP30
TDC1049	TP30
TDC1058	TP30

Part Number	Related App Notes
TDC1112	TP33
TDC1147	TP30
TDC1318	TP33
TDC1334	TP33
THC1068	TP30
THC1069	TP30
THC1070	TP30
THC1200	TP30, TP45
THC1201	TP30, TP45
THC1202	TP30, TP45
TMC2023	TP17B
TMC2208	TP1A
TMC2210	TP1A, TP9A, TP31
TMC2220	TP17B
TMC2221	TP17B
TMC2243	TP22
TMC2301	TP39, TP40
TMC2302	TP39, TP40

Ordering Information

Ordering Information

Product Numbering System



Screening

A - High Reliability, T_C = -55°C to 125°C
B - Industrial, T_C = -25°C to 85°C
C - Commercial, T_A = 0°C to 70°C
F - Commercial, T_C = -55°C to 125°C
V - 833 Compliant, T_C = -55° to 125°C

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